Configuring the ML507 for Partial Reconfiguration

Setting up the Xilinx ML507 platform for partial reconfiguration

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Contents

Introduction

This tutorial will guide you through the process of creating partially reconfigurable bit streams for the Xilinx ML507 development board with the minimalistic using the existing base system created in the Xilkernel Configuration and Application Tutorial. You will create a black box module for use by an Impulse C application. Lastly, this tutorial will walk your through loading the base system and then swapping out Impulse C applications on the fly.

After completing this tutorial you will be able to:

1. Preserve an existing Xilinx project for the ML507 development board while supporting partial reconfiguration of the FPGA fabric.
2. Plan out the placement of the base system and a black box module in the FPGA fabric.
3. Develop an Impulse C application, synthesize it, and swap it into the system on the fly.

Resources

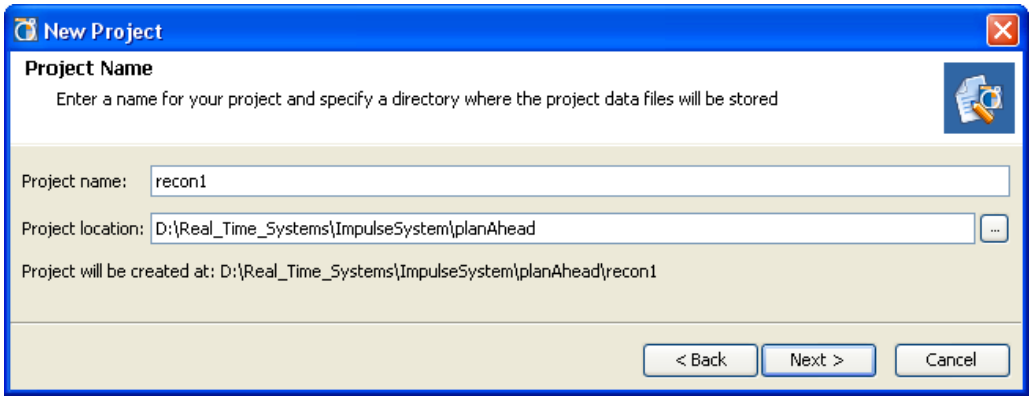
To complete this tutorial you will need the following resources:

- Xilinx ML507 development board with a Virtex-5 FPGA.
- Platform cable USB II adapter (USB-to-JTAG).
- Licensed copy of version 12.3 of the Xilinx tool suite, including Xilinx PlanAhead.
- Completed system from the Xilkernel Configuration and Application Tutorial.

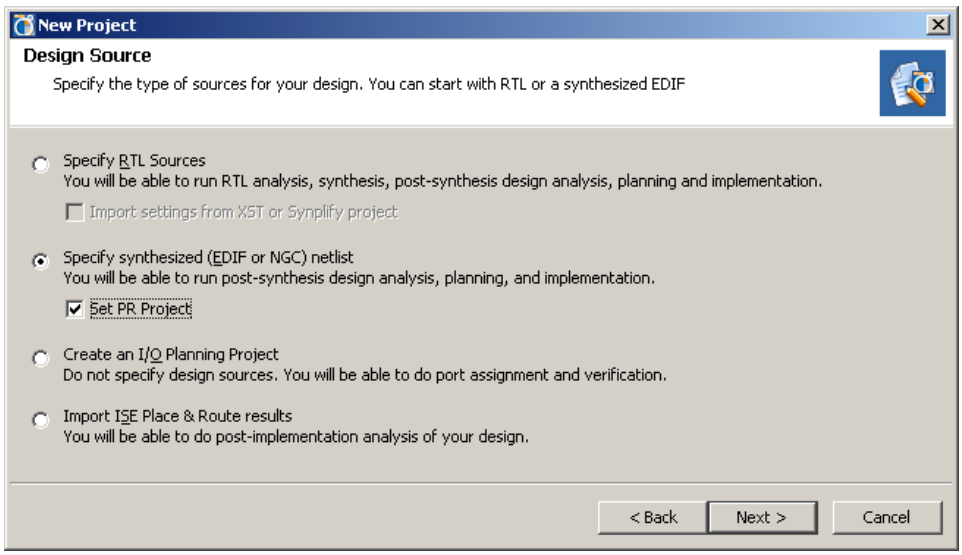
Create a PlanAhead Partial Reconfiguration Project

1. Open the Xilinx PlanAhead tool (version 12.3). When the application is finished loading, click on the Create New Project Link to begin the new project wizard. Then click next.

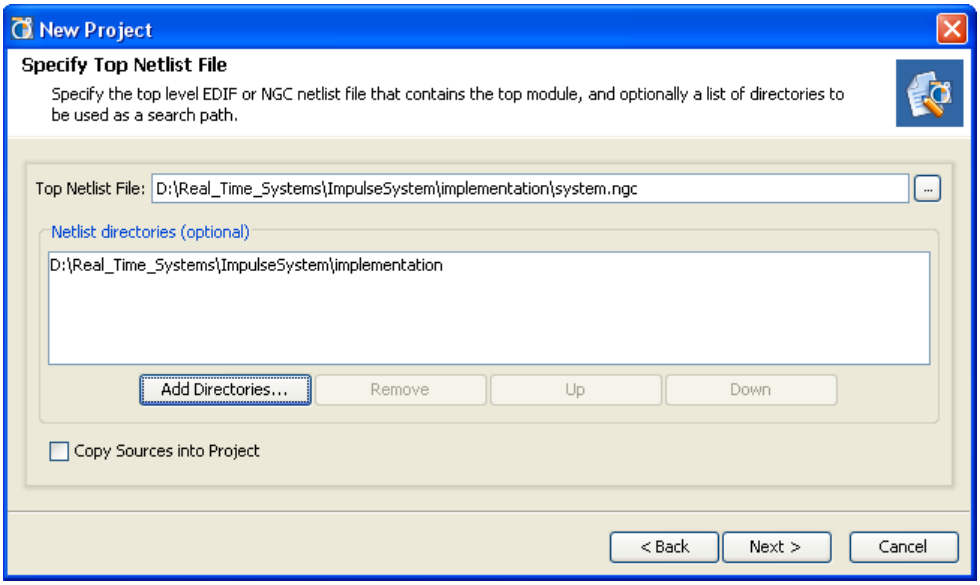
2. You will be prompted to enter a project next and location. The project path should not have any spaces in it. After selecting a location, click next.



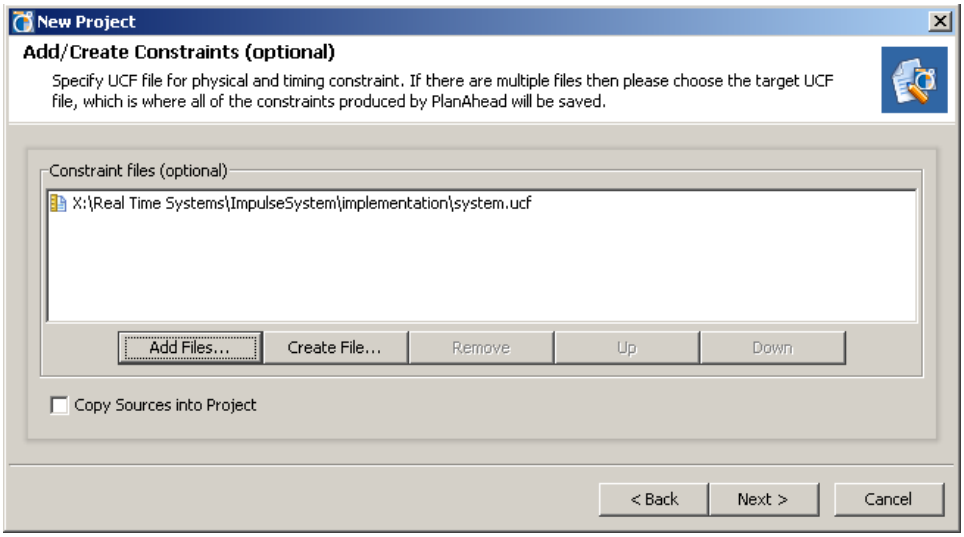
3. Select the Specify synthesized (EDIF or NGC) netlist bubble and make sure that Set PR Project is checked. Then click next.



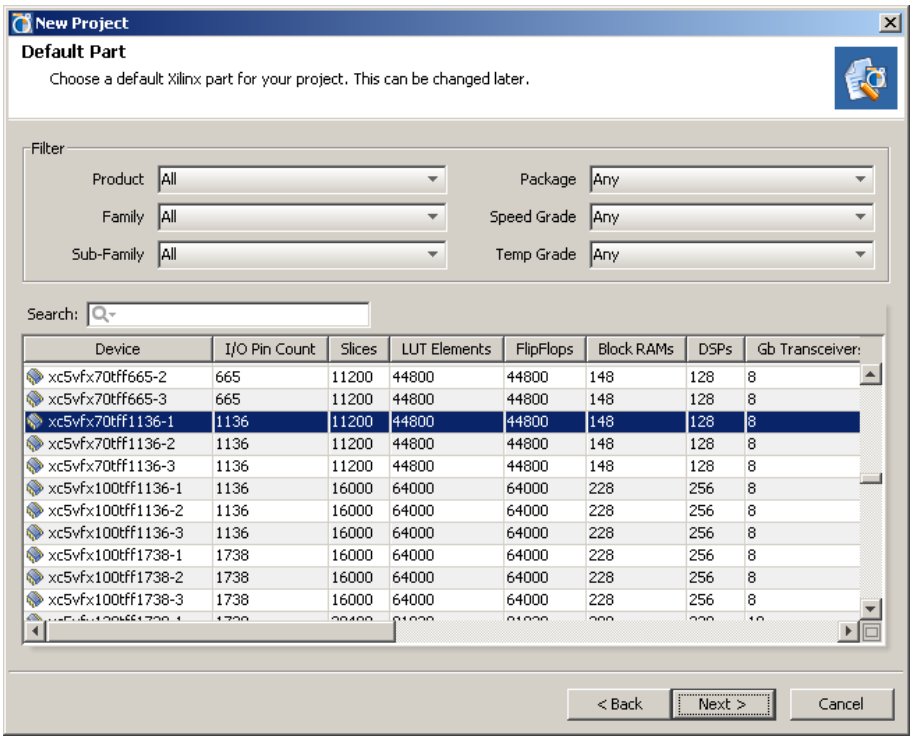
4. Locate the netlist file you created in the Xilkernel Configuration and Application Tutorial in the implementation directory. Then add the implementation directory to the project. Uncheck copy sources to project. Then select next.



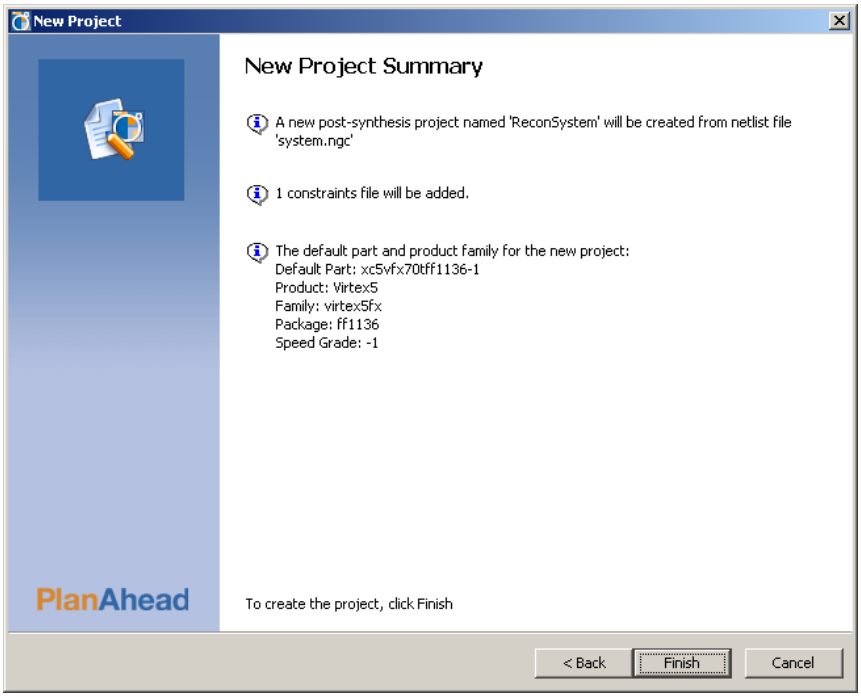
5. The constraints file should be selected automatically. If not, click add file and locate the ucf file in the implementation directory. Then click next.



6. Verify that the correct FPGA device is selected (xc5vf70tff1136-1). Then click next.

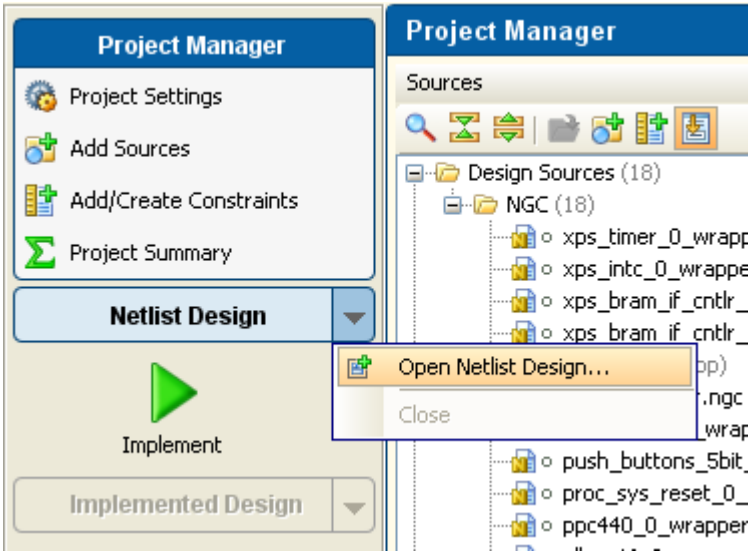


7. Verify that the summary page looks like the one below, then click Finish to complete the wizard.

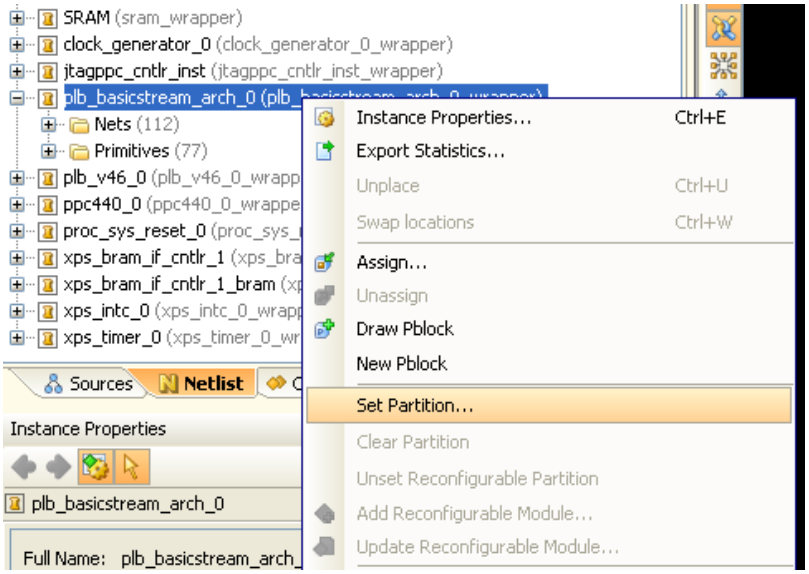


Create a Reconfigurable Partition

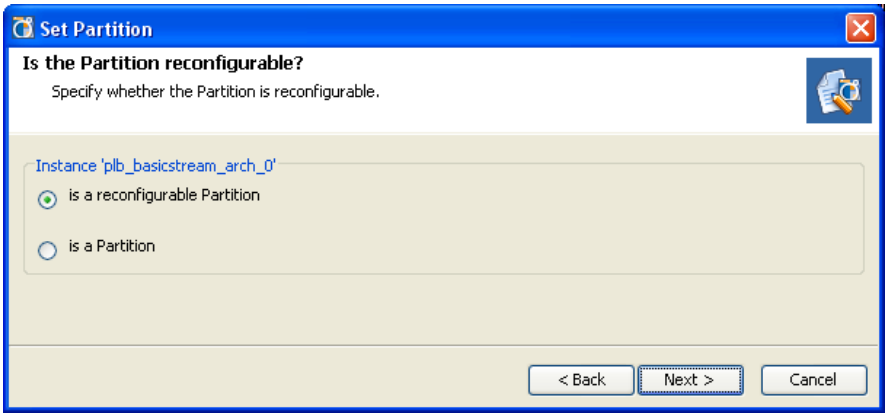
1. After the new project wizard is completed, open the netlist design by clicking Netlist Design under the Project Manager and then selecting Open Netlist Design. When prompted, ensure that the correct board is selected and then click OK. PlanAhead will take a few moments load the full project netlist into memory and scan for various components. There should be no unspecified components at this time, so if a warning pops up go back and ensure that all necessary files are included in the project directory.



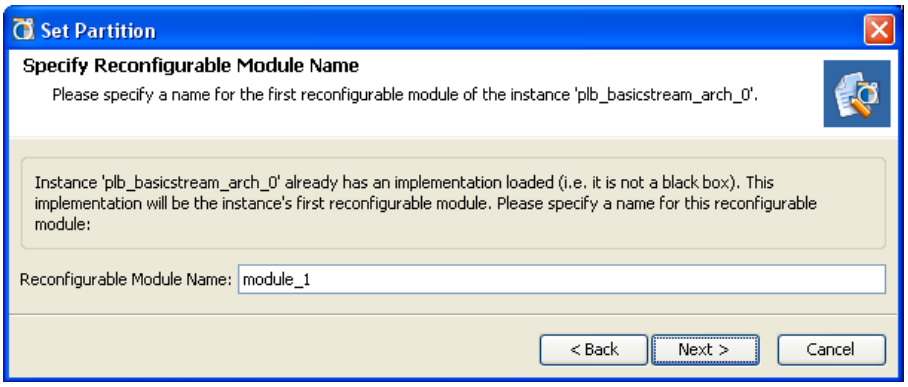
2. After the netlist loads, locate the module called plb_basicstream_arch_0. Right click and select Set Partition.



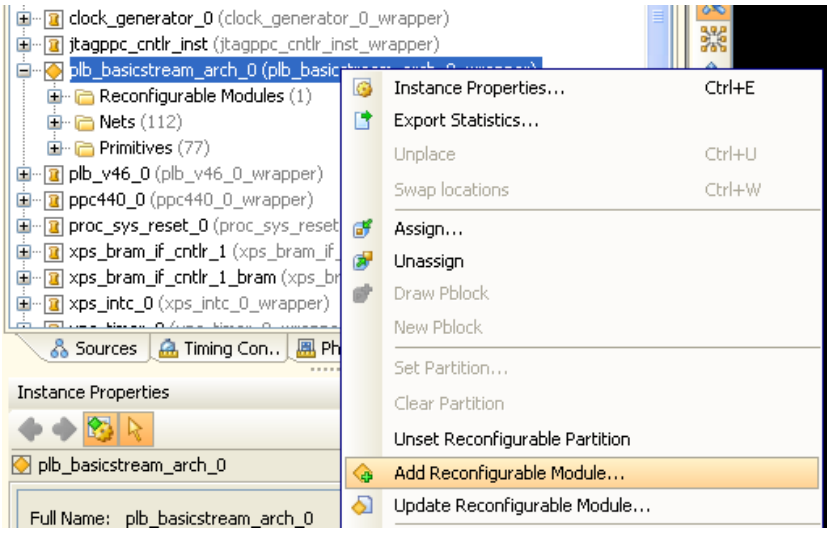
3. The Set Partition wizard will pop up. Click next. Then select “is a reconfigurable partition” and click next.



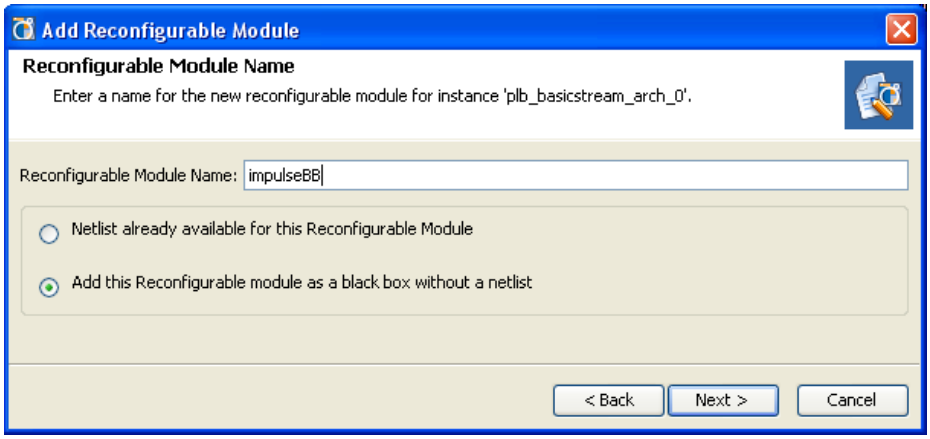
4. Name the existing module and click next. Click Finish to complete the wizard.



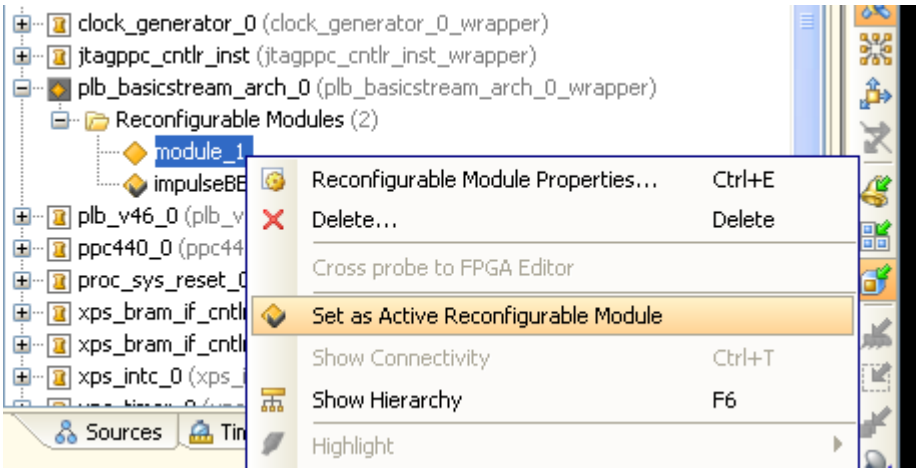
5. Right click plb_basicstream_arch_0 again and select Add Reconfigurable Module.



6. Name the module impulseBB, and select “Add this Reconfigurable module as a black box without a netlist.” This will be used for blanking the reconfigurable partition. Click Next and then Finish to complete the wizard.

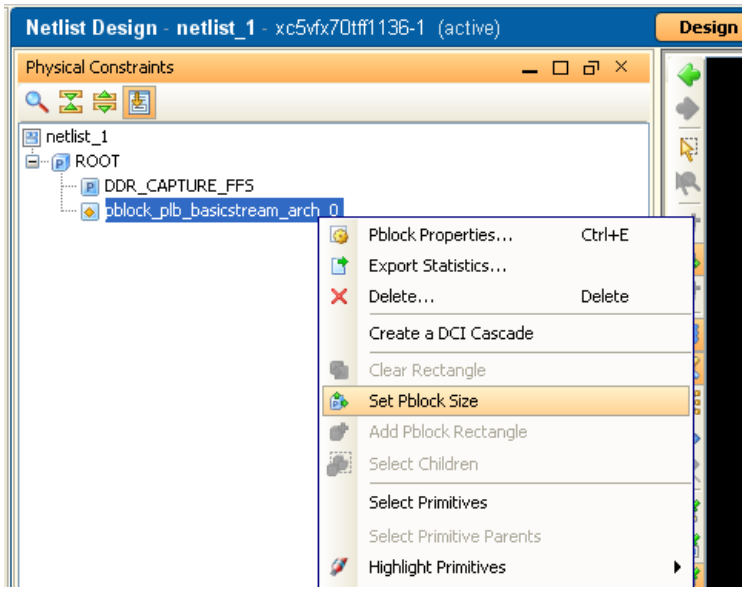


7. Before proceeding to the next section, make sure that module_1 is the active reconfigurable module. The active module will have a checkmark next to it and can be set by right clicking and selecting “Set as Active Reconfigurable Module.” Ideally the active module will have equivalent or a superset of resources needed for all Impulse C modules to be swapped in.

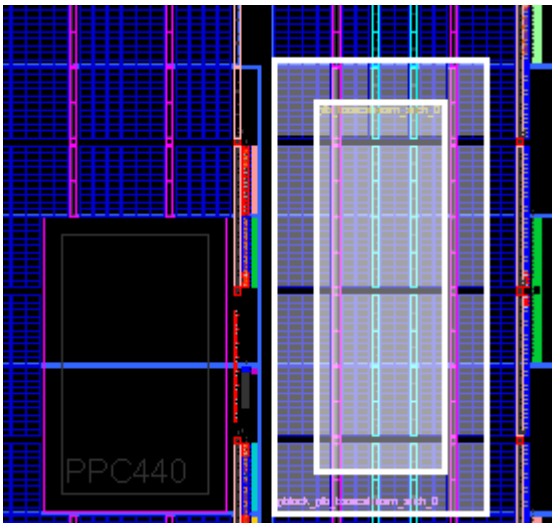


Set Physical Constraints

1. Select the Physical Constraints tab at the bottom of the netlist window. Right click pblock_plb_basicstream_arch_0 and select Set Pblock Size.

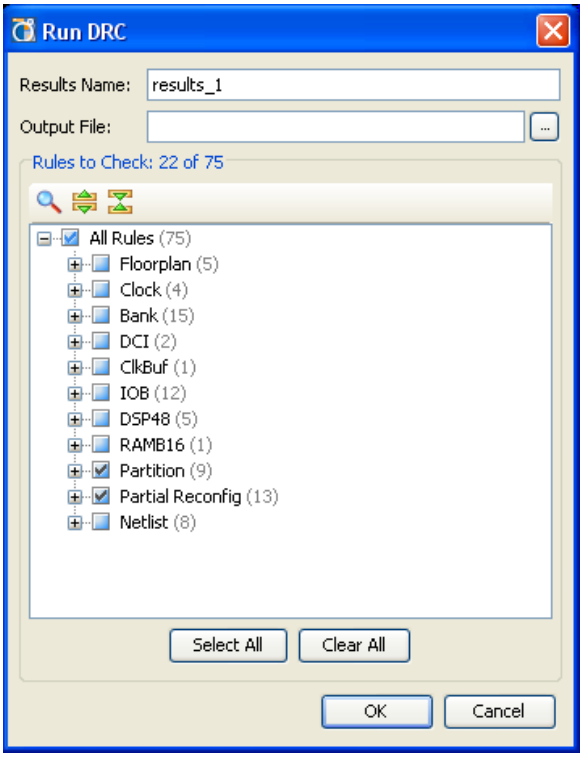


2. Click and drag a rectangular area in the Design Planner window, making ensure to span multiple columns. This is where the reconfigurable partition will be in the FPGA fabric. When prompted, check all resources and click OK.

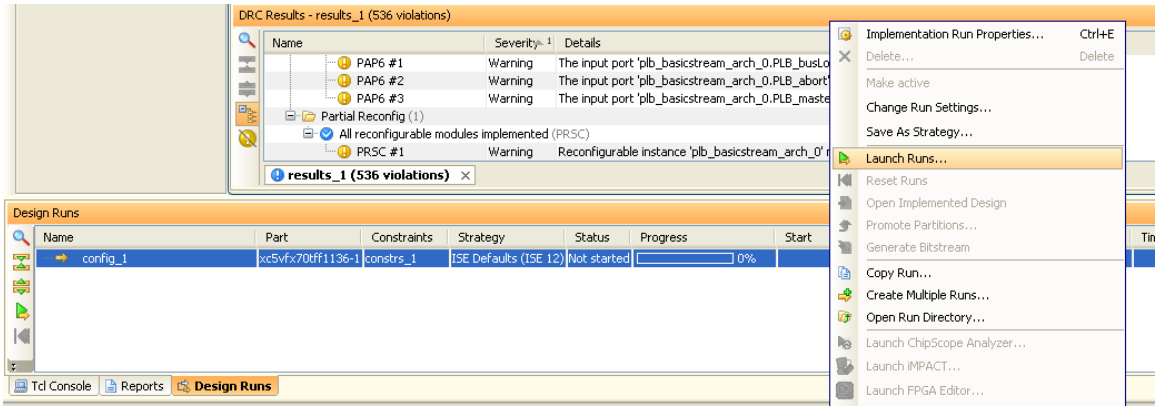


Implement the Design

1. Under the Project Manager, click Run DRC to begin the Design Rule Check. When prompted, select Partition and Partial Reconfig and then click OK.



2. After DRC completes, ensure that there are no fatal errors. Then click on the Design Runs tab in the bottom window. Right click config_1 and click Launch Runs.



3. When prompted to launch the selected runs, click OK to being implementation of the partial reconfiguration design.

Unfinished Work and Next Steps

1. After completing the last step of this tutorial, the implementation task queues but never runs. The reasons for this are unclear at the time of submission.
2. Because the PlanAhead project cannot be implemented, it is unclear whether or not there are conflicts between the base system and the reconfigurable partition, or where the best location for the reconfigurable partition should be. It is also unclear if the same area constraints will work for multiple Impulse C applications.
3. Future work should investigate these implementation issues and identify a suitable area for the Impulse C module.

Issues and Troubleshooting

All issues, questions, and concerns can be directed to Robert LiVolsi at rjl3050@rit.edu.