A Standard Cell Library for Student Projects

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Abstract

A standard-cell library for MOSIS scaleable CMOS rules has been developed. It is intended for use with Synopsys Design Compiler, Cadence Silicon Ensemble, and Cadence Virtuoso or Magic. The library is targeted for the AMI $0.5\mu m$ process, which currently offers the smallest feature size in the MOSIS educational program. The library also includes I/O pad cells and fully places and routes a padframe if desired. All steps in the design flow are fully automated with only three scripts and have been tested successfully in a large VLSI design class at the Illinois Institute of Technology. To customize and run these three scripts, for a given design, typically takes less than five minutes, since all details are transparent to the students, allowing them to focus on the design instead of worrying about the tools.

1 Introduction

Teaching semi-custom design has become very important in contemporary VLSI education. Techniques, such as synthesis, placement and routing (P&R) are commonly used in industry and students need to demonstrate knowledge in these fields. In order to provide knowledge and experience at the industry level to students, it is prudent to use popular commercial tools that are likely to be used by potential employers as well. In addition a good laboratory course should offer the possibility to fabricate student projects through the MOSIS Educational Program [1].

This report summarizes the development of a public-domain standard-cell library that supports a fully automated design flow for synthesis with Synopsys Design Compiler and P&R with Cadence Silicon Ensemble. This paper also addresses how this design flow is utilized within a one-semester VLSI system design course. The main objective was to support a contemporary sub-micron feature size and the layout editors Magic and Cadence Virtuoso. The synthesis process as well as P&R are script automated to enable students to rapidly use the tools without a steep learning curve.

In the following section, currently available libraries are discussed and in section 3 the newly designed cells are described. The report concludes with a description of the design-flow and the results of its use in student projects.

2 Existing Cell Libraries

Today, there are already several standard-cell libraries available, often free of charge for educational institutions. Virginia Tech offers an extensive library for the TSMC $0.25\mu m$ process [2]. However, this technology is not available with the MOSIS Educational Program. Alternatively, MOSIS provides a standard-cell library with documentation, as developed by Tanner Research. However, these cells are intended for use with the L-Edit tools and all cell characterization data is also only available for Tanner tools. A third possibility is the use of a commercial standard-cell library for the AMI $0.5\mu m$ process. However, AMI Semiconductor libraries are not available to the general public.

It can be concluded that none of the currently available standard-cell libraries are suitable for this desired purpose. Therefore, a new standard-cell library according to the MOSIS submicron scaleable CMOS (SCMOS_SUBM) rules is developed, making it possible to use the cells for the AMI $0.5\mu m$, which allows fabrication through the MOSIS Educational Program. This new library is based on ideas from a small library from Mississippi State University [3].

3 Cell Development

This section illustrates how the cells were created and gives more background on the library as a whole. The routing grid is chosen to be 10λ for metal1 and metal3, and 8λ for metal2. This is because metal1 and metal3 are designated for horizontal routing, while metal2 is chosen for vertical routing. This results in a 1:1 ratio between metal1 and

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metal3 that is suitable for fast routing in Cadence Silicon Ensemble. The cell height is chosen to be 100λ. All cell pins are placed on grid points, thus avoiding slow off-grid routing. Whenever possible, pins are staggered, allowing for easier pin access by the router. Table 1 summarizes all cells that are currently available in the first release of the library. Various drive strengths are available and more cells will be added with time.

During placement, every other row is flipped, allowing for overlapping power supply rails and creating a very dense layout without routing channels. Pins are equally distributed around the core area. Pad cells are integrated into the library and included if so desired. In that case, the floorplan is automatically chosen to create overall dimensions of 0.5mm by 0.5mm, the size of the MOSIS tinychip frame unit for the educational program.

The Cadence Abstract Generator is used to prepare the library for use with Cadence Silicon Ensemble. The final result is a LEF-file, containing abstracts for all cells. The cells are characterized with Cadence SignalStorm (previously from Simplex). The timing and power consumption numbers for the lib-file are obtained with non-linear models in four-by-four wide lookup tables. Backanotated libraries for Verilog and VHDL are available as well.

Table 1. Standard Cell Library

Cell	Purpose
inv	Inverter
nand2, nand3	Two and Three-Input NAND
nor2, nor3	Two and Three-Input NOR
and2	Two-Input AND
or2	Two-Input OR
xor2	Two-Input XOR
dffpos	Positive Edge D-Flip Flop

4 Design Flow

The design flow hides as many details as possible, such that students focus on their design and not on the details of the underlying synthesis and place and route tools. The library comes with a set of script templates. All parameters work for a wide variety of designs, such that the students only have to insert the file and module names of their particular design. Editing these scripts and running them, typically takes less than five minutes.

Synthesis is performed with Synopsys Design Compiler. Students can choose, whether the design should include pad cells or not. Cadence Silicon Ensemble is used in script mode and performs both, placement and routing. Several parameters can be adjusted by advanced students to control the resulting layout that is output in GDSII format. A final script automatically creates a DFII database for Cadence IC-Tools and/or a Magic design from the GDSII file. Finally, a tape out script prepares the submission to MOSIS.

5 Results and Conclusion

The presented design flow has been tested in a large VLSI class for senior undergraduate students. The students have completed introductory digital logic design and basic electronic circuit design courses. Final semi-custom design projects are implemented in teams of two students each. Overall the course has high approval ratings and students generally are satisfied with their progress.

The standard-cell library and design flow have been verified through several fabrication runs at MOSIS and work as expected. The automated flow makes it possible for students to focus on the Verilog coding and to gain experience in design styles suitable for synthesis. The automation with scripts takes away many interfacing problems between tools and teaches students to save time and energy by automating tasks with scripts. Finally, the library can easily be extended or modified since all steps of the library development process are available and documented [4].

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