

# AES Encryption over PCI Express

## Design Review

Zack Curosh  
Matt Swanson  
Jevin Sweval

# Advanced Encryption Standard (AES)

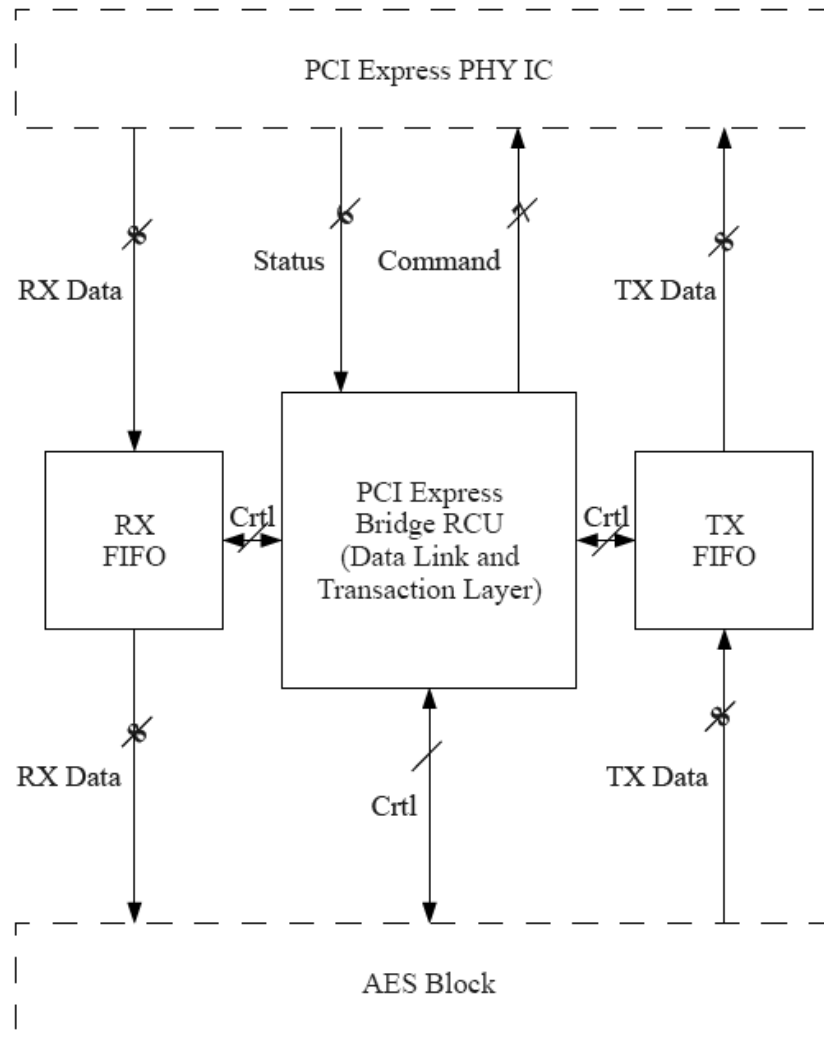
- US government encryption standard since 2002
- Based on Rijndael cipher
- AES is fast in hardware and requires little memory
- User inputs an encryption key and then data in 128-bit blocks
  - Key may be 128, 192, or 256 bits long

# Our Design

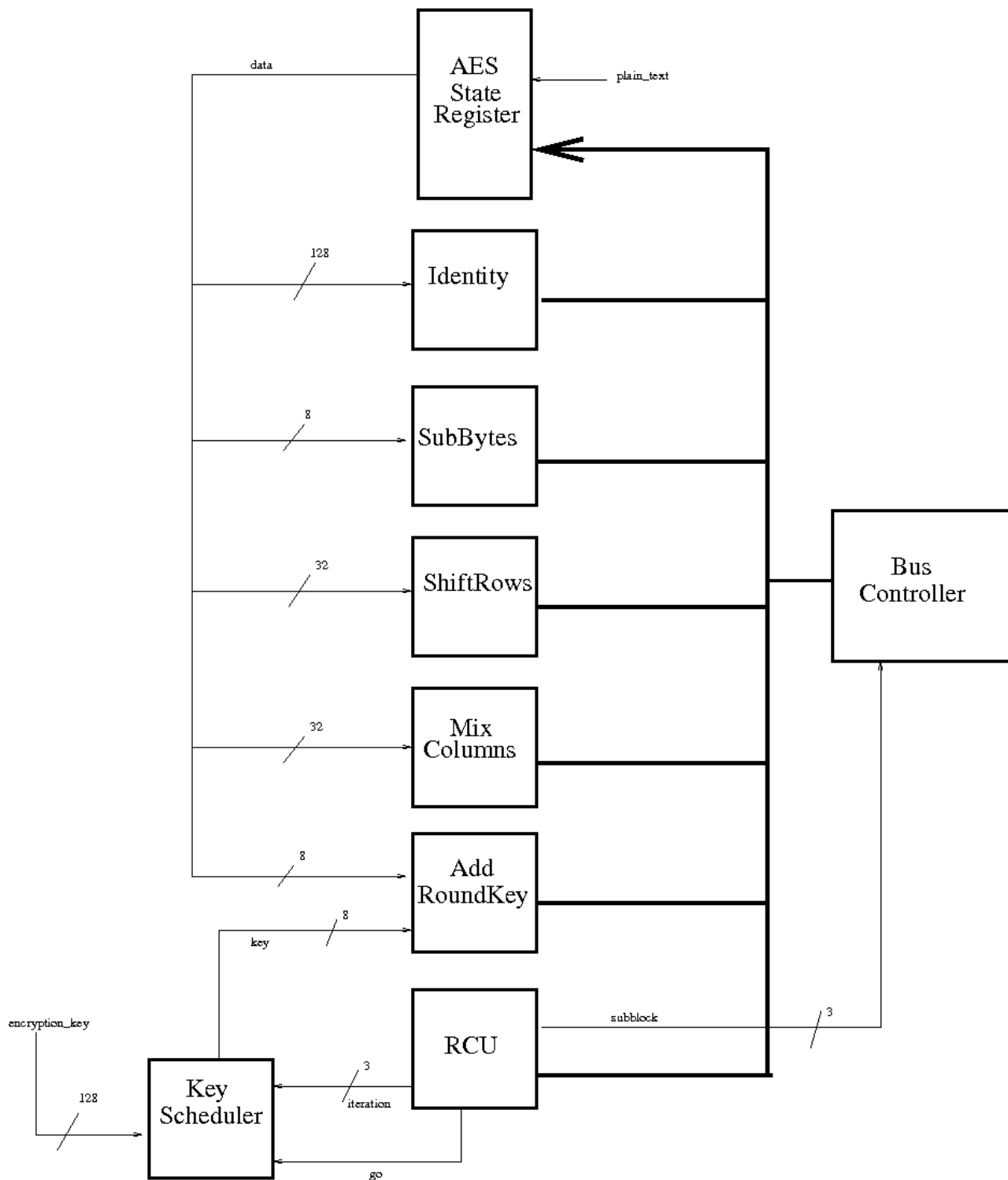
- 128-bit key AES core
- I/O will be done using PCI Express protocol
  - PCI Express bridge: we design
  - TX/RX FIFOs: gold\_lib
  - PCI Express transceiver: external hardware
- Hardware implementation gives high-throughput and low power
- PCI Express selected for high performance and widespread use

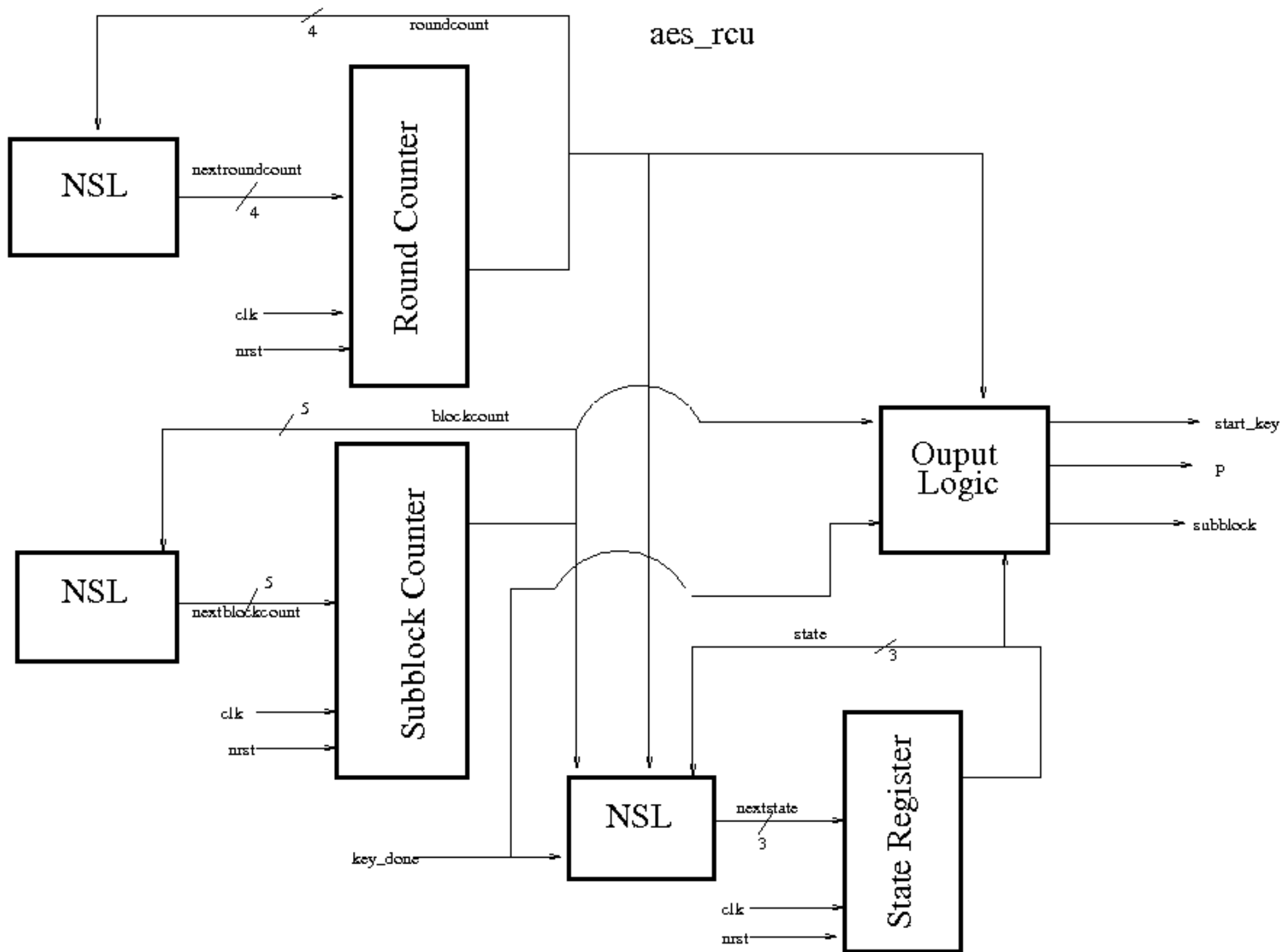
# System Level Diagram

NXP PX1011B  
PCIe PHY IC

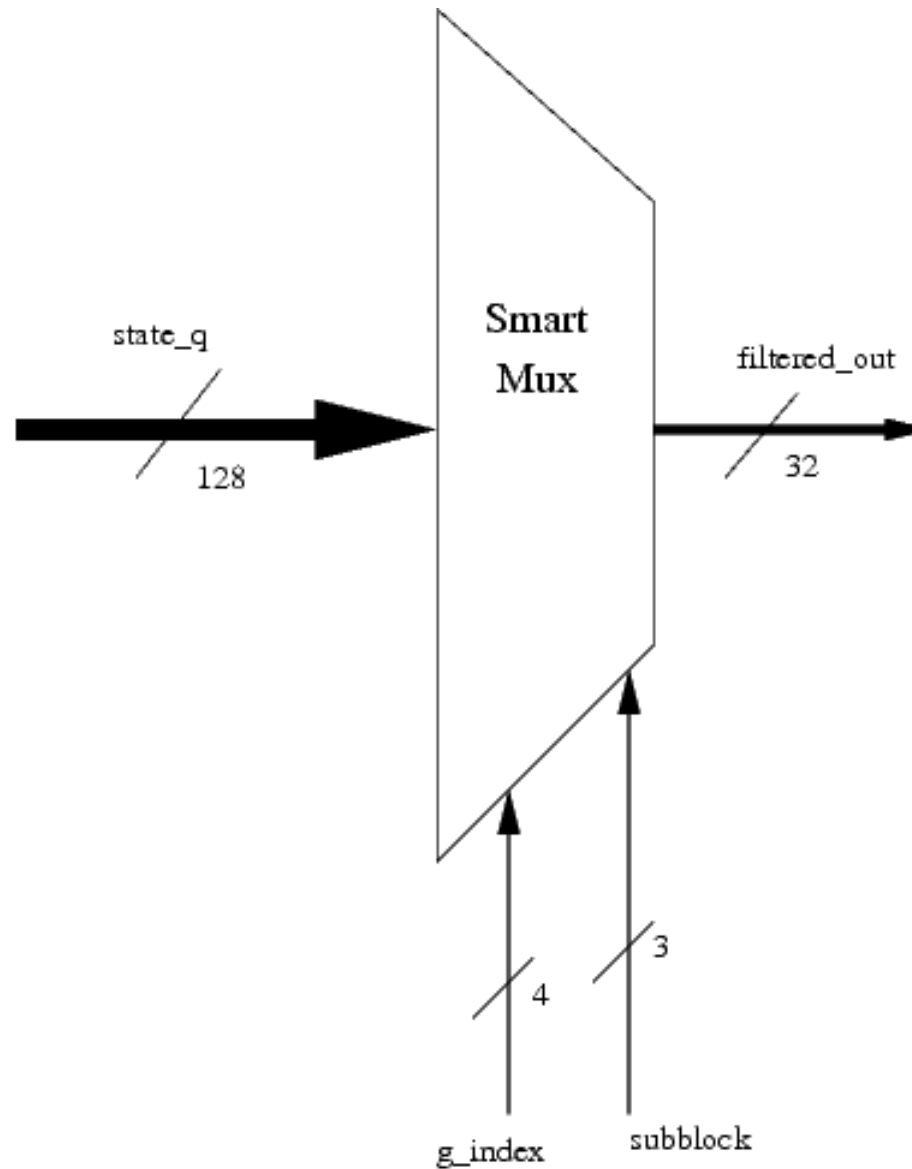


# AES Top Level Diagram

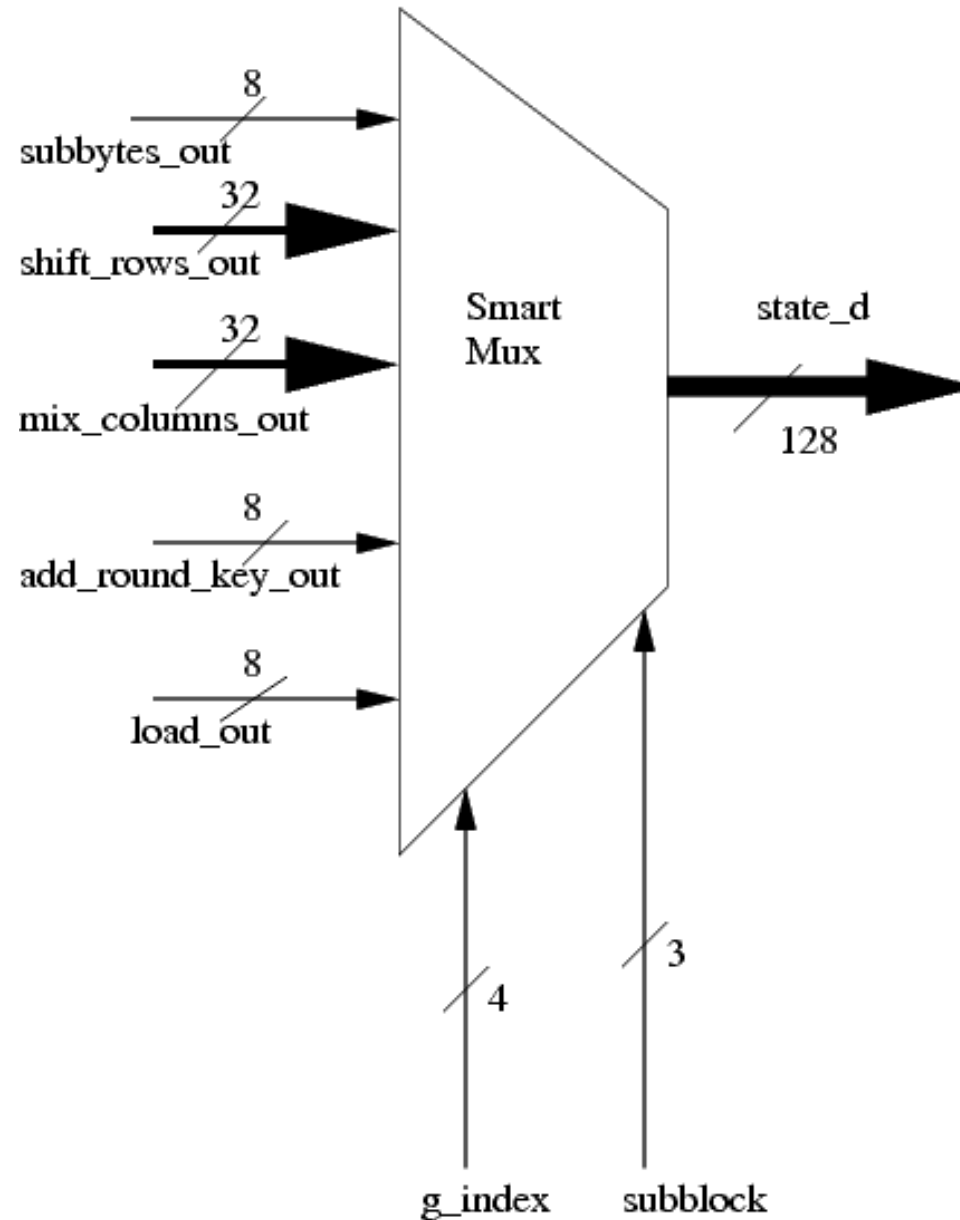




# bus\_controller (from state)

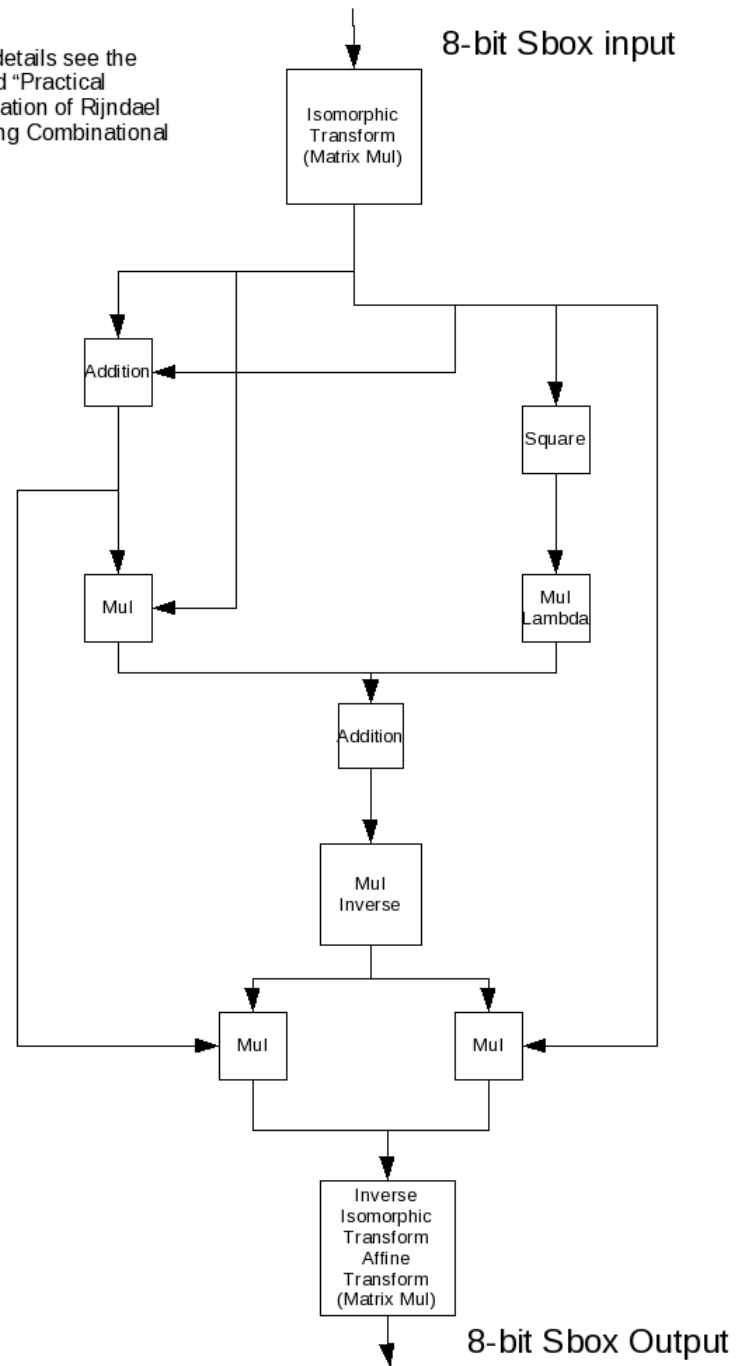


# bus\_controller (to state)

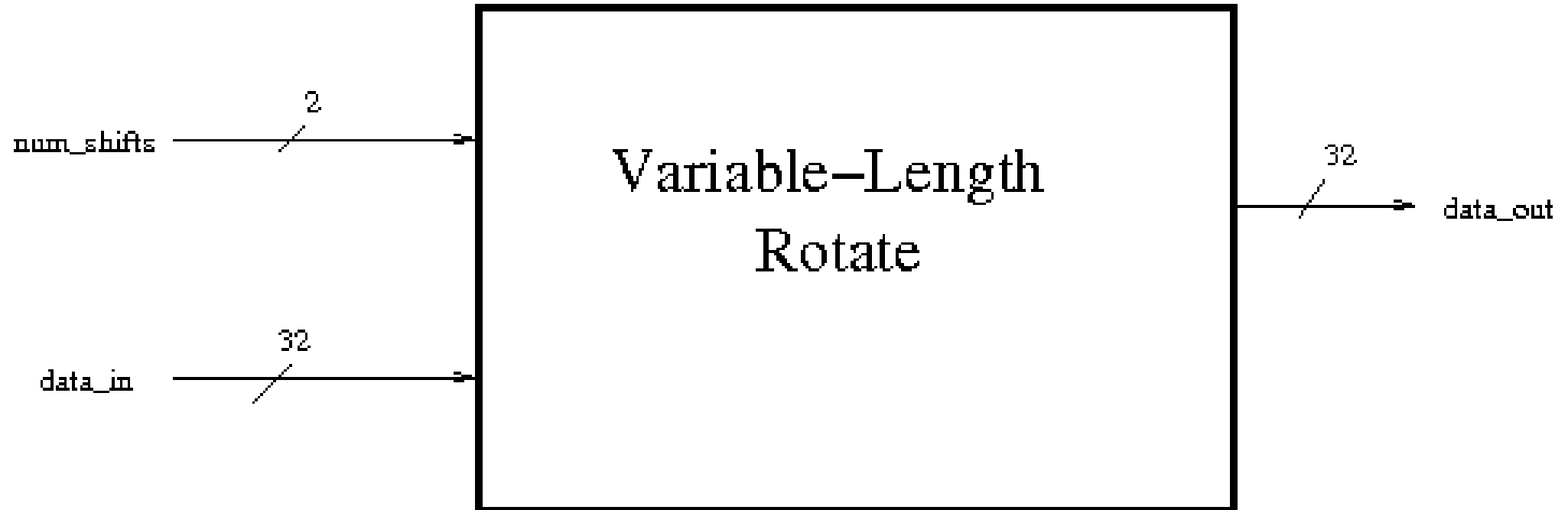




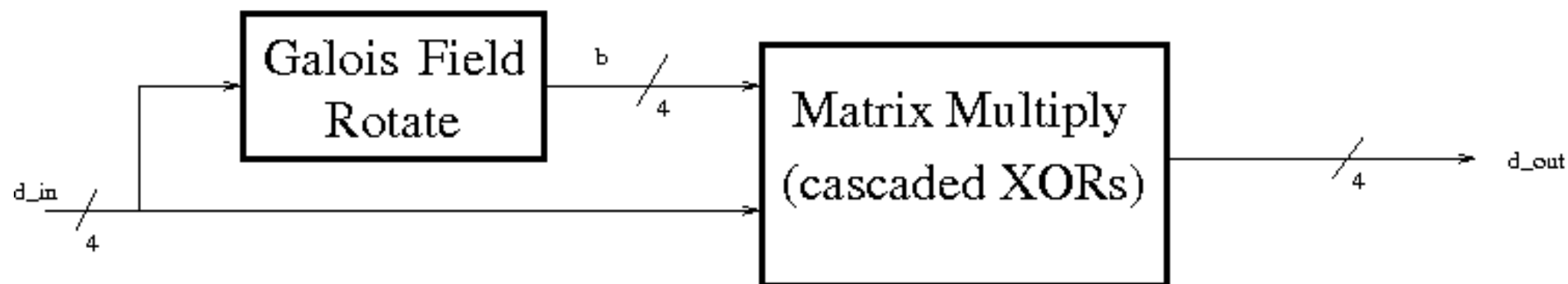
For more details see the  
paper titled "Practical  
Implementation of Rijndael  
S-Box Using Combinational  
Logic"

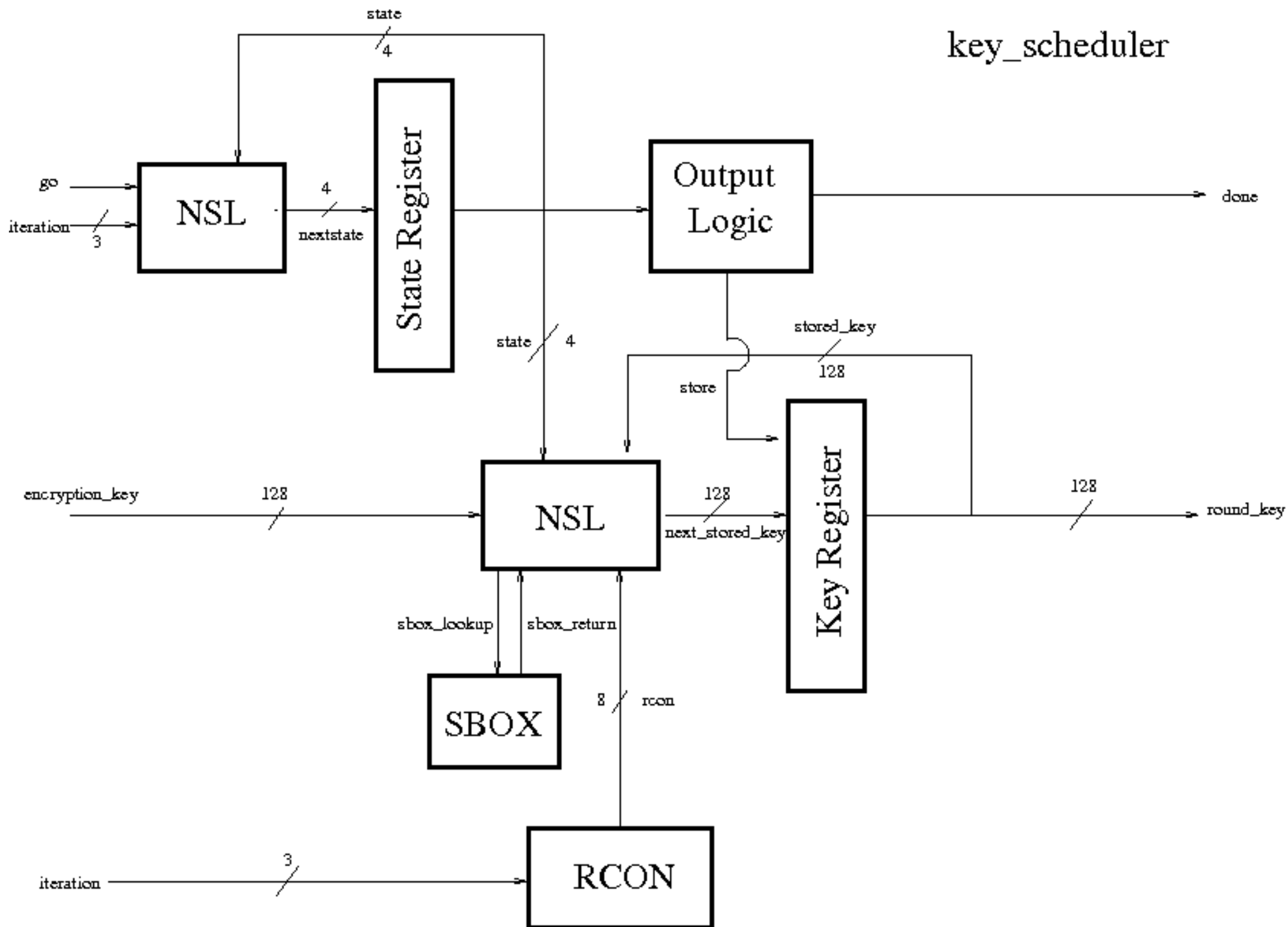


shift\_rows

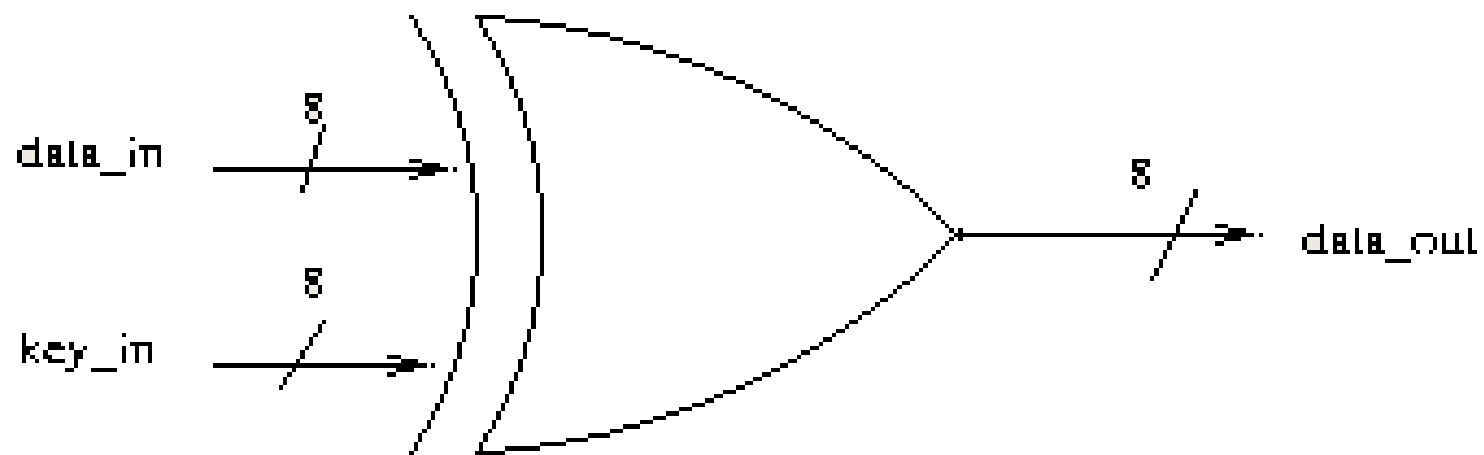


mix\_columns

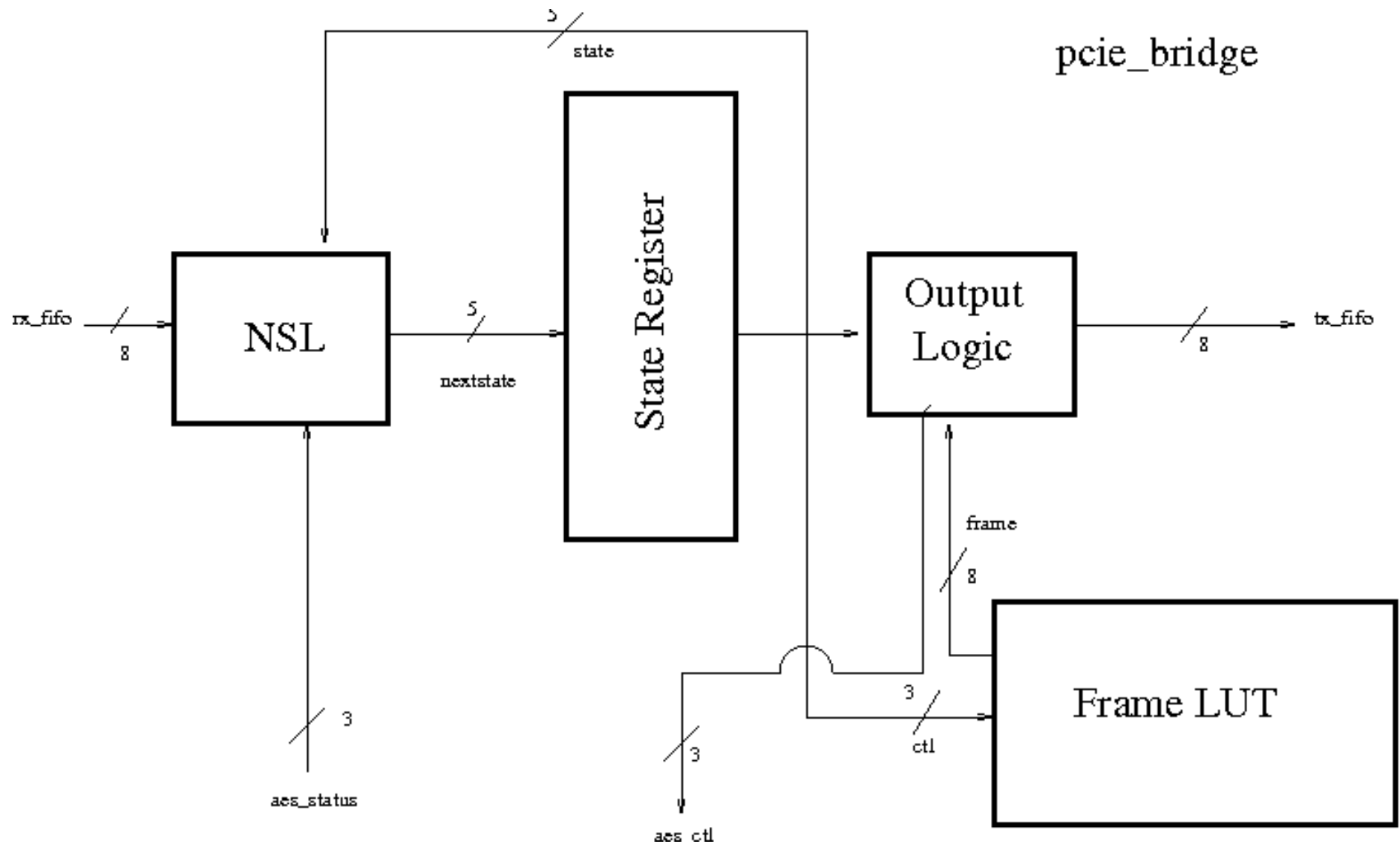




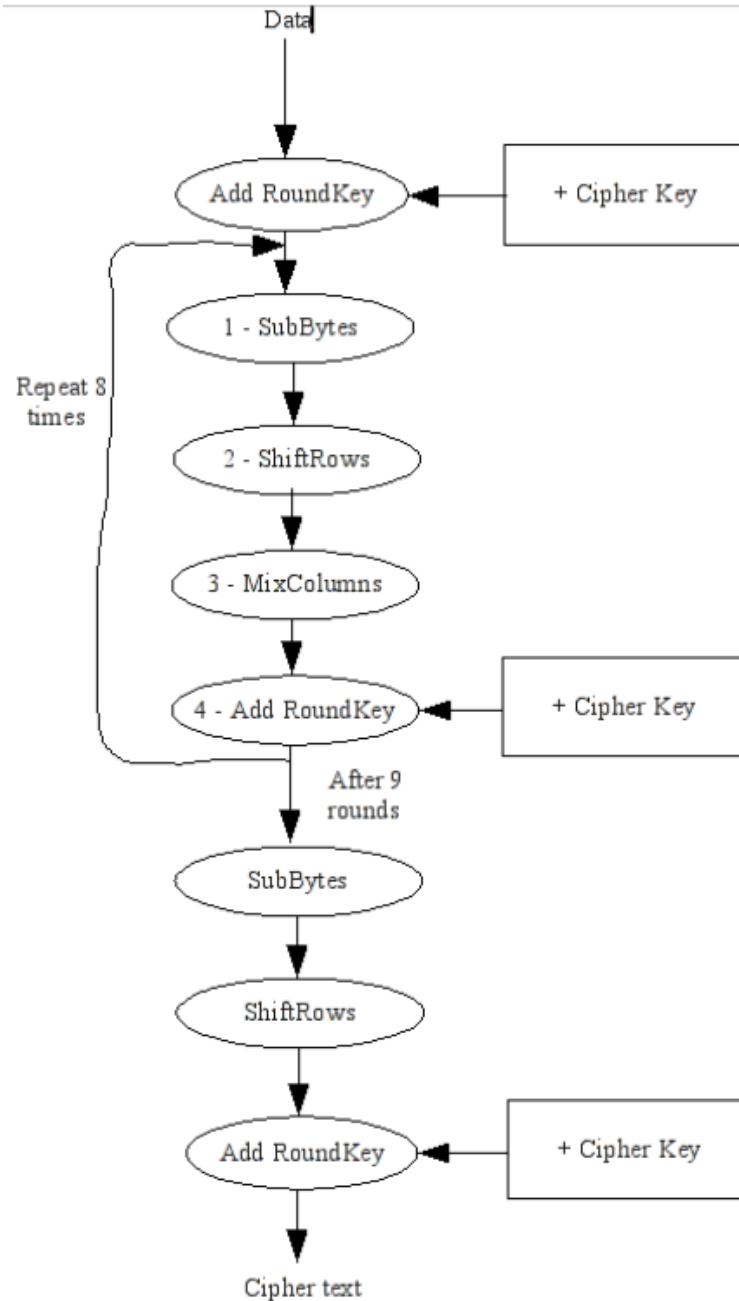
# add\_round\_key



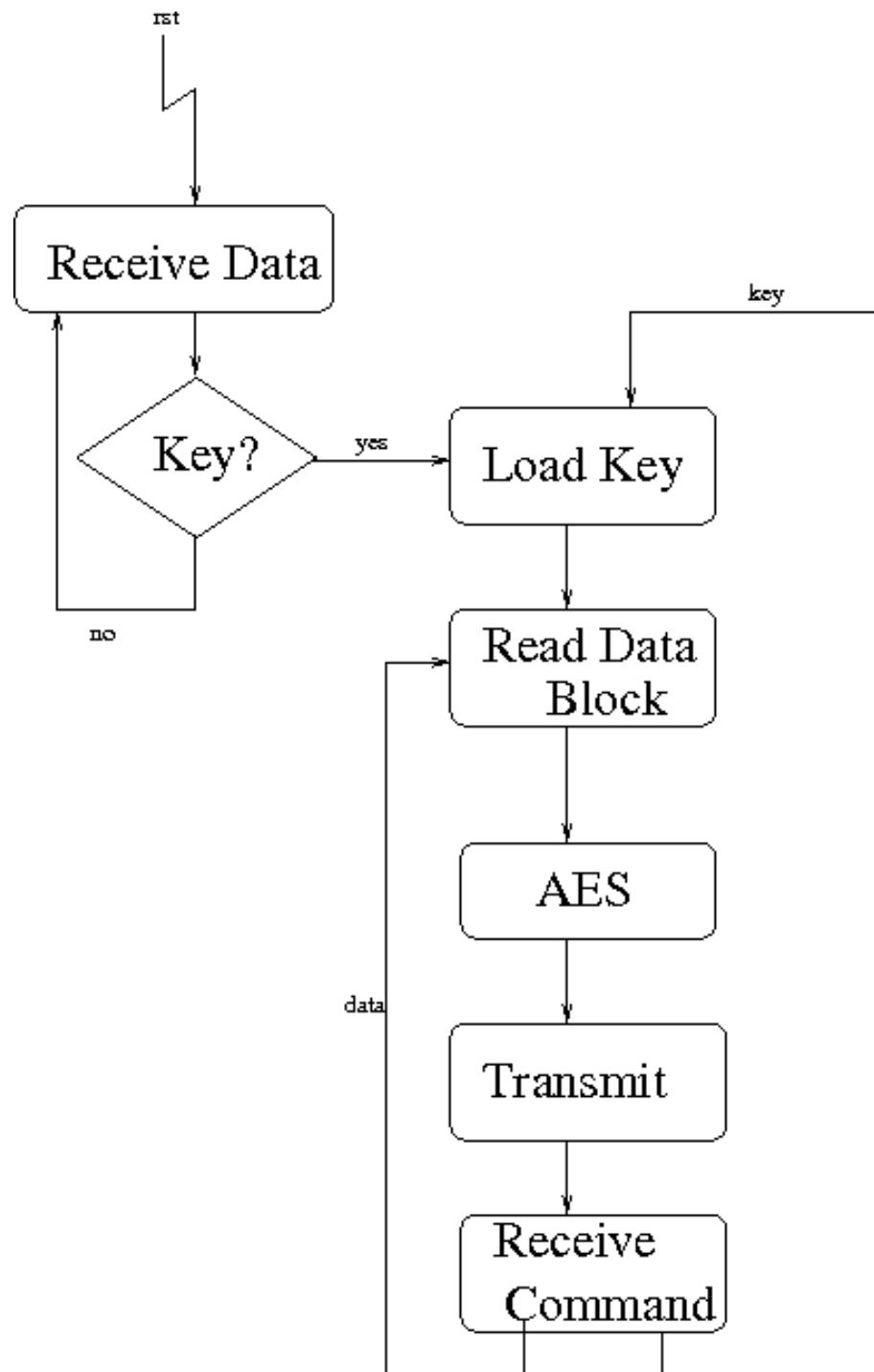
# PCIe Bridge Diagram



# AES Flowchart



# PCIe Bridge Flowchart





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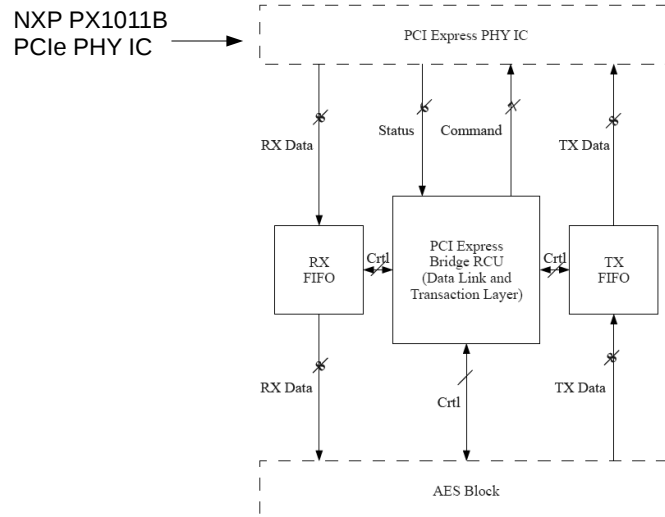
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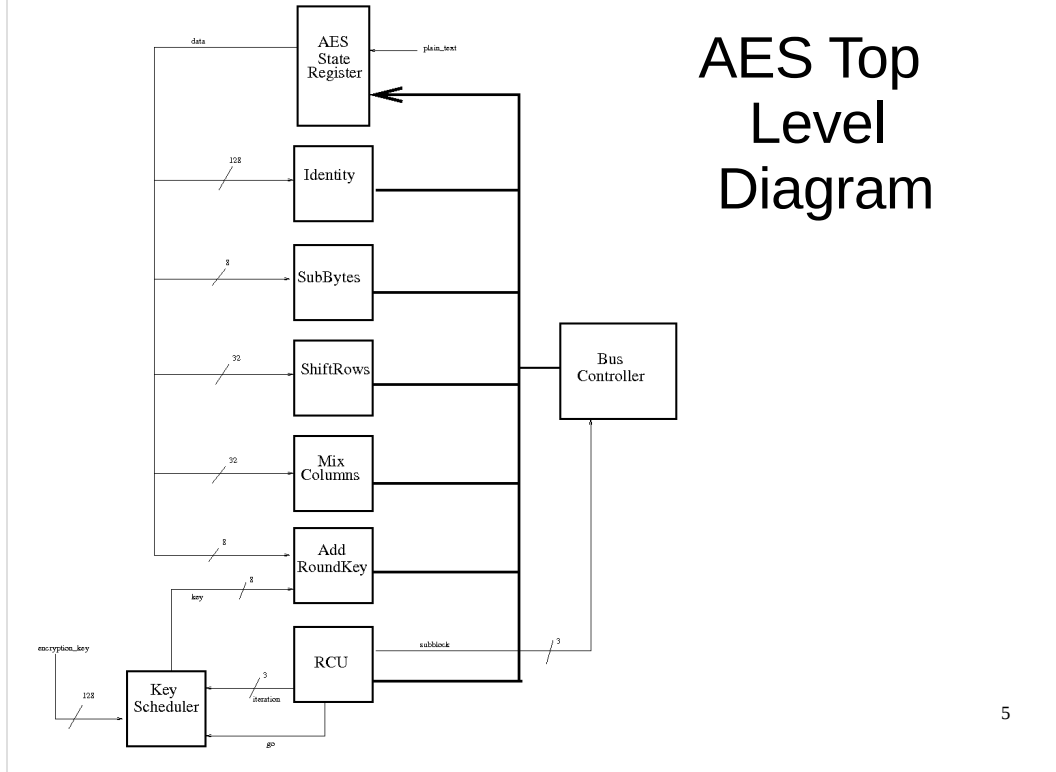
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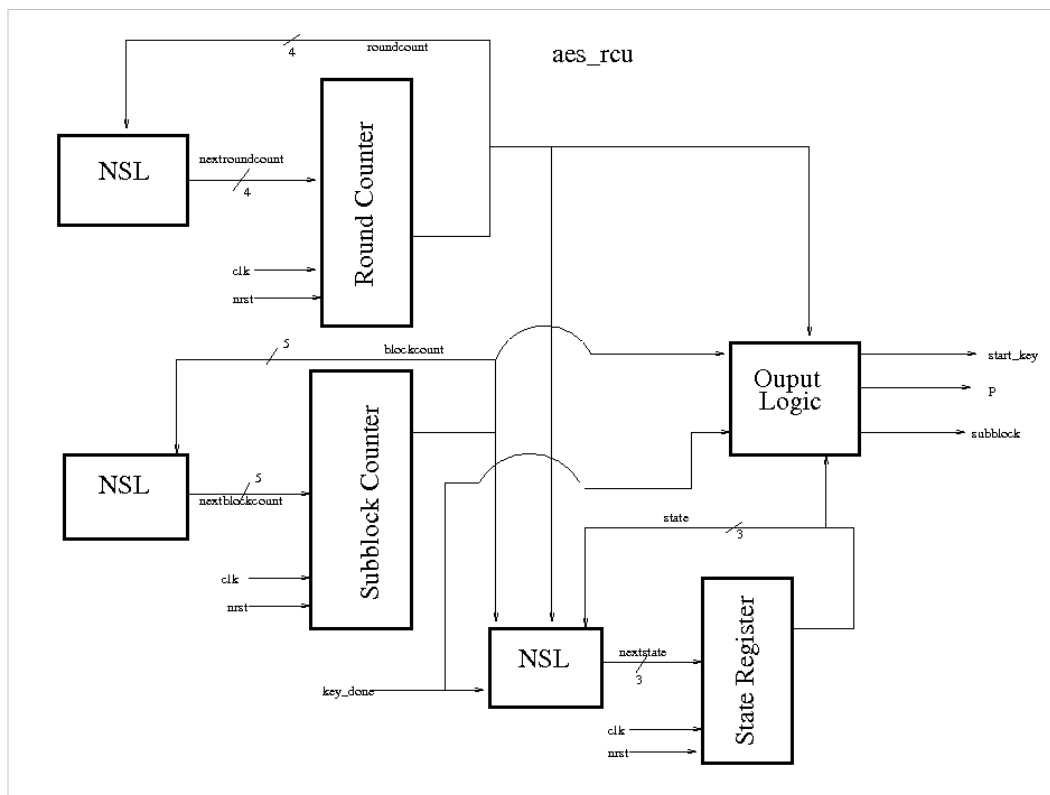
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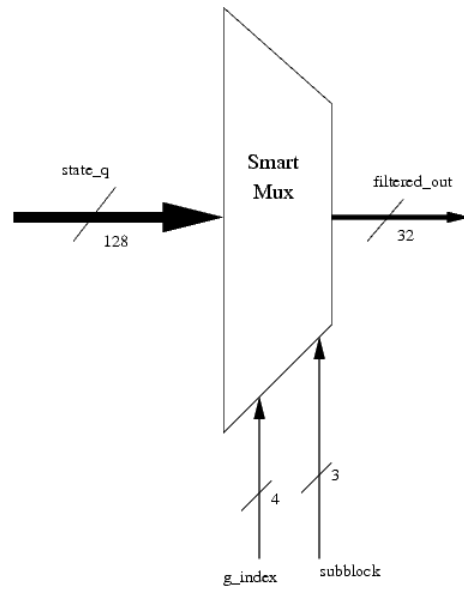


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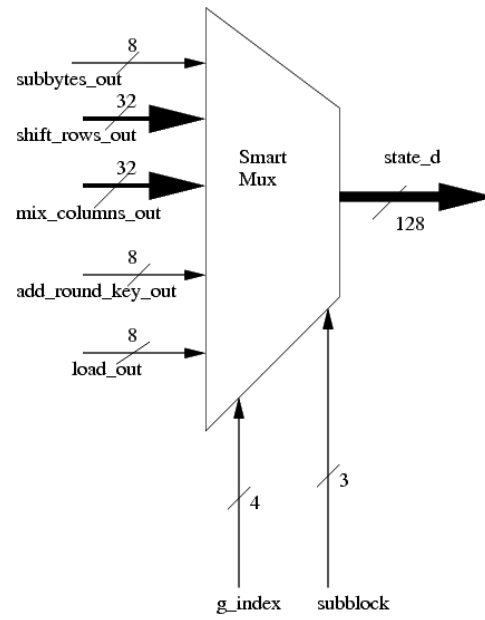




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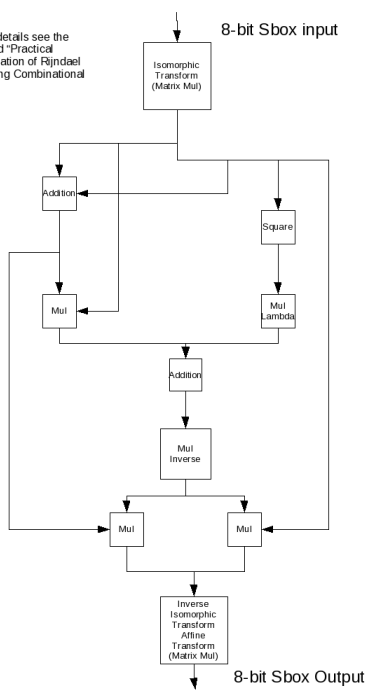


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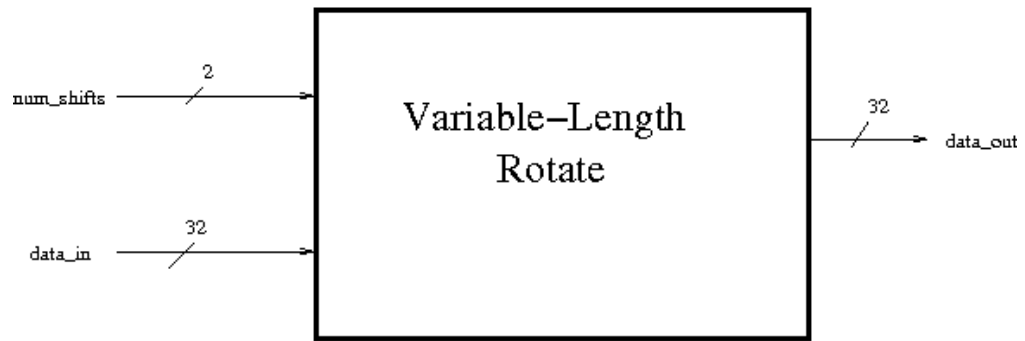




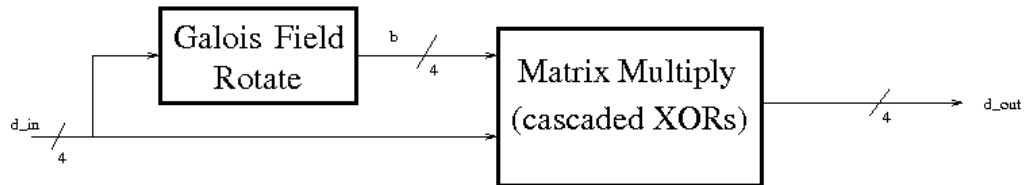
For more details see the paper titled "Practical Implementation of Rijndael S-Box Using Combinational Logic"

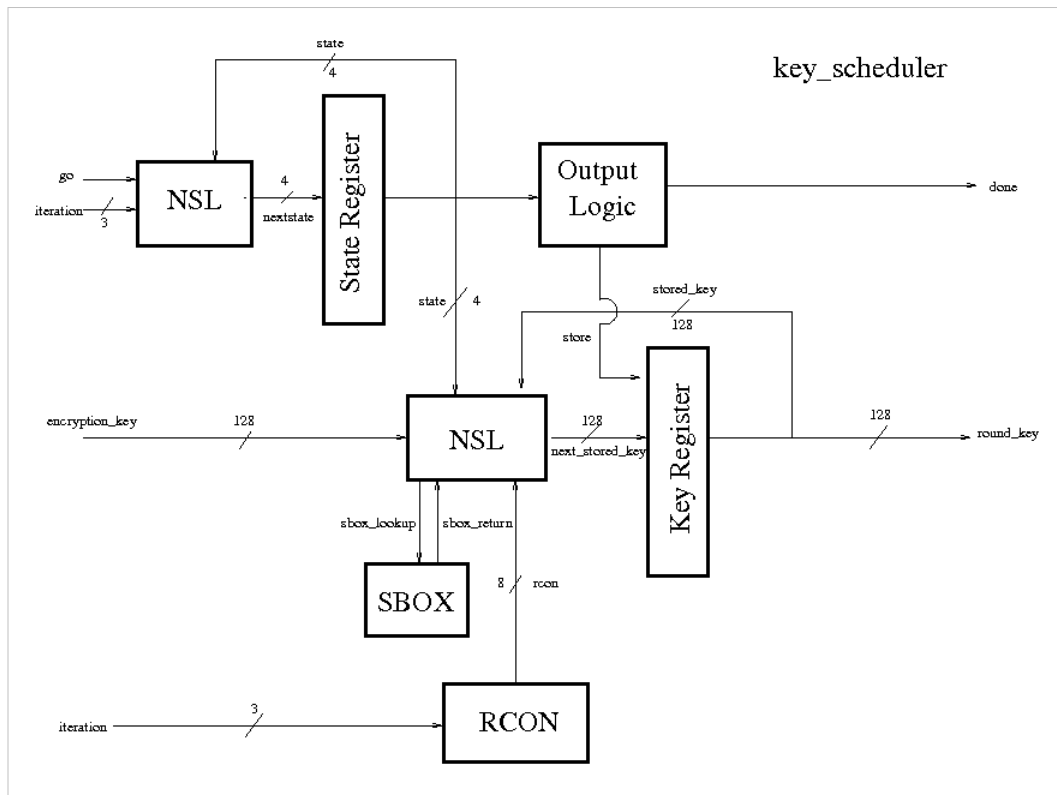


shift\_rows

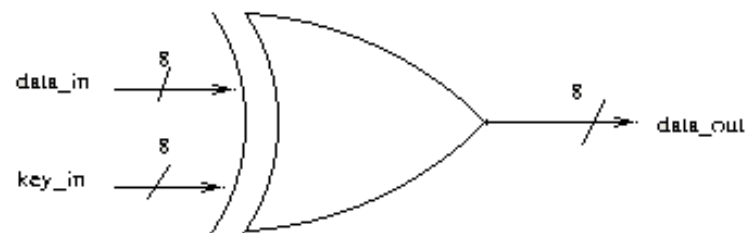


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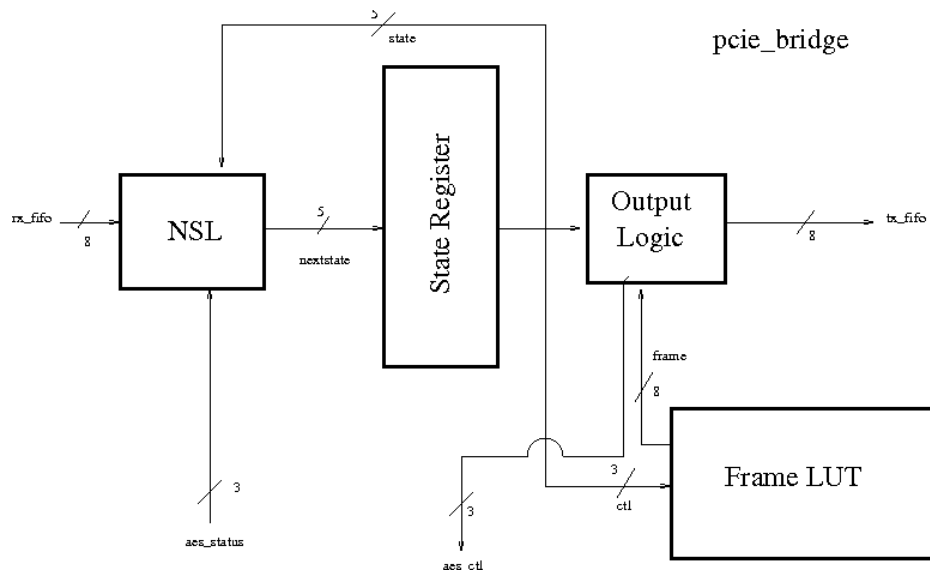




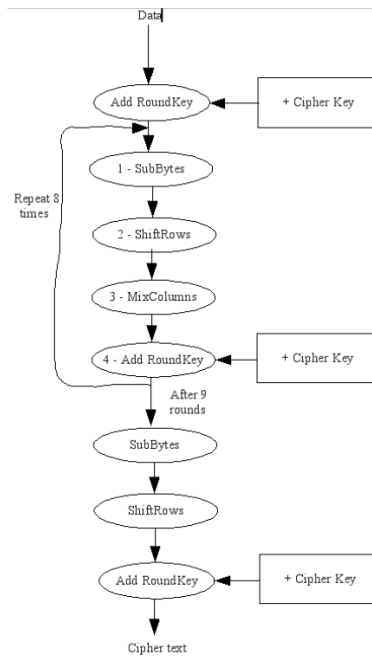
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