Christopher R. Aberger

caberger@stanford.edu 608-738-8876

Education

Stanford University, Palo Alto, California
Master of Science in Electrical Engineering **Expected Spring 2015**

University of Wisconsin, Madison, Wisconsin
Bachelor of Science in Computer Science
Bachelor of Science in Computer Engineering
Minor in Mathematics **May 2013**
Cumulative GPA: *3.9/4.0*

Zhejiang University, Hangzhou, China
Technical communication and Mandarin course **Summer 2009**

Professional Experience

Stanford University, Palo Alto, California
Research Assistant for Professor Kunle Olukotun **Current**
Implementing a domain specific language for large-scale graph analytics. Parallel algorithms, with an emphasis on functional programming, available to end-user.

Apple Inc., Austin, TX
Design Performance Intern **Summer 2013**
Performance analysis of mobile A7 chip design through software modeling.

IBM, Austin, TX
Hardware Engineering Co-op **Summer 2012**
Functional verification and lab bring-up procedures for Power8 chip.

Epic Systems, Madison, WI
Finance Intern **Summers 2010, 2011**

Skills

C, C++, Java, JavaScript, Python, Perl, SQL, OpenGL, WebGL, XML, Scala, Verilog, VHDL, Haskell, Matlab

Awards

2010-2011, International Engineering Consortium Everitt Award Winner
2009, 2010, Claude and Dora Richardson Engineering Scholarship
2011-2012, Tau Beta Pi National Scholar
2012, Fred W. and Josephine H. Colbeck Scholarship Award
2010, Polygon Excellence in Engineering Scholarship
2008-2012, Wisconsin Academic Excellence Scholarship
2008, La Crosse Community Foundation Engineering Scholarship
2008, La Crosse Central High School graduation rank: 1/317

Selected Design Projects

WebGL Demo **Spring 2013**
Open ended graphics course project implemented in JavaScript using the WebGL API. Learned how to utilize a device's GPU in a browser without plugins. Built a low-level, self-contained, extensible graphics library.

Consolidated Rename Issue & Bypass **Spring 2012**
Team leader in designing an advanced academic microarchitecture. Synthesized and flashed to a Xilinx Virtex II board with minimal I/O system, RS232, and VGA Display.