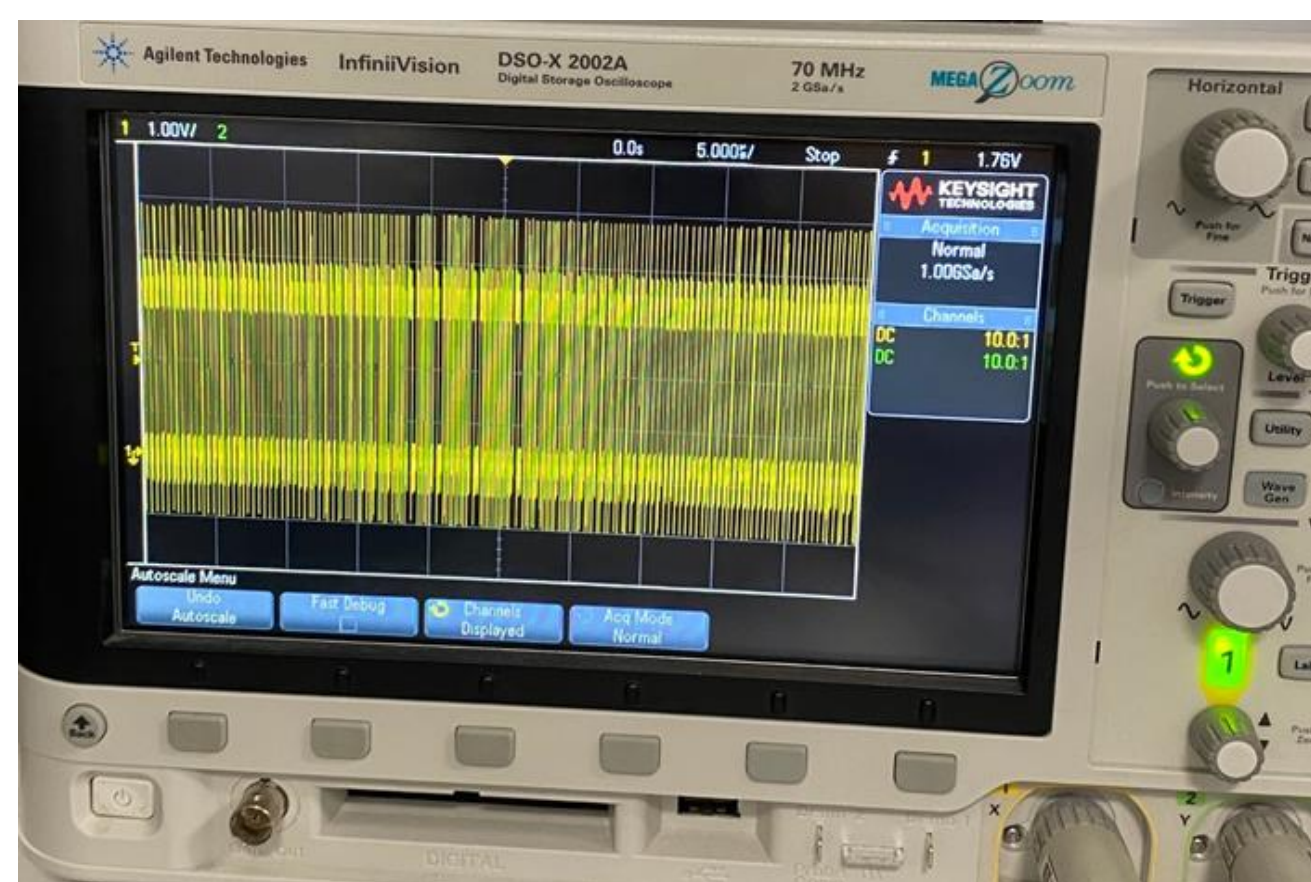


Introduction

Underwater communications are very important to enable civilian and military application such as sensor networks, offshore exploration, pollution monitoring and underwater surveillance. However, laying down fiber cables on seabed is hugely expensive task; also the electromagnetic waves does not propagate well under the surface of the ocean. Hence, the use of acoustic signals can be an alternative solution to these problems.

Objectives

- Pre-process a Pulse Density Modulated (PDM) waveform using a filter and provide the appropriate amplitude to the input of the power amplifier.

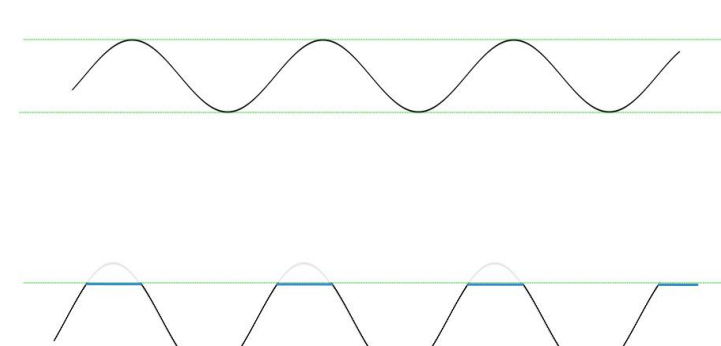


- The circuit will fit into a watertight enclosure that will be deployed in the ocean and function autonomously.
- The circuit should be mechanically able to support a Field Programmable Gate Array (FPGA) board and a power amplifier.

Circuit Flow

The series of events the signal undergoes is as follows:

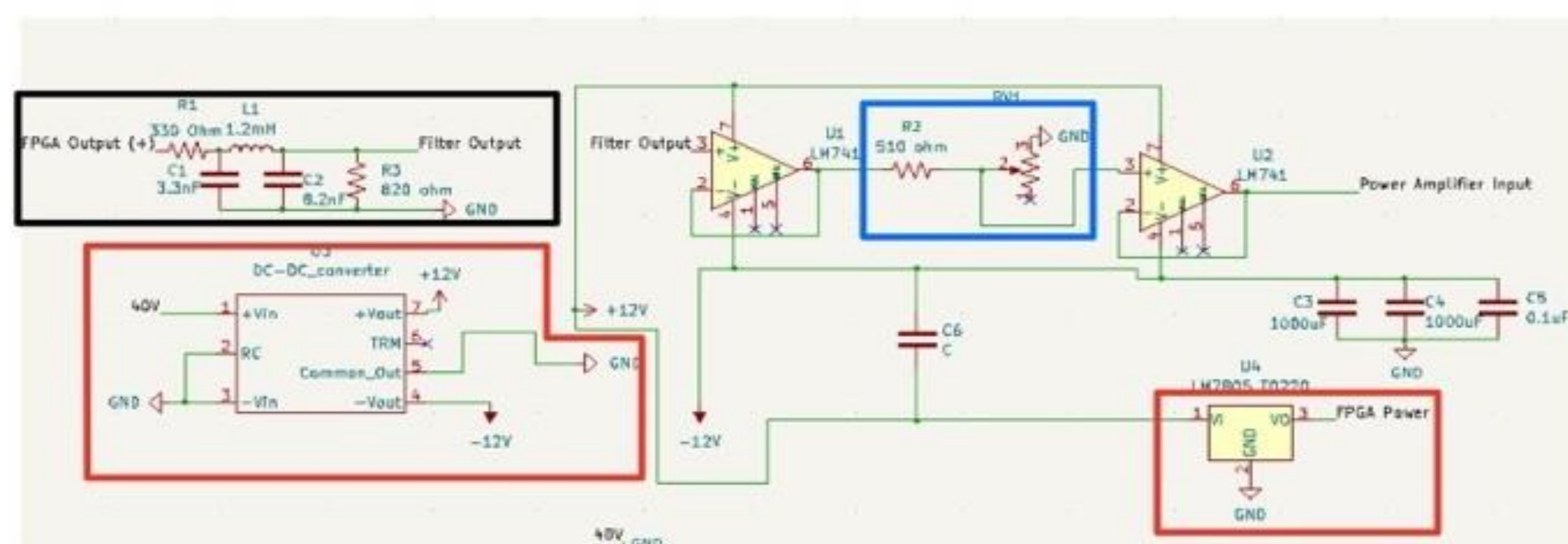
- The FPGA digital output signal is passed into a 3rd order Butterworth filter with a cut-off frequency at 85KHz. The filter recovers the enveloped signal.
- The filter output then becomes the buffer input. The buffer prevents the filter's output impedance from loading on the control system's output impedance, which stops undesirable loss of signal transfer, and reduces noise.
- The buffer's output is passed to the control system consisting of a resistor and a potentiometer. The potentiometer varies the signal's output amplitude. The importance of the control system is to prevent the signal's amplitude from being out of the receiver's range, which results to signal clipping.
- The control system's output is finally passed to a second buffer to reduce noise and loss of signal transfer. The output of the second buffer goes to a power amplifier connected to a transmitter



Circuit Architecture

The circuit board has 3 sub-systems:

- Filter System
- Control System
- Power System

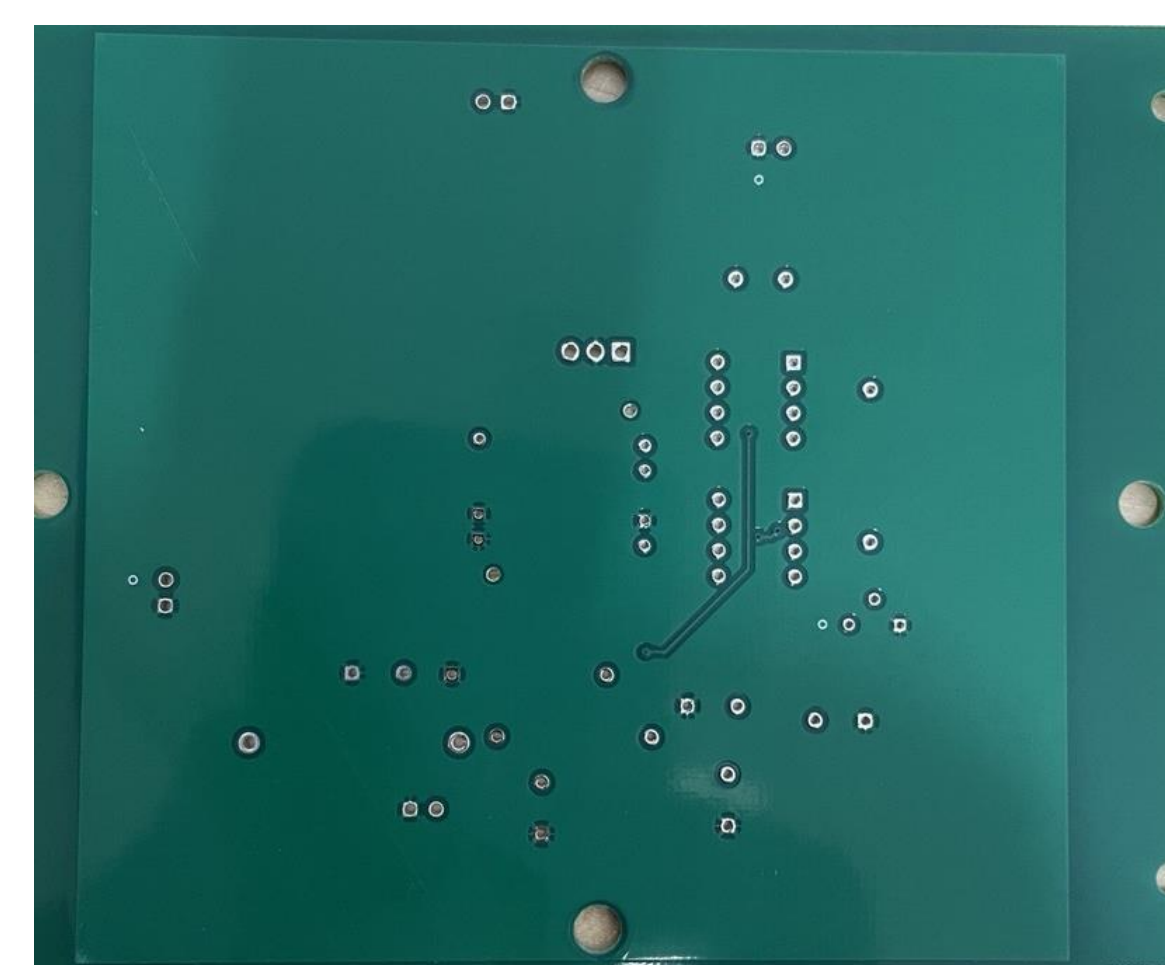


Filter Power Control

- To ensure our transmitter can work independently, I designed the PCB to be able to power up the buffers and FPGA using a DC-DC converter and a voltage regulator.
- The main power supply will come from 40V batteries.
- To reduce noise transmission in our system, capacitors and op-amps were used.

Board

- A PCB was designed using the AutoCAD software, KiCAD.
- Connectors were placed on the board edge to reduce wire length which may affect PDM signal, due to its 10MHz frequency.
- An error occurred in the design of the DC-DC convertor footprint. To improvise, wires were soldered to the footprint holes to supply voltage to the op-amps
- Electric zones were added to improve high and low voltage distribution



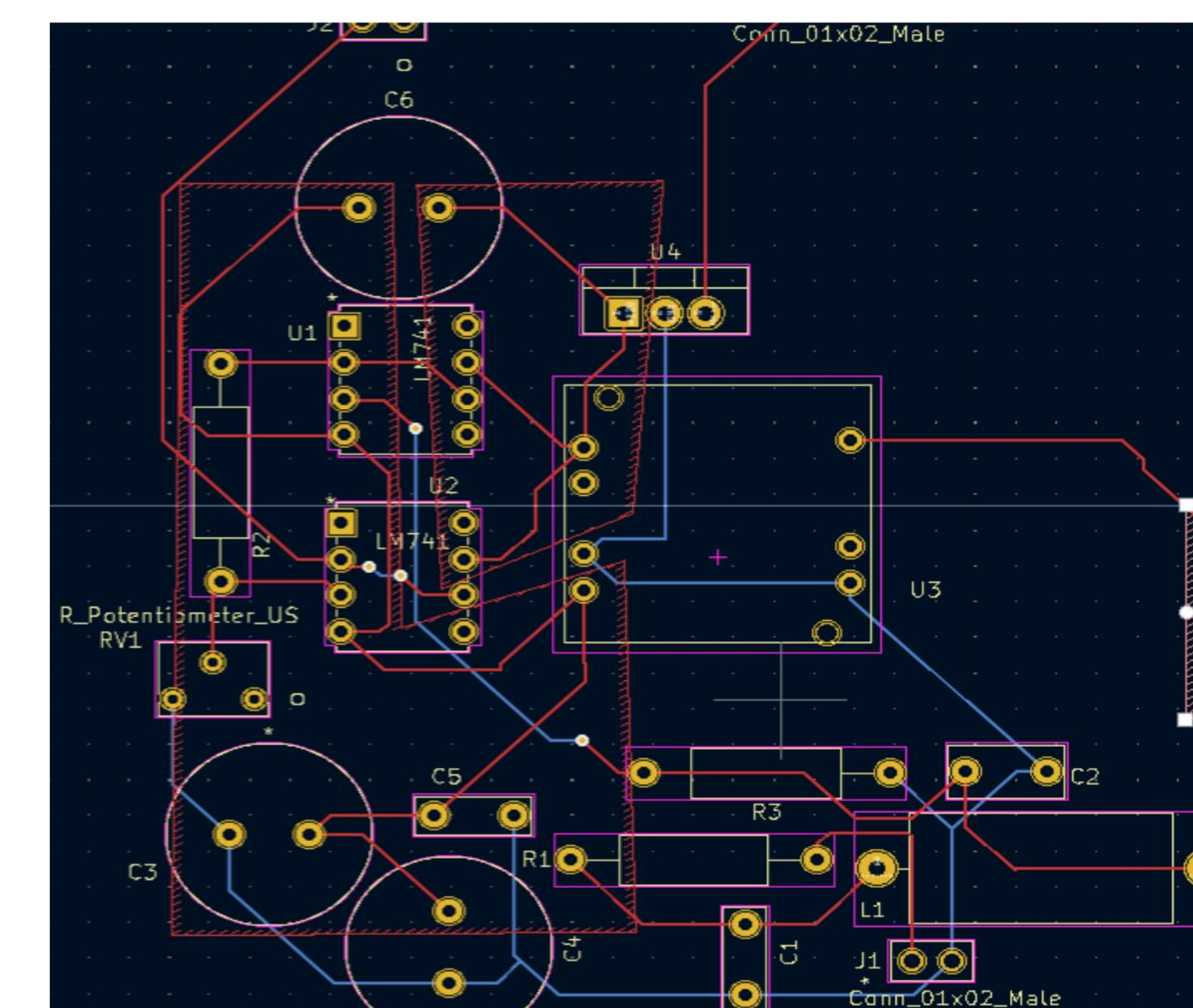
Noise was reduced by:

- Isolating high-voltage ground planes to prevent ground bouncing.
- Making a common zone for low-voltage ground planes

Future Work & Conclusion

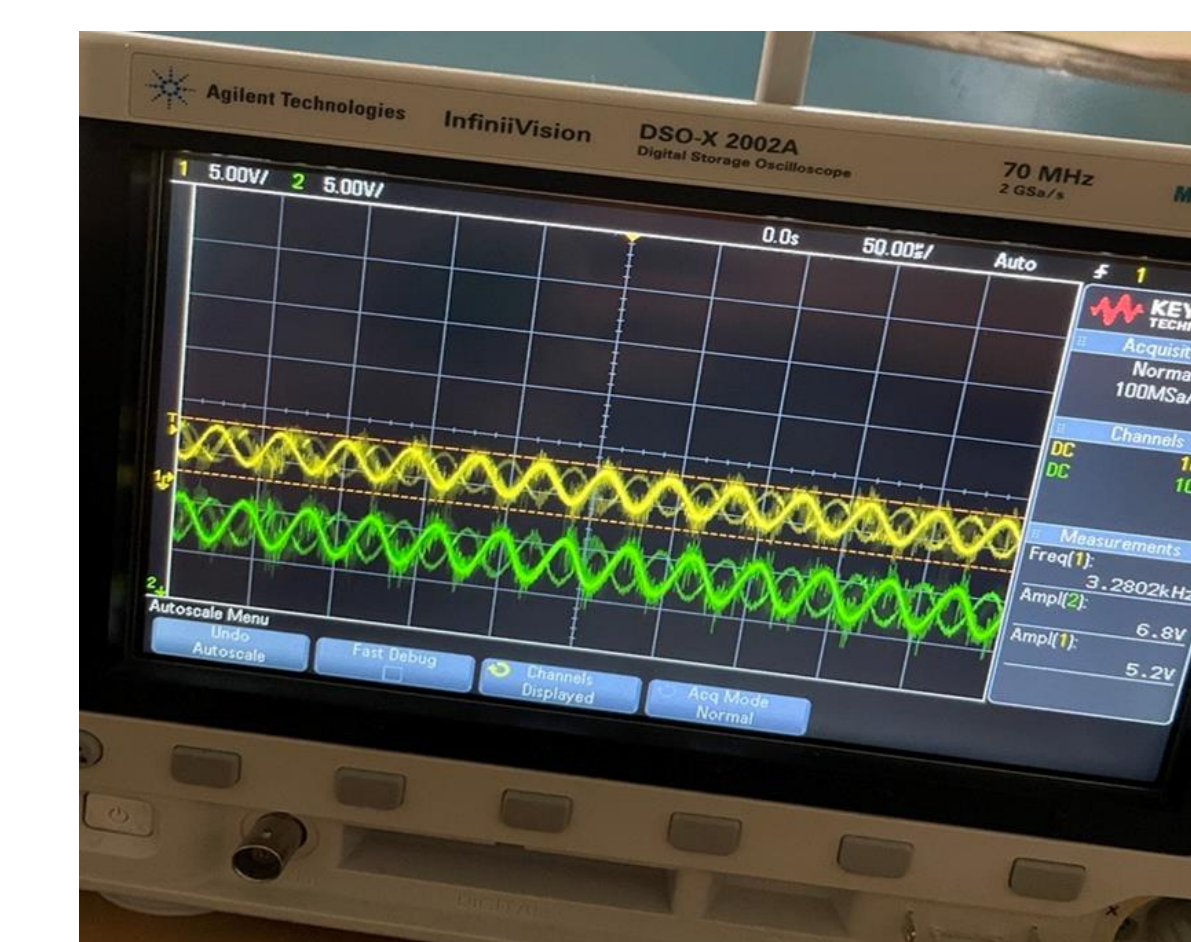
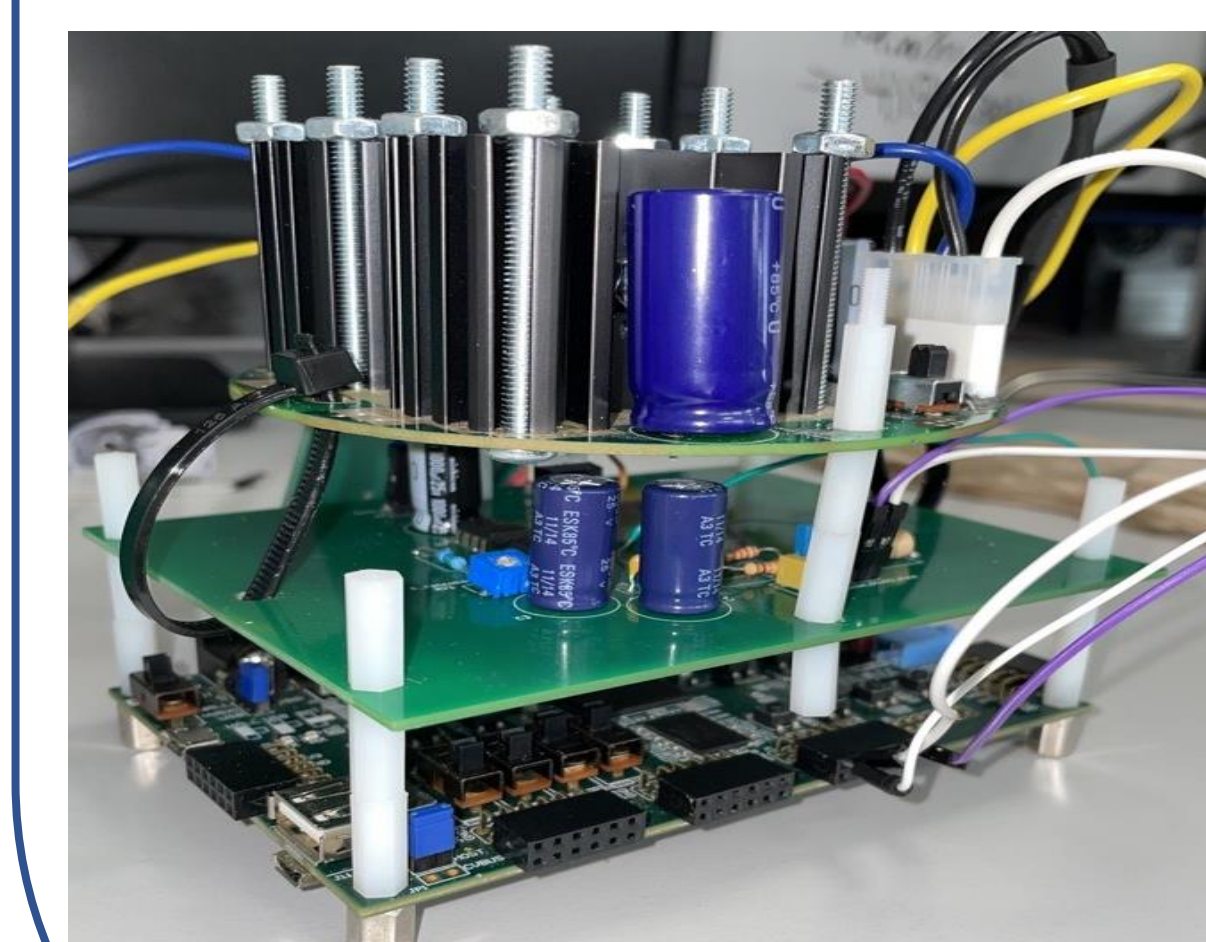
Transmitter needs to be made more autonomous by:

- Fixing DC-DC footprint design.
- Research, test, and analyse battery types to use in water-tight encasing
- Redesigning PCBs connecting the power amplifier to the load and power supplies.
- Make design more ergonomic by changing the position of potentiometer.



In conclusion:

- the board successfully decodes the encoded PDM signal and was able to control its amplitude.
- Noise levels are as minimal as possible.
- The board is mechanically able to support both FPGA and power amplifier
- The board's autonomous power feature requires minimal improvement



References

- Surinder. S, "Deployment Of A 27.5 KHz Link Using Non-coherent Space Time Block Coded Frequency Shift Keying"
- https://mackie.com/en/blog/all/what_clipping.html