# Basic Processor Components and Testbenches

## MUX5

Mux 5 takes in two 5-bit vectors and a selector bit which determines which 5-bit vector will be passed to the output.

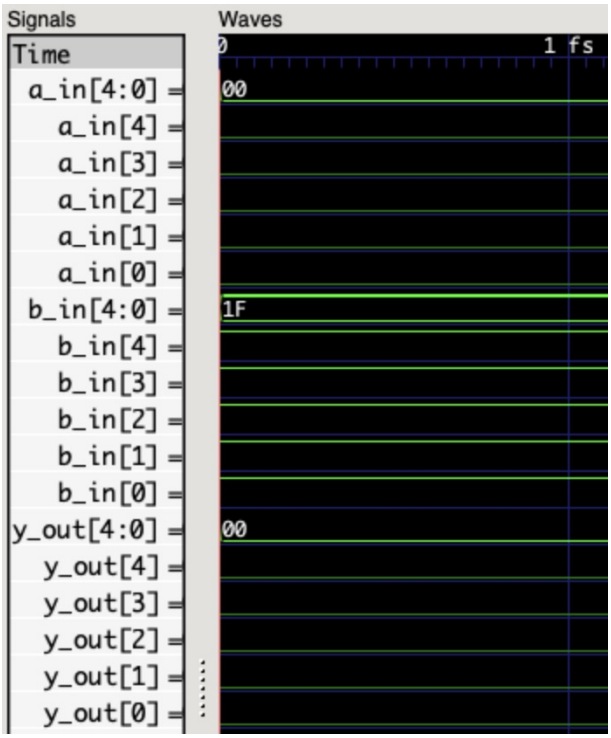


Figure 1: Mux 5 with Sel as '0'

## MUX64

Mux 64 takes in two 64-bit vectors and a selector bit which determines which 64-bit vector will be passed to the output.

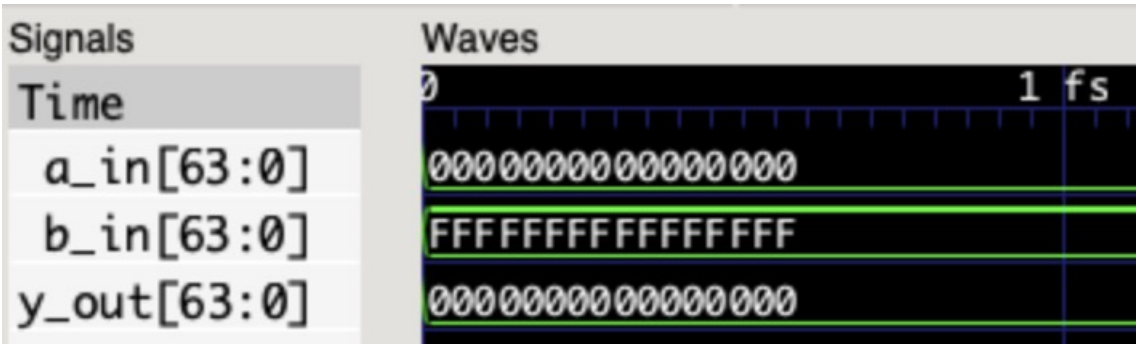


Figure 2: Mux 64 with Sel as '0'

## ShiftLeft2

Shift Left 2 takes in a 64-bit vector and shifts all of its bits 2 to the left, filling in the remaining space with 0s, outputting a 64-bit.

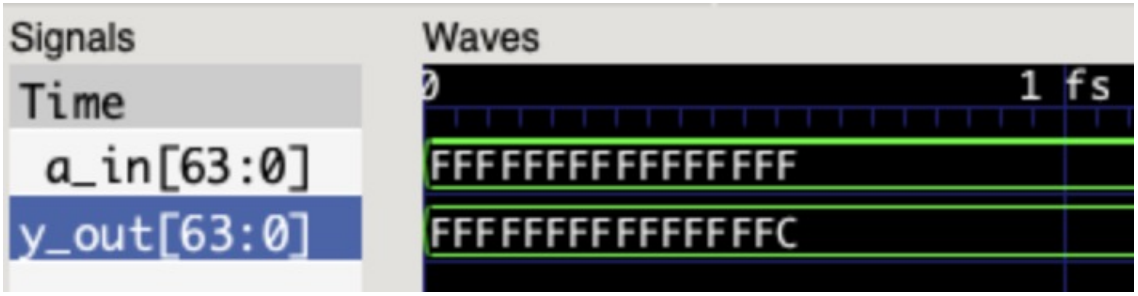


Figure 3: Shift vector array left by 2 bits

## SignExtend

Sign Extend observes the first bit of a 32-bit vector and fills in the remaining 32 bits with either 1 or 0 (+ or -), to output a 64-bit extension of the original vector.

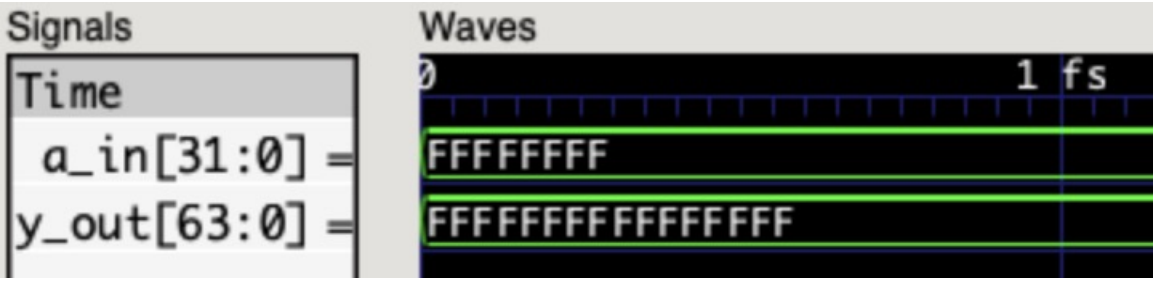


Figure 4: Sign Extend a negative sign ('1')

## Modeling Type:

I chose to use dataflow for all the components because it was used to describe simple input/output flow of data in the circuit. I then chose to use structural for all of my test benches as it allows me to set up a more complex set up including entities and port mapping components to then test its functionality.