MODULE 3: Boolean Algebra and Digital Logic

Lecture 3.6
Flip-Flops

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Lecture 3.6 Objectives

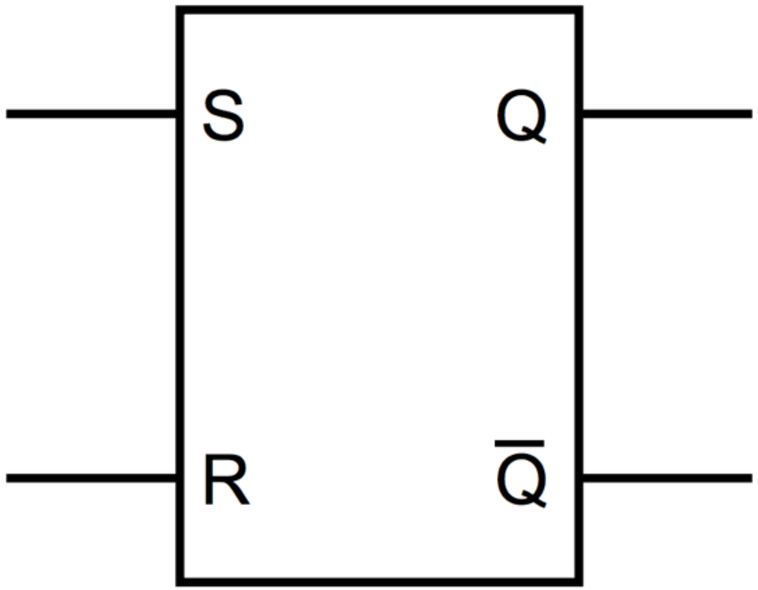
- Describe the operation of the unlocked S-R flip-flop and the clocked S-R, J-K, and D flip-flops
- Describe the need for a clock signal in a flip-flop

Flip-Flops

- Flip-flops are relatively simple circuits that store one bit of information
- The output (the state) depends on the current inputs and the current state
- A flip-flop is a sequential circuit
- Common types of flip-flops
  - S-R (set-reset)
  - J-K
  - D (data)

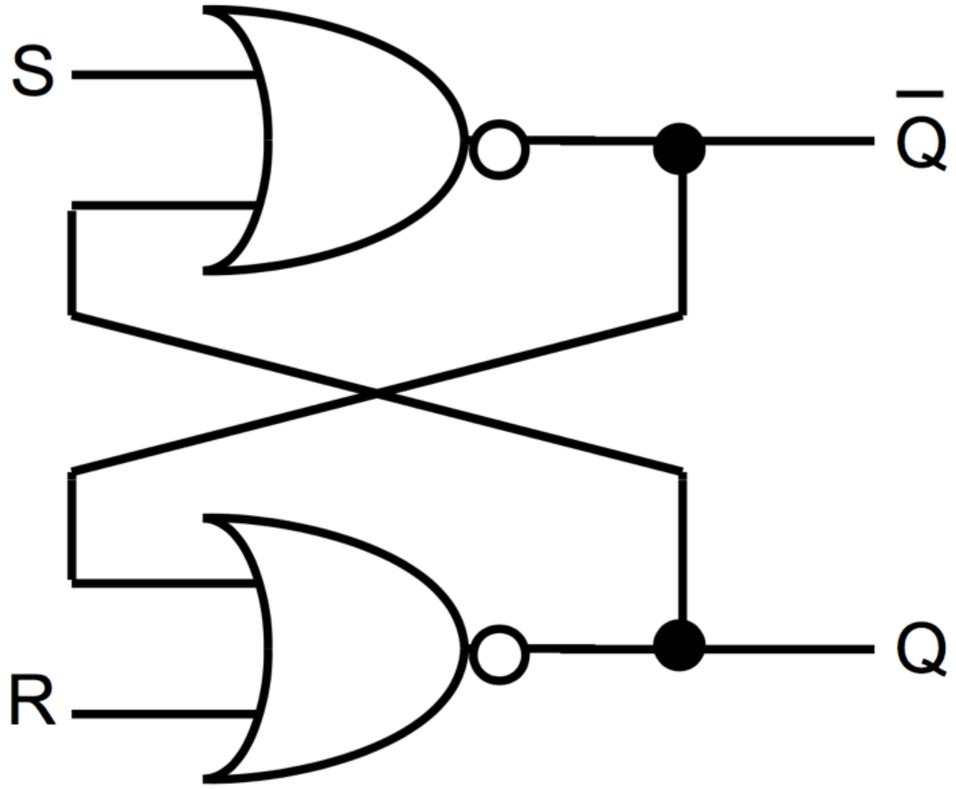
Block Diagram of an S-R Flip-Flop

- Unclocked (asynchronous) version of the S-R flip-flop
- Inputs S (SET) and R (RESET)
- Output Q (and Q') that depends on present and past inputs of S and R



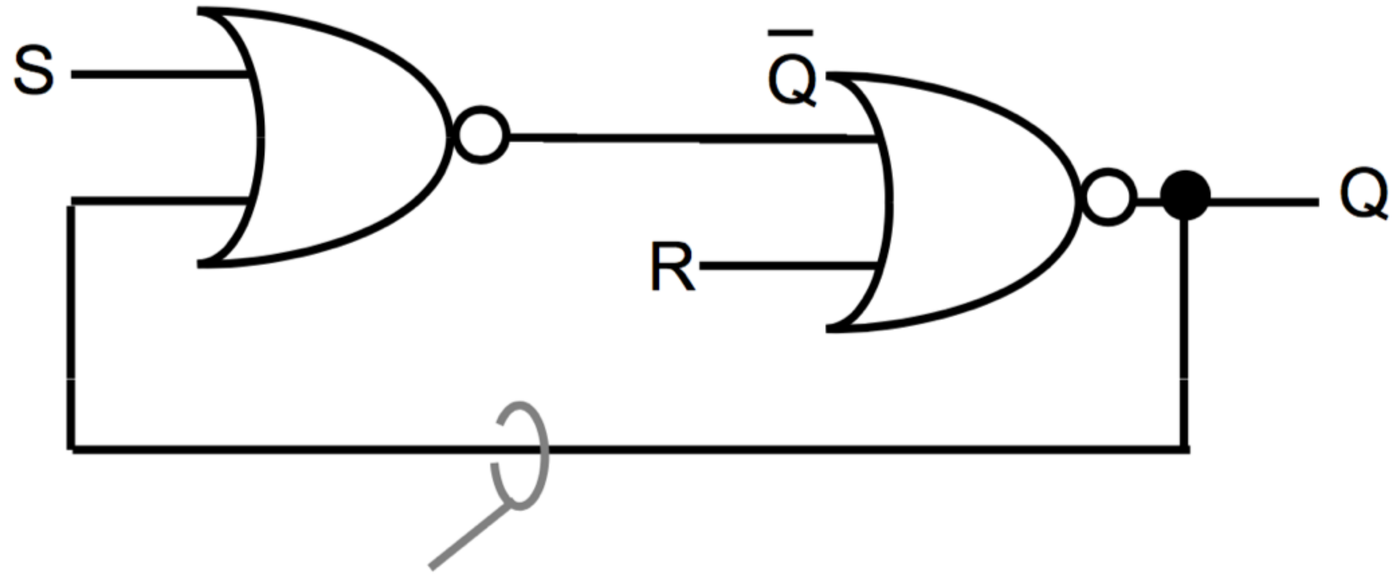
S-R Flip-Flop (1)

- One form of an S-R flip-flop is built from “cross-coupled” NOR gates



S-R Flip-Flop (2)

- Redrawing the gate-level diagram reveals that there is one “feedback” path that returns an output back to an input
- This path provides 1 bit of memory



1 feedback path ⇒ storage of 1 bit of information

CHECK POINT

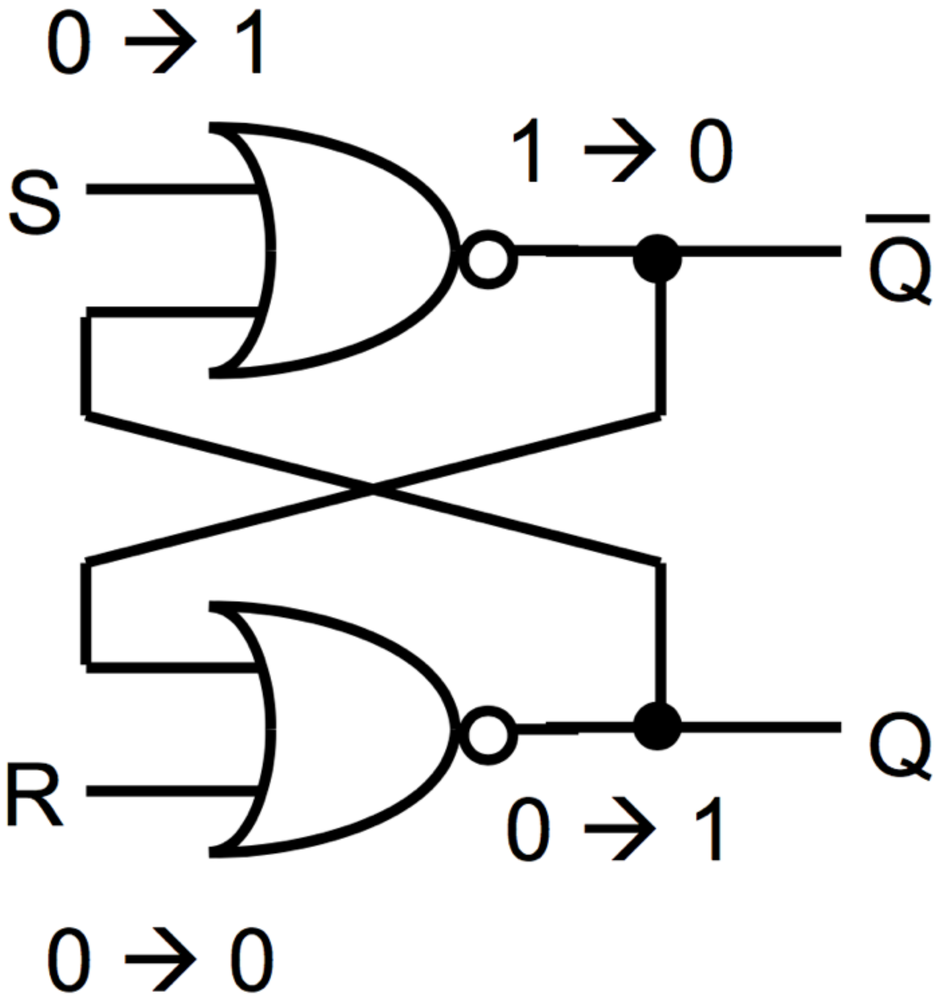
As a checkpoint of your understanding, please pause the video and make sure you can do the following:

- Draw the block diagram of an unclocked S-R flip-flop, including labeling the inputs and outputs

If you have any difficulties, please review the lecture video before continuing.

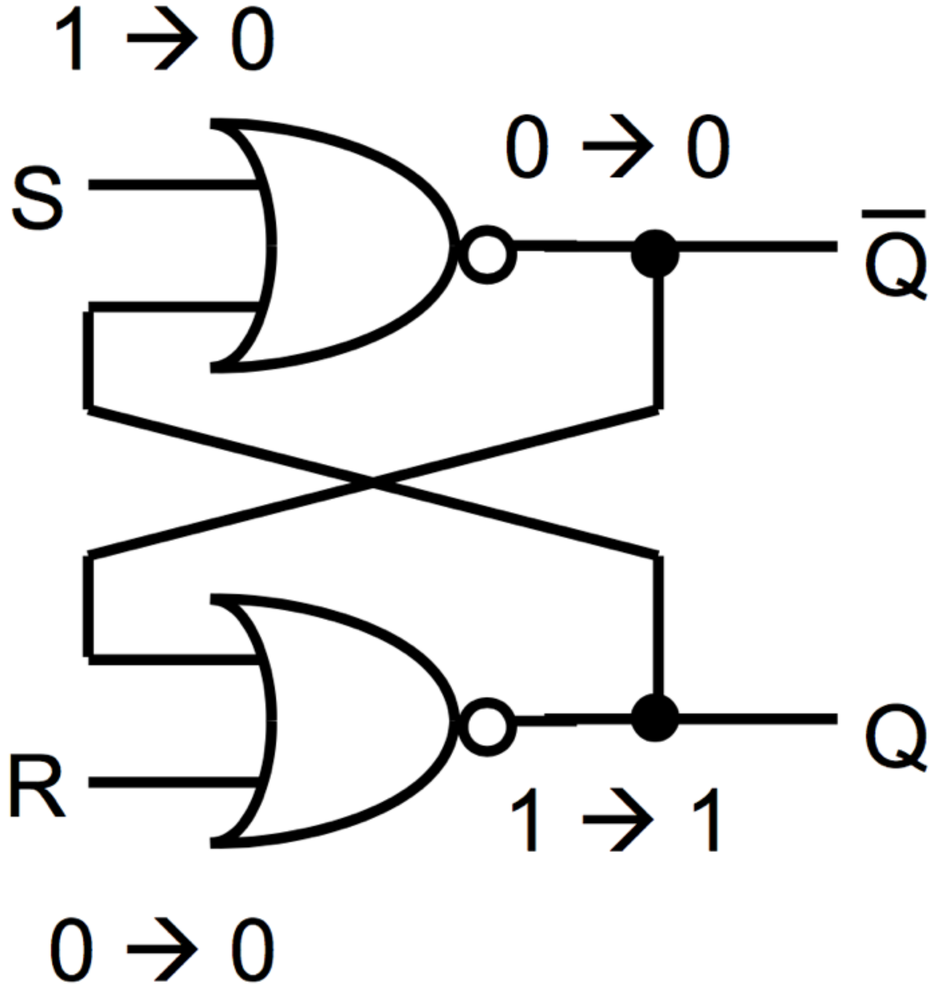
Analyzing the S-R Flip-Flop (1)

- Start with the case of S=0, R=0, Q=0
  - Output of Q stays at 0
  - This is a stable state
- Change S to 1, so S=1, R=0
  - S changing to 1 causes Q' to change from 1 to 0
  - Q' changing from 1 to 0 causes Q to change from 0 to 1
- S=1, R=0 "sets" the state ("set" means setting Q=1)



Analyzing the S-R Flip-Flop (2)

- Continue with the case where the state Q is set, S=1, R=0, Q=1
  - This is a stable state
- Now, change S from 1 back to 0, so S=0, R=0
  - Q' stays at 0 since Q=1
  - Q stays at 1 since Q'=0, R=0
- S=0, R=0 "holds" the present state



Analyzing the S-R Flip-Flop (3)

- Further analysis shows that:
  - S=0, R=1 “resets” the state, i.e. resets Q to 0, regardless of the original state of Q
  - S=1, R=1 leads to indeterminate results and is, thus, an invalid or forbidden input to the S-R flip-flop

Analyzing the S-R Flip-Flop (4)

- The S-R flip-flop provides memory for one state bit
  - We can store “1” by doing a SET (S=1, R=0)
  - We can store “0” by doing a RESET (S=0, R=1)
  - We can hold the present state by doing a HOLD (S=0, R=0)
- This or similar circuits are the basis for other sequential logic elements such as clocked flip-flops and static random access memory (SRAM)

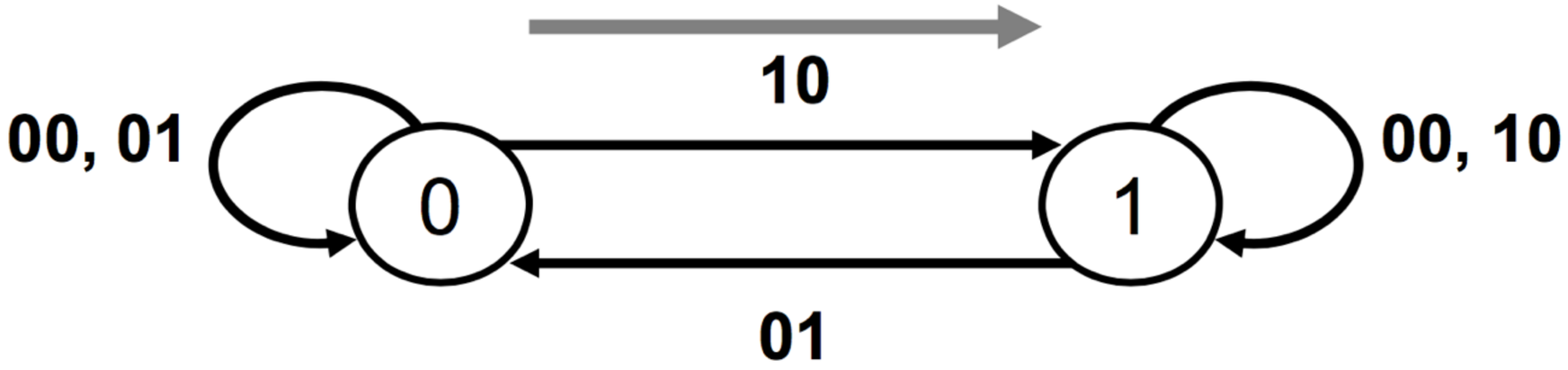
State (Truth) Table for the S-R Flip-Flop

- Specifies value of Q_{t+1} as a function of S, R, and Q_t
  - Q_t is the present state of state bit Q
  - Q_{t+1} is the next state of state bit Q
- Three operations
  - Hold (Q does not change)
  - Reset (Q is reset to 0)
  - Set (Q is set to 1)
- Input S=1, R=1 is invalid

	S	R	Q_t	Q_{t+1}
HOLD	0	0	0	0
	0	0	1	1
RESET	0	1	0	0
	0	1	1	0
SET	1	0	0	1
	1	0	1	1
invalid	1	1	0	—
	1	1	1	—

State Transition Diagram for S-R F-F

- Two nodes, for Q=0 and Q=1
- Edges labeled with values of SR that cause the indicated transition
- For example, analysis showed that SR=10 with Q=0 caused a state change to Q=1
    - This transition corresponds to one edge in the graph



CHECK POINT

As a checkpoint of your understanding, please pause the video and make sure you can do the following:

- Describe the operation of the unclocked S-R flip-flop using a state-transition diagram

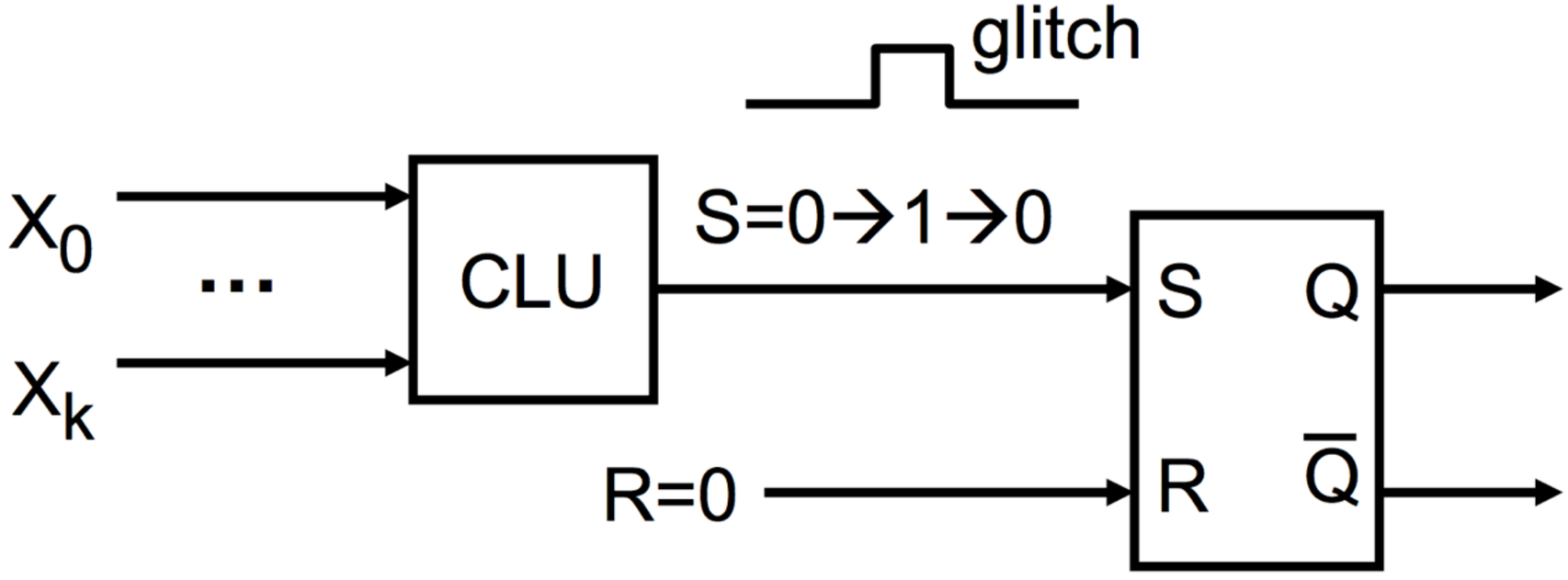
If you have any difficulties, please review the lecture video before continuing.

Glitches and Unclocked Flip-Flops (1)

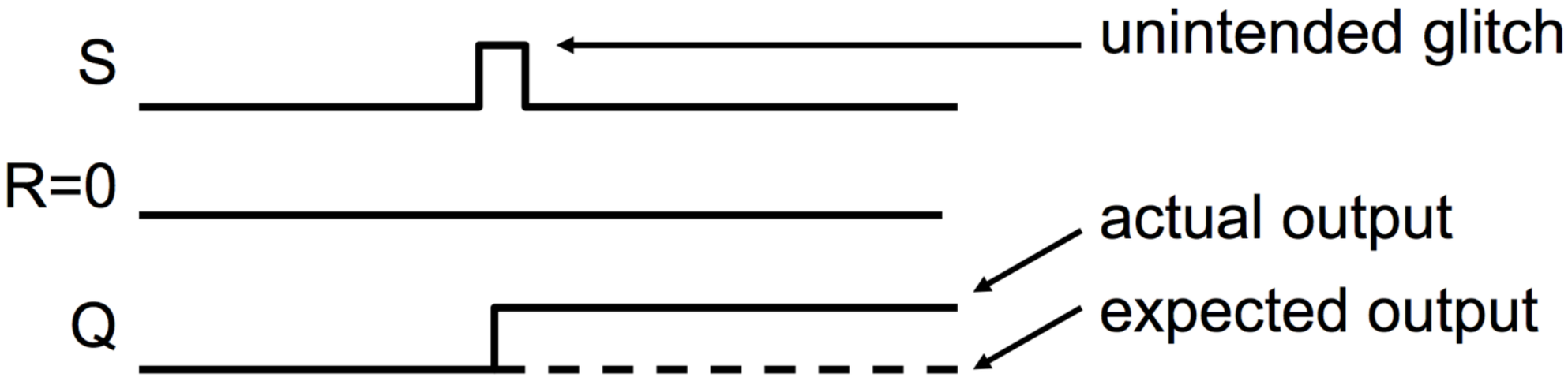
- Spurious, short transitions (glitches) can occur on the output of combinational logic units
  - Such glitches are due to differences in propagation delays through the logic circuit when one or more inputs changes its value
  - A circuit has a “hazard” if it can produce a glitch at its output
- A glitch can cause problems for an unclocked (asynchronous) sequential circuit

Glitches and Unclocked Flip-Flops (2)

- Consider a combinational logic unit (CLU) that drives the S input on an unclocked S-R flip-flop
- A glitch on input S can cause an unintended transition in Q



Glitches and Unclocked Flip-Flops (3)



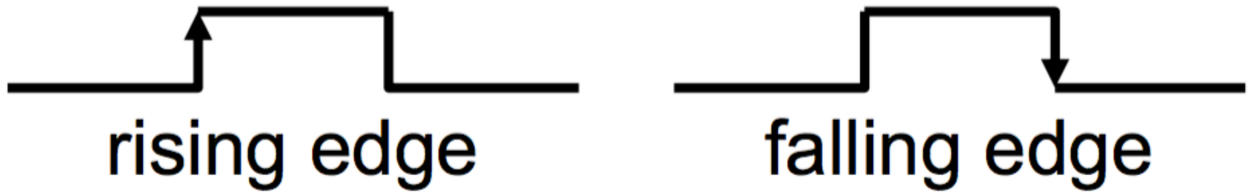
- The unexpected glitch in S causes an unexpected SET operation to be performed, causing Q to go to 1 when we want it to stay (since S=0, R=0)

Clocked Flip-Flops (1)

- A solution to the problems of such glitches is to use a clock to create a “synchronous” sequential circuit
- Clock events cause the flip-flop to sample the inputs and to use the sampled values to determine a change in the output

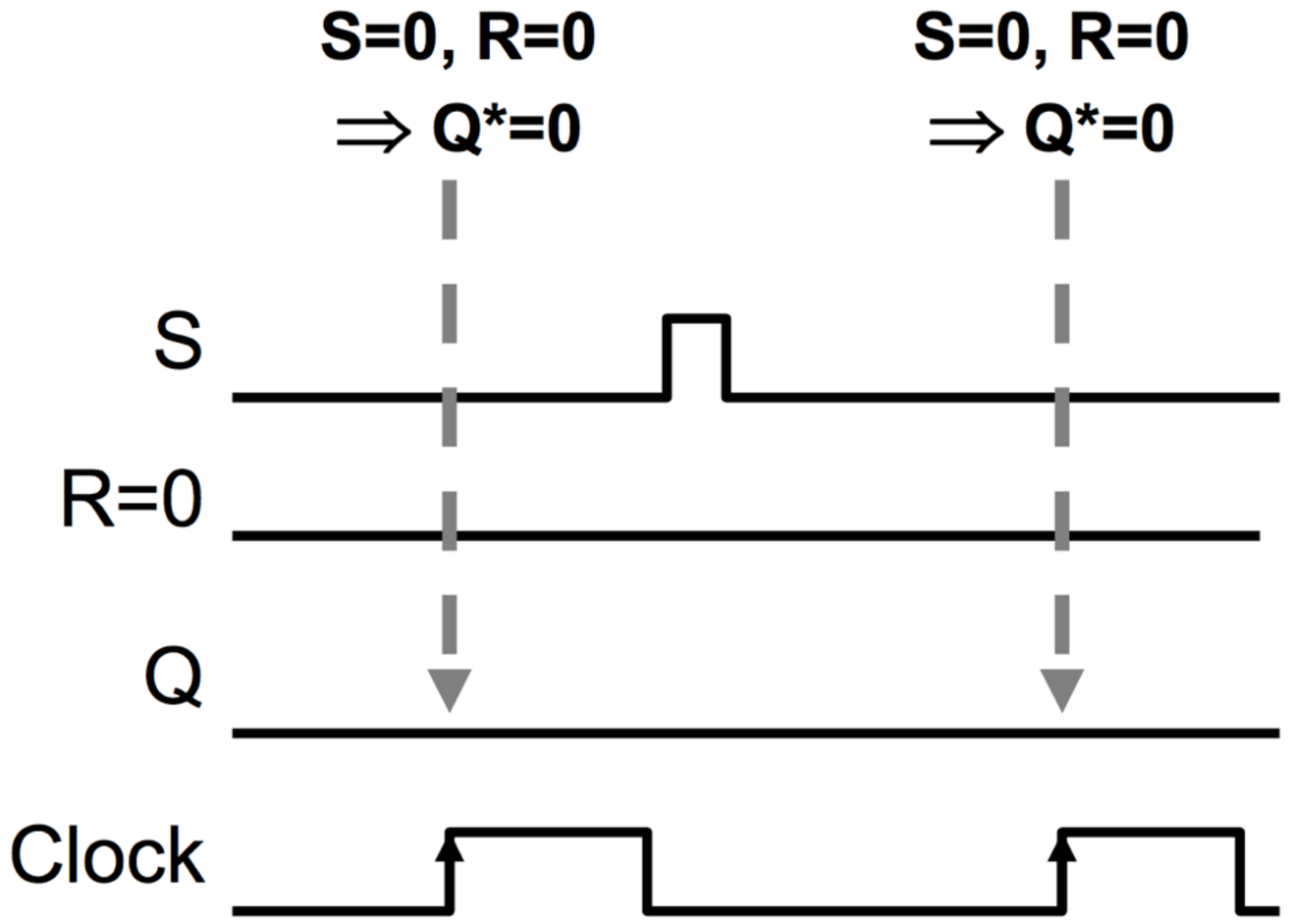
Clocked Flip-Flops (2)

- Output only changes due to a clock event
  - Rising (0-to-1) clock edge: positive edge-triggered flip-flop
  - Falling (1-to-0) clock edge: negative edge-triggered flip- flop
  - High clock: level triggered



Clocking to Avoid Glitches

- Rising edge in clock determines when the S-R flip-flop changes it state
- Operates as expected as glitch is between rising edges of the clock and is ignored



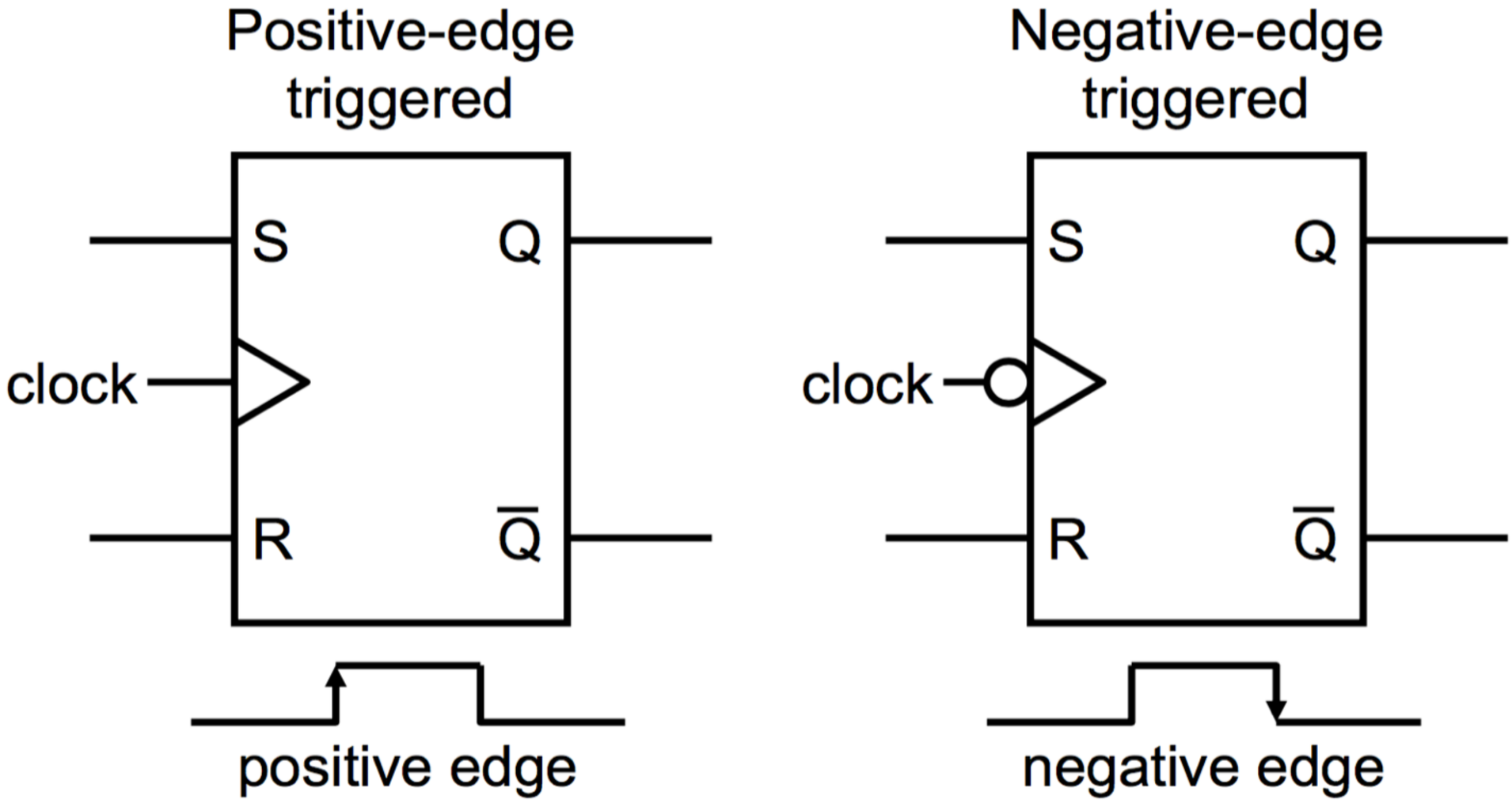
CHECK POINT

As a checkpoint of your understanding, please pause the video and make sure you can do the following:

- Use input and output signal timelines to describe how clocking helps avoid glitches in the operation of the S-R flip-flop

If you have any difficulties, please review the lecture video before continuing.

Block Diagrams for Clocked S-R F-F



Clocking

- The clock must be properly designed
  - Slow enough to ensure that all flip-flop inputs are stable before the next clock event occurs
  - Fast enough to provide fast circuit operation (desirable for most designs)

Other Flip-Flops

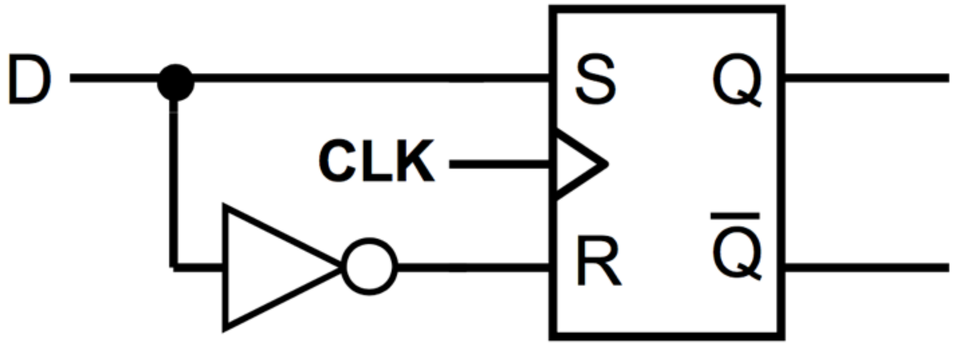
- The clocked S-R flip-flop can be used as a basis for other types of clocked flip-flops, including:
  - D or “Data” flip-flop
  - J-K flip-flop (modified S-R flip-flop function)
- We assume clocked, edge-triggered flip-flops

“Data” or D Flip-Flop

- The D flip-flop simply stores the D input (0 or 1) that is present at each clock event
- Can be built using an S-R flip-flop
  - If D=1, then S=1 and R=0 for a SET operation (Q=1)
  - If D=0, then S=0 and R=1 for a RESET operation (Q=0)

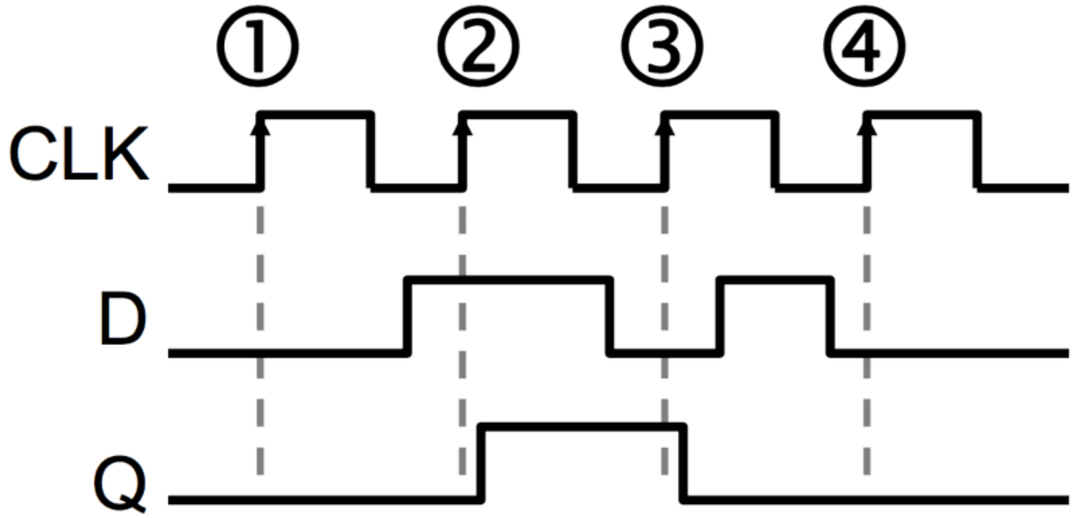
State Table

D	Q_t	Q_{t+1}
0	0	0
0	1	0
1	0	1
1	1	1



D Flip-Flop Operation

- Output Q takes on the value of D present at each positive clock edge
- For example:
- At (2), D=1, so Q changes from 0 to 1
- At(3), D=0, so Q changes from 1 to 0
- Value of D=1 between (3) and (4) is ignored since not clocked



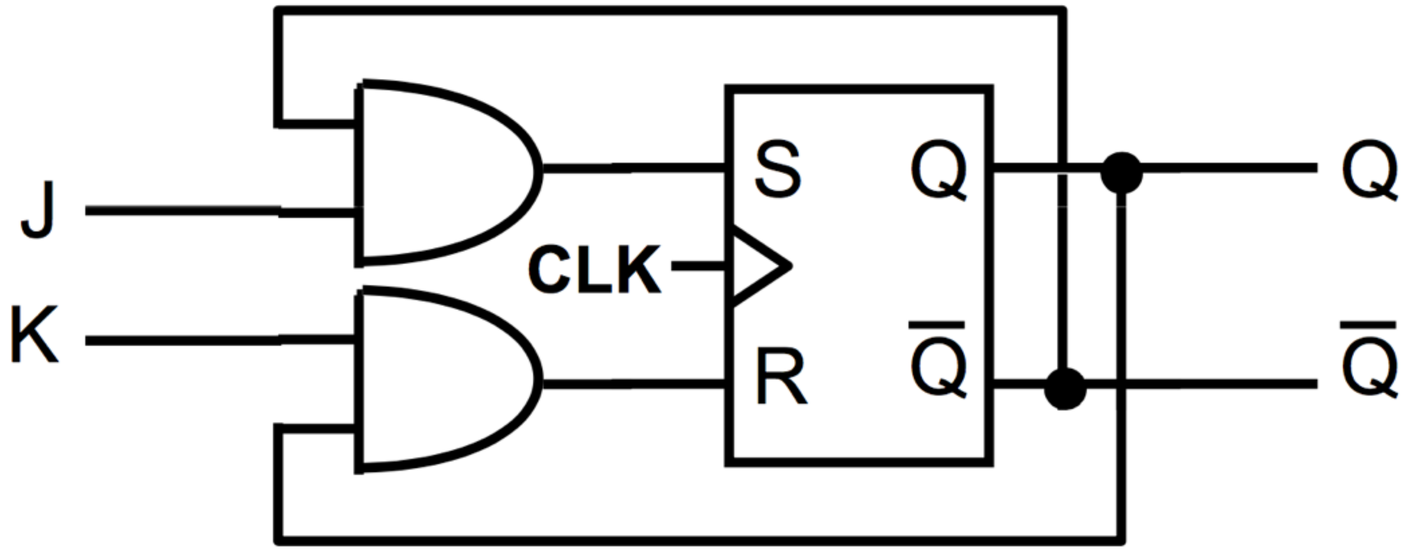
J-K Flip-Flop

- J-K flip-flop is like an S-R flip-flop (with J=S and K=R) except for the case where inputs are both 1
- S=1, R=1 not allowed for the S-R flip-flop
- J=1, K=1 is allowed and causes the state to toggle
- Q=0 toggles to Q=1
- Q=1 toggles to Q=0

	J	K	Q_t	Q_{t+1}
HOLD	0	0	0	0
	0	0	1	1
RESET	0	1	0	0
	0	1	1	0
SET	1	0	0	1
	1	0	1	1
TOGGLE	1	1	0	1
	1	1	1	0

J-K Flip-Flop Logic

- Logic implements S=JQ’ and R=KQ
- Example: AssumeJ=K=1 (TOGGLE operation)
- If Q=0, then S=1, R=0 (to SET) and next state is Q=1
- If Q=1, then S=0, R=1 (to RESET) and next state is Q=0



CHECK POINT

As a checkpoint of your understanding, please pause the video and make sure you can do the following:

- Use a state table to describe the operation of a D flip-flop
- Draw the J-K flip-flop logic circuit using the block diagram of a clocked S-R flip-flop and two AND gates

If you have any difficulties, please review the lecture video before continuing.

Summary (1)

- S-R flip-flop constructed from two NOR gates (or two NAND gates)
  - Analyzed logic circuit to determine behavior
  - Specified behavior using a state table and state transition diagram
- Glitches create problems for unclocked flip-flops, but are not a problem for valid designs using clocked flip-flops
- Clocked flip-flops only change state when a clock event occurs, e.g., a negative edge in the clock signal

Summary (2)

- Common types of flip-flops
  - S-R flip-flop
  - J-K flip-flop
  - D flip-flop
- Some variations
  - Negative and positive edge-triggered
  - Asynchronous PRESET and CLEAR initialization input signals
- J-K and D flip-flops can be implemented using an S-R flip-flop and some additional combinational logic

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