MODULE 13: Selected Topics

Lecture 13.1
RISC Processors

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Lecture 13.1 Objectives

- Cite specific features to differentiate between CISC and RISC architectures
- Discuss the performance equation and how it relates to the performance of CISC and RISC processors
- Describe the concept of register windows

RISC Processors

- Traditional processors were Complex Instructions Set Computers (CISC)
- Reduced Instruction Set Computer (RISC) concept was a departure from the CISC approach
  - Use a “simple” instruction set to reduce the clock rate
  - Hardware resources saved due to simpler control can be reallocated to more on-chip registers, instructions pipelines, and cache memory for instructions and data

History of RISC Processors

- Concept used at by John Cocke at IBM in the mid-1970s in the Model 801 processor, but not widely disseminated
- 1980 paper by Patterson and Ditzel popularized the idea
  - Defined and disseminated the concept
  - Provide analysis to support the concept
- Several RISC processors were widely used – MIPS, Motorola/IBM PowerPC, Sun SPARC, and others
- Availability of more hardware has blurred the differences between RISC and CISC architectures
  - RISC processors have become more complex
  - CISC processors have adopted some RISC ideas

CISC versus RISC

CISC

- Complex instruction set computers evolved as more functionality was added to processors
- Powerful instructions reduce program size
- Closely matched to high-level languages

RISC

- Simple instructions with few operations and limited options
- Simplicity enables high clock rates (low execution time per instruction)
- Leverages compiler technology
- More “real estate” available for registers

CHECK POINT

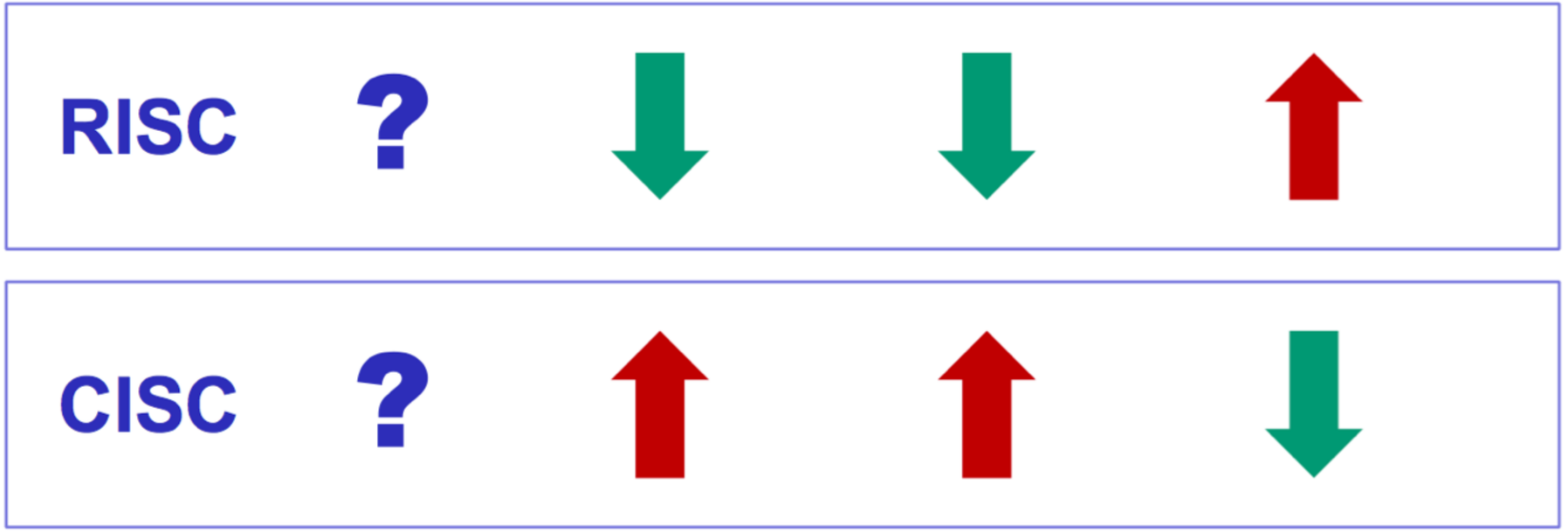
As a checkpoint of your understanding, please pause the video and make sure you can do the following:

- Cite specific features to differentiate between CISC and RISC architectures

If you have any difficulties, please review the lecture video before continuing.

Computer Performance Equation

$$\frac{time}{program} = \frac{time}{cycle} \times \frac{cycles}{instruction} \times \frac{instructions}{program}$$



Which factors lead to the best performance?

CISC Versus RISC Example

Compute 4×12

CISC

```
        mov ax,12
        mov bx,4
        mul bx,ax
```

Cycles = 2 + 2 + 30

Cycles = 34

RISC

```
        mov ax,0
        mov bx,12
        mov cx,4
LP:     add ax,bx
        loop LP
```

Cycles = 1+1+1+4(1+1)

Cycles = 11

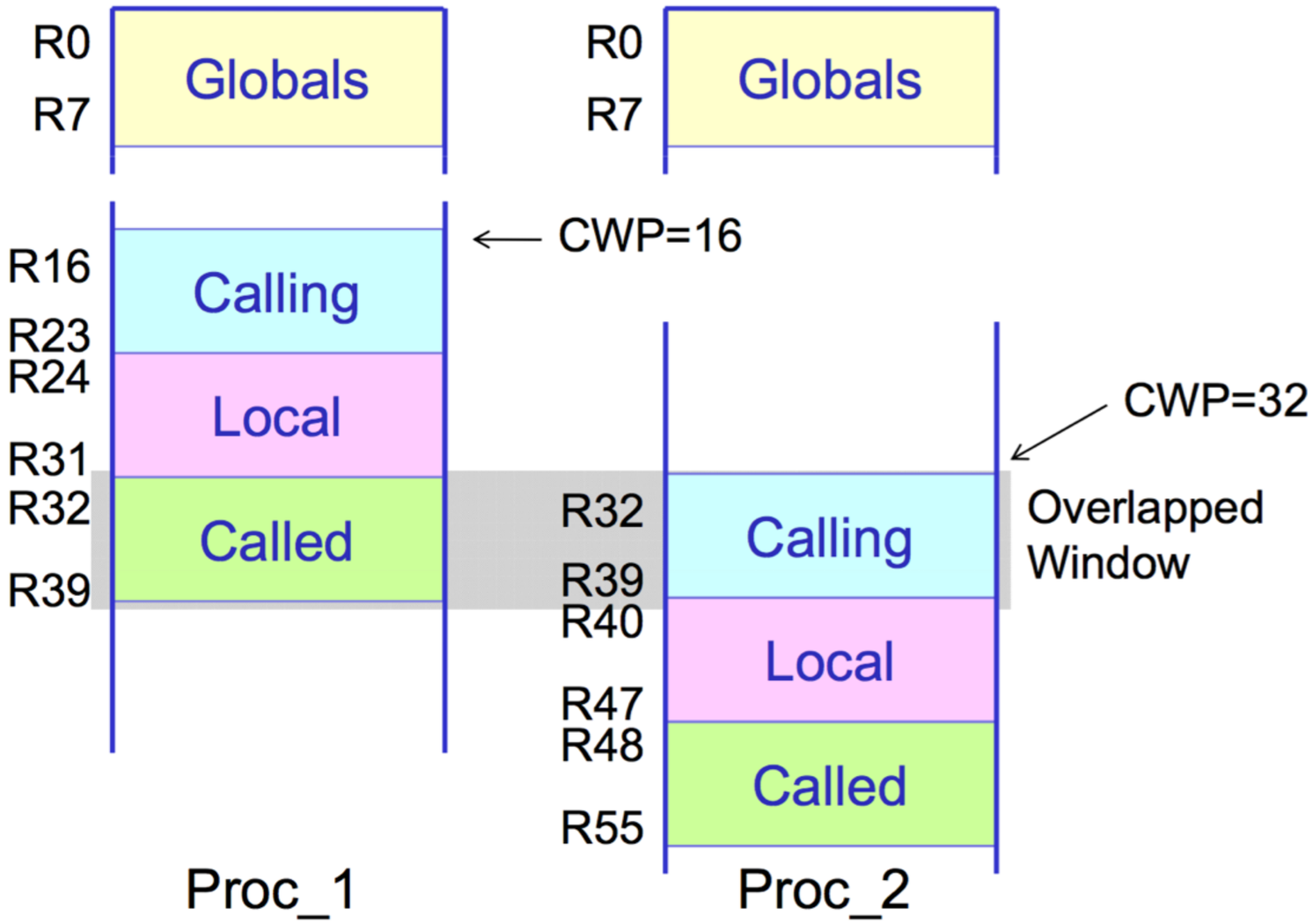
CISC Versus RISC Example (cont'd)

- Cycles to perform the computation
  - CISC: 34 cycles (due to relatively expensive multiply)
  - RISC: 11 cycles (but depends on the data)
- For this particular example:
  - RISC requires fewer cycles, so it is likely faster
  - RISC cycles should be faster than CISC cycles, so the computation is, indeed, faster on a RISC
- Your results may vary!

Register Windows

- RISC architecture frees transistors for use as registers
- Register window concept grew out of RISC processors
- A procedure needs registers for four purposes
  - Registers to hold global data (for all procedures)
  - Registers to hold parameters from the calling procedure (inputs)
  - Registers for local data
  - Registers to hold parameters for called procedures (outputs)

Register Windows Example



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Summary

- Reduced Instruction Set Computers
  - Simplify the instruction set to reduce the number of cycles per instruction
  - Simpler control logic reduces the time per cycle
  - Savings in transistors can be used for registers, instruction pipelines, and cache
  - But, simpler instructions means that a program requires more instructions to be executed
- Today:
  - “RISC” processors use some more complex features
  - “CISC” processors have adopted some RISC features

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