Virginia Tech - ECE 5484 - Summer 2020

Homework 2

Before starting this homework assignment, please be sure that you have completed all of the following activities.

- View the relevant online lectures and read associated sections in the textbook before or while you work on this homework assignment.
- Review the course syllabus. Note the grading policies, including policies for submitting assignments.
- Review the course schedule. Note the due dates for course assignments, including this one.
- Review the Graduate Honor System at https://graduateschool.vt.edu/academics/expectations/graduate-honor-system.html. Review the Graduate Honor System Constitution, especially Articles I (Sections 1, 2, and 3), V, VI, VII, VIII, and IX.

Please note the following.

- Solutions must be clear and presented in the order assigned. Solutions must show work needed, as appropriate, to derive your answers. Written answers should be concise, but sufficiently complete to answer the question. Neat hand drawings, where needed, are acceptable. Your final solution for each problem must be easily identified.
- At the top of the first page, include: your name (as recorded by the university); your email address; and the assignment name ("ECE 5484, Homework 2"). Do *not* include your Virginia Tech ID number or your social security number.
- Homework must be submitted as a PDF (.pdf) file with the file name *lastname_firstname*_HW2.pdf, where *lastname* is your last or family name and *firstname* is your first or given name. Submit a single file.
- Submit your assignment using the Assignments area of the class website. You must submit your assignment by 11:55 p.m. on the due date.

Homework 2 consists of the following problems.

1. Construct a truth table for the following:

   F = (x + y)(x' + z')(y' + z')

2. Using truth tables, show that:

   xz = (x+y)(x+y')(x'+z)

3. The truth table for a Boolean expression is shown. Write the Boolean expression in sum-of-products form.

x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

4. Draw the combinational circuit that directly implements the following Boolean expression: F(x,y,z) = y' + xy + y'z.

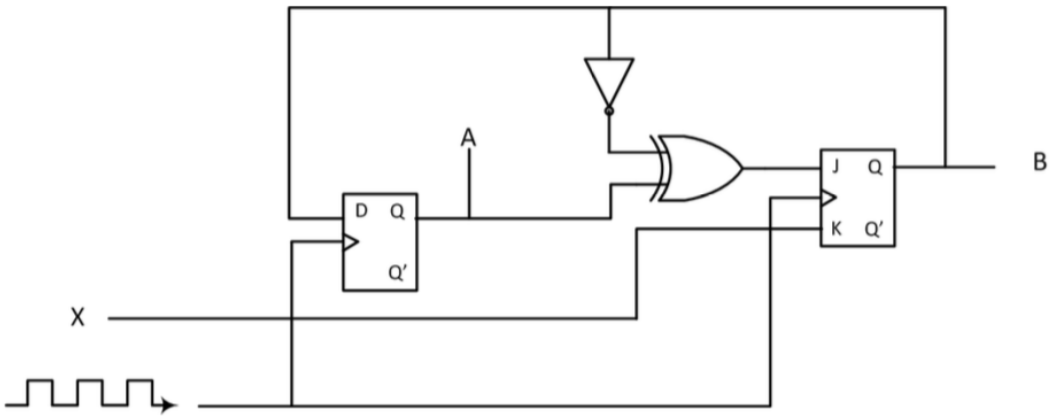
5. Consider the parity generator (even parity) shown in the truth table below. The parity bit Y is a

function of Boolean variables A, B, and C. Represent this parity function in the following ways:

1. As a Boolean algebraic expression.
2. As a combinational logic diagram (logic circuit).

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

6. Complete the truth table for the following circuit



7. Complete the tutorial provided with Logisim 2.7.1. The tutorial is under the "Help" menu in Logisim or at http://www.cburch.com/logisim/docs/2.7/en/html/guide/tutorial/. Insert a picture of the circuit, as drawn in Logisim, into your homework submission. INCLUDE A TEXT LABEL WITH YOUR NAME AND DATE. Use the "Export Image" function in the "File" menu to save an image file and then insert that in your submission. Uncheck the "Printer View" box when exporting the image from Logisim. *Do not provide the picture as a separate file.*
8. For this problem, you are to design a simple combinational logic circuit and then use Logisim to simulate and test the circuit. The circuit is a 2-bit priority encoder with inputs I_2 and I_1 and outputs Z_1 and Z_0. The circuit behaves as follows:
   - If $I_2I_1 = 00$, then $Z_1Z_0 = 00$ (no active input)
   - If $I_2I_1 = 01$, then $Z_1Z_0 = 01$ (low-priority input, I_1, is active)
   - If $I_2I_1 = 1$-, then $Z_1Z_0 = 10$ (high-priority input, I_2, is active)

Note that the value of input I_1 does not matter if the high-priority input, I_2, is active. Also, output combination $Z_1Z_0 = 11$ should never occur.

1. Give the truth table that shows outputs Z_1 and Z_0 as functions of inputs I_2 and I_1.

2. Give the Boolean algebra expressions for output Z_1 and output Z_0.

3. Simulate your circuit using Logisim. Label all inputs and the output. Test for all four input combinations. INCLUDE A TEXT LABEL WITH YOUR NAME AND DATE. Insert a picture of the circuit, as drawn in Logisim, into your homework submission. Uncheck the "Printer View" box when exporting the image from Logisim. Your picture should show the circuit with input combination $I_2I_1 = 11$. *Do not provide the picture as a separate file.*

9. *Scavenger Hunt:* The JK flip-flop is sometimes called the "Jump-Kill" flip-flop. Although disputed, according to some sources it was named "JK" after one of the engineers on the team that designed a JK flip-flop circuit. The engineer's initials were "JK." This engineer later won a Nobel Prize.

   1. Who was this engineer?

   2. In your own words, why did he receive the Nobel Prize?