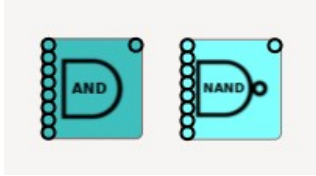
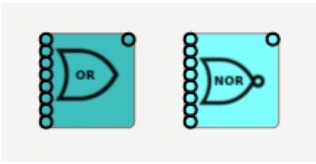


cLogicFun

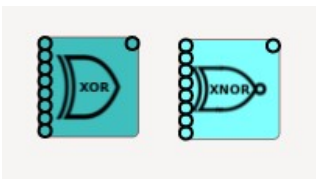
Basic Logic Nodes



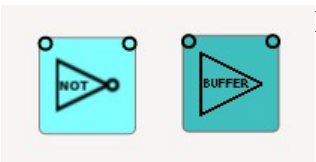
And / Nand, logical AND of the inputs, note that unused inputs are ignored.



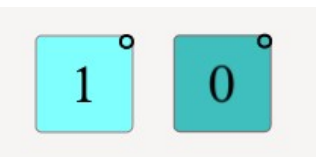
Or / Nor logical OR of inputs



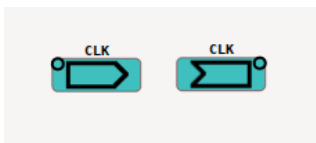
Xor / Xnor exclusive OR



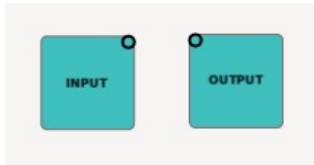
Not inverts the input, when a NOT gate is inverted it becomes a buffer



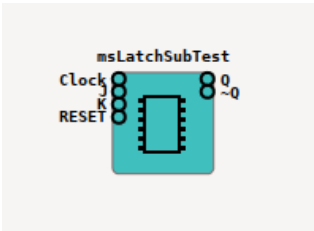
Const, used when a constant value is needed



Source and destination labels, all destination labels are set to the same logic state as the source label with the same text, there can be multiple destination labels for each source label, source label text's must be unique. There is no latency between a source and destination label



Input and Output nodes, an input node's state can be changed by right clicking on it, outputs can be useful as indicators. They are used to help define the input and output "pins" for sub circuits



Sub circuit nodes allow you to encapsulate a separate circuit loaded from a circuit file. See also the "pins" dialogue. Right click on the node to select a circuit to load into the sub node.

NB make sure your main circuit has been saved before loading a circuit into a sub node, as the sub node depends on relative paths, currently this is not caught and bad things happen if you load a sub node into an unsaved circuit.

Dialogues

Assign pins dialogue

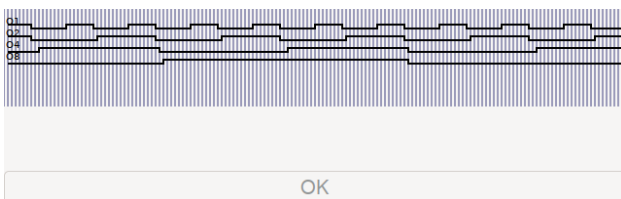
Drag and drop to order
ensure unused io's have no pin number

Inputs			Outputs		
Name	Pin		Name	Pin	
4	-	+	2	-	+
Clock	0		Q	0	
J	1		~Q	1	
K	2		outTest		
RESET	3				
test					

OK Cancel

Using this dialogue you define the "pins" for a sub circuit. Input nodes that are labelled are used as input pins, the same for output nodes. You do not need to use every input or output for a sub circuits out/inputs. You can reorder the labels by dragging and dropping them to change their order.

Chart dialogue



The chart dialogue is very rudimentary all it does is step the simulation for sufficient steps to fill up a graph of output values

Node dialogue

AND

Invert ☐

Rotation

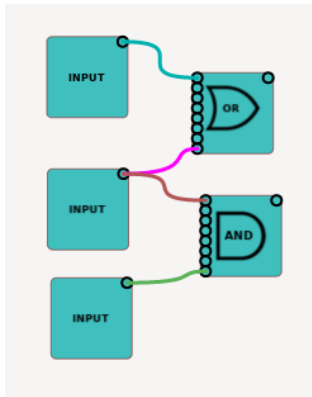
Text

latency

Cancel Delete OK

Some logic nodes can have their outputs inverted (an AND becomes a NAND for example) every node can have its own rotation and a text label. Latency is how long it takes for a change in the inputs to affect the outputs. A node can also be deleted which also deletes all wires connected to it

Wires



Wires are represented by curved lines, they connect one node's output to another nodes inputs.

To create a wire click and drag from a nodes output to another nodes input.

An output can have multiple wires connected to it.

An input can only have one wire connected to it.

To delete a wire click on the wires output end.