COMP 4611 Homework #1

Due on Oct. 8, 2013 at 17:00 pm

Name:_____ Student ID: _____Email:_____

Instructions

1. Please read each question very carefully before answering questions.
2. Show all the steps used in deriving your answer, wherever appropriate.

Q1. [20 marks] Cost and Price

You are trying to figure out whether to construct a new fabrication facility for your IBM Power5 chips. It costs $1.5 billion to build a new fabrication facility. The benefit of the new fabrication is that you predict that you will be able to sell 3 times as many chips at 2 times the price of the old chips. The new chip will have an area of 186 mm^2, with a defect rate of .7 defects per cm^2. Assume the wafer has a diameter of 300 mm. In both the old and new fabrications, it costs $1000 to fabricate a wafer, and the packaging and testing cost is $20 per chip (after final testing). You were selling the old chips for 40% more than their cost. Assume $\alpha = 4$, Wafer Yield = 1.
The old fabrication process' parameters are shown in the following table.

Chip	**Die size (mm^2)**	**Estimated defect rate (per cm^2)**	**Manufacturing feature size (nm)**	**Transistors (millions)**
IBM Power5	389	.30	130	276

Note: In this question, you will use equations based on empirical study and approximations. For simplicity, when you need to round to integer numbers, use the mathematical round function (e.g., round 3.24 to 3.2 or round 3.51 to 4) without considering whether the floor or ceiling function would be more appropriate.
Remember not all calculation results need to be rounded to integer numbers.

a) [2 marks] With the old fabrication, how many dies can we get from a wafer before we test individual dies? (Round the result to an integer number)

b) [2 marks] With the old fabrication, what is the die yield?

c) [3 marks] What is the cost of the old Power5 chip? Assume the final test yield is 100%.

d) [2 marks] With the new fabrication, how many dies can we get from a wafer before we test individual dies? (Round the result to an integer number)

e) [2 marks] With the new fabrication, what is the die yield?

f) [2 marks] What is the cost of the new Power5 chip? Assume the final test yield is 100%.

g) [2 marks] What was the selling price of each old Power5 chip?

h) [2 marks] What is the selling price of each new Power5 chip? What is the difference between the selling price and the cost of the new chip?

i) [3 marks] Suppose 50% of the difference between the selling price and the chip cost is your profit. If you sold 500,000 old Power5 chips per month, how long would it take for the accumulated profit to recoup the costs of the new fabrication facility?

Q2. [16 marks] Performance Metrics

An application running on a 1GHz pipelined processor has 55% load-store, 30% arithmetic, and 15% branch instructions. The individual CPIs of these instructions are 5, 4 and 4, respectively.

a) [5 marks] Determine the overall CPI of this program execution on the given processor.

b) A new embedded version of the processor is being modified to operate at 600 MHz. In this new version, the individual CPIs of load-store and arithmetic instructions are remaining unchanged. However, the individual CPI of branch instructions is getting stretched to 6 clock cycles. A new compiler is also developed for the new processor which eliminates 25% of load-store and 5% of arithmetic instructions for the given application (e.g., if there were 1 million load-store instructions before, now the program compiled by the new compiler would have only 750000).

b1) [5 marks] Determine the overall CPI of this program execution on the new processor together with the new compiler technology.

b2) [5 marks] Determine the factor by which the application will run faster or slower on the new processor with the new compiler technology.

Q3. [15 marks] Amdahl's Law

Suppose there is a program which takes 200 seconds to execute. Of this time, 30% is used for multiplication, 60% for memory access instructions and 10% for other tasks. Suppose your goal is to enhance the performance of a processor by 2 times and there are two ways of doing so: either make multiply instructions run faster than before, or memory access instructions run faster than before, but not both.

a) [4 marks] How much shall we improve the memory access instructions in order to achieve the performance enhancement? Is it possible?

b) [4 marks] How much shall we improve the multiplication in order to achieve the performance enhancement? Is it possible?

c) [7 marks] Suppose we now improve the memory access by 5 times (Time(old execution) / Time(new execution) = 5). Unfortunately, the design makes multiplication slow down by 20% (i.e., Time(old execution) / Time(new execution) = 5/6). What will the overall speedup be?

Q4. [15 marks] Geometric versus Arithmetic Mean

The following is a set of individual benchmark scores for each of the programs in the integer portion of the SPEC CPU 2000 benchmark.

Benchmark	Score before improvement	Score after improvement
164.gzip	10	12
175.vpr	14	16
176.gcc	23	28
181.mcf	36	40
186.crafty	9	12
197.parser	12	120
252.eon	25	28
253.perlbmk	18	21
254.gap	30	28
255.vortex	17	21
256.bzip2	7	10
300.twolf	38	42

a) [4 marks] Calculate the speedup after the improvement using the arithmetic mean.

b) [4 marks] Calculate the speedup after the improvement using the geometric mean.

c) [7 marks] Note that there is a difference between the above two improvement ratios, what is the main reason?

Q5. [14 marks] Endian-ness

Is the Internet Big Endian or Little Endian? Give your answer and provide justification and evidence. The evidence can be a protocol, a piece of software or other real-world technical used in the Internet.

Q6. [12 marks] Instruction set

a) (6 marks) Design an instruction set that contains only one instruction but can express all the arithmetic and logical instructions in the MIPS instruction set (refer to http://users.ece.gatech.edu/~dblough/3055/mips_isa.jpg).

b) (6 marks) Use this single instruction to express "or $1, $2, $3".

Q7. [8 marks]

Two instructions a and b have 5 steps, and the time it takes to complete each step is given in the following table:

	F	D	E	M	W
a.	230ps	460ps	150ps	300ps	100ps
b.	200ps	150ps	220ps	190ps	140ps

Now we design a processor that can execute these two instructions. Assume that when pipelining, each pipeline stage takes 20ps extra time for data transportation and signaling. Also assume all programs are composed of both of the two instructions.

a) [2 marks] Non-pipelined processor: if we require that every instruction be completed in one cycle, what is the minimum cycle time for the processor? What is the latency of an instruction? What is the throughput?

b) [3 marks] Pipelined processor: If the processor has 5 stage corresponding to the 5 steps for the instructions, what is the minimum cycle time? What is the latency of an instruction? What is the throughput? Assume the pipeline is perfect and has no pipeline hazards or stalls.

c) [3 marks] If you could split one of the pipeline stages into 2 equal halves, which one would you choose? What is the new cycle time? What is the new latency? What is the new throughput?