Design of the Folded Cascode OTA

For a Generic 180nm Bulk CMOS Process (Version 2)

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1 Introduction

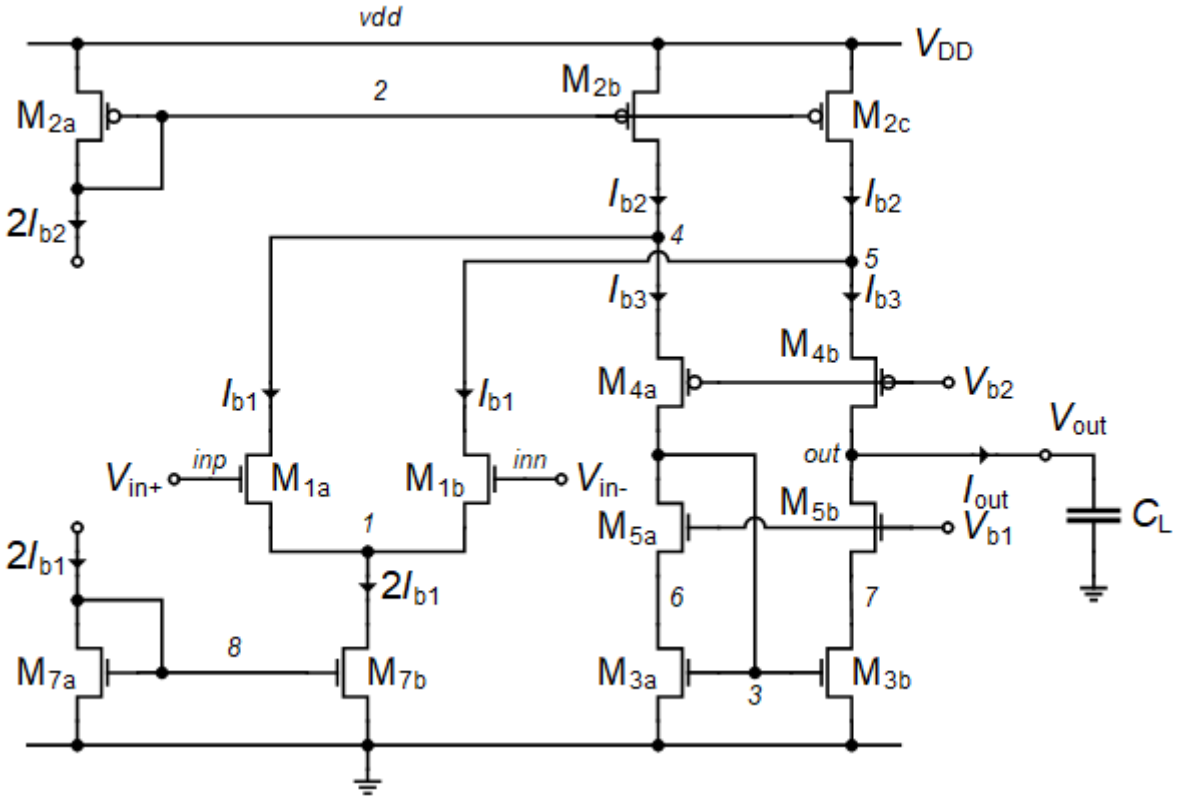

Figure 1.1: Schematic of the folded cascode differential OTA [1].

> **Note**
>
> Note that all nMOS transistors in Figure 1.1 have an odd number and all the pMOS transistors an even number which explains the numbering process (this is the reason why there is no M_6 transistor!).

This notebook presents the design of the folded cascode differential OTA [1] shown in Figure 1.1 for the same specifications used for the other OTAs. The folded cascode OTA is similar to the telescopic OTA except that the current I_{b3} flowing in the current mirror M_{3a}-M_{3b} can be different than the current I_{b1} flowing in the differential pair. How to choose the ratio $\alpha \triangleq I_{b3}/I_{b1}$? If the current I_{b3} is made equal to current I_{b1} ($\alpha = 1$), then if the differential input voltage is largely positive, the differential pair will saturate and all the bias current $2\,I_{b1}$ is then steered into M_{1a}. This means that all the bias current I_{b2} is flowing into M_{1a} and no current is available at the input of the cascode current mirror M_{3a}-M_{3b}. This situation should be avoided because it introduces an additional delay to charge the parasitic capacitance at node 3 and bring the current mirror M_{3a}-M_{3b} back to normal operation. Usually, the ratio α is taken $1.2 < \alpha < 2$. In order to minimize the current consumption, we will choose $\alpha = 1.2$. This means that the folded cascode OTA unavoidably consumes more current than the telescopic OTA (more than twice).

We will start with a detailed analysis of the OTA which will allow to derive all the design equations that will be used in the design phase. The OTA is then designed for a given set of specifications for a

generic 180 nm bulk CMOS technology. The design is then validated by simulations with ngspice [2] using the EKV 2.6 compact model [3] [4] [5] [6] with parameters corresponding to a generic 180 nm bulk CMOS technology [7] [8].

We now start with the small-signal analysis.

2 Analysis

2.1 Small-signal analysis

In a 1st-order analysis, we can neglect the capacitances at the low impedance cascode nodes 4, 5, 6 and 7 and only account for the capacitances at high impedance nodes 3 (gate of current mirror M_{3a}-M_{3b}) and out (output node). The circuit becomes similar to that of the simple OTA, with the dominant pole ω_0 at the output node (out) and the non-dominant pole ω_p at the current mirror node 3. The transfer function also has a pole-zero doublet. Its transfer function is then given by

$$A_{dm}(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} \cong A_{dc} \cdot \frac{1 + s/\omega_z}{(1 + s/\omega_0)(1 + s/\omega_p)} \cong \frac{A_{dc}}{1 + s/\omega_0} \cong \frac{\omega_u}{s}, \tag{2.1}$$

where

$$A_{dc} \cong \frac{G_{m1}}{G_o}, \tag{2.2}$$

$$G_o \cong \frac{G_{ds3}\, G_{ds5}}{G_{ms5}} + \frac{(G_{ds1} + G_{ds2})\, G_{ds4}}{G_{ms4}}, \tag{2.3}$$

$$\omega_0 \cong \frac{G_o}{C_L}, \tag{2.4}$$

$$\omega_p \cong \frac{G_{m3}}{C_3}, \tag{2.5}$$

$$\omega_z = 2\,\omega_p, \tag{2.6}$$

$$\omega_u = A_{dc} \cdot \omega_0 \cong \frac{G_{m1}}{C_L}. \tag{2.7}$$

2.2 Noise Analysis

At low-frequency the noise of the cascode transistors M_{4a}-M_{4b} and M_{5a}-M_{5b} can be neglected and the noise analysis is then identical to that of the simple OTA. The PSD of the output noise current is given by

$$S_{nout} \cong 2\,(S_{I_{n1}} + S_{I_{n2}} + S_{I_{n3}}) \tag{2.8}$$

which can be expressed in terms of the output noise conductance

$$S_{nout} = 4kT \cdot G_{nout}, \tag{2.9}$$

where

$$G_{nout} \cong 2\,(G_{n1} + G_{n2}G_{n3}), \tag{2.10}$$

with

$$G_{ni} = \gamma_{ni} \cdot G_{mi} + G_{mi}^2 \cdot \frac{\rho_i}{W_i\, L_i\, f} \quad \text{for } i = 1, 2, 3. \tag{2.11}$$

The input-referred noise resistance is then given by

$$R_{nin} \triangleq \frac{G_{nout}}{G_{m1}^2} = \frac{2\,(G_{n1} + G_{n2} + G_{n3})}{G_{m1}^2} = \frac{2\,G_{n1}}{G_{m1}^2} \cdot \left(1 + \frac{G_{n2}}{G_{n1}} + \frac{G_{n3}}{G_{n1}}\right) \tag{2.12}$$

which we rewrite as

$$R_{nin} = \frac{2\,G_{n1}}{G_{m1}^2} \cdot (1+\eta) \tag{2.13}$$

with

$$\eta = \frac{G_{n2}}{G_{n1}} + \frac{G_{n3}}{G_{n1}}. \tag{2.14}$$

η represents the contribution of the current source M_{2b}-M_{2c} and the current mirror M_{3a}-M_{3b} referred to the input and normalized to the contribution of the differential pair M_{1a}-M_{1b}. Of course during the design phase we will try to minimize η.

2.2.1 Input-referred thermal noise

The input-referred thermal noise resistance is given by

$$R_{nth} = \frac{2\,\gamma_{n1}}{G_{m1}} \cdot (1+\eta_{th}), \tag{2.15}$$

where

$$\eta_{th} = \frac{\gamma_{n2}}{\gamma_{n1}} \cdot \frac{G_{m2}}{G_{m1}} + \frac{\gamma_{n3}}{\gamma_{n1}} \cdot \frac{G_{m3}}{G_{m1}} \tag{2.16}$$

represents the contribution to the input-referred thermal noise of the current source M_{2b}-M_{2c} and the current mirror M_{3a}-M_{3b} relative to that of the differential pair M_{1a}-M_{1b}. In case $G_{m1} \gg G_{m2}$ and $G_{m1} \gg G_{m3}$, then $\eta_{th} \ll 1$ and the thermal noise is dominated by the input differential pair. Eqn. (2.15) can then be simplified to

$$R_{nth} \cong \frac{2\,\gamma_{n1}}{G_{m1}}. \tag{2.17}$$

The OTA thermal noise excess factor is defined as

$$\gamma_{ota} \triangleq G_m \cdot R_{nth} \tag{2.18}$$

with $G_m = G_{m1}$ the OTA equivalent transconductance. The OTA thermal noise excess factor then writes

$$\gamma_{ota} = 2\,\gamma_{n1} \cdot (1+\eta_{th}). \tag{2.19}$$

In the case $G_{m1} \gg G_{m2}$ and $G_{m1} \gg G_{m3}$, then $\eta_{th} \ll 1$ and the noise is dominated by the input differential pair M_{1a}-M_{1b}. The OTA thermal noise excess factor can then be simplified as

$$\gamma_{ota} \cong 2\,\gamma_{n1}. \tag{2.20}$$

2.2.2 Input-referred flicker noise

The input-referred flicker noise is given by

$$R_{nfl} = \frac{2}{f}\left[\frac{\rho_n}{W_1\,L_1} + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{\rho_p}{W_2\,L_2} + \left(\frac{G_{m3}}{G_{m1}}\right)^2 \frac{\rho_n}{W_3\,L_3}\right] \tag{2.21}$$

which can be rewritten as

$$R_{nfl} = \frac{2\rho_n}{W_1\,L_1\,f} \cdot (1+\eta_{fl}) \tag{2.22}$$

where

$$\eta_{fl} = \frac{\rho_p}{\rho_n}\left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{W_1\,L_1}{W_2\,L_2} + \left(\frac{G_{m3}}{G_{m1}}\right)^2 \frac{W_1\,L_1}{W_3\,L_3} \tag{2.23}$$

represents the contribution to the input-referred flicker noise of the current source M_{2b}-M_{2c} and the current mirror M_{3a}-M_{3b} relative to that of the differential pair M_{1a}-M_{1b}.

The corner frequency is the frequency at which the flicker noise becomes equal to the thermal noise

$$R_{nfl}(f = f_k) = R_{nth} \tag{2.24}$$

which is given by

$$f_k = \frac{1}{R_{nth}} \cdot \frac{2\rho_n}{W_1\, L_1} \cdot (1 + \eta_{fl}) = \frac{G_{m1}\, \rho_n}{\gamma_{n1}\, W_1\, L_1} \cdot \frac{1 + \eta_{fl}}{1 + \eta_{th}}. \tag{2.25}$$

The transconductance G_{m1} is set by the constraints either on thermal noise or on bandwidth (GBW product). The corner frequency f_k can be reduced by increasing $W_1\, L_1$ but also $W_2\, L_2$ and $W_3\, L_3$ at the same time to conserve the same η_{fl} factor. Assuming that $G_{m2}/G_{m1} \ll 1$ and $G_{m1} \gg G_{m3}$, as required by the constraints on minimizing the contribution of the current source M_{2b}-M_{2c} and current mirror M_{3a}-M_{3b} to the input-referred offset and thermal noise, then $\eta_{th} \ll 1$ and $\eta_{fl} \ll 1$ and the corner frequency f_k is then mainly set by the differential pair transconductance and gate transistor area

$$f_k \cong \frac{G_{m1}\, \rho_n}{\gamma_{n1}\, W_1\, L_1}. \tag{2.26}$$

2.3 Input-referred offset voltage

The offset analysis is similar to that of the simple OTA because the contribution of the mismatch of the cascode transistors can be neglected. The random offset current is then mainly due to the mismatch between M_{1a} and M_{1b}, M_{2b} and M_{2c} and M_{3a} and M_{3b}. The variance of the output offset current is then given by

$$\sigma^2_{I_{os}} \cong \sigma^2_{\Delta I_{D1}} + \sigma^2_{\Delta I_{D2}} + \sigma^2_{\Delta I_{D3}} = I^2_{b1} \cdot \sigma^2_{\frac{\Delta I_{D1}}{I_{D1}}} + I^2_{b2} \cdot \sigma^2_{\frac{\Delta I_{D2}}{I_{D2}}} + I^2_{b3} \cdot \sigma^2_{\frac{\Delta I_{D3}}{I_{D3}}}, \tag{2.27}$$

with

$$\sigma^2_{\frac{\Delta I_{Di}}{I_{Di}}} = \sigma^2_{\beta_i} + \left(\frac{G_{mi}}{I_b}\right)^2 \sigma^2_{V_{Ti}} \quad \text{for } i = 1, 2, 3, \tag{2.28}$$

where

$$\sigma^2_{\beta_i} = \frac{A^2_\beta}{W_i\, L_i} \quad \text{for } i = 1, 2, 3 \tag{2.29}$$

are the β-mismatches and

$$\sigma^2_{V_{Ti}} = \frac{A^2_{V_T}}{W_i\, L_i} \quad \text{for } i = 1, 2, 3 \tag{2.30}$$

are the V_T-mismatches.

The variance of the output offset current then becomes

$$\sigma^2_{I_{os}} = I^2_{b1} \cdot \sigma^2_{\beta_1} + I^2_{b2} \cdot \sigma^2_{\beta_2} + I^2_{b3} \cdot \sigma^2_{\beta_3} + G^2_{m1} \cdot \sigma^2_{V_{T1}} + G^2_{m2} \cdot \sigma^2_{V_{T2}} + G^2_{m3} \cdot \sigma^2_{V_{T3}}. \tag{2.31}$$

The variance of the input-referred offset voltage is obtained by dividing the variance of the output offset current by G^2_{m1} resulting in

$$\sigma^2_{V_{os}} = \sigma^2_{V_T} + \sigma^2_\beta. \tag{2.32}$$

$\sigma^2_{V_T}$ is the V_T-mismatch given by

$$\sigma^2_{V_T} = \sigma^2_{V_{T1}} \cdot (1 + \xi_{V_T}) \tag{2.33}$$

where

$$\xi_{V_T} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \cdot \frac{\sigma^2_{V_{T2}}}{\sigma^2_{V_{T1}}} + \left(\frac{G_{m3}}{G_{m1}}\right)^2 \cdot \frac{\sigma^2_{V_{T3}}}{\sigma^2_{V_{T1}}} \tag{2.34}$$

represents the V_T-mismatch contributions to the input-referred offset of the current source M_{2b}-M_{2c} and current mirror M_{3a}-M_{3b} relative to that of the differential pair with

$$\sigma_{V_{T1}} = \frac{A^2_{V_{Tn}}}{W_1\, L_1}, \tag{2.35}$$

$$\sigma_{V_{T2}} = \frac{A^2_{V_{Tp}}}{W_2\, L_2}, \tag{2.36}$$

$$\sigma_{V_{T3}} = \frac{A^2_{V_{Tn}}}{W_3\, L_3}, \tag{2.37}$$

σ^2_β is the β-mismatch given by

$$\sigma^2_\beta = \left(\frac{I_{b1}}{G_{m1}}\right)^2 \cdot \sigma^2_{\beta_1} \cdot (1 + \xi_\beta) \tag{2.38}$$

where

$$\xi_\beta = \left(\frac{I_{b2}}{I_{b1}}\right)^2 \frac{\sigma^2_{\beta_2}}{\sigma^2_{\beta_1}} + \left(\frac{I_{b3}}{I_{b1}}\right)^2 \frac{\sigma^2_{\beta_3}}{\sigma^2_{\beta_1}} \tag{2.39}$$

represents the β-mismatch contributions to the input-referred offset of the current source M_{2b}-M_{2c} and current mirror M_{3a}-M_{3b} relative to that of the differential pair with

$$\sigma^2_{\beta_1} = \frac{A^2_{\beta_n}}{W_1\, L_1}, \tag{2.40}$$

$$\sigma^2_{\beta_2} = \frac{A^2_{\beta_p}}{W_2\, L_2}, \tag{2.41}$$

$$\sigma^2_{\beta_3} = \frac{A^2_{\beta_n}}{W_3\, L_3}. \tag{2.42}$$

Replacing in (2.34) and (2.39) results in

$$\xi_{V_T} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \left(\frac{A_{V_{Tp}}}{A_{V_{Tp}}}\right)^2 \frac{W_1\, L_1}{W_2\, L_2} + \left(\frac{G_{m3}}{G_{m1}}\right)^2 \frac{W_1\, L_1}{W_3\, L_3} \tag{2.43}$$

and

$$\xi_\beta = \left(\frac{I_{b2}}{I_{b1}}\right)^2 \left(\frac{A_{\beta_p}}{A_{\beta_n}}\right)^2 \frac{W_1\, L_1}{W_2\, L_2} + \left(\frac{I_{b3}}{I_{b1}}\right)^2 \frac{W_1\, L_1}{W_2\, L_2}. \tag{2.44}$$

Similarly to the flicker noise, the input-referred offset (variance or standard deviation) can be reduced by increasing the area $W_1\, L_1$ of M_{1a}-M_{1b} but at the same time also increasing the area $W_2\, L_2$ of the current source M_{2b}-M_{2c} and also the area $W_3\, L_3$ of the current mirror M_{3a}-M_{3b}.

3 Design

3.1 Specifications

The OTA specifications are given in Table 3.1.

> **Note**
>
> The specifications given in Table 3.1 are simplified specifications. They are mainly targeting the achievement of a certain gain-bandwidth product GBW and DC gain at lowest current consumption. The GBW sets the differential pair transconductance while the DC gain sets the output conductance. There is an additional specification on the random input-referred offset voltage which, if not met, might eventually require to increase the transistors area. There are no specifications on thermal noise since the transconductance is set by the GBW. There are no specifications on the flicker noise but if the corner frequency was set lower this would required to increase the transistors area. There are also no specifications on the slew-rate, which might be small because of the low-power objective. Finally, there are many more specifications such as CMRR, PSRR, input common-mode voltage range, output-voltage swing, etc... that are not discussed in this example.

Table 3.1: OTA specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	100	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF
Maximum input-referred random offset voltage	V_{os}	10	mV
Phase margin	PM	60	$^\circ$

3.2 Process

We will design the cascode gain stage for a generic 180nm bulk CMOS process. The physical parameters are given in Table 3.2, the global process parameters in Table 3.3 and finally the MOSFET parameters in Table 3.4.

Table 3.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 3.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 3.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	715	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	20	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	8.1e-24	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

3.3 Design procedure

> **!** Important
>
> For this process, the transistor dimensions are rounded to 10nm. We also will ignore the length and width reduction parameters DL and DW. The main reason is that most of the transistor length and width are sufficiently large that ignoring these parameters has little impact.

We start sizing the differential pair M_{1a}-M_{1b}.

3.3.1 Sizing the differential pair M_{1a}-M_{1b}

In this example there is no specification on the thermal noise. Therefore the transconductance G_{m1} is set by the gain-bandwidth product according to

$$GBW = \frac{G_{m1}}{2\pi C_{out}}, \tag{3.1}$$

where G_{m1} is the gate transconductance of M_{1a} and M_{1b} and C_{out} the total output capacitance

$$C_{out} = C_o + C_L \tag{3.2}$$

with C_o the parasitic capacitance at the output node and C_L the load capacitance.

In order to minimize the input-referred noise and offset, the input differential pair should be biased in weak inversion. The transconductance G_{m1} in deep weak inversion is then given by

$$G_{m1} = \frac{I_{b1}}{nU_T}. \tag{3.3}$$

The bias current I_{b1} is the current flowing in each transistor M_{1a} and M_{1b} when the input differential voltage is zero. The bias current provided by M_{5b} is therefore $2I_{b1}$. The bias current must satisfy the following inequality:

$$I_{b1} \geq 2\pi n_{0n} U_T C_{out} GBW_{min}. \tag{3.4}$$

which for the given specifications gives $I_{b1,min} = 207\ nA$. The corresponding slew-rate is then equal to $SR_{min} = 207\ mV/\mu s$ which we will consider as sufficient.

> **!** Important
>
> If the slew-rate is not sufficient, the bias current I_b should be increased resulting in a higher current and power consumption. Other options include the use of a class AB OTA [9] or a dynamic/adaptive biasing OTA [10].

To have some margin to account for the additional parasitic capacitance at the output C_o due mostly to the junction capacitances that add to the load capacitance C_L, we set $I_{b1} = 250\ nA$ and the inversion coefficient to $IC_1 = 0.1$. The transconductance can be calculated from the G_m/I_D function as $G_{m1} = 6.962\ \mu A/V$. This leads to a gain-bandwidth product $GBW = 1.1\ MHz$, which is slightly higher than the target specification offering some margin. Knowing the drain current I_{D1} and the inversion coefficient, we can calculate the specific current $I_{spec1} = 2.500\ \mu A$ and the aspect ratio $W_1/L_1 = 3.5$.

The degree of freedom left (W_1 or L_1) can be determined by constraints either on the dc gain, the offset voltage or the flicker noise.

Before finalizing the sizing of the differential pair, we first will size the current mirror M_{3a}-M_{3b} and the current sources M_{2a}-M_{2b}-M_{2c}.

3.4 Sizing of M_{3a}-M_{3b}

The current mirror M_{3a}-M_{3b} should be biased as much in strong inversion as the voltage constraint allows for. We can set its V_{GS} voltage to the desired quiescent output voltage which we set to $V_{GS3} = V_{outq} = V_{DD}/2 = 900\ mV$, which corresponds to an inversion coefficient $IC_3 = 40.429$ and a saturation voltage $V_{DSsat3} = 345\ mV$. We see that choosing a large IC and hence a large V_{GS} voltage comes at the cost of a large saturation voltage and hence a reduced output voltage swing. As discussed in the introduction we have chosen $\alpha = 1.200$ so that $I_{b3} = 300\ nA$ and $I_{b2} = I_{b1} + I_{b3} = 550\ nA$. Having set the inversion coefficient and bias current we can derive the specific current $I_{spec3} = 7.42$

nA and the aspect ration $W_3/L_3 = 0.010$. Having IC and I_D, we can deduce the transconductance $G_{m3} = 1.326\ \mu A/V$.

We will now have to make sure that the non-dominant pole f_p at node 3 is sufficiently higher than the gain-bandwidth product GBW to insure the desired phase margin. The non-dominant pole is given

$$\omega_p = \frac{G_{m3}}{C_3}, \tag{3.5}$$

where C_3 is given by

$$C_3 = 2(C_{GS3} + C_{GB3}) \tag{3.6}$$

Assuming that M_{3a}-M_{3b} are in saturation, the gate-to-source capacitance C_{GS3} is given by

$$C_{GS3} \cong W_3\, L_3\, C_{ox} \cdot c_{gsi} + C_{GSon} \cdot W_3, \tag{3.7}$$

where C_{GSon} is the gate-to-source overlap capacitance per unit width for nMOS transistors. c_{gsi} is the intrinsic gate-to-source capacitance normalized to the total gate capacitance $W\, L\, C_{ox}$, which is typically equal to 2/3 in strong inversion and is proportionnal to IC in weak inversion.

The gate-to-bulk capacitance C_{GB3} is given by

$$C_{GB3} \cong\ W_3\, L_3\, C_{ox} \cdot c_{gbi} + C_{GBon} \cdot W_3, \tag{3.8}$$

where C_{GBon} is the gate-to-bulk overlap capacitance per unit width and c_{gbi} is the gate-to-bulk intrinsic capacitance normalized to the total gate capacitance $W\, L\, C_{ox}$ and given by

$$c_{gbi} = \frac{n-1}{n} \cdot c_{gsi}. \tag{3.9}$$

The capacitance at node 3 then scales with W_3 and L_3 according to

$$C_3 = W_3\, L_3 \cdot C_{WL} + W_3 \cdot C_W, \tag{3.10}$$

with

$$C_{WL} = 2\, C_{ox} \cdot (c_{gsi} + c_{gbi}), \tag{3.11}$$

$$C_W = 2(C_{GSon} + G_{GBon}). \tag{3.12}$$

We already have set the inversion coefficient $IC_3 = 40.429$, from which we can calculate $c_{gsi} = 0.611$ and $c_{gbi} = 0.083$. Since the W/L has already been set by the transconductance and the current, we can derive W_3 and L_3 for achieving a given capacitance C_3 according to

$$W_3 = \frac{-C_W \cdot W_3/L_3 + \sqrt{W_3/L_3} \cdot \sqrt{4\, C_3\, C_{WL} + C_W^2 \cdot W_3/L_3}}{2\, C_{WL}}, \tag{3.13}$$

$$L_3 = \frac{W_3}{W_3/L_3}. \tag{3.14}$$

Setting the non-dominant pole f_p to 10 times the GBW, we get $C_3 = 21$ fF, $W_3 = 140\ nm$ and $L_3 = 13.49\ \mu m$. We see that W_3 is smaller than the minimum width. If we don't want to increase $W_3\, L_3$ and hence C_3, we need to reduce the inversion coefficient IC_3. We can find the IC such that $W_3 = W_{min}$ for the given f_p by looking at Figure 3.1.

We get $IC_3 = 22.9$, $W_3 = 200\ nm$, $L_3 = 10.93\ \mu m$, $C_3 = 13.4\ fF$, $G_{m3} = 1.716\ \mu A/V$ and $I_{spec3} = 13.08\ nA$. This leads to the desired ratio $f_p/GBW = 10.0$.

The inversion coefficient of M_{3a}-M_{3b} is therefore reduced from 40.4 to 22.9 in order to maintain a reasonable parasitic capacitance at node 3 to make sure that f_p is 10 times higher than the GBW.

Note that the V_{GS3} voltage has also dropped to $V_{GS3} = 787\ mV$, so that the quiescent output voltage is now lower than $V_{outq} = V_{DD}/2 = 900\ mV$. We might need to introduce an offset voltage to shift the output back to V_{outq} (in the high gain region). On the other hand the saturation voltage is now also lower $V_{DSsat3} = 269\ mV$ improving the output swing.

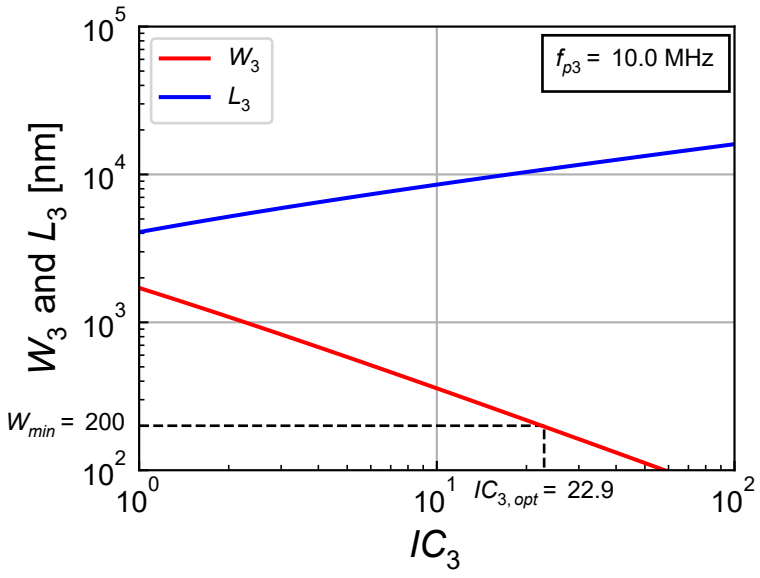

Figure 3.1: Length L_3 and width W_3 of M_3 versus IC_3 for a given f_{p3}/GBW ratio.

3.5 Sizing of M_{4a}-M_{4b} and M_{5a}-M_{5b}

The cascode transistors are sized according to the desired DC gain given by

$$A_{dc} = \frac{G_{m1}}{G_o} \tag{3.15}$$

where G_o is the conductance at the output node given by

$$G_o \cong G_{o35} + G_{o124} \tag{3.16}$$

where

$$G_{o35} \triangleq \frac{G_{ds3}\, G_{ds5}}{G_{ms5}}, \tag{3.17}$$

$$G_{o124} \triangleq \frac{(G_{ds1} + G_{ds2})\, G_{ds4}}{G_{ms4}}. \tag{3.18}$$

The minimum DC gain specification is given by A_{dc} = 1.0e+05 or A_{dc} = 100 dB. We can then deduce the total output conductance $G_o = 69.618\ pA/V$. We will split the output conductance G_o equally between G_{o35} and G_{o124}s.

To minimize the saturation voltage and maximize the current efficiency, the cascode transistors M_{4a}-M_{4b} and M_{5a}-M_{5b} are biased in weak inversion. We choose their inversion coefficient as $IC_4 = IC_5 = 0.1$, which gives a saturation voltage $V_{DSsat4} = V_{DSsat5} = 105\ mV$. Having set the inversion coefficient and knowing the bias current, we can deduce the specific current $I_{spec4} = 3.0\ \mu A$ and the aspect ratio $W_4/L_4 = 17.328$ for M_{4a}-M_{4b} and $I_{spec5} = 3.0\ \mu A$ and $W_5/L_5 = 4.196$ for M_{5a}-M_{5b}.

We can now calculate the source transconductances that are needed for the calculation of the output conductances $G_{ms4} = 10.621\ \mu A/V$ and $G_{ms5} = 10.621\ \mu A/V$. Having already the length of M_{3a}-M_{3b}, we can estimate its output conductance $G_{ds3} = 1.372\ nA/V$. We can then deduce the output conductance of M_{5a}-M_{5b} $G_{ds5} = 269.4\ nA/V$, which corresponds to a cascode gain $G_{ms5}/G_{ds5} = 39.4$. We can then deduce the length of M_{5a}-M_{5b} from G_{ds5} as $L_5 = 56\ nm$, which is lower than L_{min}.

We could choose $L_5 = L_{min}$, but in order to avoid DIBL and secure the DC gain, we increase the length of M_{5a}-M_{5b} to $L_5 = 540\ nm$. Keeping the same W/L we get the width $W_5 = 2.27\ \mu m$.

We can recalculate the contribution of M_{3a}-M_{3b} and M_{5a}-M_{5b} to the total output conductance $G_{o35} = 3.6\ pA/V$ and deduce the remaining contribution allocated to M_{1a}-M_{1b}, M_{2b}-M_{2c} and M_{4a}-M_{4b} $G_{o124} = 0.1\ nA/V$.

At this point we don't know the lengths neither of M_{1a}-M_{1b} nor of M_{2b}-M_{2c} and M_{4a}-M_{4b}. We can choose that $G_{ds1} + G_{ds2} = G_{ds4}$ and $G_{ds1} = G_{ds2}$ so that $G_{ds1} = G_{ds2} = G_{ds4}/2$. We can then deduce the output conductance of M_{4a}-M_{4b} $G_{ds4} = 26.316\ nA/V$ from which we get the length $L_4 = 570\ nm$ and width $W_4 = 9.88\ \mu m$. The cascode voltage gain is then given by $G_{ms4}/G_{ds4} = 403.6$. We can deduce the length of M_{1a}-M_{1b} and M_{2b}-M_{2c} accounting for the different currents flowing in M_{4a}-M_{4b}, M_{1a}-M_{1b} and M_{2b}-M_{2c} $L_1 = 0.94\ \mu m$ and $L_2 = 2.08\ \mu m$.

We can now finalize the sizing of M_{1a}-M_{1b} with $W_1 = 3.29\ \mu m$. We can check the theoretical DC gain $A_{dc} = 1.0\text{e+}05$ (estimation) or $A_{dc} = 100$ dB (estimation).

3.6 Sizing of M_{2a}-M_{2b}-M_{2c}

To size M_{2b}-M_{2c} we will choose its saturation voltage to $V_{SDsat2} = 300\ mV$ in order to maximize the output swing. This leads to an inversion coefficient $IC_2 = 29.606$, a specific current $I_{spec2} = 0.019\ \mu A$ and an aspect ratio $W_2/L_2 = 0.107$. Knowing $L_2 = 2.08\ \mu m$ we deduce $W_2 = 220\ nm$.

The contribution to the input-referred noise PSD of M_{2b}-M_{2c} can be quite large compared to that of the differential pair M_{1a}-M_{1b} because the current I_{b2} is at least two times I_{b1}. It is therefore hard to make G_{m2} much smaller than G_{m1} without drastically increasing IC and hence V_{DSsat} and loosing output swing. We can check the contribution of M_{2a}-M_{2b}-M_{2c} to the input-referred noise. If M_{2a}-M_{2b}-M_{2c} are perfectly matched, the noise produced by M_{2a} is canceled out at the output and can therefore be neglected. Since the noise is usually dominated by the flicker noise we can calculate the contribution of M_{2b}-M_{2c} to the input-referred flicker noise relative to the contribution of the differential pair M_{1a}-M_{1b}

$$\eta_{fl}|_{M_{2b}\text{-}M_{2c}} = \frac{\rho_p}{\rho_n} \left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{W_1\, L_1}{W_2\, L_2} \tag{3.19}$$

We get $\eta_{fl}|_{M_{2b}\text{-}M_{2c}} = 6.693$ which is very large.

Setting $\eta_{fl}|_{M_{2b}\text{-}M_{2c}}$ to 1, results in $W_2 = 0.63\ \mu m$ and $L_2 = 5.86\ \mu m$ which reduces $\eta_{fl}|_{M_{2b}\text{-}M_{2c}}$ to 0.930 when accounting for the effective width and length.

We can also check the contribution of M_{3a}-M_{3b} to the input-referred noise by calculating

$$\eta_{fl}|_{M_{3a}\text{-}M_{3b}} = \left(\frac{G_{m3}}{G_{m1}}\right)^2 \frac{W_1\, L_1}{W_3\, L_3} \tag{3.20}$$

which is equal to 0.170.

3.7 Sizing M_{7a}-M_{7b}

The size of M_{7a}-M_{7b} is conditioned by the minimum input common-mode voltage $V_{ic,min}$

$$V_{ic,min} = V_{GS1} + V_{DSsat7}. \tag{3.21}$$

The gate-to-source voltage V_{GS1} is given by

$$V_{GS1} = V_{T0n} + (n_{0n} - 1)\, V_{S1} + n_{0n}\, U_T\, (v_p - v_s) \tag{3.22}$$

Unfortunately, at this point we don't know the value of the source voltage V_{S1} of M_{1a}-M_{1b} (voltage at common-source node 1). In weak inversion $v_p - v_s \cong 0$ so that

$$V_{GS1} \cong V_{T0n} + (n_{0n} - 1)\, V_{S1} \tag{3.23}$$

Since we don't know V_{S1} we can approximate V_{GS1} by $V_{T0n} = 455\ mV$. If we set the minimum input common-mode voltage to $V_{ic,min} = 0.75\ V$, it results in a saturation voltage voltage for M_{7a}-M_{7b} equal to $V_{DSsat7} = 295\ mV$, which corresponds to an inversion coefficient $IC_7 = 28.5$. Having the IC and the current we can derive the specific current $I_{spec7} = 18\ nA$ and the aspect ratio $W_7/L_7 = 0.025$. Since the W/L is small, we need to set the width to $W_7 = W_{min} = 200\ nm$ resulting in a length $L_7 = 8.15\ \mu m$.

We now need to set the bias voltages V_{b1} and V_{b2}.

3.8 Bias voltages V_{b1} and V_{b2}

We still need to calculate the required bias voltages V_{b1} for M_{5a}-M_{5b} and V_{b2} for M_{4a}-M_{4b}.

We start calculating the maximum bias voltage $V_{b2,max}$ still keeping M_{2a}-M_{2b} in saturation

$$V_{b2,max} = V_{DD} - V_{SG4} - V_{SDsat2} \tag{3.24}$$

The saturation voltage of M_{2a}-M_{2b} is given by IC_2 as $V_{SDsat2} = 300\ mV$. The source-to-gate voltage V_{SG4} is given by

$$V_{SG4} = V_{T0p} + (n_{0p} - 1)\, V_{BS4} + n_{0p}\, U_T\, (v_p - v_s) \tag{3.25}$$

In weak inversion $v_p - v_s \cong 0$ and therefore

$$V_{SG4} \cong V_{T0p} + (n_{0p} - 1)\, V_{BS4} \tag{3.26}$$

However, at this point we don't know the source voltage of M_{4a}-M_{4b}. We can estimate that $V_{SG4} \cong V_{T0p} = 445\ mV$ which results in $V_{b2,max} = 1055\ mV$.

We also want to make sure that the V_{SD} voltage across M_{4a}-M_{4b} is large enough not to degrade the output conductance. We can choose $V_{SD4} = 200\ mV$, which gives $V_{b2,min} = 542\ mV$.

The maximum value of V_{b1} is set by keeping a sufficient V_{DS} voltage for M_{5a}-M_{5b}

$$V_{b1,max} = V_{GS5} - V_{DS5} + V_{GS3} \tag{3.27}$$

where

$$V_{GS5} = V_{T0n} + (n_{0n} - 1)\, V_{SB5} + n_{0n}\, U_T\, (v_p - v_s) \cong V_{T0n} + (n_{0n} - 1)\, V_{SB5} \cong V_{T0n}. \tag{3.28}$$

If we choose $V_{DS5} = 200\ mV$, we get $V_{b1,max} = 1042\ mV$.

The minimum V_{b1} voltage is set by keeping M_{3a}-M_{3b} in saturation

$$V_{b1,min} = V_{GS5} + V_{DSsat3} \tag{3.29}$$

resulting in $V_{b1,min} = 724\ mV$.

So the bias voltages V_{b1} and V_{b2} shuld satisfy the following inequalities

$0.724\ V \leq V_{b1} \leq 1.042\ V$ and

$0.542\ V \leq V_{b2} \leq 1.055\ V$

We finally choose $V_{b1} = 1.000\ V$ and $V_{b2} = 0.600\ V$.

The sizing process is now completed. The transistor sizes and bias are summarized below.

3.9 Summary

3.9.1 Specifications

The specifications are recalled in Table 3.5.

Table 3.5: OTA specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	100	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF
Maximum input-referred random offset voltage	V_{os}	10	mV
Phase margin	PM	60	$^\circ$

3.9.2 Bias

The bias information are summarized in Table 3.6.

Table 3.6: OTA bias.

Bias voltage or current	Symbol	Value	Unit
Supply voltage	V_{DD}	1.80	V
Bias current	I_{b1}	250.00	nA
Bias current	I_{b2}	550.00	nA
Cascode bias voltage	V_{b1}	1.00	V
Cascode bias voltage	V_{b2}	0.60	V

3.9.3 Transistor information

The transistor sizes and large-signal variables are summarized in Table 3.7, whereas Table 3.8 gives the small-signal and thermal noise parameters. An Excel table is generated with more information (e.g. all the parasitic capacitances).

Table 3.7: Transistor size and bias information.

Transistor	W $[\mu m]$	L $[\mu m]$	I_D $[nA]$	I_{spec} $[nA]$	IC	$V_G - V_{T0}$ $[mV]$	V_{DSsat} $[mV]$
M1a	3.29	0.94	250	2503	0.1	-45	105
M1b	3.29	0.94	250	2503	0.1	-45	105
M2a	1.26	5.86	1100	37	29.5	228	300
M2b	0.63	5.86	550	19	29.5	228	300
M2c	0.63	5.86	550	19	29.5	228	300
M3a	0.20	10.93	300	13	22.9	205	269
M3b	0.20	10.93	300	13	22.9	205	269
M4a	9.88	0.57	300	3001	0.1	-44	105
M4b	9.88	0.57	300	3001	0.1	-44	105
M5a	2.27	0.54	300	3006	0.1	-45	105
M5b	2.27	0.54	300	3006	0.1	-45	105
M7a	0.20	8.15	500	18	28.5	230	295
M7b	0.20	8.15	500	18	28.5	230	295

Table 3.8: Transistor small-signal and thermal noise parameters.

Transistor	n	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M1a	1.271	96.716	8.852	6.962	13.298	0.653
M1b	1.271	96.716	8.852	6.962	13.298	0.653
M2a	1.306	1.439	7.134	5.463	9.386	0.834
M2b	1.306	0.719	3.567	2.731	4.693	0.834
M2c	1.306	0.719	3.567	2.731	4.693	0.834
M3a	1.271	0.506	2.182	1.716	1.372	0.808
M3b	1.271	0.506	2.182	1.716	1.372	0.808
M4a	1.306	115.980	10.621	8.133	26.316	0.671
M4b	1.306	115.980	10.621	8.133	26.316	0.671
M5a	1.271	116.161	10.623	8.355	27.778	0.653
M5b	1.271	116.161	10.623	8.355	27.778	0.653
M7a	1.271	0.678	3.297	2.593	3.067	0.811
M7b	1.271	0.678	3.297	2.593	3.067	0.811

4 OTA Characteristics

In this section, we check whether the specs are achieved.

4.1 Open-loop gain

We can calculate the various OTA features related to the open-loop transfer function, which are given in Table 4.1.

Table 4.1: OTA gain variables.

Symbol	Theoretical Value	Unit
A_{dc}	103.201	dB
G_{m1}	6.962	$\mu A/V$
G_{m2}	2.731	$\mu A/V$
G_{m3}	1.716	$\mu A/V$
G_{ms4}	10.621	$\mu A/V$
G_{ms5}	10.623	$\mu A/V$
G_{ds1}	13.298	nA/V
G_{ds2}	4.693	nA/V
G_{ds3}	1.372	nA/V
G_{ds4}	26.316	nA/V
G_{ds5}	27.778	nA/V
C_3	25.217	fF
C_4	54.747	fF
f_0	7.530	Hz
GBW	1.089	MHz
f_p	10.830	MHz
f_z	21.660	MHz
f_{p4}	30.877	MHz

The gain-bandwidth product from the specifications is repeated here

$GBW = 1.000$ MHz (from spec).

The estimate value assuming that all the non-dominant poles are much higher than the GBW is given by

$GBW_{est} = 1.089$ MHz (estimation).

The GBW accounting for the effect of the additional non-dominant poles is given by

$GBW_{the} = 1.084$ MHz (theory).

We see that there is only a small difference between GBW_{est} and GBW_{the}, which confirms that the non-dominant poles are sufficiently far from GBW as stated in Table 4.1.

We can now plot the gain response Using the variables given in Table 4.1. It is shown in Figure 4.1.

From Figure 4.1, we see that the GBW and DC gain are met.

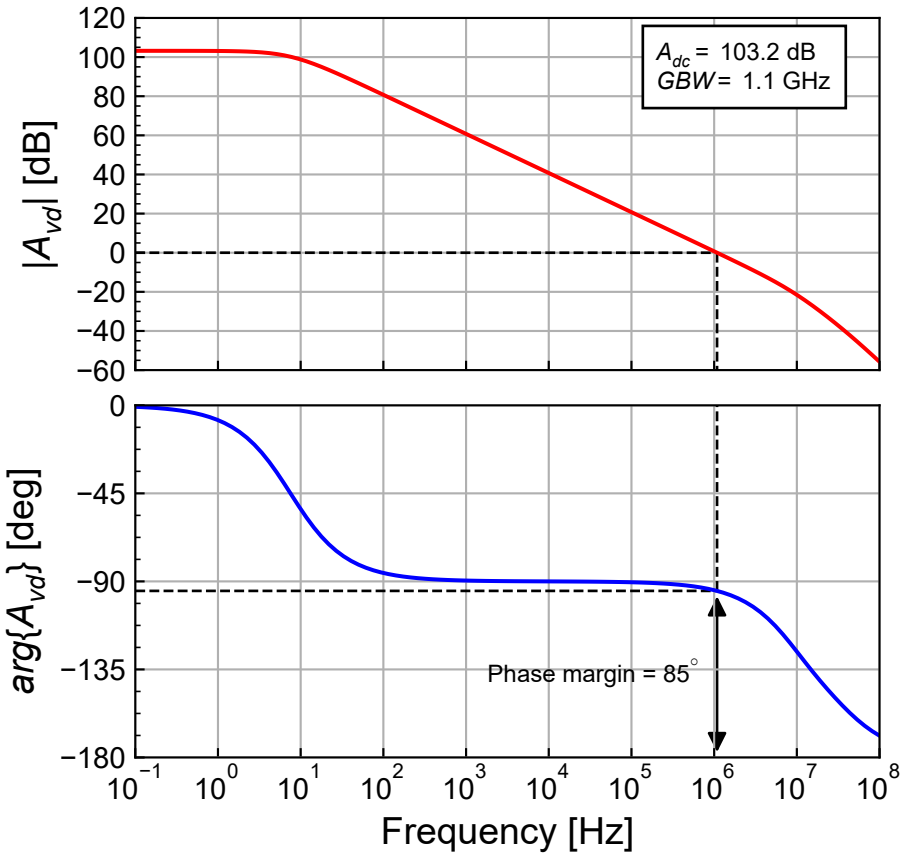

Figure 4.1: OTA theoretical transfer function.

We can now have a look at the input-refrred noise PSD.

4.2 Input-referred noise

We can now compute all the parameters needed for the calculation of the OTA thermal noise excess factor and its input-referred thermal noise PSD and resistance. They are given in Table 4.2.

Table 4.2: OTA thermal noise parameters.

Symbol	Theoretical Value	Unit
G_{m1}	6.962	$\mu A/V$
G_{m2}	2.731	$\mu A/V$
G_{m3}	1.716	$\mu A/V$
G_{m1}/G_{m2}	2.549	-
G_{m1}/G_{m3}	4.057	-
γ_{n1}	0.653	-
γ_{n2}	0.834	-
γ_{n3}	0.808	-
η_{th}	0.805	-
γ_{ota}	2.359	-
R_{nt}	338.892	$k\Omega$
S_{ninth}	5.6e-15	V^2/Hz
$\sqrt{S_{ninth}}$	74.914	$nV/\sqrt{Hz}$
$10 \cdot \log(S_{ninth})$	-142.509	$dBv/\sqrt{Hz}$

From Table 4.2, we see that the contribution of M_{2b}-M_{2c} and M_{3a}-M_{3b} is only 0.805 that of M_{1a}-M_{1b}. This leads to an OTA thermal noise excess factor $\gamma_{n,ota} = 2.359$, which is 1.8 times larger than that of the differential pair $2\,\gamma_{n1} = 1.307$.

We can now compute all the parameters needed for the calculation of the input-referred flicker noise and the corner frequency. They are given in Table 4.3.

Table 4.3: OTA flicker noise parameters.

Symbol	Theoretical Value	Unit
$(G_{m1}/G_{m2})^2$	6.5	-
$(G_{m1}/G_{m3})^2$	16.5	-
ρ_p/ρ_n	8.3	-
$\frac{W_1 \cdot L_1}{W_2 \cdot L_2}$	0.7	-
$\frac{W_1 \cdot L_1}{W_3 \cdot L_3}$	1.1	-
η_{fl}	0.999	-
$\sqrt{S_{ninfl}(1\,Hz)}$	36.5	$\mu V/\sqrt{Hz}$
$10 \cdot \log(S_{ninfl}(1\,Hz))$	-88.7	$dBv/\sqrt{Hz}$
f_k	238	kHz

As desired, from Table 4.3, we see that the contribution of M_{2b}-M_{2c} and M_{3a}-M_{3b} to the flicker noise is only 0.999 that of M_{1a}-M_{1b}. It is sligthly lower than the value obtained in the design phse simply because the calculations use the effective width and length.

We can plot the input-reffered noise which is shown in Figure 4.2.

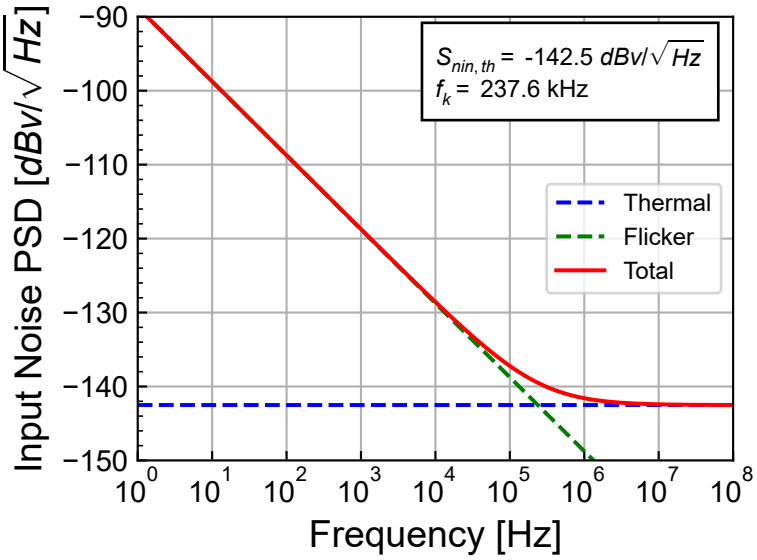

Figure 4.2: OTA theoretical input-referred noise PSD.

4.3 Input-referred offset

The variance of the input-referred offset voltage is given by (2.32), which is repeated below

$$\sigma^2_{V_{os}} = \sigma^2_{V_T} + \sigma^2_{\beta}. \tag{4.1}$$

$\sigma^2_{V_T}$ is the V_T-mismatch given by

$$\sigma^2_{V_T} = \sigma^2_{V_{T1}} \cdot (1 + \xi_{V_T}) \tag{4.2}$$

where

$$\xi_{V_T} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \left(\frac{A_{V_{Tp}}}{A_{V_{Tp}}}\right)^2 \frac{W_1\,L_1}{W_2\,L_2} + \left(\frac{G_{m3}}{G_{m1}}\right)^2 \frac{W_1\,L_1}{W_3\,L_3} \tag{4.3}$$

represents the V_T-mismatch contributions to the input-referred offset of the current source M_{2b}-M_{2c} and current mirror M_{3a}-M_{3b} relative to that of the differential pair.

σ_β^2 is the β-mismatch given by

$$\sigma_\beta^2 = \left(\frac{I_{b1}}{G_{m1}}\right)^2 \cdot \sigma_{\beta_1}^2 \cdot (1 + \xi_\beta) \tag{4.4}$$

where

$$\xi_\beta = \left(\frac{I_{b2}}{I_{b1}}\right)^2 \left(\frac{A_{\beta_p}}{A_{\beta_n}}\right)^2 \frac{W_1\,L_1}{W_2\,L_2} + \left(\frac{I_{b3}}{I_{b1}}\right)^2 \frac{W_1\,L_1}{W_2\,L_2}. \tag{4.5}$$

The parameter for calculating the standard deviation of the input-referred offset voltage are given in Table 4.4.

Table 4.4: OTA input-referred offset parameters.

Symbol	Theoretical Value	Unit
σ_{VT1}	2.843	mV
σ_{VT2}	2.602	mV
σ_{VT3}	3.382	mV
$\sigma_{\beta 1}$	0.569	%
$\sigma_{\beta 2}$	0.520	%
$\sigma_{\beta 3}$	0.676	%
$(G_{m2}/G_{m1})^2$	0.154	-
$(G_{m3}/G_{m1})^2$	0.061	-
$W_1\,L_1/(W_2\,L_2)$	0.838	-
$W_1\,L_1/(W_3\,L_3)$	1.415	-
$(I_{b2}/I_{b1})^2$	4.840	-
$(I_{b3}/I_{b1})^2$	1.440	-
ξ_{VT}	0.215	-
ξ_β	6.092	-
$\sigma_{V_T}^2$	9.821	mV^2
σ_{V_T}	3.134	mV
σ_β^2	0.296	mV^2
σ_β	0.544	mV
σ_{Vos}	3.181	mV

From Table 4.4 and contrary to the other OTA, we see that in the case of the folded cascode OTA the β-mismatch cannot be neglected. This is mostly because of the $W_1\,L_1/(W_3\,L_3)$ ratio equal to 1.415.

4.4 Current and power consumption

The total current consumption, ignoring the current drawn by M_{2a} and M_{7a}, is $I_{tot} = 2I_{b2} = 1.1\ \mu A$ and the power consumption is $P = 1.980\ \mu W$.

Assuming the input differential pait M_{1a}-M_{1b} is biased in deep weak inversion, the minimum bias current $I_{b1,min}$ is directly related to the gain-bandwidth product GBW according to

$$I_{b1,min} \cong nU_T \cdot C_L \cdot \omega_u = nU_T \cdot C_L \cdot 2\pi\,GBW, \tag{4.6}$$

which is equal to 207 nA. The minimum total current consumption assuming $\alpha \triangleq I_{b3}/I_{b1} = 1.2$ can then be estimated as $I_{tot,min} \cong 2I_{b2,min} = 2(I_{b1,min} + I_{b3,min}) = 2I_{b1,min}\,(1+\alpha) = 909\ nA$. The actual current consumption accounting for some margin taken on the GBW is therefore 21% higher than the minimum.

The current consumption of the folded cascode OTA is 2.2 times larger than that of the telescopic OTA for the same specifications.

> **Note**
>
> Note that the telescopic OTA is the differential OTA that has the minimum power consumption for similar gain-bandwidth product, DC gain and phase margin specifications. Of course it has the smallest input and output voltage swings.

The above design will now be checked against simulations.

5 Simulation results from ngspice

The theoretical results can be validated with the results obtained from simulations performed with ngspice. In order to run the simulations you need to have ngspice correctly installed. Please refer to the installation instructions.

> **Note**
>
> The simulations are performed with ngspice [2] using the EKV 2.6 compact model [4] [3] [11]. For ngspice, we use the original Verilog-A implementation of EKV 2.6 [6] modified by C. Enz to get the operating point informations and available on the Gitub va-models site provided by D. Warning at [5] [12]. The Verilog-A code was then compiled with OpenVAF [13] to generate the OSDI for running it with ngspice. The parameters correspond to a generic 180 nm bulk CMOS process [7].

5.1 Operating point

We first write the parameter file for this specific design for running the ngspice simulations. Before running the AC and NOISE simulations, we first need to check the quiescent voltages and currents and the operating points of all transistors by running a .OP simulation.

Table 5.1: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
vb1	1
vb2	0.6
inp	0.9
inn	0.9
out	0.785397
ic	0.9
id	0
1	0.391179
2	0.930824
3	0.785397
4	1.18638
5	1.18638
6	0.462576
7	0.462576
8	0.813271

We can extract the OTA quiescent node voltages from the ngspice .ic file. They are presented in Table 5.1. We see that the simulated quiescent output voltage is $V_{outq} = 785\ mV$. This is fine and the OTA is biased in the high gain region. Similarly to the telescopic OTA, the quiescent output voltage is actually set by the V_{GS} voltage of M_{3a}. Indeed, if perfect matching is assumed (which is the case in

the simulation), since M_{5a}-M_{5b} have the same drain current and share the same gate voltage, they have the same V_{GS} voltage and also have the same drain voltage. We therefore don't need to extract any offset voltage at this point and can proceed with the simulation of the large-signal characteristic.

The operating point information for all transistors are extracted from the ngspice .op file. The data is split into the large-signal operating informations in Table 5.2, the small-signal operating point informations in Table 5.3 and the noise operating point informations in Table 5.4.

Table 5.2: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[nA]$	I_{spec} $[nA]$	IC	n	V_{Dsat} $[mV]$
M1a	249	2539	0.098	1.27	120
M1b	249	2539	0.098	1.27	120
M2a	1100	32	33.992	1.31	405
M2b	572	17	33.988	1.31	405
M2c	572	17	33.988	1.31	405
M3a	323	14	23.420	1.27	354
M3b	323	14	23.420	1.27	354
M4a	323	2738	0.118	1.31	121
M4b	323	2738	0.118	1.31	121
M5a	323	3216	0.100	1.27	120
M5b	323	3216	0.100	1.27	120
M7a	500	18	27.292	1.27	374
M7b	499	18	27.282	1.27	374

Table 5.3: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	G_m $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_{ds} $[nA/V]$
M1a	7.105	8.816	13.317
M1b	7.105	8.816	13.317
M2a	4.845	6.584	3.794
M2b	2.519	3.424	2.239
M2c	2.519	3.424	2.239
M3a	1.759	2.268	1.493
M3b	1.759	2.268	1.493
M4a	8.975	11.266	23.312
M4b	8.975	11.266	23.312
M5a	9.230	11.371	46.171
M5b	9.230	11.371	46.171
M7a	2.538	3.272	1.645
M7b	2.522	3.267	16.297

Table 5.4: Noise operating point information extracted from ngspice .op file for each transistor.

Transistor	R_n $[k\Omega]$	$\sqrt{S_{ID,th}}$ $[nA/\sqrt{Hz}]$	γ_n [-]	$\sqrt{S_{ID,fl}}$ at 1Hz $[nA/\sqrt{Hz}]$
M1a	90.681	38.770	0.644	18245
M1b	90.681	38.770	0.644	18245
M2a	184.599	55.317	0.894	32389.5
M2b	354.989	76.709	0.894	44892.6
M2c	354.989	76.709	0.894	44892.6
M3a	481.883	89.374	0.848	19211.6

Table 5.4: Noise operating point information extracted from ngspice .op file for each transistor.

Transistor	R_n [$k\Omega$]	$\sqrt{S_{ID,th}}$ [$nA/\sqrt{Hz}$]	γ_n [-]	$\sqrt{S_{ID,fl}}$ at 1Hz [$nA/\sqrt{Hz}$]
M3b	481.883	89.374	0.848	19211.6
M4a	72.719	34.719	0.653	40159.7
M4b	72.719	34.719	0.653	40159.7
M5a	69.428	33.924	0.641	29894.2
M5b	69.428	33.924	0.641	29894.2
M7a	336.221	74.654	0.853	22274.8
M7b	340.070	75.080	0.858	22274.8

We can also check the bias voltages and operating region of each transistor which are given in Table 5.5.

Table 5.5: Bias voltages and operating regions extracted from ngspice for each transistor.

Trans.	Type	Funct.	V_G [V]	V_S [V]	V_D [V]	V_{DS} [mV]	V_{DSsat} [mV]	Reg.	Sat.
M1a	n	DP	0.900	0.391	1.186	795	120	WI	sat
M1b	n	DP	0.900	0.391	1.186	795	120	WI	sat
M2a	p	CM	0.869	0.000	0.869	869	405	SI	sat
M2b	p	CM	0.869	0.000	0.614	614	405	SI	sat
M2c	p	CM	0.869	0.000	0.614	614	405	SI	sat
M3a	n	CM	0.785	0.000	0.463	463	354	SI	sat
M3b	n	CM	0.785	0.000	0.463	463	354	SI	sat
M4a	p	CA	1.200	0.614	1.015	401	121	MI	sat
M4b	p	CA	1.200	0.614	1.015	401	121	MI	sat
M5a	n	CA	1.000	0.463	0.785	323	120	MI	sat
M5b	n	CA	1.000	0.463	0.785	323	120	MI	sat
M7a	n	CM	0.813	0.000	0.813	813	374	SI	sat
M7b	n	CM	0.813	0.000	0.391	391	374	SI	sat

From Table 5.2, we see that all transistors have a sufficiently large V_{DS} voltage and are therefore biased in saturation. Additionnally we see that all the saturation voltages in the output current branch M_{2d}, M_4, M_7 and M_{3b} are summing up to 1000 mV leaving an output voltage swing about equal to $V_{out,swing} \cong 800\ mV$. This output voltage swing could be increased by about 250 mV by biasing M_{2d} and M_{3b} in weak inversion. This would be at the cost of larger transistors and a less current matching in the current mirrors.

From Table 5.5, we see that all transistors are biased in saturation. The operating points look fine. We can now proceed with the simulation of the open-loop large-signal transfer characteristic.

5.2 Large-signal differential transfer characteristic

We now simulate the DC differential transfer characteristic. The simulation of the large-signal input-output characteristic is presented in Figure 5.1.

From Figure 5.1, we see that the output swing is about $V_{out,swing} = 400\ mV$, which is even smaller than the above estimation. We can now zoom into the high gain region in order to extract the offset voltage that is needed to bring the output voltage back to $V_{outq} = 0.900\ V$. The simulation results are presented in Figure 5.2.

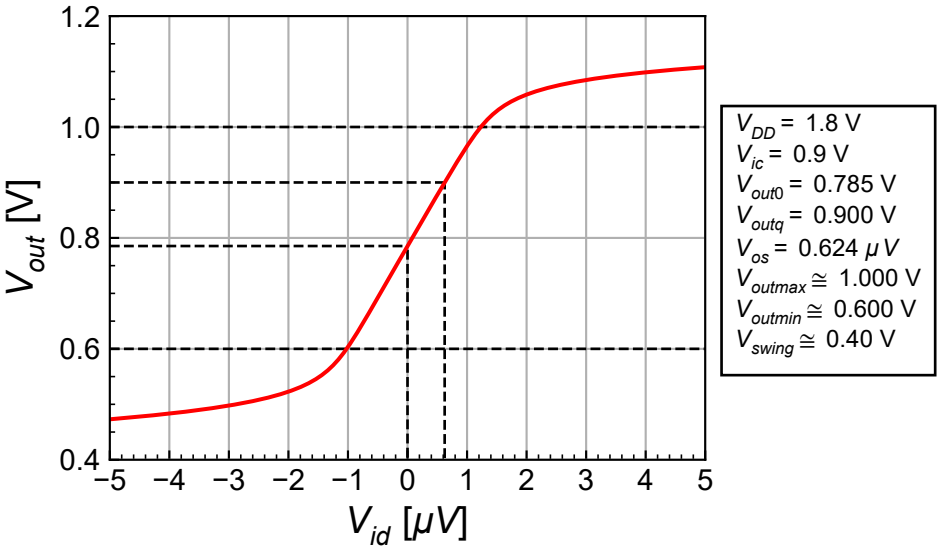

Figure 5.1: Simulated large-signal input-output characteristic.

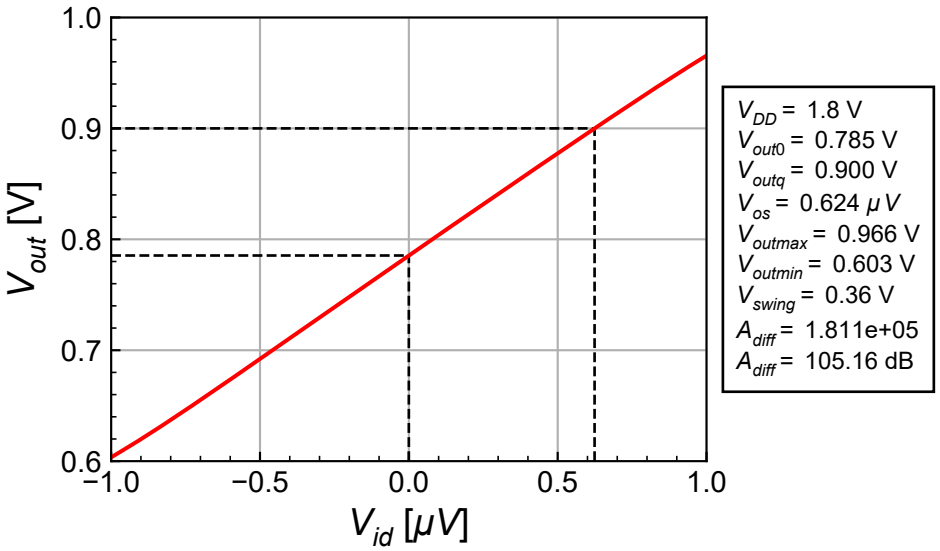

Figure 5.2: Zoom of the simulated large-signal input-output characteristic in the gain region.

We can now save the extracted offset voltage $V_{os} = 0.624\ \mu V$ that is required to bring the output voltage to $V_{outq} = 0.900\ V$ and that will be used for the following .AC and .NOISE simulations.

5.3 Open-loop gain

After having checked the operating point information and making sure that the OTA output is not saturated by extracting the required offset voltage for bringing the output operating point to the desired value $V_{outq} = 0.900\ V$, we can now perform the AC simulation.

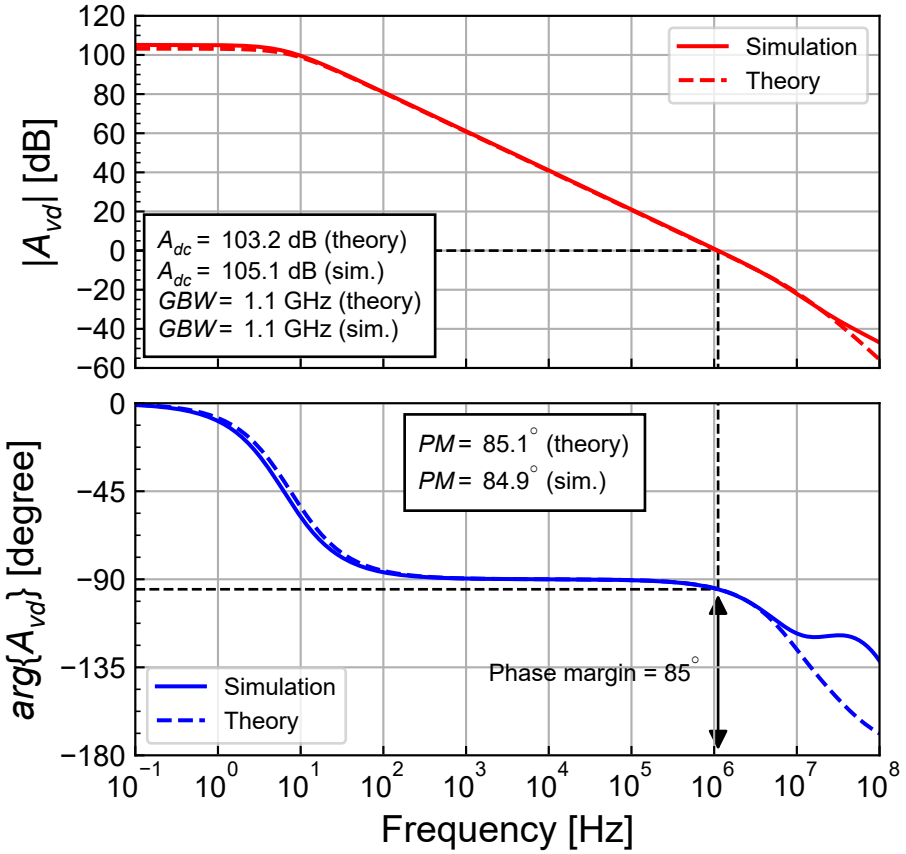

Figure 5.3: Simulated gain response compared to theoretical estimation.

From Figure 5.3, we see that the simulated transfer function is very close to the theoretical estimation below the GBW. The simulated gain-bandwidth product $GBW = 1.116\ MHz$ is equal to the theoretical estimation $1.084\ MHz$ and slightly above target $1.000\ MHz$. The simulated DC gain $A_{dc} = 105.131\ dB$ is slightly higher than the estimated DC gain $103.201\ dB$ and higher than the specifications $100\ dB$, offering some margin. Notice that he DC gain obtained from the AC simulation is consistent with the value extracted above from the DC transfer characteristic.

We now will have a look at the input-referred noise power spectral density (PSD).

5.4 Input-referred noise

The simulated input-referred noise PSD is presented in Figure 5.4 and compared to the theoretical estimation.

From Figure 5.4, we see a perfect match between simulation and theoretical estimation for both the flicker and the white noise except above the GBW where the simulated noise PSD becomes larger than

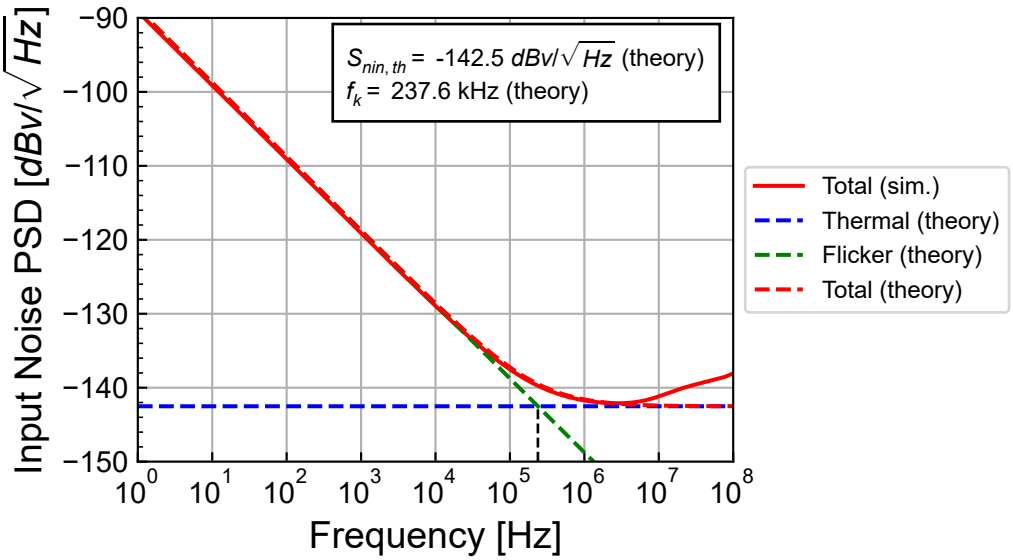

Figure 5.4: Simulated input-referred noise PSD compared to theoretical estimation.

the theoretical estimation. This is simply due to the fact that the theoretical input-referred noise PSD has been obtain by dividing the output current noise by the square of the equivalent trnasconductance without accouting for the frequency dependence occuring above the GBW.

The individual contributions of the various transistors to the input-referred white noise PSD are detailed in Figure 5.5 and compared to the theoretical white noise.

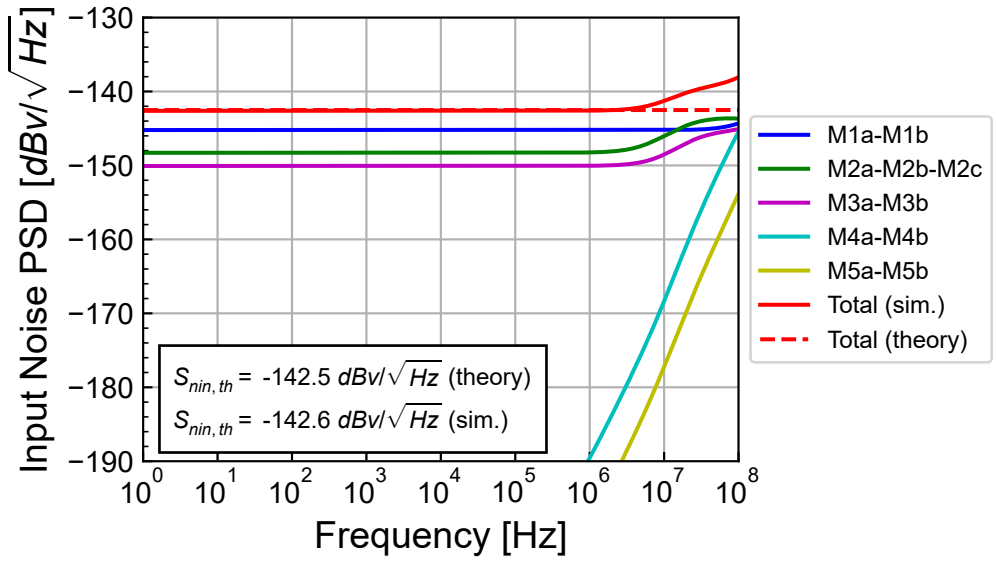

Figure 5.5: Breakdown of the contributions to the simulated input-referred white noise PSD.

From Figure 5.5, we can observe a perfect match of the total input-referred white noise PSD between simulation and the theoretical estimation below the GBW. The white noise is dominated by the differential pair M_{1a}-M_{1b} which is $1+\eta_{th} = 1.819$ times (or 2.598 dB) lower than the total white noise. The contribution of M_{2a}-M_{2b}-M_{2c} is about 2.031 times (or 3.078 dB) lower than the contribution of M_{1a}-M_{1b}. Note that it is mostly M_{2b}-M_{2c} that contribute since the contribution of M_{2a} is a common mode signal that is cancelled at the output if we assume perfect matching. The contribution of M_{3a}-M_{3b} is about 3.062 times (or 4.860 dB) lower than the contribution of M_{1a}-M_{1b}. Finally, the contributions of the cascode transistors M_4 and M_5 are completely negligible. (56.128 dB lower for M_4 and 76.521 dB lower for M_5). This confirms that the noise of the cascode transistors M_4 and M_5 can be totally

neglected in the above analysis.

The simulated value of $\eta_{th} = 0.819$ is close to the theoretical estimation $\eta_{th} = 0.805$. Finally, the simulated OTA thermal noise excess factor $\gamma_{n,ota} = 2.349$ is about equal to the predicted value $\gamma_{n,ota} = 2.359$.

Figure 5.6 presents the breakdown of the contributions of the various transistors to the input-referred flicker noise.

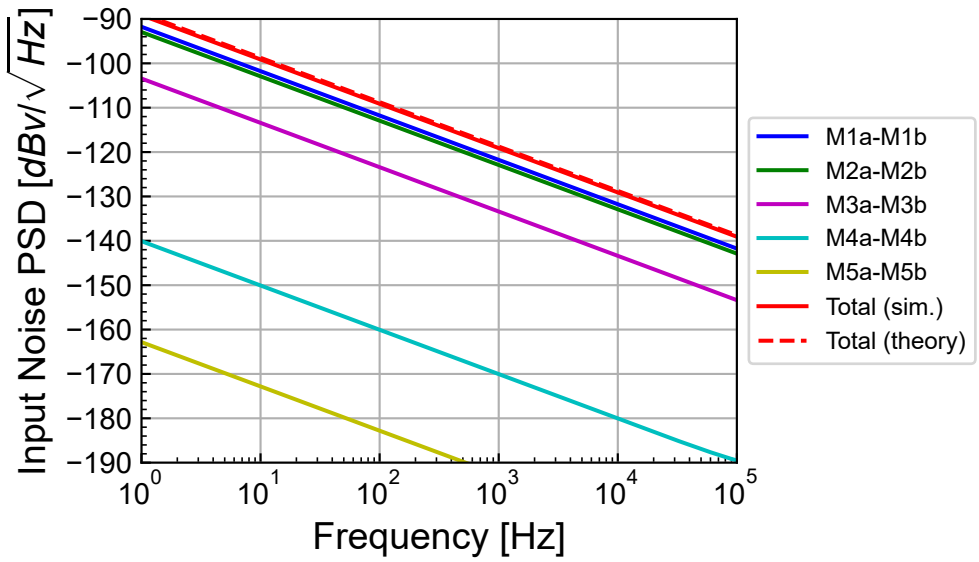

Figure 5.6: Breakdown of the contributions to the simulated input-referred flicker noise PSD.

Similarly to the white noise, Figure 5.6 shows that the total simulated input-referred flicker noise PSD perfectly matches the theoretical prediction. We can observe M_{2a}-M_{2b}-M_{2c} have a slightly less contribution than M_{1a}-M_{1b}. This is confirmed by the value of $\eta_{fl} = 0.830$ (-0.812 in dB) which is is slightly lower than the theoretical value $\eta_{fl} = 0.999$. The contribution of M3a-M3b is 11.666 dB lower than the contribution of M1a-M1b. Finally, the contributions of the cascode transistors M_{4a}-M_{4b} and M_{5a}-M_{5b} are completely negligible.

The contributions of the various transistors to the total input-referred noise PSD is shown in Figure 5.7.

5.5 Input common-mode voltage range

We can check the input common-mode voltage range by connecting the OTA as a voltage follower and sweeping the positive input.

As shown in Figure 5.8, the output follows the input voltage from 0.34 V up to 1.50 V. So the input common-mode voltage range is about 1.16 V.

5.6 Step-response

In this section we will check the step response of the OTA operating as a voltage follower as shown in Figure 5.9 with its output connected to the negative input and with the same load capacitance $C_L = 1$ pF.

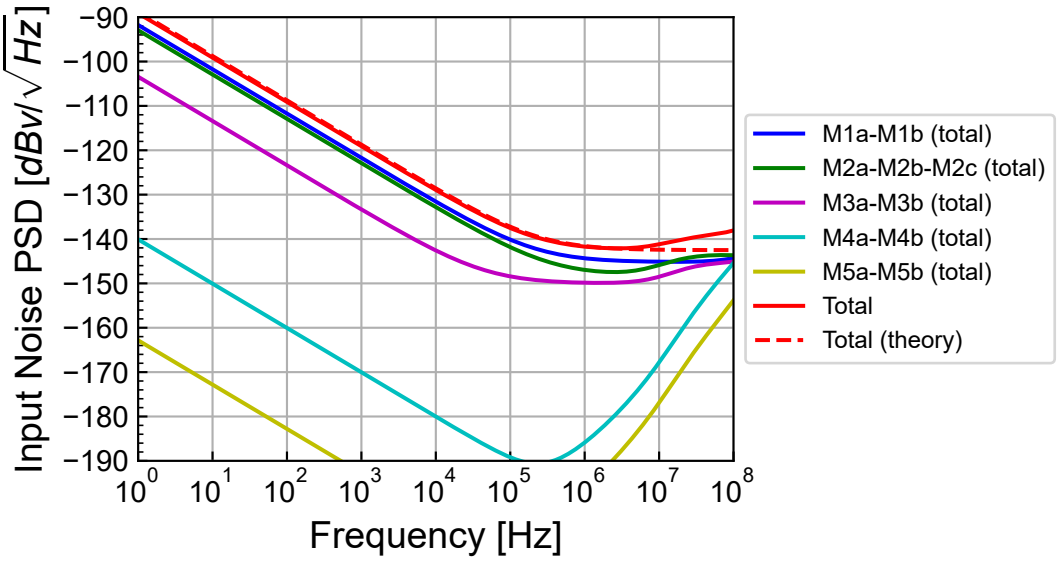

Figure 5.7: Breakdown of the contributions to the simulated input-referred noise PSD.

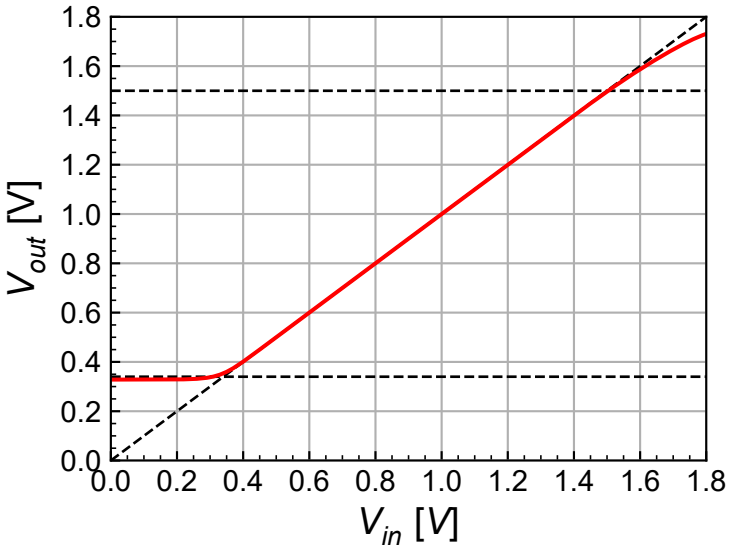

Figure 5.8: Simulated input common-mode voltage range.

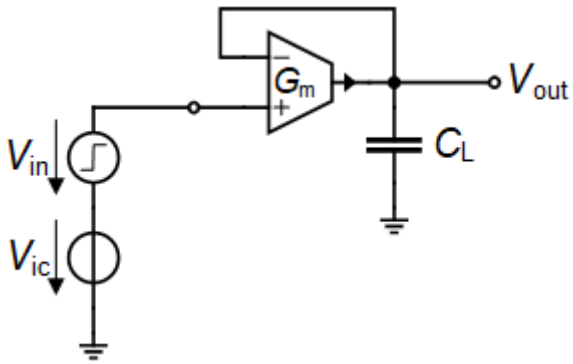

Figure 5.9: Schematic of the OTA connected as a voltage follower.

5.6.1 Small-step

According to the input common-mode voltage range established above, we will set the input common-mode voltage to $V_{ic} = 0.900\ V$ to make sure that the OTA is in the high gain region. We start by imposing a small step $\Delta V_{in} = 10\ mV$ on top of a common mode voltage $V_{ic} = 0.900\ V$. The simulation results are shown in Figure 5.10 where $\Delta V_{in}(t) \triangleq V_{in+}(t) - V_{ic}$ and $\Delta V_{out}(t) \triangleq V_{out}(t) - V_{outq}$ with $V_{outq} \cong V_{ic}$ is the quiescent output voltage. ΔV_{in} and ΔV_{out} are compared to the response of a single pole circuit having a cut-off frequency equal to the GBW. From Figure 5.10, we see that the simulation result is very close to the first-order response.

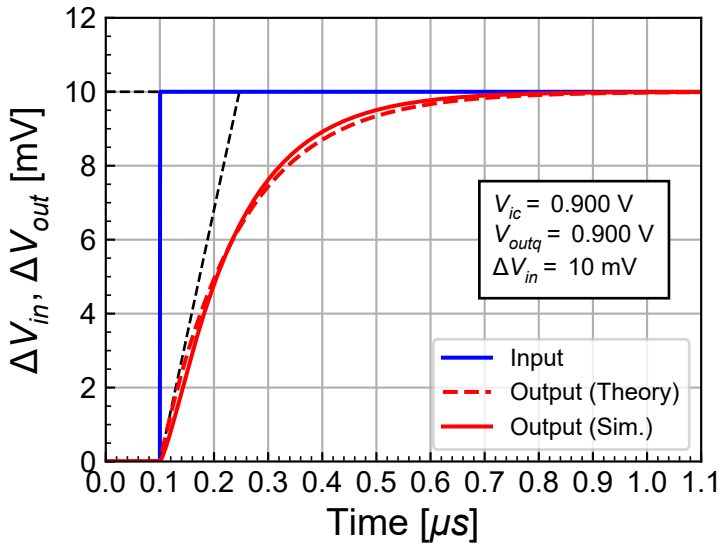

Figure 5.10: Step response of the OTA connected as a voltage follower for a small input step.

5.6.2 Large step

The simulation results for a larger step $\Delta V_{in} = 300\ mV$ are shown in Figure 5.11 where $\Delta V_{in}(t) \triangleq V_{in+}(t) - V_{ic}$ and $\Delta V_{out}(t) \triangleq V_{out}(t) - V_{outq}$ with $V_{outq} \cong V_{ic}$ is the quiescent output voltage. ΔV_{in} and ΔV_{out} are compared to the response of a single pole circuit having a cut-off frequency equal to the GBW. We now observe the effect of slew-rate which increases the settling time.

5.7 Current and power consumption

The total current consumption, ignoring the current drawn by M_{2a} and M_{7a}, is $I_{tot} = 2I_{b2} = 1.1\ \mu A$ and the power consumption is $P = 1.980\ \mu W$.

Assuming the input differential pait M_{1a}-M_{1b} is biased in deep weak inversion, the minimum bias current $I_{b1,min}$ is directly related to the gain-bandwidth product GBW according to

$$I_{b1,min} \cong nU_T \cdot C_L \cdot \omega_u = nU_T \cdot C_L \cdot 2\pi\, GBW, \tag{5.1}$$

which is equal to 207 nA. The minimum total current consumption assuming $\alpha \triangleq I_{b3}/I_{b1} = 1.2$ can then be estimated as $I_{tot,min} \cong 2I_{b2,min} = 2(I_{b1,min} + I_{b3,min}) = 2I_{b1,min}\,(1+\alpha) = 909\ nA$. The actual current consumption accounting for some margin taken on the GBW is therefore 21% higher than the minimum.

The current consumption of the folded cascode OTA is 2.2 times larger than that of the telescopic OTA for the same specifications.

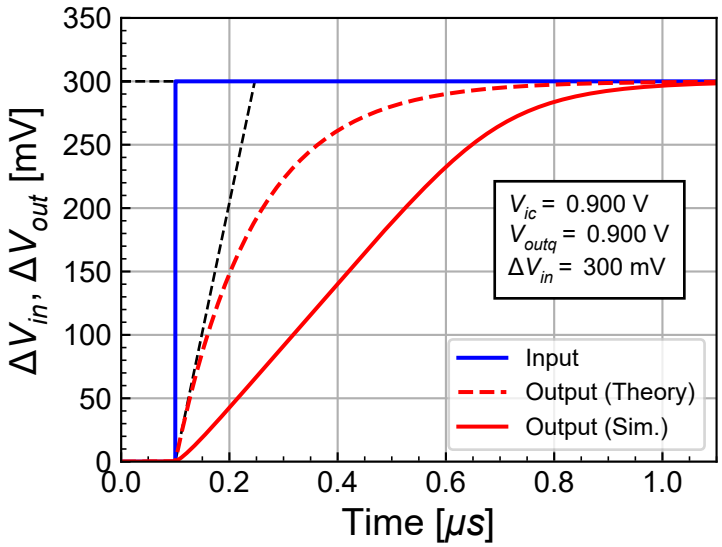

Figure 5.11: Step response of the OTA connected as a voltage follower for a large input step highlighting the slew-rate effect.

> **Note**
>
> Note that the telescopic OTA is the differential OTA that has the minimum power consumption for similar gain-bandwidth product, DC gain and phase margin specifications. Of course it has the smallest input and output voltage swings.

6 Conclusion

This notebook presented the analysis, design and verification of the folded-cascode OTA [1] designed for a generic 180nm bulk CMOS process. The detailed analysis provided all the equations that were then used in the design phase to reach the target specifications. The design was then performed using the inversion coefficient approach with the sEKV transistor model [11] [14] [15]. The theoretical performance resulting from the design were then evaluated.

The design was then verified by simulation using ngspice [2] with the EKV 2.6 compact model [4] and the parameters of a generic 180 nm bulk CMOS process. After carefully checking the operating point, the large-signal transfer characteristic was simulated. The small-signal open-loop transfer function was then simulated making sure the OTA was biased in the high gain region. The simulated transfer function was very close to the theoretical prediction except for the DC gain which is slightly smaller but still in spec. The simulations have also shown that the gain-bandwidth product GBW and the DC gain specifications are both achieved.

The input-referred noise was then simulated. The total simulated input-referred noise PSD perfectly matches the theoretical estimation for both the white noise and the flicker noise. The contributions of the various transistors to the input-referred white noise were then extracted from the noise simulation and compared to the theoretical estimation. It was shown that the total white noise is very close to the theoretical estimation. The simulation of the input-referred flicker noise have shown that it is dominated by the input differential pair M_{1a}-M_{1b} and the current sources M_{2b}-M_{2c}. Finally, the simulations have confirmed that the noise contributions of the cascode transistors are completely negligible.

The input common-mode voltage range was then simulated with the OTA connected as a voltage follower. The common-mode input voltage is ranging from 0.34 V to 1.50 V.

Finally, the small-signal step response was simulated and succesfully compared to the response of a single-pole system. The step-response with a large input step highlighted the effect of slew-rate.

The folded cascode OTA is easier to design than the tlescopic OTA, because of the relaxed voltage constraints. It can reach higher DC gain and output voltage swing at the cost of more noise.

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