Design of the Miller OTA

For a Generic 180nm Bulk CMOS Process (Version 2)

Christian Enz (christian.enz@epfl.ch)

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1 Introduction

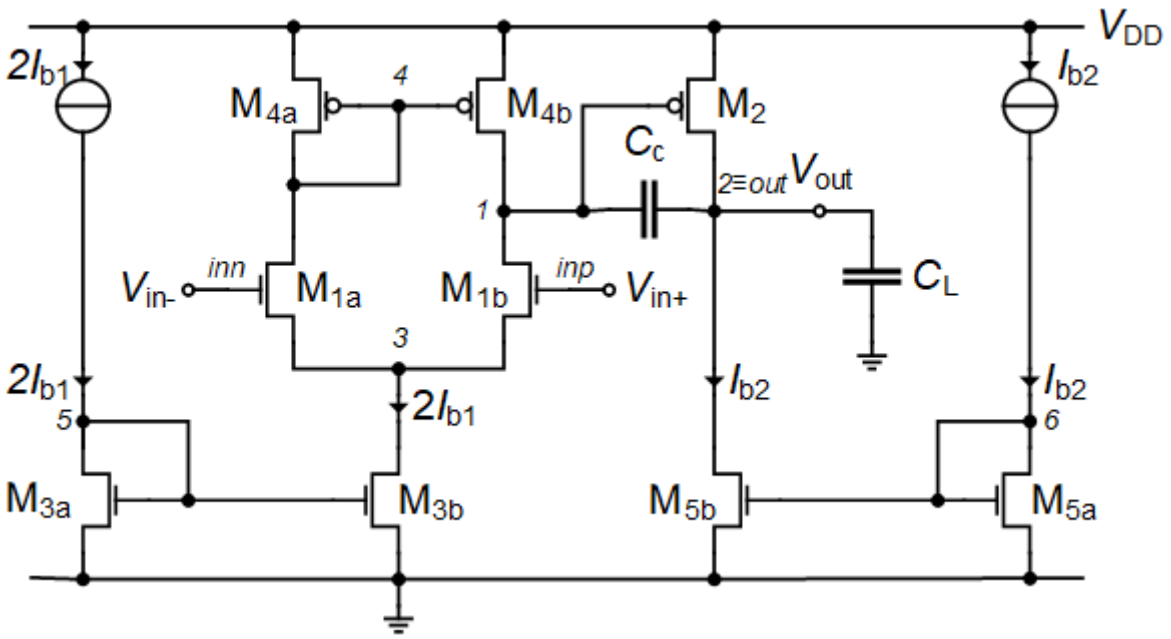

Figure 1.1: Schematic of the Miller OTA.

> **Note**
>
> Note that all nMOS transistors in Figure 1.1 have an odd number and all the pMOS transistors an even number which explains the numbering process.

This notebook presents the analysis, design and simulation of the Miller OTA which schematic is presented in Figure 1.1. The design phase is using the sEKV model and the inversion coefficient approach [1], [2], [3]. The Miller OTA is a two-stage OTA which requires frequency compensation to ensure that it will remain stable in all feedback configurations. The compensation is achieved by adding capacitor C_c which takes advantage of the Miller effect hence its name of Miller compensation or Miller OTA. We will see below that in differential mode the effects of the source transconductances on the common source node voltage are actually canceled.

We will start with a detailed analysis of the OTA which will allow to derive all the design equations that will be used in the design phase. The OTA is then designed for a given set of specifications for a generic 180 nm bulk CMOS technology. The design is then validated by simulations with ngspice [4] using the EKV 2.6 compact model [5] [6] [7] with parameters corresponding to a generic 180 nm bulk CMOS technology [8] [9].

We now start with the small-signal analysis.

2 Analysis

2.1 Small-signal analysis

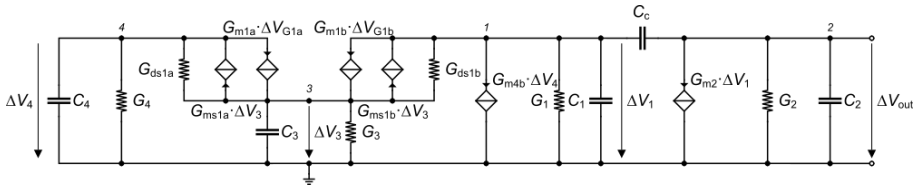

Figure 2.1: Small-signal schematic of the Miller OTA.

> **Note**
>
> This small-signal analysis and the frequency compensation analysis is largely based on [10].

We start with the small-signal analysis. The small-signal schematic corresponding to the Miller OTA is shown in Figure 2.1. Assuming perfect matching and differential operation $\Delta V_{Gb1} = -\Delta V_{Ga1} = V_{id}/2$, the voltage at the source of M_{1a}-M_{1b} (node 3) remains unchanged and hence $\Delta V_3 = 0$. The source transconductances can then be omitted leading to the simplified small-signal circuit in differential mode shown in Figure 2.2.

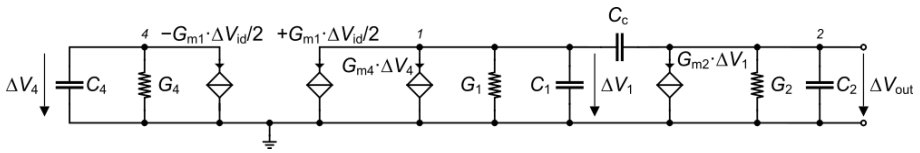

Figure 2.2: Small-signal schematic of the Miller OTA in differential mode.

If the capacitance C_4 at the current mirror node 4 is neglected and recalling that $G_4 = G_{m4} + G_{ds4} \cong G_{m4}$, then $\Delta V_4 = -G_{m1}/G_{m4} \cdot V_{id}/2$. The two transconductances connected to node 1 can then be replaced by a single transconductance resulting in the simplified schematic shown in Figure 2.3.

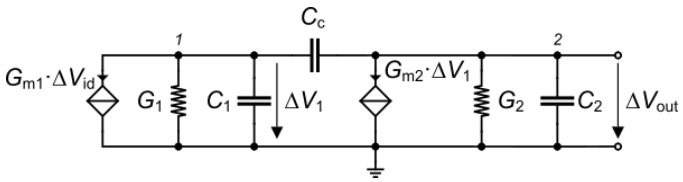

Figure 2.3: Simplified small-signal schematic of the Miller OTA in differential mode.

The small-signal differential gain of the simplified circuit shown in Figure 2.3 is then given by

$$A_{dm} \triangleq \frac{\Delta V_{out}}{\Delta V_{id}} = A_{dc} \cdot \frac{1 - s/z_1}{(1 - s/p_1)(1 - s/p_2)} \tag{2.1}$$

$$= A_{dc} \cdot \frac{1 + n_1\, s}{1 + d_1\, s + d_2\, s^2} = A_{dc} \cdot \frac{1 - \frac{s}{z_1}}{1 - \frac{s}{p_1 + p_2} + \frac{s^2}{p_1\, p_2}} \tag{2.2}$$

with

$$A_{dc} = \frac{G_{m1}}{G_1} \cdot \frac{G_{m2}}{G_2}, \tag{2.3}$$

$$n_1 = -\frac{1}{z_1} = -\frac{C_c}{G_{m2}}, \tag{2.4}$$

$$d_1 = -\left(\frac{1}{p_1} + \frac{1}{p_2}\right) = \frac{C_1}{G_1} + \frac{C_2}{G_2} + \frac{C_c}{G_1}\left(1 + \frac{G_1}{G_2} + \frac{G_{m2}}{G_2}\right), \tag{2.5}$$

$$d_2 = \frac{1}{p_1\, p_2} = \frac{C_c\, C_2 + C_c\, C_1 + C_1\, C_2}{G_1\, G_2}. \tag{2.6}$$

Note that G_{m1}/G_1 and G_{m2}/G_2 are the voltage gains of the first and second stage, respectively. G_1 and G_2 are the total conductances at nodes 1 and 2

$$G_1 = G_{ds1b} + G_{ds4b}, \tag{2.7}$$

$$G_2 = G_{ds2} + G_{ds5b}, \tag{2.8}$$

whereas C_1 and C_2 are the total capacitances at nodes 1 and 2. Note that C_2 is usually dominated by C_L.

If we ignore the compensation capacitor ($C_c = 0$), the zero disappears and the two poles are simply given by

$$p_1' = -\frac{G_1}{C_1}, \tag{2.9}$$

$$p_2' = -\frac{G_2}{C_2}. \tag{2.10}$$

We see that the poles are actually associated to the nodes 1 and 2 (output).

The compensation capacitor introduces a right half-plane (RHP) zero

$$z_1 = \frac{G_{m2}}{C_c} \tag{2.11}$$

and the transfer function A_{dm} has two real poles p_1 and p_2. Assuming that $C_1 \ll C_2$ and that G_1 and G_2 are of the same order of magnitude, the poles can be considered as widely separated $|p_1| \ll |p_2|$ then

$$d_1 \cong -\frac{1}{p_1} = \frac{C_1}{G_1} + \frac{C_2}{G_2} + \frac{C_c}{G_1} \cdot \left(1 + \frac{G_1}{G_2} + \frac{G_{m2}}{G_2}\right). \tag{2.12}$$

We can further assume that $G_{m2}/G_2 \gg 1$ and the dominant pole p_1 is approximately given by

$$p_1 \cong -\frac{G_1\, G_2}{G_{m2}\, C_c}. \tag{2.13}$$

The gain-bandwidth product GBW is then approximately given by

$$GBW = |p_1| \cdot A_{dc} \cong \frac{G_{m1}}{C_c}. \tag{2.14}$$

Contrary to the single-stage OTAs (simple OTA, symmetrical OTA, telescopic OTA), the GBW is no more set by the load capacitance but by the compensation capacitance C_c. Note that $|p_2|$ must be at least equal to GBW for the above approximation to hold

$$GBW < \frac{G_{m2}}{C_2}. \tag{2.15}$$

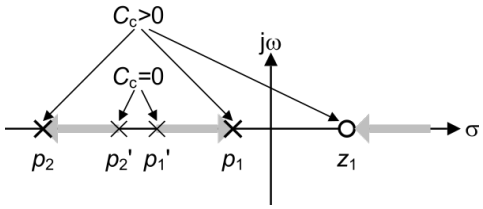

Figure 2.4: The mechanism of pole splitting.

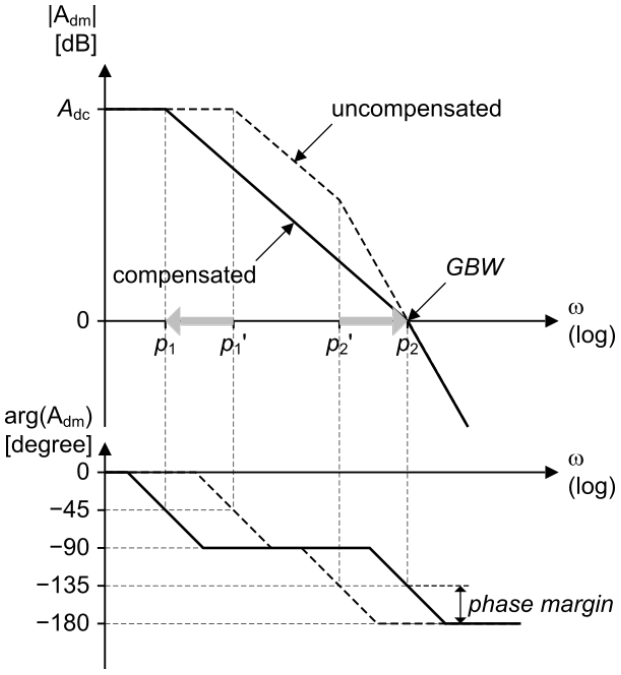

Figure 2.5: The frequency compensation process.

The non-dominant pole p_2 is then approximately given by

$$p_2 \cong \frac{1}{p_1\, d_2} \cong -\frac{G_{m2}C_c}{C_cC_2 + C_cC_1 + C_1C_2}. \tag{2.16}$$

We see that the dominant pole magnitude $|p_1|$ decreases as C_c increases, whereas $|p_2|$ increases as C_c increases. Thus, increasing C_c causes the poles to split apart as illustrated in Figure 2.4. If C_2 and C_c can be considered much larger than C_1, the non-dominant pole is approximately set by the output capacitance

$$p_2 \cong -\frac{G_{m2}}{C_2}. \tag{2.17}$$

It can be shown that if the zero is ten times higher than the GBW, then in order to achieve a phase margin better than 60°, the second pole must be placed at least 2.2 times higher than the GBW. This translates into the following constraints

$$|z_1| > 10\, GBW \;\Rightarrow\; \frac{G_{m2}}{C_c} > 10\,\frac{G_{m1}}{C_c} \;\Rightarrow\; G_{m2} > 10\, G_{m1}, \tag{2.18}$$

$$\tag{2.19}$$

which results in

$$C_c > 2.2\,\frac{G_{m1}}{G_{m2}}\, C_2 > 0.22\, C_2. \tag{2.20}$$

The dominant-pole is often called a Miller pole because it takes advantage of the Miller effect. The dominant-pole can actually be found by using the Miller approximation. Using the result obtained earlier without the compensation capacitor and replacing C_1 by the Miller capacitance

$$C_M \cong \frac{G_{m2}}{G_2} \cdot C_2 \tag{2.21}$$

results in

$$p_1 \cong -\frac{G_1G_2}{G_{m2}\, C_c} \tag{2.22}$$

which is identical to the result found above. However, the Miller approximation does account for the RHP zero. The latter introduces very undesirable effects with regards to stability: it increases the phase shift and at the same time increases the magnitude. The effects of the RHP zero can be mitigated by different means [10].

2.2 Noise analysis

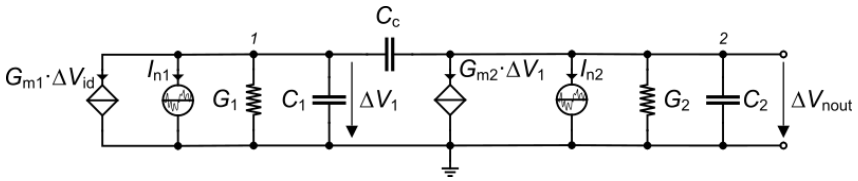

Figure 2.6: Small-signal schematic for noise analysis.

The small-signal schematic for the noise analysis is shown in Figure 2.6. We can reuse the noise analysis performed for the simple OTA. If we neglect the capacitances at the 1st-stage current mirror node and assume a perfect matching, the noise coming from the first stage can be modeled by the noisy current source I_{n1} due to transistors M_{1a}-M_{1b} and M_{3a}-M_{3b}, whereas I_{n2} models the noise coming from transistors M_2 and M_{5b}. The input-referred equivalent noise voltage is then given by

$$V_{neq} = \frac{I_{n1}}{G_{m1}} - \frac{G_1}{G_{m1}\, G_{m2}} \cdot \frac{1 + s\,(C_1 + C_c)/G_1}{1 - s\, C_c/G_{m2}} \cdot I_{n2}. \tag{2.23}$$

For $\omega \ll G_1/(C_1 + C_c) < G_{m2}/C_c$, V_{neq} can be approximated by

$$V_{neq} \cong \frac{I_{n1}}{G_{m1}} - \frac{G_1}{G_{m1}\, G_{m2}} \cdot I_{n2}. \tag{2.24}$$

The input-referred PSD is then given by

$$S_{V_{neq}} \cong \frac{S_{I_{n1}}}{G_{m1}^2} + \left(\frac{G_1}{G_{m1}\, G_{m2}}\right)^2 \cdot S_{I_{n2}}. \tag{2.25}$$

2.2.1 Input-referred thermal noise

For thermal noise we have

$$S_{I_{n1}} = 4kT \cdot 2 \cdot (\gamma_{n1} \cdot G_{m1} + \gamma_{n4} \cdot G_{m4}), \tag{2.26}$$
$$S_{I_{n2}} = 4kT \cdot (\gamma_{n2} \cdot G_{m2} + 2\gamma_{n5} \cdot G_{m5}). \tag{2.27}$$

The input-referred thermal noise resistance $R_{nin,th}$ is then given by

$$R_{nin,th} = \frac{2\gamma_{n1}}{G_{m1}} \cdot (1 + \eta_{th}) \tag{2.28}$$

where

$$\eta_{th} = \frac{\gamma_{n4}}{\gamma_{n1}} \frac{G_{m4}}{G_{m1}} + \frac{G_1^2}{2G_{m1}\, G_{m2}} \cdot \left(\frac{\gamma_{n2}}{\gamma_{n1}} + \frac{2\gamma_{n5}}{\gamma_{n1}} \cdot \frac{G_{m5}}{G_{m2}}\right) \tag{2.29}$$

is the contribution of the current mirror M_{4a}-M_{4b}, 2nd-stage M_2 and current mirror M_{5a}-M_{5b} relative to that of the differential pair M_{1a}-M_{1b}.

The input-referred thermal noise resistance $R_{nin,th}$ can also be written as

$$R_{nin,th} = \frac{\gamma_{neq}}{G_{m1}} \tag{2.30}$$

where γ_{neq} is the amplifier equivalent thermal noise excess factor given by

$$\gamma_{neq} = 2\,\gamma_{n1}\,(1 + \eta_{th}) = 2\,\gamma_{n1}\left[1 + \frac{\gamma_{n4}}{\gamma_{n1}} \frac{G_{m4}}{G_{m1}} + \frac{G_1^2}{2G_{m1}\, G_{m2}} \cdot \left(\frac{\gamma_{n2}}{\gamma_{n1}} + \frac{2\gamma_{n5}}{\gamma_{n1}} \cdot \frac{G_{m5}}{G_{m2}}\right)\right]. \tag{2.31}$$

We see that the contribution of the current mirror M_{4a}-M_{4b} can be minimized by choosing $G_{m1} \gg G_{m4}$ (same as for the simple OTA). The contribution of M_2 and M_{5a}-M_{5b} are small thanks to the term

$$\frac{G_1^2}{2G_{m1}\, G_{m2}} = \frac{(G_{ds1} + G_{ds4})^2}{2G_{m1}\, G_{m2}} \gg 1 \tag{2.32}$$

which is in the order of the DC gain. The contribution of the current mirror M_{5a}-M_{5b} can be made negligible by choosing $G_{m2} \gg G_{m5}$.

2.2.2 Input-referred flicker noise

For flicker noise we have

$$S_{I_{n1}} = \frac{4kT}{f} \cdot 2 \cdot \left(G_{m1}^2 \frac{\rho_n}{W_1 L_1} + G_{m4}^2 \frac{\rho_p}{W_4 L_4}\right), \tag{2.33}$$
$$S_{I_{n2}} = \frac{4kT}{f} \cdot \left(G_{m2}^2 \frac{\rho_p}{W_2 L_2} + 2G_{m5}^2 \frac{\rho_n}{W_5 L_5}\right). \tag{2.34}$$

The input-referred flicker noise resistance is then given by

$$f \cdot R_{nin,fl} = 2\left[\frac{\rho_n}{W_1 L_1} + \left(\frac{G_{m4}}{G_{m1}}\right)^2 \frac{\rho_p}{W_4 L_4}\right] + \left(\frac{G_1}{G_{m1}}\right)^2 \left[\frac{\rho_p}{W_2 L_2} + 2\left(\frac{G_{m5}}{G_{m2}}\right)^2 \frac{\rho_n}{W_5 L_5}\right] \tag{2.35}$$

which can be written in terms of the individual contributions relative to that of the differential pair

$$f \cdot R_{nin,fl} = \frac{2\rho_n}{W_1 L_1} \cdot (1 + \eta_{fl}), \tag{2.36}$$

with

$$\eta_{fl} = \left(\frac{G_{m4}}{G_{m1}}\right)^2 \frac{\rho_p}{\rho_n} \frac{W_1 L_1}{W_4 L_4} + \frac{1}{2}\left(\frac{G_1}{G_{m1}}\right)^2 \left[\frac{\rho_p}{\rho_n} \frac{W_1 L_1}{W_2 L_2} + 2\left(\frac{G_{m5}}{G_{m1}}\right)^2 \frac{W_1 L_1}{W_5 L_5}\right]. \tag{2.37}$$

We see that the contribution of the current mirror M_{4a}-M_{4b} can be minimized by choosing $G_{m1} \gg G_{m4}$ (same as for the simple OTA). The contribution of M_2 and M_{5a}-M_{5b} are small thanks to the first stage gain

$$\left(\frac{G_1}{G_{m1}}\right)^2 = \left(\frac{G_{ds1} + G_{ds4}}{G_{m1}}\right)^2 \gg 1. \tag{2.38}$$

The contribution of the current source M_{5a}-M_{5b} can be made negligible by choosing $G_{m2} \gg G_{m5}$.

2.3 Input-referred offset voltage

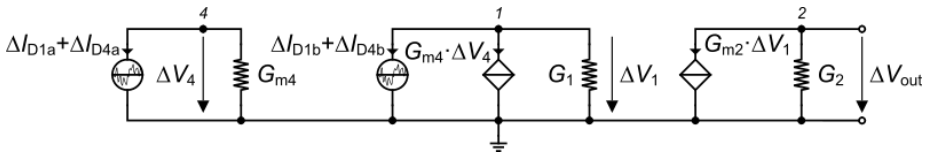

Figure 2.7: Small-signal schematic for mismatch analysis.

The estimation of the offset voltage can be handled similarly to the noise. It is essentially due to the first stage and is therefore similar to what was done for the simple OTA. Using the schematic shown in Figure 2.7, we can derive the input-referred offset voltage variance as

$$\sigma^2_{V_{os}} = \sigma^2_{VT1} + \left(\frac{G_{m4}}{G_{m1}}\right)^2 \cdot \sigma^2_{VT4} + \left(\frac{I_b}{G_{m1}}\right)^2 \cdot \left(\sigma^2_{\beta 1} + \sigma^2_{\beta 4}\right) \tag{2.39}$$

where

$$\sigma^2_{VT1} = \frac{A^2_{VTn}}{W_1 L_1}, \tag{2.40}$$

$$\sigma^2_{VT4} = \frac{A^2_{VTp}}{W_4 L_4}, \tag{2.41}$$

$$\sigma^2_{\beta 1} = \frac{A^2_{\beta n}}{W_1 L_1}, \tag{2.42}$$

$$\sigma^2_{\beta 4} = \frac{A^2_{\beta_p}}{W_4 L_4}. \tag{2.43}$$

We can rewrite the variance of the input-referred offset separating the contributions of the V_T- and β-mismatch

$$\sigma^2_{V_{os}} = \sigma^2_{V_T} + \sigma^2_{\beta} \tag{2.44}$$

where

$$\sigma^2_{V_T} = \sigma^2_{V_{T1}} \cdot (1 + \xi_{V_T}) \tag{2.45}$$

and

$$\sigma_\beta^2 = \left(\frac{I_b}{G_{m1}}\right)^2 \cdot \sigma_{\beta_1}^2 \cdot (1 + \xi_\beta). \tag{2.46}$$

ξ_{V_T} represents the V_T-mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_{V_T} = \left(\frac{G_{m4}}{G_{m1}}\right)^2 \cdot \left(\frac{A_{VTp}}{A_{VTn}}\right)^2 \cdot \frac{W_1 L_1}{W_4 L_4} \tag{2.47}$$

and ξ_β represents the β-mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_\beta = \left(\frac{A_{\beta p}}{A_{\beta n}}\right)^2 \cdot \frac{W_1 L_1}{W_4 L_4}. \tag{2.48}$$

Having done the small-signal, noise and offset analysis, we can now proceed with the design.

3 Design

3.1 Specifications

The OTA specifications are given in Table 3.1.

> **Note**
>
> The specifications given in Table 3.1 are simplified specifications. They are mainly targeting the achievement of a certain gain-bandwidth product GBW and DC gain at lowest current consumption. The GBW sets the differential pair transconductance while the DC gain sets the output conductance. There is an additional specification on the random input-referred offset voltage which, if not met, might eventually require to increase the transistors area. There are no specifications on thermal noise since the transconductance is set by the GBW. There are no specifications on the flicker noise but if the corner frequency was set lower this would required to increase the transistors area. There are also no specifications on the slew-rate, which might be small because of the low-power objective. Finally, there are many more specifications such as CMRR, PSRR, input common-mode voltage range, output-voltage swing, etc... that are not discussed in this example.

Table 3.1: OTA specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	100	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF
Maximum input-referred random offset voltage	V_{os}	10	mV
Phase margin	PM	60	$^\circ$

3.2 Process

We will design the cascode gain stage for a generic 180nm bulk CMOS process. The physical parameters are given in Table 3.2, the global process parameters in Table 3.3 and finally the MOSFET parameters in Table 3.4.

Table 3.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 3.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 3.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	715	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	20	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	8.1e-24	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

3.3 Design procedure

If the DC gain of the second stage G_{m2}/G_2 can be assumed to be much larger than 1, the dominant pole can be approximated by

$$\omega_{p1} = |p_1| \cong \frac{G_1 G_2}{G_{m2} C_c}. \tag{3.1}$$

Since C_1 is a parasitic capacitance, it is reasonable to consider that it is much smaller than the compensation capacitance C_c and the load capacitance C_L. Both assumptions $C_1 \ll C_c$ and $C_1 \ll C_L$ lead to the following approximation of the non-dominant pole

$$\omega_{p2} = |p_2| \cong \frac{G_{m2}}{C_L}. \tag{3.2}$$

In the design procedure we need to make sure that the non-dominant pole ω_{p2} and the RHP zero $\omega_z = G_{m2}/C_c$ are sufficiently larger than the GBW in order to secure enough phase margin. The ratio of the non-dominant pole and the zero to the unity gain frequency are given by

$$\frac{\omega_{p2}}{\omega_u} = \frac{G_{m2}}{G_{m1}} \cdot \frac{C_c}{C_L}, \tag{3.3}$$

$$\frac{\omega_z}{\omega_u} = \frac{G_{m2}}{G_{m1}} \tag{3.4}$$

and hence

$$\frac{\omega_{p2}}{\omega_u} = \frac{\omega_z}{\omega_u} \cdot \frac{C_c}{C_L}, \tag{3.5}$$

$$\frac{\omega_z}{\omega_{p2}} = \frac{C_L}{C_c}. \tag{3.6}$$

The unity gain frequency ω_u, non-dominant pole ω_{p2} and zero ω_z need to satisfy

$$\omega_u < \omega_{p2} < \omega_z, \tag{3.7}$$

or

$$1 < \frac{\omega_{p2}}{\omega_u} < \frac{\omega_z}{\omega_u}. \tag{3.8}$$

This translates to the following inequality

$$1 < \frac{C_L}{C_c} < \frac{G_{m2}}{G_{m1}}. \tag{3.9}$$

This means that the compensation capacitance C_c should stay smaller than the load capacitance C_L and that the ratio of the transconductance of M_2 to that of M_1 should be larger than C_L/C_c.

Usually the compensation capacitance C_c is a fraction of the load capacitance C_L which can be determined from the specified phase margin PM which is given by

$$PM = \arctan\left(\frac{\omega_u}{\omega_z}\right) + \arctan\left(\frac{\omega_u}{\omega_{p2}}\right) - \frac{\pi}{2}. \tag{3.10}$$

For example if $\omega_{p2}/\omega_u = 4$ and $\omega_z/\omega_{p2} = 2$, then $\omega_z/\omega_u = 8$ and $PM = 68.839$ °, which is usually more than sufficient. However we need to account for parasitic capacitances which add to the load capacitance and reduce the non-dominant pole. Therefore a good trade-off to start the design and achieve a sufficient PM (typically larger than 45 degree) is to choose $\omega_{p2} = 4\ \omega_u$, and $\omega_z = 2\ \omega_{p2} = 8\ \omega_u$. This results in choosing

$C_c = \frac{C_L}{\omega_z/\omega_{p2}} = C_L/\ 2 = 0.5$ pF.

It is important to note that choosing $\omega_z/\omega_u = G_{m2}/G_{m1} = 8$ for securing enough phase margin has a direct impact on the power consumption. Indeed, if we assume that both M_{1a}-M_{1b} and M_2 are biased in weak inversion for maximizing the current efficiency, then $G_{m1} = I_{b1}/(n_n\, U_T)$ and $G_{m2} = I_{b2}/(n_p\, U_T)$. Assuming that $n_n = n_p$, $G_{m2}/G_{m1} = I_{b2}/I_{b1} = \omega_z/\omega_u = 8$. This means that the bias current of M_2 is 8 times larger than that of M_{1a}-M_{1b}! The total current consumption, without accounting for the current flowing in M_{3a} and M_{5a}, is then $I_{tot} = 2I_{b1} + I_{b2} = 10\ \ I_{b1}$. We can express the minimum total current consumption in terms of the gain-bandwidth product GBW as $I_{tot} \cong 10\ \ nU_T \cdot C_c \cdot GBW = 5\ nU_T \cdot C_L \cdot GBW$. This can be compared to the total current consumption of the symmetrical cascode OTA $I_{tot} = 4\, nU_T \cdot C_L \cdot GBW$. We deduce that for the same gain-bandwidth product GBW and load capacitance C_L, the Miller OTA consumes about 25% more current than the symmetrical cascode OTA.

3.3.1 Sizing the differential pair M_{1a}-M_{1b}

We can now size the differential pair M_{1a}-M_{1b} knowing that its transconductance is set by the gain-bandwidth product GBW and the compensation capacitance C_c according to $G_{m1} = \omega_u \cdot C_c = 3.142$ $\mu A/V$. The minimum current to achieve this transconductance assuming that M_{1a}-M_{1b} are biased in deep weak inversion is given by $I_{b1,min} = 103$ nA. We know that the differential pair M_{1a}-M_{1b} should be biased in weak inversion in order to minimize the input-referred offset. If we set the inversion coefficient of M_{1a}-M_{1b} to $IC_1 = 0.1$, the required bias current I_{b1} for M_{1a}-M_{1b} to achieve $G_{m1} = 3.142$ $\mu A/V$ with $IC_1 = 0.1$ is then given by $I_{b1} = 113$ nA.

Let's take some margin and set $I_{b1} = 130$ nA. The transconductance can be recalculated from the G_m/I_D function as $G_{m1} = 3.620$ $\mu A/V$. The corresponding GBW is then given by $GBW = 1.2$ MHz, which is slightly higher than the target specification offering some margin. The specific current is then given by $I_{spec1} = 1.3$ μA and the aspect ratio by $W_1/L_1 = 1.8$. The length L_1 will be calculated below from the specifications on the DC gain.

The biasing of M_2 should however be compatible with that of M_{4a}-M_{4b}. The latter should be biased in strong inversion for better matching but also to achieve a transconductance G_{m4} smaller than G_{m1} in order to reduce its noise contribution. So we will first size M_{4a}-M_{4b}.

3.3.2 Sizing the pMOS current mirror M_{4a}-M_{4b}

The maximum gate voltage of M_{4a} is set by the maximum common mode input voltage still keeping M_{1a} in saturation according to

$$V_{SG4} = V_{DD} - V_{icmax} + V_{GS1} - V_{DSsat1}. \tag{3.11}$$

The gate-to-source voltage V_{GS1} is given by

$$V_{GS1} = V_{T0n} + (n_{0n} - 1)\, V_{S1} + n_{0n}\, U_T\, (v_p - v_s). \tag{3.12}$$

Unfortunately, at this point we don't know the value of the source voltage V_{S1} of M_{1a}-M_{1b} (voltage at common-source node 1). In weak inversion $v_p - v_s \cong 0$ so that

$$V_{GS1} \cong V_{T0n} + (n_{0n} - 1)\, V_{S1} \tag{3.13}$$

For a common-mode input voltage V_{ic} set at $V_{DD}/2 = 0.9$, we estimate V_{S1} to be about $V_{S1} = 400$ mV. This gives $V_{GS1} \cong 564$ mV. The saturation voltage V_{DSsat1} of M_{1a}-M_{1b} is given by $V_{DSsat1} = 105$ mV.

For a maximum input common-mode voltage given by $V_{ic,max} = 1.45$ V, the maximum source-to-gate voltage of M_{4a}-M_{4b} V_{SG4} is equal to $V_{SG4} = 809$ mV, which corresponds to an inversion coefficient $IC_4 = 25.935$ and a saturation voltage $V_{DSsat4} = 370$ mV. The specific current is equal to $I_{spec4} = 5.01$ nA, the aspect ratio to $W_4/L_4 = 0.029$ and the transconductance to $G_{m4} = 0.685$ $\mu A/V$.

We will use the specification on the DC gain to set the length of the various transistors. The DC gain is given by $A_{dc} = A_{dc1} \cdot A_{dc2} = 1e{+}05$, where A_{dc1} and A_{dc2} are the DC gains of the first and second stage, respectively. We can distribute the DC gain equally among the first and second stage so that $A_{dc1} = A_{dc2} = 316.2$.

The conductance G_1 at node 1 is then given by $G_1 = 11.448$ nA/V. G_1 depends on the output conductances of M_{1b} and M_{4b} according to $G_1 = G_{ds1b} + G_{ds4b}$. We can split it half-half between M_{1b} and M_{4b}, which leads to the length of M_{1b} $L_1 = 1.14$ μm, from which we get the width $W_1 = 2.07$ μm.

Similarly for M_4 we get the length from the output conductance G_{ds4} as $L_4 = 1.14$ μm, from which we get the width $W_4 = 30.00$ nm, which is smaller than the minimum width $W_{min} = 200$ nm.

We then set W_4 to the minimum width $W_4 = W_{min} = 200\ nm$ and get the length $L_4 = 6.91\ \mu m$.

We can estimate the relative contribution of M_{4a}-M_{4b} to the input-referred flicker noise PSD from

$$\eta_{fl}|_{M_{4a}\text{-}M_{4b}} = \left(\frac{G_{m4}}{G_{m1}}\right)^2 \frac{\rho_p}{\rho_n} \frac{W_1 L_1}{W_4 L_4}. \tag{3.14}$$

which is equal to 0.509. This means that the contribution of M_{4a}-M_{4b} to the input-referred flicker is about 0.509 that of M_{1a}-M_{1b}. This is reasonable accounting for the large $\rho_p/\rho_n = 8.333$ factor.

3.3.3 Sizing the second-stage M_2

We now set G_{m2} to 8 times the recalculated value of G_{m1} resulting in $G_{m2} = 28.961\ \mu A/V$. To size M_2, we first calculate the second stage voltage gain $A_{dc2} = 316.2$.

The sizing of M_2 is tricky. Indeed, ideally, for low-power we would choose to bias M_2 in weak inversion for a maximum current efficiency. This will set the bulk-to-gate voltage of M_2 to about V_{T0p}. On the other hand the quiescent voltage at node 1 (gate of M_2) is equal to that of node 4 which is equal to V_{SG4}. Having chosen to bias M_{4a}-M_{4b} in strong inversion results in V_{SG4} to be larger than V_{T0p} by the overdrive voltage of M_{4a}-M_{4b}, $V_{SG4} - V_{T0p}$. Therefore the bulk-to-gate voltage of M_2 is actually larger than V_{T0p} and since M_2 is biased in weak inversion, the current that M_2 would need to carry is much larger than the current imposed by the current source M_{5b}. The only degree of freedom left is the source-to-drain voltage of M_2 which becomes very small to reduce the current to the level of the bias current imposed by M_{5b}. M_2 is therefore biased in the linear region with a source-to-drain voltage close to zero. That means that the output voltage will saturate to V_{DD}. In order to bring the output voltage back into the high gain region (for example equal to the input common-mode voltage), a differential input voltage needs to be applied which actually corresponds to a systematic offset which can be quite large. If the OTA is used in a closed-loop configuration, which is usually the case, this offset voltage should not be a problem.

A more important consequence of biasing M_2 in weak inversion is that this results in a very large transistor increasing the parasitic capacitance at node 1 and therefore reducing the non-dominant pole and hence the phase margin. Increasing the inversion coefficient IC_2 keeping the same transconductance G_{m2} and DC gain $A_{dc2} = G_{m2}/G_2$ (or keeping the same conductance G_2), reduces the gate area of M_2 at the cost of less current efficiency.

To find what is the optimum inversion coefficient for M_2 that minimizes the parasitic capacitance at node 1 and secures enough phase margin, we can plot its area $W_2\,L_2$ versus IC_2 for a given value of G_{m2} and of the second stage gain A_{dc2} which is presented in Figure 3.1.

From Figure 3.1, we observe that there is an optimum value of IC_2 for which the area of M_2 and hence its related parasitic capacitance are minimum. This optimum IC is in the moderate inversion. Let's now set IC_2 to this optimum value $IC_2 = IC_{2,min} = 2.1$. The current can be derived from G_{m2} and the G_m/I_D ratio as $I_{b2} = 1.986\ \mu A$, which is about twice the minimum value we would get if M_2 is biased in weak inversion $I_{b2}/I_{b2,min} = 2.0$.

We round I_{b2} to $2.0\ \mu A$. We can now recompute G_{m2} as $G_{m2} = 29.162\ \mu A/V$ and derive the specific current $I_{spec2} = 957.26\ nA$ and aspect ratio $W_2/L_2 = 5.529$. The conductance G_2 at the output node is then given by $G_2 = 92.2\ nA/V$, which we split equally among M_2 and M_{5b} leading to $L_2 = 2.17\ \mu m$, from which we get the width $W_2 = 12.00\ \mu m$. M_2 is now fully sized.

3.3.4 Sizing the nMOS current mirrors M_{5a}-M_{5b}

Similarly for M_{5b} we get $L_5 = 2.17\ \mu m$ from the gain of the 2nd stage $A_{dc2} = 316$. To finalize the sizing of M_{5b} we can set its saturation voltage to $V_{DSsat5} = 300\ mV$, which corresponds to an inversion coefficient equal to $IC_5 = 29.6$. Having I_D and IC we get $W_5/L_5 = 9.4\text{e-}02$ and finally its width $W_5 = 210\ nm$.

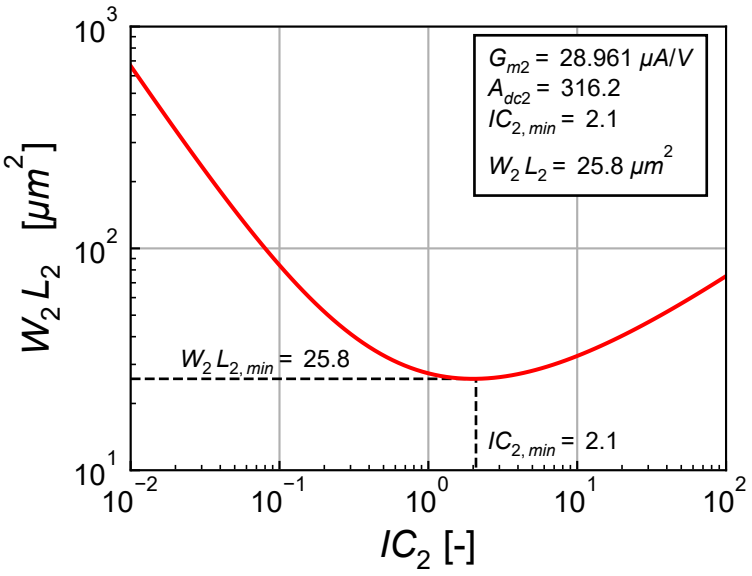

Figure 3.1: Gate area W_2L_2 versus inversion coefficient IC_2 for given G_{m2} and dc gain A_{dc2}.

3.3.5 Sizing the nMOS current mirrors M_{3a}-M_{3b}

Because of the substrate effect, the V_{GS1} voltage of M_{1a}-M_{1b} is rather large $V_{GS1} = 564\ mV$. Therefore the minimum common-mode input voltage is quite limited. On the other hand we want the current mirror M_{3a}-M_{3b} to be biased as far in strong inversion as possible. If we choose $V_{ic,min} = 0.87\ V$, which leads to the saturation voltage of M_{3b} equal to $V_{DSsat3} = V_{ic,min} - V_{GS1} = 306\ mV$. We can derive the corresponding inversion coefficient as $IC_3 = 31.1$. From I_{b1} and IC_3 we can get the specific current $I_{spec3} = 8.37\ nA$ and the aspect ratio $W_3/L_3 = 0.012$. Since W_3/L_3 is very small, we need to set W_3 to the minimum width $W_3 = W_{min} = 200\ nm$ and get the length $L_3 = 17.09\ \mu m$.

The sizing process is now finalized. We will summarize the transistor sizes and bias currents in the next section.

3.4 Summary

3.4.1 Specifications

The specifications are recalled in Table 3.5.

Table 3.5: OTA specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	100	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF
Maximum input-referred random offset voltage	V_{os}	10	mV
Phase margin	PM	60	$^\circ$

3.4.2 Bias

The bias information are summarized in Table 3.6.

Table 3.6: OTA bias.

Bias voltage or current	Symbol	Value	Unit
Supply voltage	V_{DD}	1.8	V
1st-stage bias current	I_{b1}	130.0	nA
2nd-stage bias current	I_{b2}	2.0	μA
Compensation capacitance	C_c	0.5	pF

3.4.3 Transistor information

The transistor sizes and large-signal variables are summarized in Table 3.7, whereas Table 3.8 gives the small-signal and thermal noise parameters. An Excel table is generated with more information (e.g. all the parasitic capacitances).

3.4.4 Transistor information

The transistor sizes and large-signal variables are summarized in Table 3.7, whereas Table 3.8 gives the small-signal and thermal noise parameters. An Excel table is generated with more information (e.g. all the parasitic capacitances).

Table 3.7: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M1a	2.07	1.14	130	1298	0.1	-45	105
M1b	2.07	1.14	130	1298	0.1	-45	105
M2	12.00	2.17	2000	957	2.1	41	128
M3a	0.20	17.09	260	8	31.1	241	306
M3b	0.20	17.09	260	8	31.1	241	306
M4a	0.20	6.91	130	5	25.9	213	283
M4b	0.20	6.91	130	5	25.9	213	283
M5a	0.21	2.17	2000	69	28.9	232	297
M5b	0.21	2.17	2000	69	28.9	232	297

Table 3.8: Transistor small-signal and thermal noise parameters.

Transistor	$G_{spec}\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{ds}\ [nA/V]$	γ_n
M1a	50.176	4.602	3.620	5.702	0.653
M1b	50.176	4.602	3.620	5.702	0.653
M2	37.002	38.088	29.163	46.083	0.763
M3a	0.323	1.648	1.296	0.761	0.813
M3b	0.323	1.648	1.296	0.761	0.813
M4a	0.194	0.894	0.685	0.941	0.832
M4b	0.194	0.894	0.685	0.941	0.832
M5a	2.674	13.102	10.305	46.083	0.812
M5b	2.674	13.102	10.305	46.083	0.812

4 OTA Characteristics

In this section, we check whether the specs are achieved.

4.1 Open-loop gain

We start with cheking the open-loop transfer function. The DC gains of the 1st- and 2nd-stage and the overall gain are estimated and given in Table 4.1. We see that the 1st-stage DC gain is slightly larger than required whereas the 2nd-stage DC gain is right on target. This leads to a DC gain that is sligtly larger than the specifications. This is OK accounting for the fact that the DC gain is strongly depending on the output conductances for which we use a very crude model.

Table 4.1: OTA DC gains.

Symbol	Value	Value in dB	Unit
1st-stage gain A_{dc1}	545.0	54.7	-
2nd-stage gain A_{dc2}	316.4	50.0	-
Overall gain A_{dc}	172433.8	104.7	-

Plotting the open-loop transfer function also requires an estimation of the dominant pole f_{p1}, the non-dominant ploe f_{p2} and the zero f_z. They depend on the estimation of the capacitance C_1 and C_2 at each node 1 and 2. They are given in Table 4.2 and Table 4.3. The resulting poles and zero are then given in Table 4.4.

Table 4.2: Estimation of the parasitic capacitance at node 1 C_1.

Symbol	Theoretical Value	Unit
C_{GS2}	96.6	fF
C_{GB2}	29.8	fF
C_{BD4}	5.1	fF
C_{BD1}	3.6	fF
C_{GD1}	0.8	fF
C_1	135.9	fF

Table 4.3: Estimation of the parasitic capacitance at node 2 C_2.

Symbol	Theoretical Value	Unit
C_{BD2}	36.222	fF
C_{BD5}	1.408	fF
C_L	1.000	pF
C_2	1.038	pF

Table 4.4: Estimation of the poles and zero.

Symbol	Value	Unit	Comment
GBW	1.000	MHz	Specification
$GBW = G_{m1}/C_c$	1.152	MHz	Estimation without effect of zero
GBW	1.097	MHz	Estimation including effect of zero
f_{p1}	6.682	Hz	Dominant pole at node 1
f_{p2}	3.189	MHz	Non-dominant pole at node 2
f_{p2}/GBW	2.768	-	Non-dominant pole ratio
f_z	9.283	MHz	Zero
f_z/GBW	8.057	-	Zero ratio

From Table 4.4, we see that the non-dominant pole f_{p2} is 2.8 times higher than the GBW which should ensure the desired phase margin PM. We can now plot the magnitude and phase of the open-loop gain which is shown in Figure 4.1.

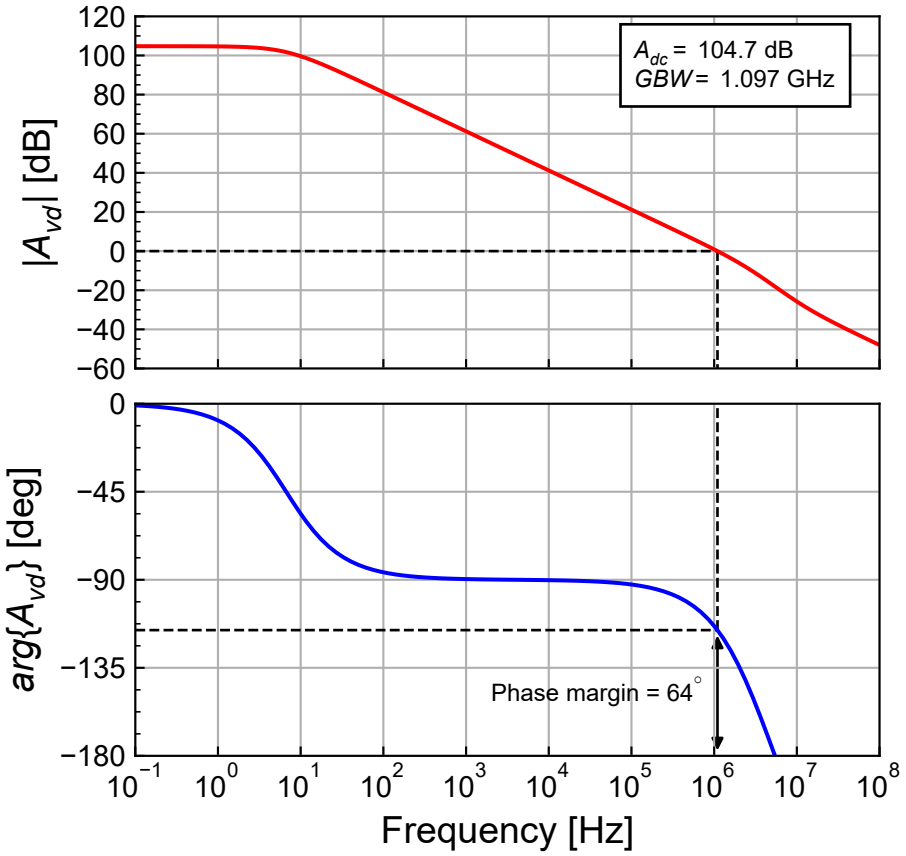

Figure 4.1: OTA theoretical transfer function.

From Figure 4.1, we see that the specifications on the DC gain, gain-bandwidth product and phase margin are all met.

4.2 Input-referred noise

We can also estimate the input-referred noise PSD. We start by evaluating the input-referred themal noise PSD S_{ninth} and resistance R_{nth}. To this purpose we calculate all the parameters that are needed for computing S_{ninth} which are given in Table 4.5.

Table 4.5: OTA thermal noise parameters.

Symbol	Theoretical Value	Unit
G_{m1}	3.620	$\frac{\mu A}{V}$
G_{m2}	29.163	$\frac{\mu A}{V}$
G_{m4}	684.759	$\frac{nA}{V}$
G_{m5}	3.620	$\frac{\mu A}{V}$
G_{m1}/G_{m4}	5.286	-
G_{m2}/G_{m5}	2.830	-
$2G_{m1}G_{m2}/G_1^2$	4785159.095	-
γ_{n1}	0.653	-
γ_{n2}	0.763	-
γ_{n4}	0.832	-
γ_{n5}	0.812	-
η_{th}	0.241	-
$2\gamma_{n1}$	1.307	-
$\gamma_{n,ota}$	1.622	-
R_{nth}	448.016	$k\Omega$
$\sqrt{S_{ninth}}$	86.134	$\frac{nV}{\sqrt{Hz}}$
$10 \cdot \log(S_{ninth})$	-141.296	$\frac{dBv}{\sqrt{Hz}}$

From Table 4.5, we see that M_{4a}-M_{4b}, M_2 and M_{5a}-M_{5b} only contribute 24 % of the total input-referred thermal noise. This leads to an OTA thermal noise excess factor that is only 24 % larger than the minimum 1.3 contributed by the differential pair M_{1a}-M_{1b} only.

We can also calculate all the parameters required to compute the flicker noise. They are given in Table 4.6.

Table 4.6: OTA flicker noise parameters.

Symbol	Theoretical Value	Unit
$(G_{m1}/G_{m4})^2$	27.944	-
$(G_{m1}/G_1)^2$	296971.306	-
$(G_{m2}/G_{m5})^2$	8.008	-
$\frac{W_1 \cdot L_1}{W_4 \cdot L_4}$	1.708	-
$\frac{W_1 \cdot L_1}{W_2 \cdot L_2}$	0.091	-
$\frac{W_1 \cdot L_1}{W_5 \cdot L_5}$	5.178	-
η_{fl}	0.509	-
f_k	165.408	kHz

From Table 4.6, we see that $\eta - fl = 0.2$, which means that the input-referred flicker noise PSD is dominated by M_{4a}-M_{4b}, M_2 and M_{5a}-M_{5b}. From From Table 4.6, we can actually identify that the dominant contribtuion to the input-referred flicker noise PSD is due to M_{4a}-M_{4b}. As discussed when sizing M_{4a}-M_{4b}, we could increase the area of M_{4a}-M_{4b} but at the cost of more paraisitc capacitance at the node 4 and hence les phase margin, which is undesirable. The corner frequency is actually quite low at $f_k = 165.4$ kHz. The input-referred noise PSD is plotted in Figure 4.2.

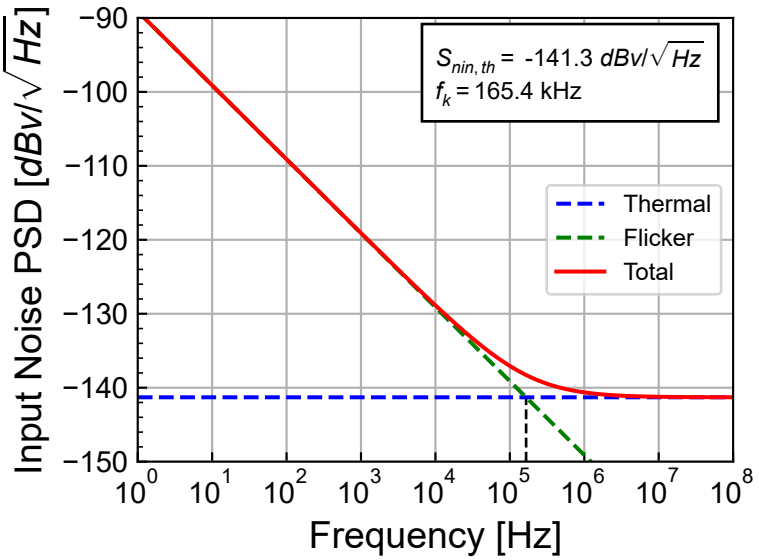

Figure 4.2: OTA theoretical input-referred noise PSD.

4.3 Input-referred random offset voltage

We have seen that the input-referred offset voltage is given by

$$\sigma^2_{V_{os}} = \sigma^2_{V_T} + \sigma^2_{\beta} \tag{4.1}$$

where

$$\sigma^2_{V_T} = \sigma^2_{V_{T1}} \cdot (1 + \xi_{V_T}) \tag{4.2}$$

and

$$\sigma^2_{\beta} = \left(\frac{I_b}{G_{m1}}\right)^2 \cdot \sigma^2_{\beta_1} \cdot (1 + \xi_{\beta}). \tag{4.3}$$

ξ_{V_T} represents the V_T-mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_{V_T} = \left(\frac{G_{m4}}{G_{m1}}\right)^2 \cdot \left(\frac{A_{VTp}}{A_{VTn}}\right)^2 \cdot \frac{W_1 L_1}{W_4 L_4} \tag{4.4}$$

and ξ_{β} represents the β-mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_{\beta} = \left(\frac{A_{\beta p}}{A_{\beta n}}\right)^2 \cdot \frac{W_1 L_1}{W_4 L_4}. \tag{4.5}$$

The various parameters used to calculate the input-referred offset voltage are given in

Table 4.7: OTA input-referred offset parameters.

Symbol	Theoretical Value	Unit	Comment
σ_{VT1}	3.255	mV	V_T-mismatch of M_{1a}-M_{1b}
σ_{VT4}	4.253	mV	V_T-mismatch of M_{4a}-M_{4b}
ξ_{V_T}	0.061	-	Input-referred V_T-mismatch of M_{4a}-M_{4b} relative to M_{1a}-M_{1b}
$\sigma_{\beta 1}$	0.651	%	β-mismatch of M_{1a}-M_{1b}
$\sigma_{\beta 4}$	0.851	%	β-mismatch of M_{4a}-M_{4b}
ξ_{β}	1.708	-	Input-referred β-mismatch of M_{4a}-M_{4b} relative to M_{1a}-M_{1b}

Table 4.7: OTA input-referred offset parameters.

Symbol	Theoretical Value	Unit	Comment
σ_{V_T}	3.353	mV	Total input-referred V_T-mismatch
σ_β	0.385	mV	Total input-referred β-mismatch
σ_{Vos}	3.375	mV	Total input-referred offset voltage

The various parameters needed to compute the input-referred random offset voltage standard deviation are given in Table 4.7. For the same reason discussed for the flicker noise, the current mirror M_{4a}-M_{4b} is contributing 0.061 times more than the differential pair M_{1a}-M_{1b} to the V_T-mismatch and 1.7 times more than the differential pair M_{1a}-M_{1b} to the β-mismatch.

4.4 Power consumption

The total current consumption, without the current flowing in M_{3a} and M_{5a}, is given by $I_{tot} = 2.26$ μA, resulting in a total power consumption $P = 4.068$ μW.

We can compare the current and power consumption of the Miller OTA to the telescopic OTA which offers the lowest power consumption for similar GBW and DC gain specifications. The current consumption of the telescopic OTA for the actual specifications can be estimated to $I_{tot,telescopic} \cong 0.5$ μA. The current and power consumption of the Miller OTA is 4.52 times larger than that of the telescopic OTA for the same specifications and performance.

5 Simulation results from ngspice

The theoretical results can be validated with the results obtained from simulations performed with ngspice. In order to run the simulations you need to have ngspice correctly installed. Please refer to the installation instructions.

> **Note**
>
> The simulations are performed with ngspice [4] using the EKV 2.6 compact model [5] [11] [1]. For ngspice, we use the original Verilog-A implementation of EKV 2.6 [7] modified by C. Enz to get the operating point informations and available on the Gitub va-models site provided by D. Warning at [6] [12]. The Verilog-A code was then compiled with OpenVAF [13] to generate the OSDI for running it with ngspice. The parameters correspond to a generic 180 nm bulk CMOS process [8].

5.1 Operating point

We first write the parameter file for this specific design for running the ngspice simulations. Before running the AC and NOISE simulations, we first need to check the quiescent voltages and currents and the operating points of all transistors by running a .OP simulation.

Table 5.1: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
inp	0.9
inn	0.9
out	1.78482
ic	0.9
id	0
1	0.999893
3	0.394011
4	0.999893
5	0.82975
6	0.828234

We can extract the OTA quiescent node voltages from the .ic file. They are presented in Table 5.1. As expected, we see that the output voltage $V_{outq} = 1.785\ V$ is saturated to V_{DD} pushing M_2 in the linear region. This is due to the fact that M_2 is biased in moderate inversion with a source-to-gate voltage V_{SG2} about equal to V_{T0p}. However, for a zero differential input voltage, the voltage at node 1 is actually set to the same value than the voltage at node 4 which is equal to the V_{SG4} voltage of M_4. This voltage is larger than V_{T0p} by its overdrive voltage $V_{BG4} - V_{T0p}$ because M_{4a}-M_{4b} are biased in strong inversion. The only way for M_2 to carry the current it would carry in moderate inversion if it was biased in saturation is to reduce its V_{SD} voltage and therefore drive M_2 in the linear region with a V_{SD} voltage almost equal to zero. For this reason, the output voltage is saturating to V_{DD}. We

therefore cannot simulate the open-loop transfer function because the operating points, in particular that of M_2, are wrong.

Simulating the open-loop gain for high gain amplifiers is not easy to perform without closing the loop. There are basically two approaches to simulate the open-loop gain for high-gain amplifiers:

1) Imposing a DC offset voltage to the amplifier in open-loop configuration that brings the output voltage back to the high gain region (for example equal to the input common-mode voltage) or
2) Simulating the closed-loop gain (for example in voltage follower mode with a feedback gain of 1 and extracting the open-loop gain from the closed loop gain according to

$$A_{ol}(\omega) = \frac{A_{cl}(\omega)}{1 - A_{cl}(\omega)}, \tag{5.1}$$

where $A_{cl}(\omega)$ is the simulated closed-loop transfer function and $A_{ol}(\omega)$, the computed open-loop transfer function. The above relation assumes that the open-loop DC gain is large enough for the input-referred offset voltage to be ignored.

The input-referred offset voltage can be extracted from the closed-loop voltage follower circuit as

$$V_{os} = V_{in} - \left(1 + \frac{1}{A}\right) \cdot V_{out} \cong V_{in} - V_{out} \quad \text{for } A \gg 1, \tag{5.2}$$

where $A \triangleq A_{ol}(0)$ is the open-loop DC gain which can be assumed to be much larger than 1. This means that, provided the DC open-loop gain is sufficiently large, the offset voltage can be measured at the amplifier differential input after imposing the proper input common-mode voltage V_{ic}.

We can now simulate the OTA in closed-loop as a voltage follower.

Table 5.2: OTA node voltages with the OTA in voltage follower configuration.

Node	Voltage
vdd	1.8
inp	0.9
out	0.900446
1	1.26438
3	0.394357
4	0.999809
5	0.82975
6	0.828234

From the node voltages of the OTA in voltage follower configuration shown in Table 5.2, we see that now the ouput voltage $V_{outq} = 900\ mV$ is very close to the input voltage that has been set to $V_{ic} = 900\ mV$. We can then extract the corresponding offset voltage $V_{os} \cong V_{in} - V_{out} = -0.446\ mV$.

We can now apply this offset voltage to the open-loop circuit for simulating the operating point.

Table 5.3: OTA node voltages with the OTA in open-loop including offset correction.

Node	Voltage
vdd	1.8
inp	0.899777
inn	0.900223
out	0.86158
ic	0.9

Table 5.3: OTA node voltages with the OTA in open-loop including offset correction.

Node	Voltage
id	-0.000446
1	1.26444
3	0.394178
4	0.99981
5	0.82975
6	0.828234

From the node voltages of the OTA in open-loop configuration shown in Table 5.3 after adding the offset voltage at the input, we see that now the ouput voltage $V_{outq} = 862\ mV$ of the open-loop circuit is sufficiently close to the common-mode input voltage $V_{ic} = 900\ mV$.

The operating point information for all transistors are extracted from the ngspice .op file. The data is split into the large-signal operating point informations in Table 5.4, the small-signal operating point informations in Table 5.5 and the noise operating point informations in Table 5.6.

We can compare the results of the .op file (for example the inversion coefficient IC) to the results of the design given in Table 3.7. We observe that the values are close.

Similarly we can compare the small-signal parameters (for example the gate transconductance G_m) resulting from the .op file to the results of the design presented in Table 3.8. Again, we see that they are reasonably close.

Table 5.4: Operating point information extracted from ngspice .op file for each transistor.

Transistor	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC [-]	n [-]	$V_{DSsat}\ [mV]$
M1a	129.8	1295.2	0.100	1.27	120
M1b	129.7	1300.9	0.100	1.27	120
M2	2000.8	954.7	2.099	1.31	178
M3a	260.0	8.7	29.956	1.27	387
M3b	259.5	8.7	29.951	1.27	387
M4a	129.8	5.5	23.834	1.31	356
M4b	129.7	5.5	23.831	1.31	356
M5a	2000.0	72.4	27.867	1.27	377
M5b	2000.8	72.4	27.870	1.27	377

Table 5.5: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	$G_m\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_{ds}\ [nA/V]$
M1a	3.693	4.585	6.274
M1b	3.691	4.582	5.410
M2	28.411	37.938	21.336
M3a	1.265	1.632	0.402
M3b	1.256	1.630	9.949
M4a	0.676	0.915	0.391
M4b	0.676	0.915	0.449
M5a	9.960	12.852	24.614
M5b	9.964	12.856	23.742

Table 5.6: Noise operating point information extracted from ngspice .op file for each transistor.

Transistor	R_n [$k\Omega$]	$\sqrt{S_{ID,th}}$ [$nA/\sqrt{Hz}$]	γ_n [-]	$\sqrt{S_{ID,fl}}$ at 1Hz [$nA/\sqrt{Hz}$]
M1a	174.541	53.789	0.645	20656.1
M1b	174.562	53.792	0.644	20656.1
M2	27.904	21.507	0.793	17762.3
M3a	674.793	105.761	0.854	15344.6
M3b	684.152	106.492	0.860	15344.6
M4a	1304.513	147.050	0.882	67777.5
M4b	1305.702	147.117	0.882	67777.5
M5a	87.089	37.995	0.867	42851.8
M5b	87.048	37.986	0.867	42851.8

We can also check the bias voltages and operating region of each transistor which are given in Table 5.7.

Table 5.7: Bias voltages and operating regions extracted from ngspice for each transistor.

Trans.	Type	Funct.	V_G [V]	V_S [V]	V_D [V]	V_{DS} [mV]	V_{DSsat} [mV]	Reg.	Sat.
M1a	n	DP	0.900	0.394	1.000	606	120	MI	sat
M1b	n	DP	0.900	0.394	1.264	870	120	WI	sat
M2	p	CS	0.536	0.000	0.938	938	178	MI	sat
M3a	n	CM	0.830	0.000	0.830	830	387	SI	sat
M3b	n	CM	0.830	0.000	0.394	394	387	SI	sat
M4a	p	CM	0.800	0.000	0.800	800	356	SI	sat
M4b	p	CM	0.800	0.000	0.536	536	356	SI	sat
M5a	n	CM	0.828	0.000	0.828	828	377	SI	sat
M5b	n	CM	0.828	0.000	0.862	862	377	SI	sat

From Table 5.7, we see that all transistors are biased in saturation. The operating points look fine. We can now proceed with the simulation of the open-loop large-signal transfer characteristic.

5.2 Large-signal differential transfer characteristic

We now simulate the DC differential transfer characteristic. We can then check the systematic offset voltage that was extracted above. The simulation of the large-signal input-output characteristic is presented in Figure 5.1.

From Figure 5.1, we see that the output swing is about $V_{out,swing} = 1.1\ V$. We can now zoom into the high gain region in order to extract the offset voltage that is needed to bring the output voltage back to $V_{outq} = 0.900\ V$. The simulation results are presented in Figure 5.2.

We can now save a more accurate value of the offset voltage V_{os} = -0.446 mV that is required to bring the output voltage to $V_{ic} = 900\ mV$ and that will be used for the following .AC and .NOISE simulations.

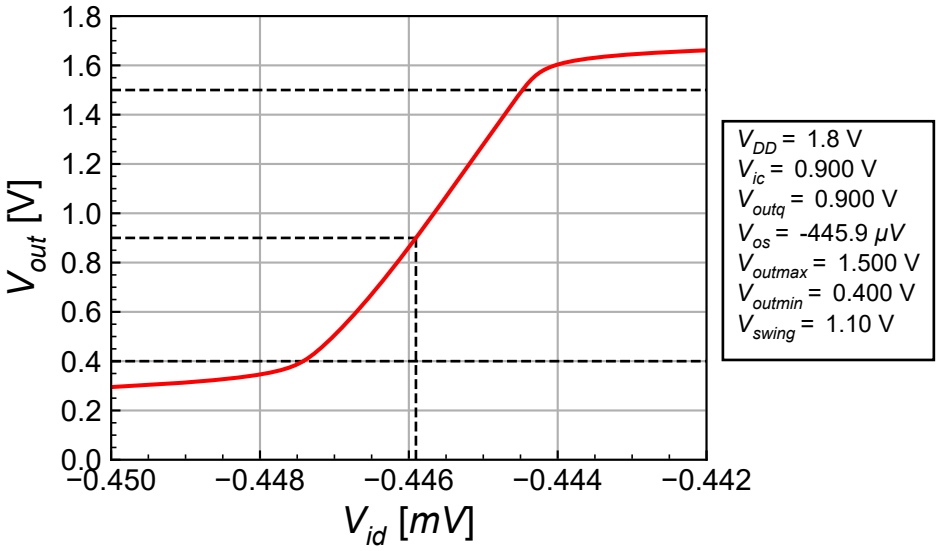

Figure 5.1: Simulated large-signal input-output characteristic.

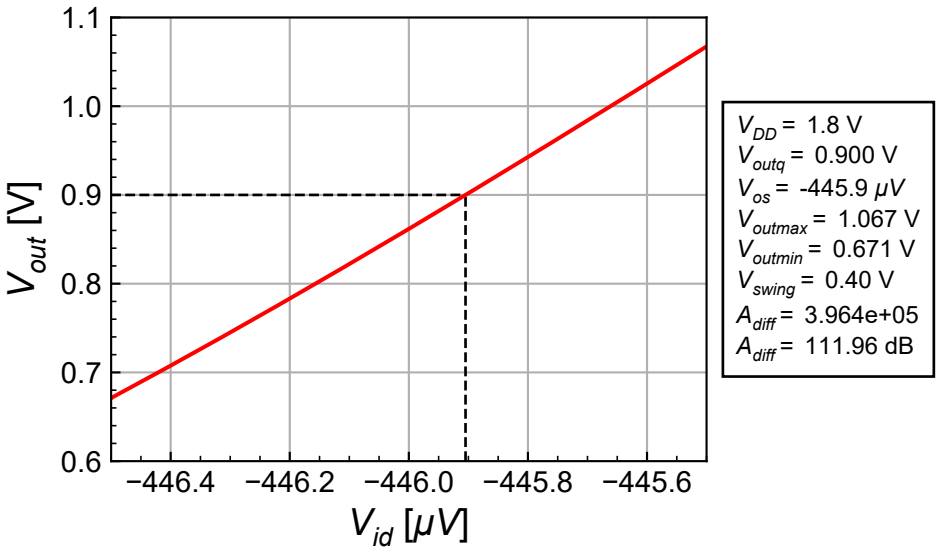

Figure 5.2: Zoom of the simulated large-signal input-output characteristic in the high gain region.

5.3 Open-loop gain

5.3.1 Closed-loop circuit

As explained above we can extract the open-loop gain from the simulated closed-loop gain with the amplifier operating as a voltage follower. The OTA open-loop gain $A_{ol}(\omega)$ is then given by

$$A_{ol}(\omega) = \frac{A_{cl}(\omega)}{1 - A_{cl}(\omega)}, \tag{5.3}$$

where $A_{cl}(\omega)$ is the simulated closed-loop transfer function and $A_{ol}(\omega)$, the computed open-loop transfer function. The above relation assumes that the open-loop DC gain is large enough for the input-referred offset voltage to be ignored. The simulations results are shown in Figure 5.3.

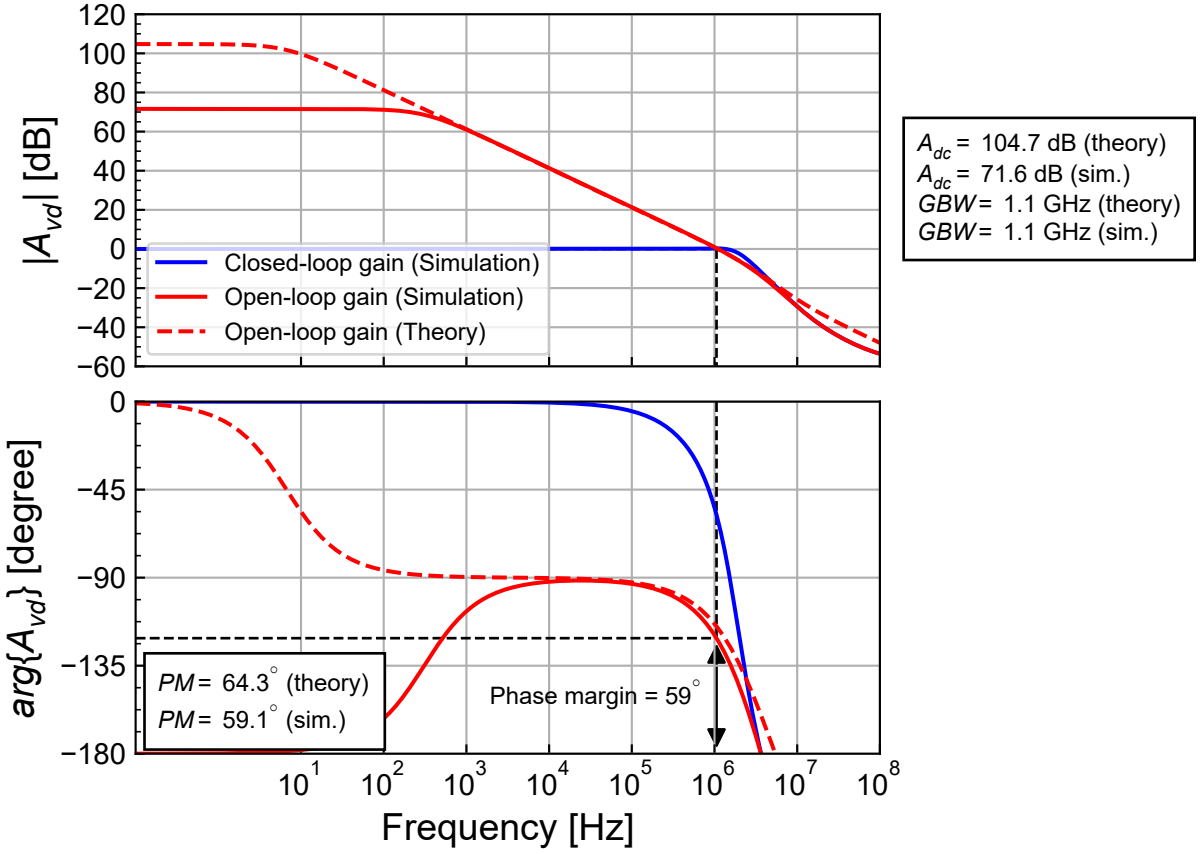

Figure 5.3: Open-loop gain response extracted from the closed-loop simulations and compared to theoretical estimation.

From Figure 5.3, we see that the simulated GBW is close to the theoretical value and slightly above the specs. The calculated open-loop gain does not seem to give correct results at low frequency. The main reason for this is that the way the open-loop gain is calculated does not account for a large offset voltage which reduces the resulting open-loop DC gain. The phase also looks incorrect at low-frequency. It is equal to $-180°$ at low frequency which indicates that the gain is negative. If we want to account for the offset voltage we need to compute the open-loop gain according to

$$A_{ol}(\omega) = \frac{1}{\frac{V_{in}-V_{os}}{V_{out}(\omega)} - 1} = \frac{1}{\frac{V_{in}}{V_{out}(\omega)} - \frac{V_{os}}{V_{out}(\omega)} - 1}. \tag{5.4}$$

Replacing $V_{out}(\omega) = A_{cl}(\omega) \cdot V_{in}$, we get

$$A_{ol}(\omega) = \frac{1}{\frac{1}{A_{cl}(\omega)}\left(1 - \frac{V_{os}}{V_{in}}\right) - 1}, \tag{5.5}$$

which dependends on V_{in}. Now, in AC analysis, the amplitude of the small-signal input voltage $V_{in} = 1$ and therefore

$$A_{ol}(\omega) = \frac{1}{\frac{1-V_{os}}{A_{cl}(\omega)} - 1}. \tag{5.6}$$

The open-loop gain extracted from the closed-loop small-signal simulation accounting for the effect of the offset voltage is presented in Figure 5.4.

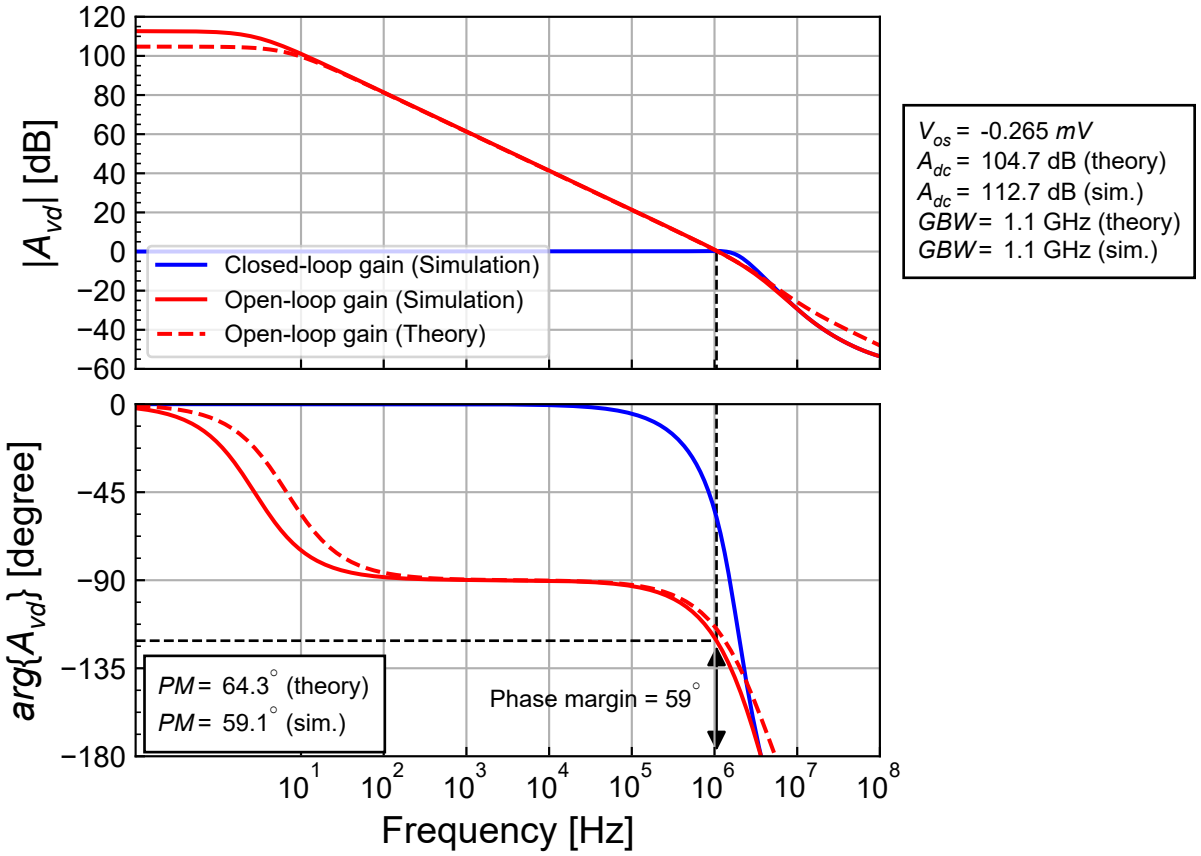

Figure 5.4: Open-loop gain response extracted from the closed-loop simulations including the effect of the offset voltage.

From Figure 5.4, we see now a much better estimation of the open-loop gain and a correct phase at low frequency. We had to adjust the offset voltage to a value V_{os} = -0.265 mV, which is slightly larger than the one extracted in the operating point simulation V_{os} = -0.446 mV.

Having extracted the offset voltage, we can also simulate the open-loop gain directly in open-loop configuration.

5.3.2 Open-loop circuit

After having checked the operating point information, extracted the offset voltage and making sure that the OTA output is not saturated, we can now proceed with the open-loop gain simulation. The simulation results are presented in Figure 5.5.

The results of the open-loop simulation in Figure 5.5 are close to the theoretical estimation. The simulated GBW is equal to the theoretical estimation and to the value extracted from the closed-loop simulation and slightly higher than the specification. The DC gain is larger than the theoretical prediction and well above the specification. Finally the phase margin is sligtly smaller than the theoretical estimation but close to the specification. This is probably due to the zero being at lower frequency.

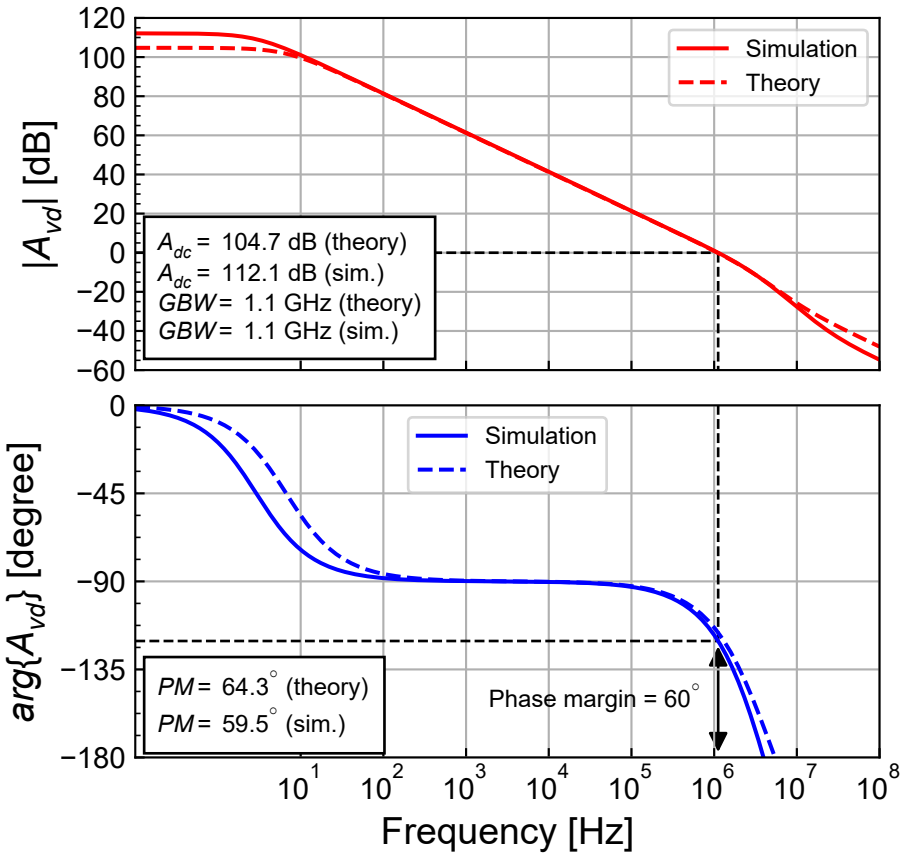

Figure 5.5: Simulated gain response compared to theoretical estimation.

5.4 Input-referred noise

The simulated input-referred noise PSD is presented in Figure 5.6 and compared to the theoretical estimation.

From Figure 5.6, we see that the simulated input-referred noise PSD perfectly matches the theoretical estimation. We can have a closer look at the contributions of the various transistors to the input-referred white noise PSD. The contributions of M_{1a}-M_{1b}, M_2, M_{3a}-M_{3b}, M_{4a}-M_{4b} and M_{5a}-M_{5b} to the input-referred white noise PSD are detailed in Figure 5.7 and compared to the theoretical white noise.

From Figure 5.7, we can observe that the total simulated white noise is equal to the theoretical estimation. The white noise is dominated by the differential pair M_{1a}-M_{1b} which is $1 + \eta_{th} = 1.251$ times (or 0.971 dB) lower than the total white noise. The contribution of M_{4a}-M_{4b} is about $\eta_{th} = 0.251$ times (or 6.011 dB) lower than the contribution of M_{1a}-M_{1b}. The simulated value of $\eta_{th} = 0.251$ is about equal to the theoretical estimation 0.241. The OTA thermal noise excess factor $\gamma_{n,ota} = 1.615$ is about equal to the predicted value $\gamma_{n,ota} = 1.622$. Figure 5.7 also shows that the noise contributions of M_2 and M_{5a}-M_{5b} are negligible at lower frequency thanks to the gain of the 1st-stage. It also shows that the contribution of M_{3a}-M_{3b} is negligible simply because it is a common-mode current contribution which is canceled at the output of the 1st-stage.

Figure 5.8 presents the breakdown of the contributions of the various transistors to the input-referred flicker noise. As expected from the value of $\eta_{fl} = 0.509$ in Table 4.6, the flicker noise is dominated by the current mirror M_{4a}-M_{4b}. The contribution of the differential pair is about 10 dB lower and the contributions of M_2 and M_{5a}-M_{5b} more than 30 dB lower.

The breakdown of the contributions of the various transistors to the total input-referred noise is presented in Figure 5.8.

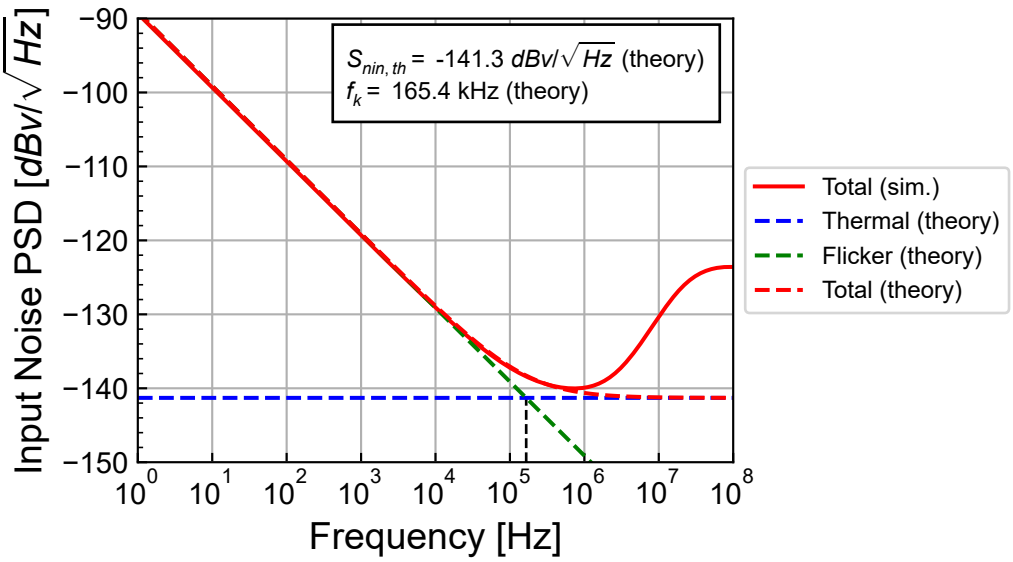

Figure 5.6: Simulated input-referred noise PSD compared to theoretical estimation.

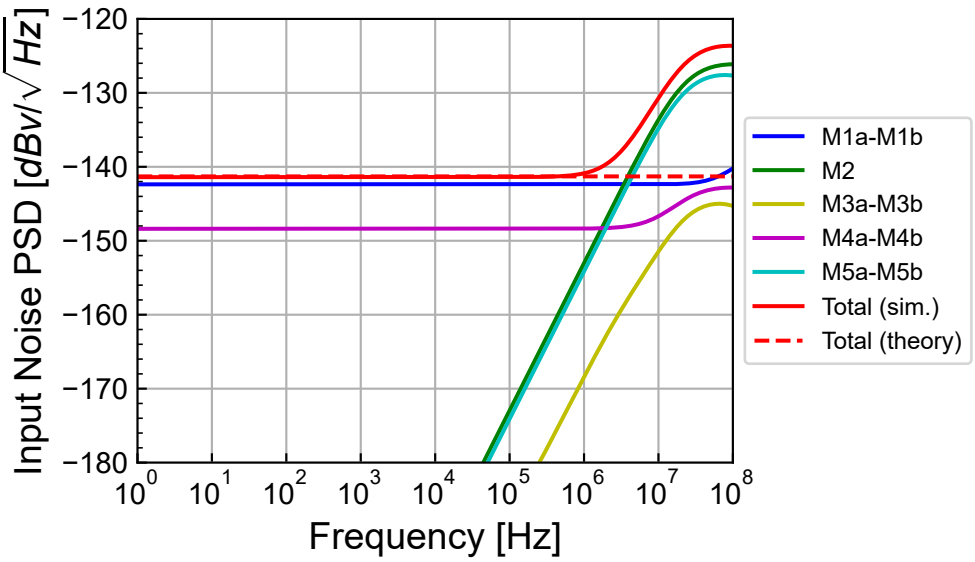

Figure 5.7: Breakdown of the contributions to the simulated input-referred white noise PSD.

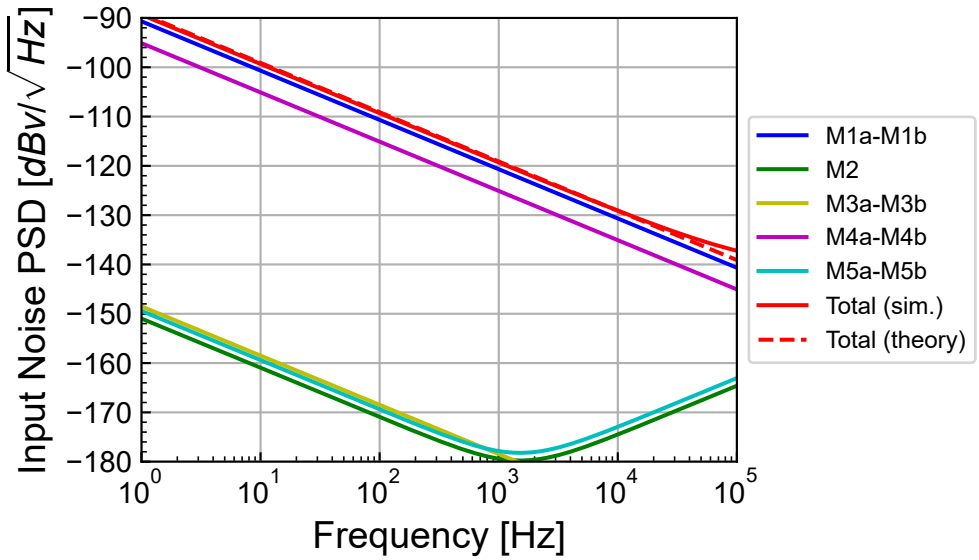

Figure 5.8: Breakdown of the contributions to the simulated input-referred flicker noise PSD.

We can observe that the simulation of the total input-referred flicker noise PSD perfectly matches the theoretical estimation. We also see that the flicker noise is dominated by the contribution of the input differential pair M_{1a}-M_{1b} which is confirmed by the simulated value of $\eta_f = 0.361$ which is even lower than the theoretical estimation $\eta_f = 0.509$. This is due to the higher simulated gain. The contribution of the current mirror M_{4a}-M_{4b} is about 4.428 dB lower than that of the differential pair M_{1a}-M_{1b}.

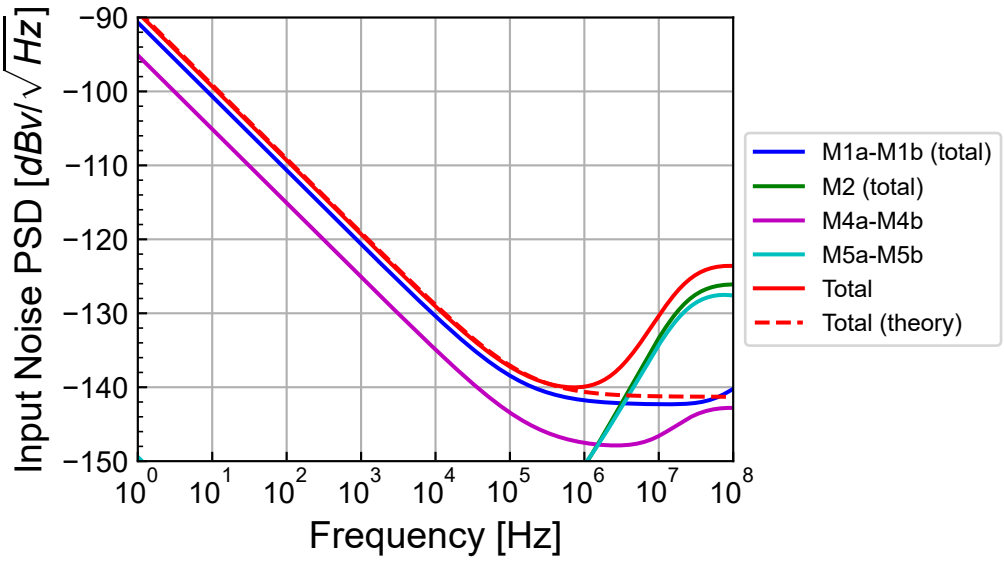

Figure 5.9: Breakdown of the contributions to the simulated input-referred noise PSD.

5.5 Input common-mode voltage range

We can check the input common-mode voltage range by connecting the OTA as a voltage follower and sweeping the positive input.

As shown in Figure 5.10, the output follows the input voltage up to about 1.50 V. So the input common-mode voltage range is about $V_{cm,max} \cong 1.50\ V$.

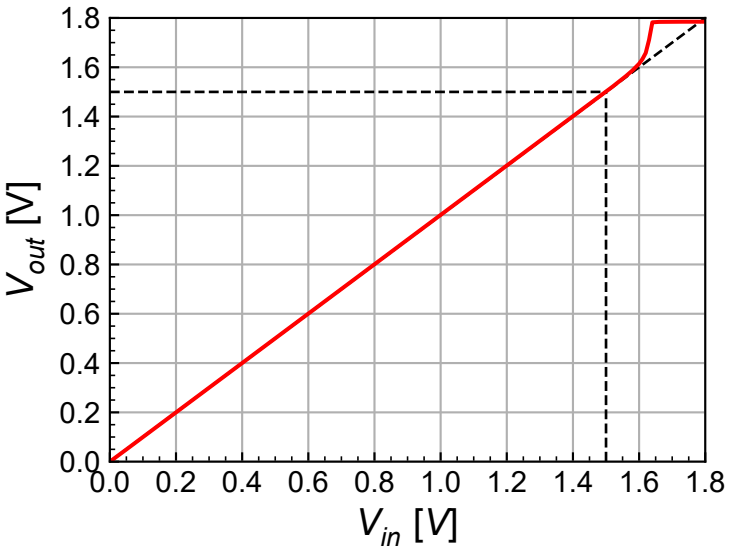

Figure 5.10: Simulated input common-mode voltage range.

5.6 Step-response

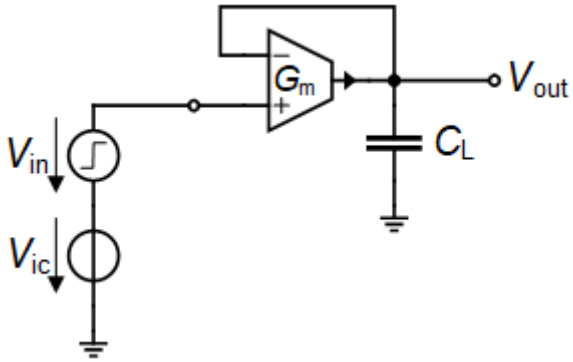

Figure 5.11: Schematic of the OTA connected as a voltage follower.

In this section we will check the step response of the OTA operating as a voltage follower as shown in Figure 5.11 with its output connected to the negative input and with the same load capacitance $C_L = 1\ pF$.

5.6.1 Small-step

We start by imposing a small step $\Delta V_{in} = 10\ mV$ on top of a common mode voltage $V_{ic} = 0.9\ V$. The simulation results are shown in Figure 5.12 where $\Delta V_{in}(t) \triangleq V_{in+}(t) - V_{ic}$ and $\Delta V_{out}(t) \triangleq V_{out}(t) - V_{outq}$ with $V_{outq} \cong V_{ic}$ is the quiescent output voltage. ΔV_{in} and ΔV_{out} are compared to the response of a single pole circuit having a cut-off frequency equal to the GBW. The difference between the simulation an the first-order model is due to the additional poles and the zero introduced by the current mirrors and the compensation capacitor, respectively.

5.6.2 Large step

We now impose a larger step $\Delta V_{in} = 300\ mV$ on top of a common mode voltage $V_{ic} = 0.9\ V$. The simulation results are shown in Figure 5.13 where $\Delta V_{in}(t) \triangleq V_{in+}(t) - V_{ic}$ and $\Delta V_{out}(t) \triangleq V_{out}(t) - V_{outq}$ with $V_{outq} \cong V_{ic}$ is the quiescent output voltage. ΔV_{in} and ΔV_{out} are compared to the response of a

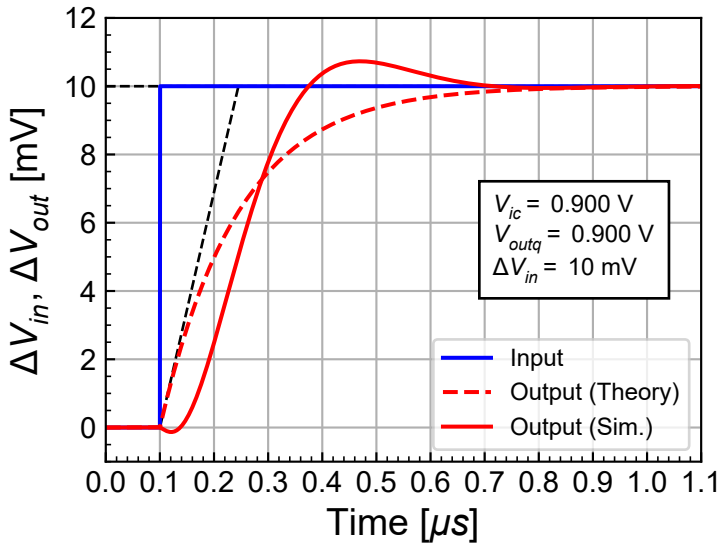

Figure 5.12: Step response of the OTA as a voltage follower for a small input step.

single pole circuit having a cut-off frequency equal to the GBW. We now observe the effect of slew-rate which increases the settling time.

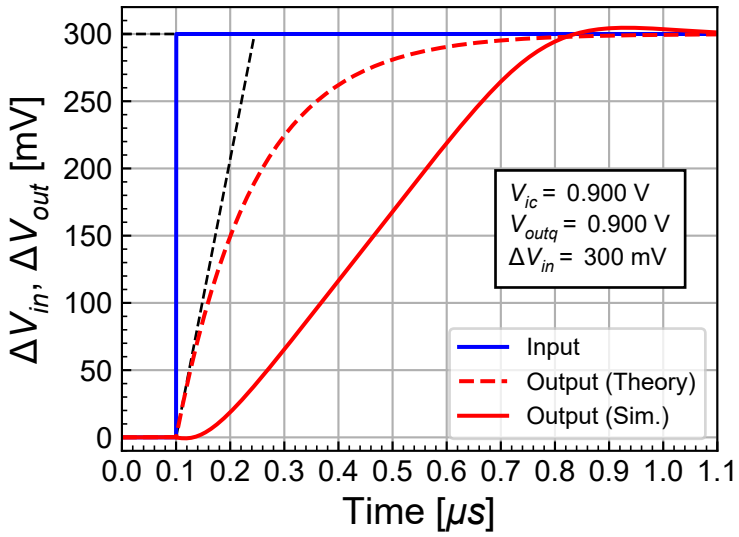

Figure 5.13: Step response of the OTA as a voltage follower for a large input step highlighting the slew-rate effect.

5.7 Power consumption

The total power consumption without accounting for the current flowing in M_{3a} and M_{5a} is equal to $I_{tot} = 2.26\ \mu A$, resulting in a total power consumption $P = 4.068\ \mu W$. We can compare the current and power consumption of the Miller OTA to the telescopic OTA which has a current consumption of about $I_{tot,telescopic} \cong 0.5\ \mu A$. The current and power consumption of the Miller OTA is 4.52 times larger than that of the telescopic OTA for the same specifications and performance.

6 Conclusion

This notebook presented the analysis, design and verification of the Miller OTA [10] designed for a generic 180nm bulk CMOS process. The detailed analysis provided all the equations that were then used in the design phase to reach the target specifications. The design was then performed using the inversion coefficient approach with the sEKV transistor model [1] [2] [3]. The theoretical performance resulting from the design were then evaluated.

The design was then verified by simulation using ngspice [4] with the EKV 2.6 compact model [5] and the parameters of a generic 180 nm bulk CMOS process. Because of the voltage at the input of the 2^{nd}-stage is set by the source-to-gate voltage V_{SG} of the 1^{st}-stage current mirror and because the latter is higher than the source-to-gate voltage of the 2^{nd}-stage transistor, the latter is driven out of saturation and the OTA output saturates to V_{DD}. The OTA was then simulated in closed-loop as a voltage follower in order to extract the offset voltage that is required to bring the quiescent output voltage in open-loop configuration back to the high gain region. After carefully checking the operating point, the large-signal transfer characteristic was then simulated. Then the small-signal transfer function of the OTA connected as a voltage follower was simulated. The open-loop transfer function could then be extracted from the closed-loop simulations provided some adjustment on the rather large offset voltage was done. The open-loop transfer function was then simulated making sure the OTA was biased in the high gain region. The transfer function was then compared to the theoretical estimation showing an excellent correspondance except for the DC gain which was higher for the simulated transfer function. The simulations have shown that the gain-bandwidth product GBW and the DC gain are both achieved.

The input-referred noise was then simulated showing results that are very close to the theoretical estimation for both the white noise and the flicker noise. The contributions of the various transistors to the input-referred white noise were then extracted from the noise simulation and compared to the theoretical estimation. It was shown that the total white noise PSD simulation perfectly matches the theoretical estimation. The detailed contributions of the various transistors to the input-referred flicker noise was then simulated. The total input-referred flicker noise PSD also perfectly matches the theoretical estimation. It has also been shown that, despite the high value of the flicker noise cioefficient for pMOS transistors, the input-referred flicker noise is dominated by the differential pair.

The input common-mode voltage range was then simulated with the OTA connected as a voltage follower.The input voltage is limited to $V_{cm,max} = 1.5\ V$.

Finally, the small-signal step response was simulated and succesfully compared to the response of a single-pole system. The step-response with a large input step highlighted the effect of slew-rate.

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