Common-source Stage Optimization using the Inversion Coefficient

In Open-loop Configuration (Version 1)

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Table of contents

1 Introduction

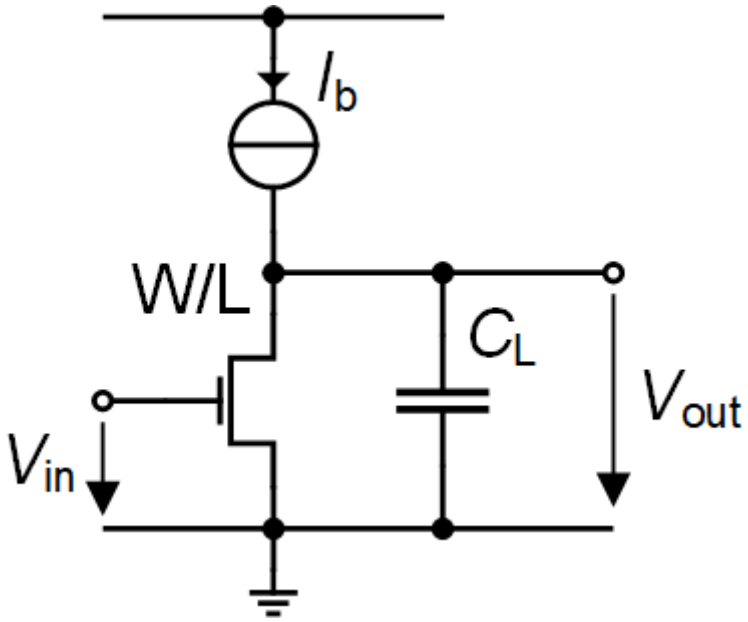

Figure 1.1: Schematic of the open-loop common-source (CS) gain stage.

The schematic of the common-source (CS) stage in open-loop (OL) configuration is shown in Figure 1.1. To size the transistor according to some specifications on the gain, bandwidth or noise, we need to find the bias current I_b and the aspect ratio W/L that satisfies the given specifications. In order to do this, we first need to analyze the circuit in terms of its key features. We will start with a small-signal analysis.

2 Small-signal analysis

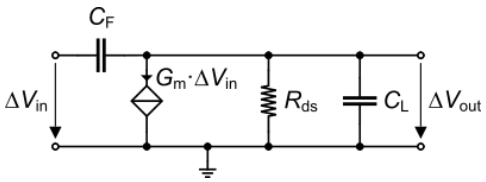

Figure 2.1: Small-signal schematic of the open-loop (OL) common-source (CS) gain stage including the feedback capacitance.

The small-signal schematic of the open-loop (OL) common-source (CS) stage of Figure 1.1 is shown in Figure 2.1. It is straightforward to show that the transfer function is given by

$$A(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = A_{dc} \cdot \frac{1 - s/\omega_z}{1 + s/\omega_p} \tag{2.1}$$

where

$$A_{dc} = -G_m \cdot R_{ds}, \tag{2.2}$$

$$\omega_z = \frac{G_m}{C_F}, \tag{2.3}$$

$$\omega_p = \frac{1}{R_{ds}\, C_{out}}, \tag{2.4}$$

with $A_{dc} = -G_m \cdot R_{ds}$ the DC voltage gain, ω_z the zero (in the right half plan), ω_p the pole and $C_{out} = C_L + C_F$ the total load capacitance at the output node including the feedback capacitance. The gain-bandwidth product (GBW) or unity gain frequency (ω_u) is then given by

$$GBW = \omega_u = |A_{dc}| \cdot \omega_p = \frac{G_m}{C_{out}}. \tag{2.5}$$

As illustrated in Figure 2.2, the gain magnitude at high frequency will settle to

$$\lim_{s \to \infty} A(s) = \frac{C_F}{C_L + C_F}, \tag{2.6}$$

and the phase will turn to $-180°$ because of the positive zero.

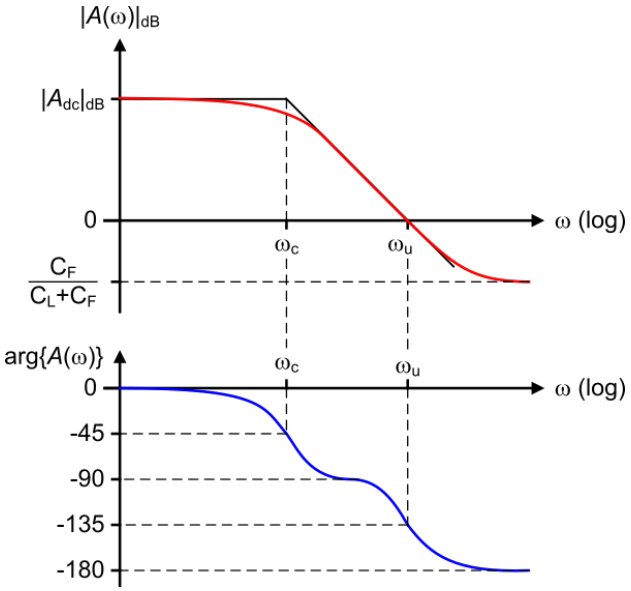

Figure 2.2: Bode plot of the small-signal transfer function of the CS OL amplifier.

3 Minimum current for a given transconductance

In this section we want to answer the following question:

> **Question**
>
> What is the minimum current I_b and transistor size (aspect ratio W/L) in order for the OL CS gain stage to achieve a given transconductance?

To answer this question we first rewrite the current as

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC \tag{3.1}$$

and the transconductance as

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{3.2}$$

where $g_{ms}(IC)$ is the normalized source transconductance which only depends on IC according to

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = \frac{n\,G_m}{G_{spec}} = \frac{\sqrt{4IC+1}-1}{2} \tag{3.3}$$

for a long-channel transistor and

$$g_{ms} = \frac{\sqrt{4IC+1+(\lambda_C\,IC)^2}-1}{2+\lambda_c^2\,IC} \tag{3.4}$$

for a short-channel transistor accounting for velocity saturation with parameter λ_c.

We then need to solve the following set of equation for I_b and W/L

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{3.5}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{3.6}$$

This leads to the following normalized results

$$i_b \triangleq \frac{I_b}{G_m \cdot nU_T} = \frac{IC}{g_{ms}}, \tag{3.7}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{I_{spec\square}}{G_m \cdot nU_T} = \frac{1}{g_{ms}}. \tag{3.8}$$

i_b and AR are plotted below for various values of λ_c

From Figure 3.1, we see that we can reduce the current i_b when moving from strong inversion to moderate inversion reaching a minimum in weak inversion. The loss of transconductance resulting from a reduction of IC is compensated by an increase of W/L as shown by the blue curves, resulting in a very large transistor and a drastic area increase. Moderate inversion turns out to be a good trade-off between low current and acceptable area for achieving a given transconductance.

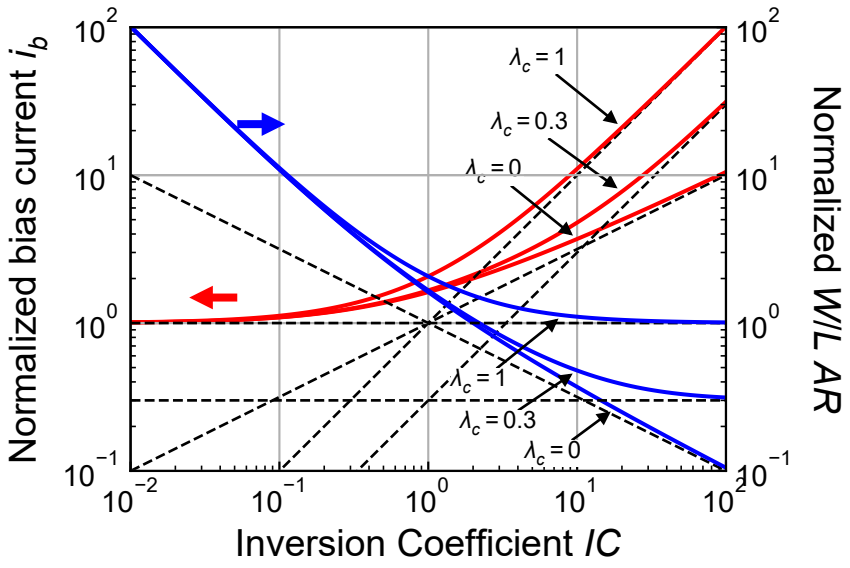

Figure 3.1: Normalized bias current i_b and aspect ratio AR versus inversion coefficient IC.

4 Minimum current for a given gain-bandwidth product (no self-loading)

We now will answer the question:

> **Question**
>
> What is the minimum bias current to achieve a given gain-bandwidth product for a given load capacitance neglecting the effect of self-loading?

We first rewrite the gain-bandwidth as

$$\omega_u = \frac{G_m}{C_L} = \omega_L \cdot \frac{W}{L} \cdot g_{ms}, \tag{4.1}$$

where

$$\omega_L \triangleq \frac{I_{spec\square}}{nU_T \cdot C_{out}}. \tag{4.2}$$

To answer this question we need to solve the following set of equations for I_b and W/L

$$\omega_u = \omega_L \cdot \frac{W}{L} \cdot g_{ms}, \tag{4.3}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{4.4}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{4.5}$$

Since the load capacitance C_L is assumed constant, the problem is similar to imposing a given transconductance With a slightly different normalization we get the same normalized functions as before

$$i_b \triangleq \frac{I_b}{G_m \cdot nU_T} \cdot \frac{1}{\Omega} = \frac{IC}{g_{ms}}, \tag{4.6}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{1}{\Omega} = \frac{1}{g_{ms}}. \tag{4.7}$$

with

$$\Omega \triangleq \frac{\omega_u}{\omega_L}. \tag{4.8}$$

A different normalization reduces to the same trade-off than constant G_m and hence the normalized bias current i_b and aspect AR are identical to the one plotted in Figure 3.1 for various values of λ_c. Moderate inversion again turns out to be a good trade-off between low current and acceptable area for achieving a given gain-bandwidth product.

When moving to moderate and weak inversion, the transistor can become very large. The parasitic capacitance at the transistor drain can then no more be ignored. We will analyze the impact of self-loading in the next section.

5 Minimum current for a given gain-bandwidth product including self-loading (long-channel)

5.1 Analysis

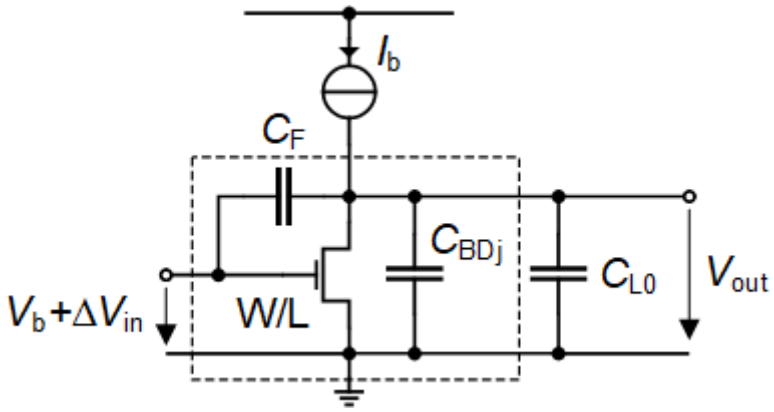

Figure 5.1: Schematic of the open-loop common-source (CS) gain stage including the self-loading capacitances at the drain.

When optimizing the OL CS amplifier for low current consumption, the transistor is often biased in moderate or even weak inversion leading to a large transistor and therefore an increased output capacitance due to the self-loading from the parasitic capacitances connected to the drain. We now want to answer the following question:

> **Question**
>
> What is the minimum bias current I_b and transistor size (aspect ratio W/L) in order for the OL CS gain stage to achieve a given gain-bandwidth product accounting for the effect of self-loading?

As shown in Figure 5.1, the self-loading capacitances include the junction capacitance at the drain C_{BDj} and the feedback capacitance C_F. The junction capacitance C_{BDj} is given by

$$C_{BDj} = 2H_{dif} \cdot W \cdot C_J + 2(2H_{dif} + W) \cdot C_{JSW} = 4H_{dif} \cdot C_{JSW} + 2(H_{dif} \cdot C_J + C_{JSW}) \cdot W \quad (5.1)$$

where C_J is the bottom junction capacitance per area, C_{JSW} is the side-wall capacitance per unit length and H_{dif} is the half minimum diffusion width, which is imposed by the layout rules. Of course the junction capacitances per area and per length C_J and C_{JSW} are bias dependent since they depend on the drain-to-bulk voltage, but we consider their highest value obtained for a zero drain-to-bulk voltage (worst case).

The feedback capacitance is due to the overlap and fringing field capacitance

$$C_F = C_{GDe} \cdot W, \quad (5.2)$$

where C_{GDe} is the extrinsic capacitance per unit width which is given by

$$C_{GDe} = C_{GDo} + C_{GDf}. \quad (5.3)$$

where C_{GDo} is the overlap capacitance per unit width and C_{GDf} is the fringing field capacitance per unit width.

> **Note**
>
> Note that the fringing field capacitance per unit width is ignored in this 180 nm technology but may become of the same order of magnitude than the overlap capacitance per unit width in more advanced technologies.

The total transistor parasitic capacitance at the drain can then be written as

$$C_D = C_{D0} + C_{DW} \cdot W. \tag{5.4}$$

with

$$C_{D0} = 4H_{dif} \cdot C_{JSW}, \tag{5.5}$$
$$C_{DW} = 2(H_{dif} \cdot C_J + C_{JSW}) + C_{GDe}. \tag{5.6}$$

The part C_{D0} of the total parasitic capacitance at the drain C_D that doesn't scale with W needs to be added to C_{L0}

$$C_L = C_{L0} + C_{D0}. \tag{5.7}$$

In order to achieve a certain bandwidth we need to have a certain transconductance for a certain load capacitance. In order to maximize the current efficiency, we should bias the transistor in weak inversion. This leads to a large transistor and therefore large parasitic capacitances which will impact the bandwidth. Imposing the bandwidth, at some point the capacitance becomes so large that it is no more possible to achieve the required transconductance in weak inversion for the desired bandwidth.

> **Question**
>
> Does this mean that there is a minimum current for the OL CS amplifier to achieve a certain gain-bandwidth product?

To answer this question we need to solve the following set of equations for I_b and W assuming a given length L

$$\omega_u = \frac{G_m}{C_{out}}, \tag{5.8}$$
$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{5.9}$$
$$C_{out} = C_L + C_{DW} \cdot W, \tag{5.10}$$
$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{5.11}$$

Solving for I_b and W/L leads to the following normalized solutions

$$i_b \triangleq \frac{I_b}{I_{spec\square} \cdot \Omega} = \frac{IC}{g_{ms}(IC) - \Theta}, \tag{5.12}$$
$$AR \triangleq \frac{W/L}{\Omega} = \frac{1}{g_{ms} - \Theta}, \tag{5.13}$$

where

$$\Omega \triangleq \frac{\omega_u}{\omega_L}, \tag{5.14}$$

$$\omega_L \triangleq \frac{I_{spec\square}}{nU_T \cdot C_L}, \tag{5.15}$$

$$\Theta \triangleq \frac{\omega_u}{\omega_W}, \tag{5.16}$$

$$\omega_W \triangleq \frac{I_{spec\square}}{nU_T \cdot C_{DW} \cdot L}. \tag{5.17}$$

The normalized current i_b and normalized aspect ratio AR are plotted in Figure 5.2 for three values of parameter Θ. The normalized current i_b is plotted alone in Figure 5.3 versus IC for more values of Θ.

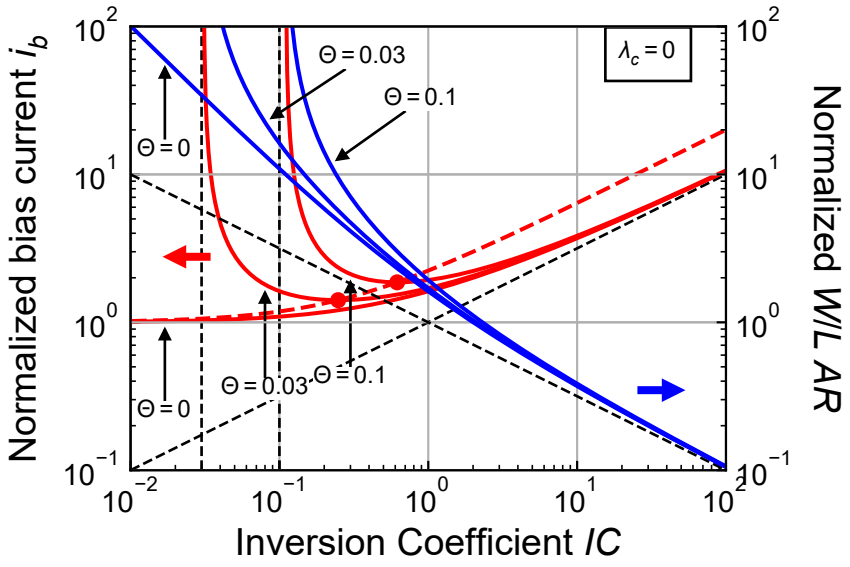

Figure 5.2: Normalized bias current i_b anbd aspect ratio AR versus inversion coefficient IC.

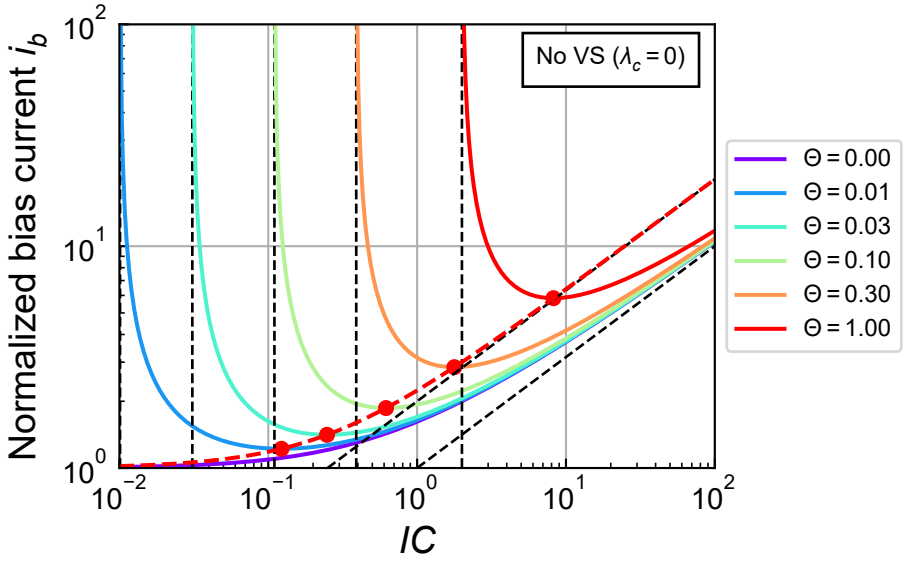

Figure 5.3: Normalized bias current i_b versus inversion coefficient IC.

From Figure 5.2 and Figure 5.3, we clearly see that there is a minimum current for a given value of

parameter Θ. We can find the optimum inversion coefficient IC_{opt} which is given by

$$IC_{opt} = \left(\sqrt{\Theta \cdot (1+\Theta)} + \Theta + \frac{1}{2}\right)^2 - \frac{1}{4} = 2\Theta \cdot (1+\Theta) + (1+2\Theta) \cdot \sqrt{\Theta \cdot (1+\Theta)}. \tag{5.18}$$

For $\Theta \ll 1$, (5.18) reduces to

$$IC_{opt} \cong 2\Theta + \sqrt{\Theta}. \tag{5.19}$$

From the above figure we also see that there is a minimum inversion coefficient IC_{lim} below which the desired gain-bandwidth product GBW can no more be achieved

$$IC_{lim} = \Theta \cdot (1+\Theta) \cong \Theta, \tag{5.20}$$

which is about equal to Θ for small values of Θ.

The optimum normalized current is given by

$$i_{bopt} \triangleq i_b(IC_{opt}) = 1 + 2\Theta + 2\sqrt{\Theta \cdot (1+\Theta)}. \tag{5.21}$$

Parameter Θ can be eliminated from equations (5.21) and (5.18) resulting in an expression of i_{opt} in terms of IC_{opt}

$$i_{bopt} = \sqrt{4IC_{opt} + 1} \tag{5.22}$$

which is plotted as a dashed red line in Figure 5.2 and Figure 5.3.

The optimum current also corresponds an optimum transistor width W and hence and optimum normalized W/L given by

$$AR_{opt} \triangleq AR(IC_{opt}) = \frac{1}{\sqrt{\Theta \cdot (1+\Theta)}}. \tag{5.23}$$

As above, parameter Θ can be eliminated between equations (5.18) and (5.23) giving an expression of AR_{opt} in terms of IC_{opt}

$$AR_{opt} = \frac{\sqrt{4IC_{opt} + 1}}{IC_{opt}}, \tag{5.24}$$

which is plotted as a dashed red line in Figure 5.4.

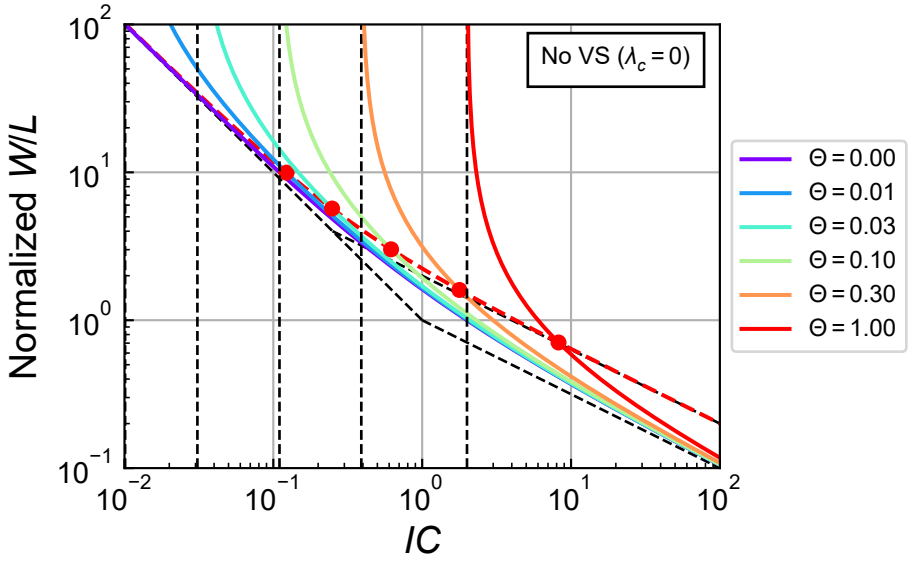

Figure 5.4: Normalized aspect ratio AR versus inversion coefficient IC.

We see from Figure 5.4 that the transistor width increases first as $1/\sqrt{IC}$ in strong inversion and then as $1/IC$ in weak inversion making the transistor quickly very large until IC reaches IC_{lim} where the width becomes infinity. The dots correspond to the AR obtained for IC_{opt}.

The optimum parameters IC_{opt}, i_{bopt} and AR_{opt} are plotted versus Θ in Figure 5.5. We can see that the optimum inversion coefficient is always located in moderate or eventually weak inversion.

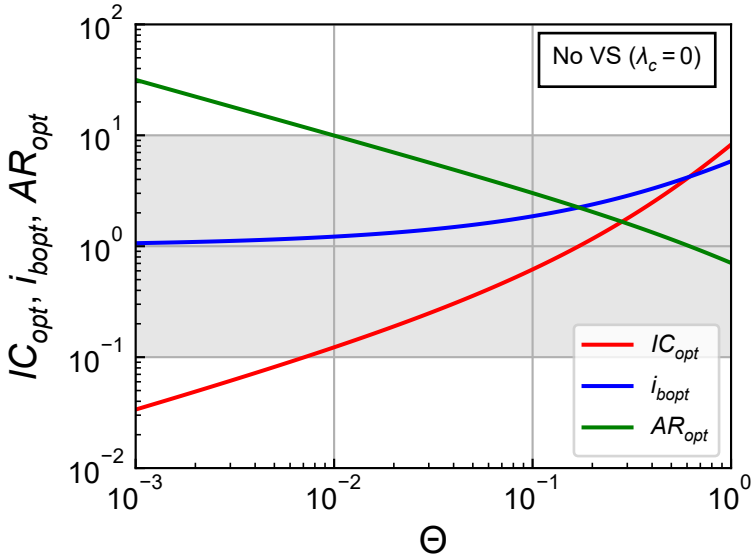

Figure 5.5: Optimum parameters versus Θ.

We now will illustrate the above analysis with a practical example.

5.2 Design example

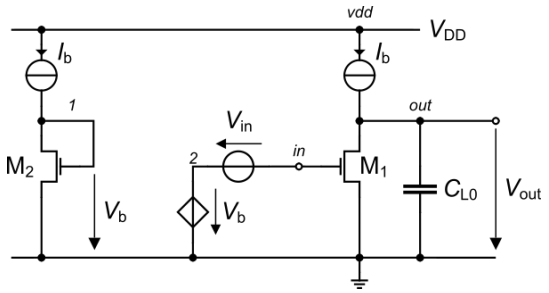

Figure 5.6: Schematic of the open-loop common-source (CS) gain stage used for simulation.

We want to size a CS SC amplifier for the specifications given in Table 5.1. We need to find the minimum current and size the transistor to achieve this specs. We will design the amplifier for a generic 180nm bulk CMOS process. The physical parameters are given in Table 5.2, the global process parameters in Table 5.3 and finally the MOSFET parameters in Table 5.4.

Table 5.1: CS amplifier specifications.

Specification	Symbol	Value	Unit
Gain bandwidth product	GBW	100	MHz
Load capacitance	C_{L0}	20	fF
Transistor length	L	1	μm

Table 5.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 5.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 5.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	15	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	8.1e-24	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

For the chosen technology we get $C_{DW} = 1.167\ fF/\mu m$ and we get $C_{D0} = 0.160\ fF$. The total load capacitance is now $C_L = 20.160\ fF$.

Table 5.5: CS OL amplifier optimum parameters.

Parameter	Value	Unit
C_{DW}	1.167	$fF/\mu m$
C_{D0}	0.16	fF
C_{L0}	20	fF
C_L	20.16	fF
f_L	171.589	MHz
f_W	2.965	GHz
Ω	0.583	-
Θ	0.03372	-
IC_{opt}	0.269	-
$i_{b,opt}$	1.441	-
AR_{opt}	5.356	-
$(W/L)_{opt}$	3.121	-
$I_{b,opt}$	600	nA
W_{opt}	3.12	μm
$G_{m,opt}$	14.955	$\mu A/V$
$C_{D,opt}$	3.641	fF
AD	1.25	μm^2
PD	7.043	μm
C_{DBJ}	2.657	fF
C_F	1.144	fF
C_{out}	23.801	fF
GBW (check)	100	MHz
f_z	2.081	GHz
A_{dc}	51.449	dB

Table 5.6: Transistor size and bias information.

Transistor	W $[\mu m]$	L $[\mu m]$	I_D $[nA]$	I_{spec} $[nA]$	IC	$V_G - V_{T0}$ $[mV]$	V_{DSsat} $[mV]$
M1	3.12	1.00	600	2232	0.269	-22	107
M2	3.12	1.00	600	2232	0.269	-22	107

Table 5.7: Transistor small-signal and thermal noise parameters.

Transistor	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M1	86.255	19.013	14.955	40.026	0.674
M2	86.255	19.013	14.955	40.026	0.674

The theoretical results can be validated by comparing them to the results obtained from simulations performed with ngspice. The cells below will run the simulations with ngspice. In order to run the simulations you need to have ngspice installed. Please refer to the ngspice instructions.

> **Note**
>
> The simulations are performed with ngspice [1] using the EKV 2.6 compact model [2]. For ngspice, we use the original Verilog-A implementation of EKV 2.6 [3] modified by C. Enz to get the operating point informations and available on the Gitub va-models site provided by D. Warning at [4]. The parameters correspond to a generic 180 nm bulk CMOS process [5].

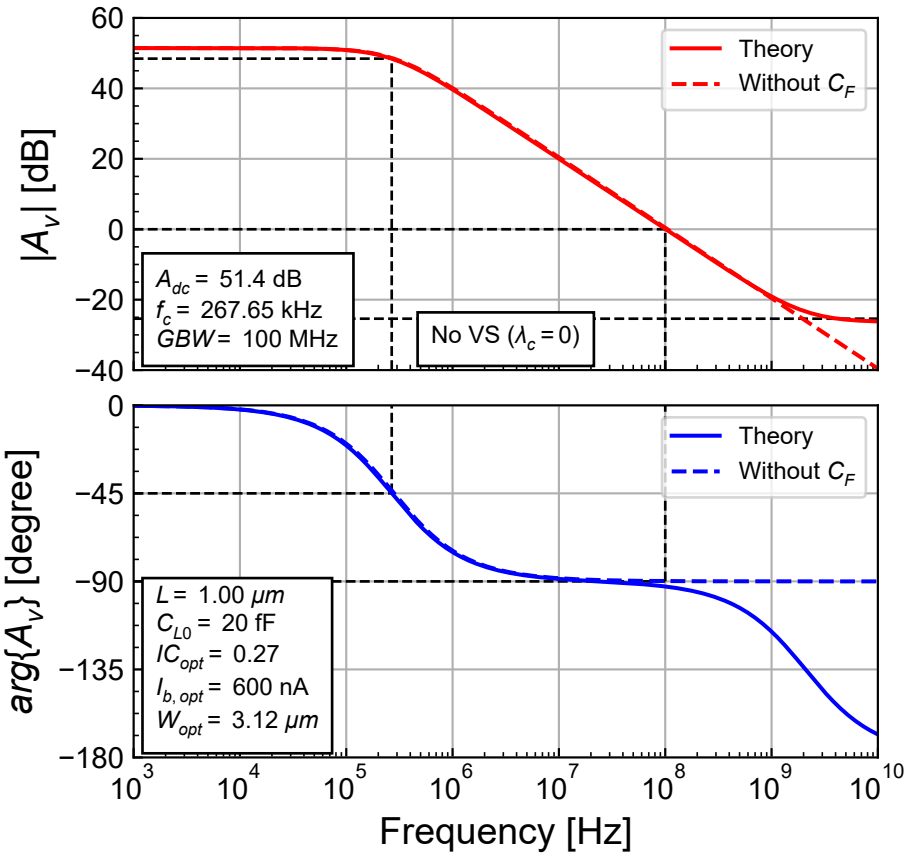

Figure 5.7: Theoretical transfer function.

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 5.8.

Table 5.8: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
in	0.443473
out	0.443473
1	0.443473
2	0.443473

Table 5.9: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[nA]$	I_{spec} $[nA]$	IC	n	V_{Dsat} $[mV]$
M1	600	2459	0.244	1.27	129
M2	600	2459	0.244	1.27	129

Table 5.10: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[nA/V]$
M1	1.27	19.197	14.898	4.265	34.556

Table 5.10: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[nA/V]$
M2	1.27	19.197	14.898	4.265	34.556

The large-signal transistor bias information and the small-signal parameters extracted from the simulation are given in Table 5.9 and Table 5.10, respectively. We see that their values are very close to the theoretical values given in Table 5.6 and Table 5.7.

The simulated transfer function is shown in Figure 5.8 and compared to the theoretical transfer function of Figure 5.7.

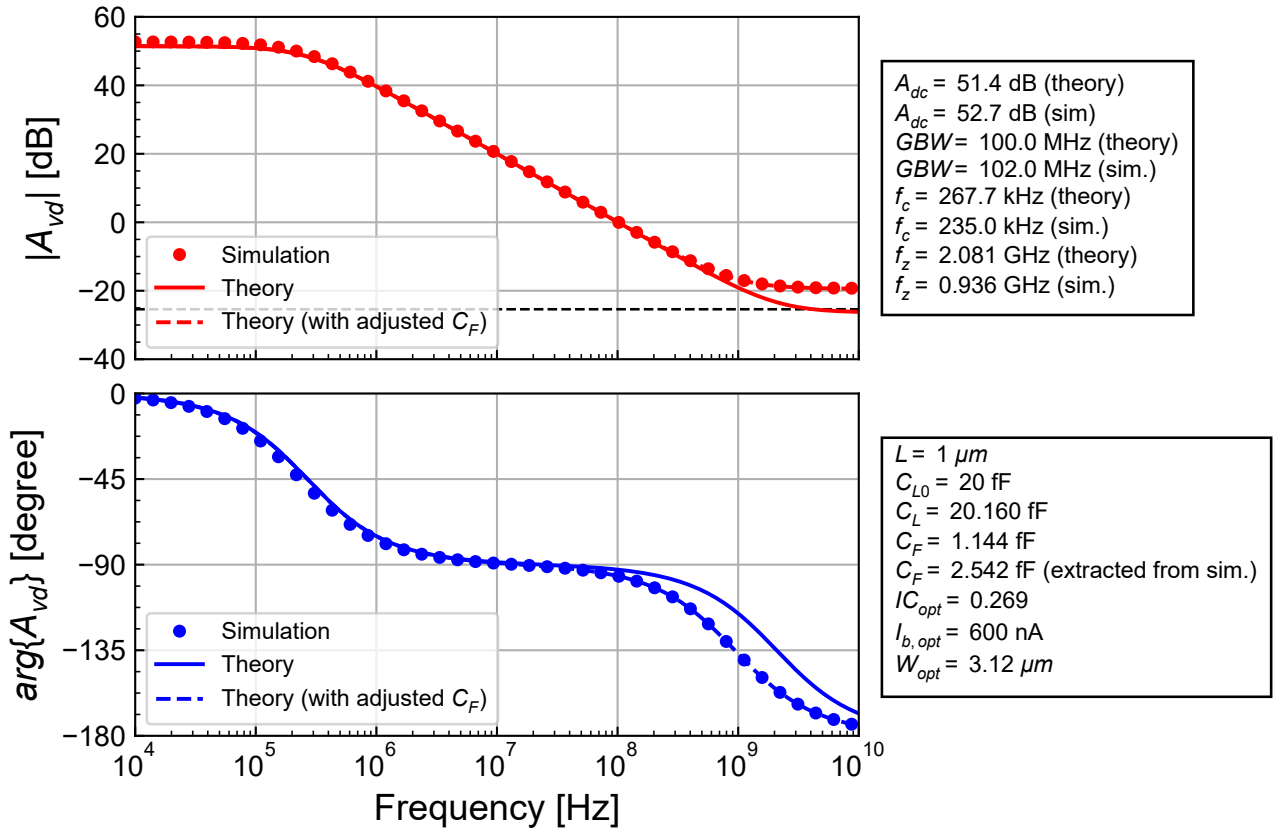

Figure 5.8: Simulated gain response compared to theoretical estimation.

From Figure 5.8 we see that the simulation matches the theoretical estimation very well, at least below the GBW. The simulated GBW and DC gain are slightly higher than the target. We observe a discrepancy at higher frequency with a simulated zero that is about two times lower than the theoretical estimation. This is due to a larger feedback capacitance. This is actually coming from the fact that we have assumed that the feedback capacitance was only due to the extrinsic capacitance, namely the overlap capacitance and we have neglected the intrinsic gate-to-drain capacitance C_{GDi} because we are in saturation. However, for a long and large transistor, the intrinsic capacitance C_{GDi} is not completely negligible even if the transistor is biased in saturation, making the total feedback capacitance larger and the zero frequency.

6 Minimum current for a given gain-bandwidth product including self-loading (short-channel)

To get the minimum current for a short-channel transistor, we simply replace the g_{ms} function by its short-channel version introducing the λ_c velocity saturation parameter and given by

$$g_{ms} = \frac{\sqrt{3IC + 1 + (\lambda_c\, IC)^2} - 1}{2 + \lambda_c^2\, IC} \tag{6.1}$$

with $\lambda_c = L_{sat}/L$. Unfortunately there is no closed-form solution anymore. However, we can solve the same equation set numerically for finding the minimum bias current $i_{b,opt}$ and the corresponding optimum inversion coefficient IC_{opt}. The normalized current i_b is plotted versus the inversion coefficient IC in Figure 6.1 for a given vlue of Θ and for different values of λ_c. We observe that the minimum current slightly increases and the optimum inversion coefficient slightly decreases. The optimum inversion coeffcient IC_{opt} is plotted versus Θ in Figure 6.2 for different values of λ_c. It shows that the optimum IC for a short-channel device is actually quite close to the long-channel value. This shows that we can use the long-channel expression of IC_{opt} as a first guess and eventually fine tune by simulation.

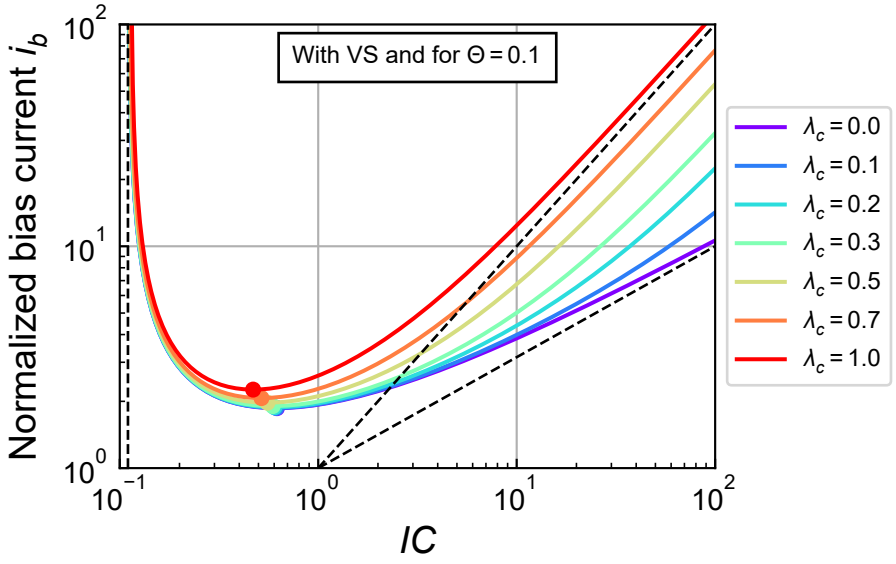

Figure 6.1: Normalized current i_b versus inversion coefficient IC for a short-channel transistor.

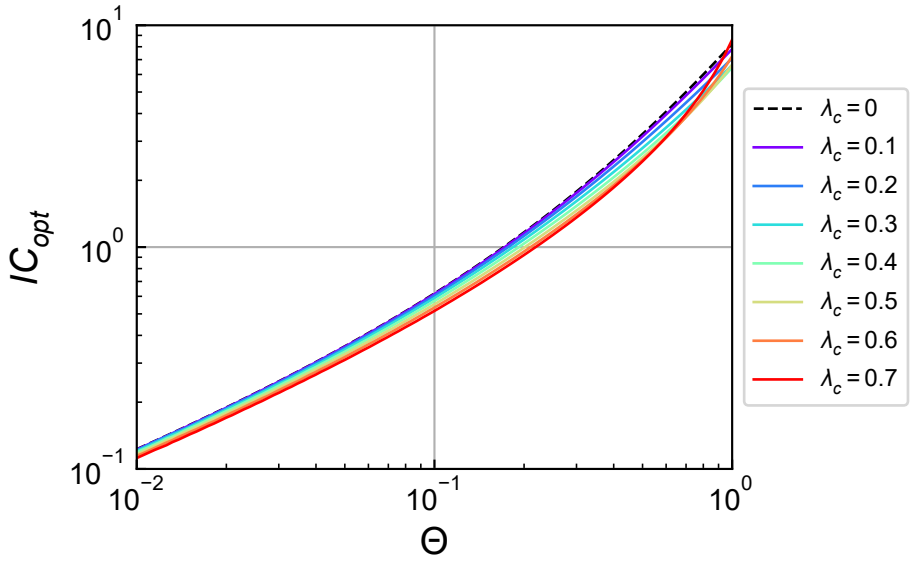

Figure 6.2: Optimum inversion coefficient IC_{opt} versus Θ for a short-channel transistor.

7 Minimum current for given GBW and DC gain

7.1 Analysis

We can actually use the additional degree of freedom, namely the transistor length L (which has been arbitrarily set in the previous example), to set the DC gain. To this purpose we can use the simple output conductance model given by

$$G_{ds} \cong \frac{I_D}{\lambda \cdot L}. \tag{7.1}$$

We now need to solve the following set of equations

$$\omega_u = \frac{G_m}{C_L} = \frac{G_m}{C_{L0} + C_{DW} \cdot W}, \tag{7.2}$$

$$A_{dc} = \frac{G_m}{G_{ds}} = \frac{G_m \cdot \lambda \cdot L}{I_b}, \tag{7.3}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{7.4}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{7.5}$$

for I_b, W, L and G_m. This leads to the following normalized results

$$i_b \triangleq \frac{I_b}{I_{norm}} = \frac{g_{ms} \cdot IC}{g_{ms}^2 - \xi \cdot IC} = \frac{g_{ms}/IC}{(g_{ms}/IC)^2 - \xi/IC}, \tag{7.6}$$

$$w \triangleq \frac{W}{W_{norm}} = \frac{IC}{g_{ms}^2 - \xi \cdot IC}, \tag{7.7}$$

$$\ell \triangleq \frac{L}{L_{norm}} = \frac{IC}{g_{ms}}, \tag{7.8}$$

where

$$\xi \triangleq \frac{C_{DW} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} \cdot A_{dc} \cdot \omega_u, \tag{7.9}$$

$$I_{norm} \triangleq n\, U_T \cdot C_{L0} \cdot \omega_u, \tag{7.10}$$

$$W_{norm} \triangleq \frac{C_{L0} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} \cdot A_{dc} \cdot \omega_u, \tag{7.11}$$

$$L_{norm} \triangleq \frac{nU_T}{\lambda} \cdot A_{dc}. \tag{7.12}$$

The normalized bias current, width and length are plotted in Figure 7.1, Figure 7.2 and Figure 7.3 for different values of the parameter ξ.

Looking at Figure 7.1, we see that there is a minimum for $\xi > 0$. The optimum value of the inversion coefficient IC_{opt} corresponding to this minimum only depends on ξ according to

$$IC_{opt} = \frac{\sqrt{\xi}}{\left(1 - \sqrt{\xi}\right)^2} \tag{7.13}$$

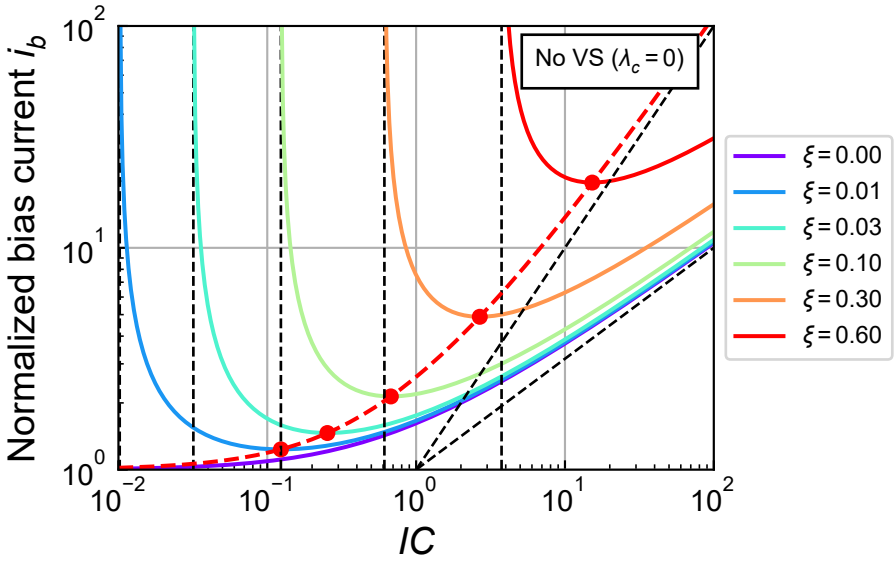

Figure 7.1: Normalized bias current i_b versus inversion coefficient IC for given gain-bandwidth product and DC gain.

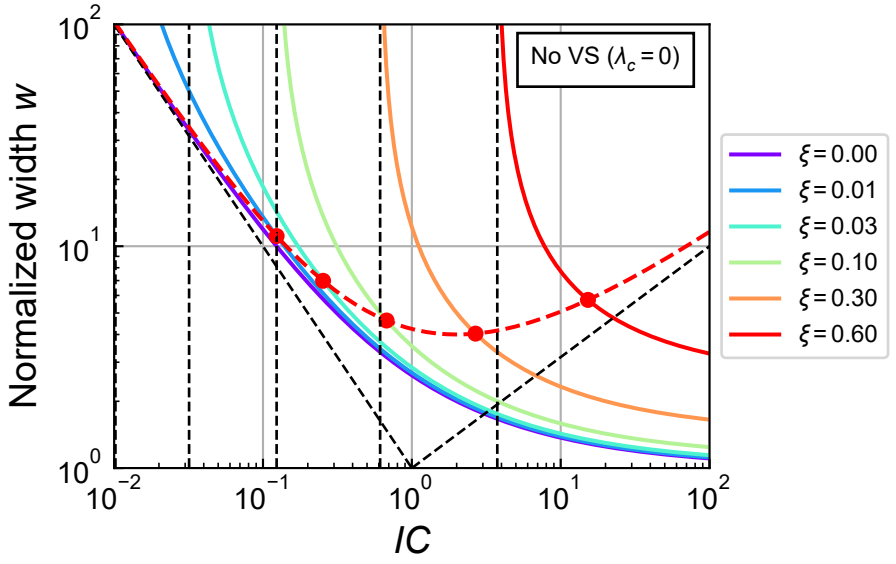

Figure 7.2: Normalized width w versus inversion coefficient IC for given gain-bandwidth product and DC gain.

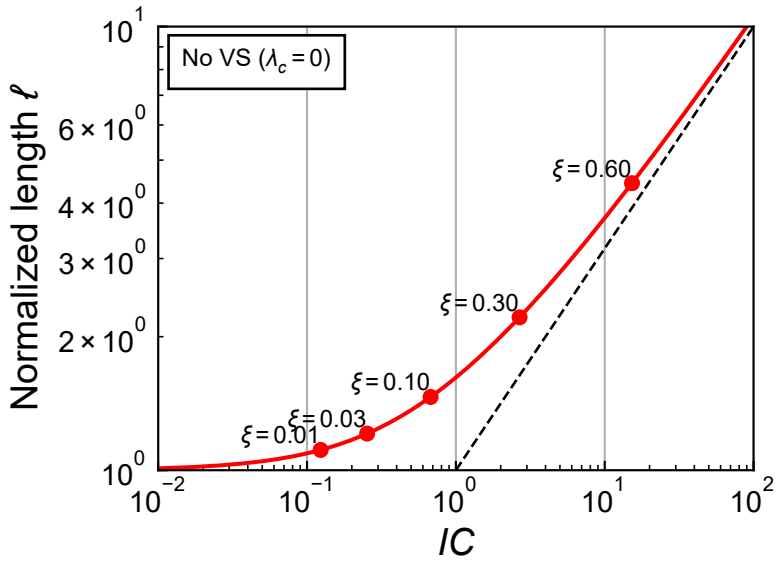

Figure 7.3: Normalized length ℓ versus inversion coefficient IC for given gain-bandwidth product and DC gain.

which is plotted in Figure 7.1 as the dashed red line. The minimum normalized current is then given by

$$i_{b,opt} \triangleq i_b(IC_{opt}) = \frac{1}{\left(1-\sqrt{\xi}\right)^2} = \frac{1+2IC_{opt}+\sqrt{4IC_{opt}+1}}{2}. \tag{7.14}$$

The optimum normalized width, length and transconductance are given by

$$w_{opt} \triangleq w(IC_{opt}) = \frac{1}{\sqrt{\xi}\ \left(1-\sqrt{\xi}\right)} = \frac{1+3IC_{opt}+(1+IC_{opt})\sqrt{4IC_{opt}+1}}{2IC_{opt}}, \tag{7.15}$$

$$\ell_{opt} \triangleq \ell(IC_{opt}) = \frac{1}{1-\sqrt{\xi}} = \frac{1+\sqrt{4IC_{opt}+1}}{2}, \tag{7.16}$$

$$g_{m,opt} \triangleq g_m(IC_{opt}) = \frac{1}{1-\sqrt{\xi}} = \frac{1+\sqrt{4IC_{opt}+1}}{2}. \tag{7.17}$$

Note that the optimum current, width, length and transconductance only depend on ξ which brings together the technology parameters and the specs according to

$$\xi \triangleq \underbrace{\frac{C_{DW}\cdot(nU_T)^2}{I_{spec\square}\cdot\lambda}}_{\text{technology parameters}} \cdot \underbrace{A_{dc}\cdot\omega_u}_{\text{specifications}}. \tag{7.18}$$

The optimum parameters are plotted versus ξ in Figure 7.4. We see that all curves tend to infinity for $\xi \to 1$. We can therefore consider that $\xi = 1$ is an upper bound so that the product of the DC gain A_{dc} times the gain bandwidth ω_u should satisfy the following inequality

$$A_{dc}\cdot\omega_u < \frac{I_{spec\square}\cdot\lambda}{C_{DW}\cdot(nU_T)^2} \tag{7.19}$$

This means that we can check whether the specifications on A_{dc} and ω_u can be achieved for a given technology (i.e. for a set of $I_{spec\square}$, λ and C_{DW}). The closer ξ gets to 1, the larger the required current and size.

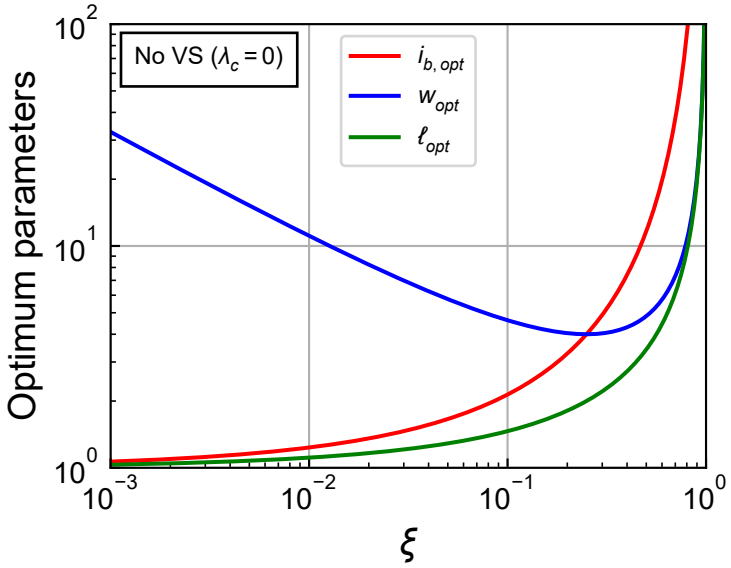

Figure 7.4: Optimum parameters versus ξ.

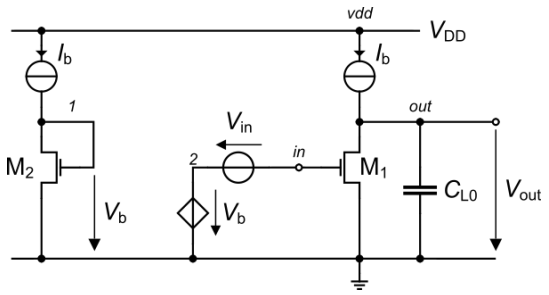

Figure 7.5: Schematic of the open-loop common-source (CS) gain stage used for simulation.

7.2 Design example

We want to size a CS SC amplifier for the specifications given in Table 7.1. We need to find the minimum current and size the transistor to achieve this specs. We will design the amplifier for a generic 180nm bulk CMOS process. The physical parameters are given in Table 5.2, the global process parameters in Table 5.3 and finally the MOSFET parameters in Table 5.4.

Table 7.1: CS SC amplifier specifications.

Specification	Symbol	Value	Unit
Gain bandwidth product	GBW	100	MHz
DC gain	A_{dc}	50	dB
Load capacitance	C_{L0}	20	fF

We can start by checking that the specifications in Table 7.1 are feasible for the given 180nm technology. For this we can check that

$$\xi \triangleq A_{dc} \cdot \omega_u \cdot \frac{C_{DW} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} < 1.$$

For the specifications in Table 7.1 and the chosen 180nm technology we have $\xi = 0.023$ which is much smaller than 1. We can now proceed with the calculation of the parameters including the optimum inversion coefficient, bias current, wodth and length. All the calculated parameters are presented in Table 7.2.

Table 7.2: CS OL amplifier optimum parameters.

Parameter	Value	Unit
C_{DW}	1.167	$fF/\mu m$
C_{D0}	0.16	fF
C_{L0}	20	fF
C_L	20.16	fF
ξ	0.023	-
IC_{opt}	0.213	-
$i_{b,opt}$	1.394	-
w_{opt}	7.72	-
ℓ_{opt}	1.181	-
$g_{m,opt}$	1.181	-
$I_{b,opt}$	581	nA
$(W/L)_{opt}$	3.121	-
I_{norm}	417	nA
W_{norm}	404	nm
L_{norm}	694	nm
$G_{m,norm}$	12.667	$\mu A/V$
$I_{b,opt}$	580.733	nA
W_{opt}	3.12	μm
L_{opt}	818.72	nm
$G_{m,opt}$	14.954	$\mu A/V$
$C_{D,opt}$	3.64	fF
AD	1.25	μm^2
PD	7.04	μm
C_{DBJ}	2.656	fF
C_F	1.144	fF
C_{out}	23.8	fF

Table 7.2: CS OL amplifier optimum parameters.

Parameter	Value	Unit
GBW (check)	100	MHz
f_z	2.081	GHz
A_{dc}	50	dB

From the parameters in Table 7.2 we can now plot the theoretical transfer function which is shown in Figure 7.6 and confirms that the specifications on the DC gain and gain-bandwidth product are met.

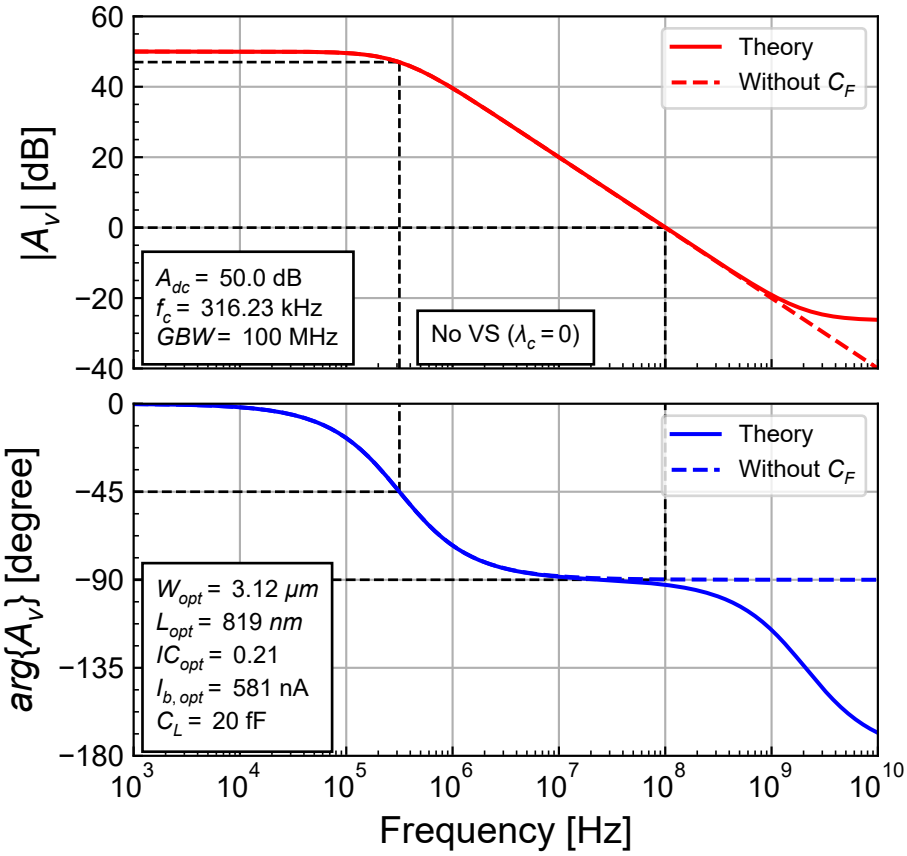

Figure 7.6: Theoretical transfer function.

Table 7.3: Transistor size and bias information.

Transistor	W $[\mu m]$	L $[\mu m]$	I_D $[nA]$	I_{spec} $[nA]$	IC	$V_G - V_{T0}$ $[mV]$	V_{DSsat} $[mV]$
M1	3.12	0.82	581	2725	0.213	-27	106
M2	3.12	0.82	581	2725	0.213	-27	106

Table 7.4: Transistor small-signal and thermal noise parameters.

Transistor	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M1	105.307	19.012	14.954	47.288	0.668
M2	105.307	19.012	14.954	47.288	0.668

The theoretical results can be validated by comparing them to the results obtained from simulations

performed with ngspice. In order to run the simulations you need to have ngspice installed. Please refer to the ngspice instructions.

> **Note**
>
> The simulations are performed with ngspice [1] using the EKV 2.6 compact model [2]. For ngspice, we use the original Verilog-A implementation of EKV 2.6 [3] modified by C. Enz to get the operating point informations and available on the Gitub va-models site provided by D. Warning at [4]. The parameters correspond to a generic 180 nm bulk CMOS process [5].

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 7.5.

Table 7.5: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
in	0.438602
out	0.438602
1	0.438602
2	0.438602

Table 7.6: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[nA]$	I_{spec} $[nA]$	IC	n	V_{Dsat} $[mV]$
M1	581	3073	0.189	1.27	126
M2	581	3073	0.189	1.27	126

Table 7.7: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[nA/V]$
M1	1.27	19.232	14.926	4.264	42.398
M2	1.27	19.232	14.926	4.264	42.398

The large-signal transistor bias information and the small-signal parameters extracted from the operating point simulation are given in Table 7.6 and Table 7.7, respectively. We see that their values are very close to the theoretical values given in Table 7.3 and Table 7.4.

The simulated transfer function is shown in Figure 7.7 and compared to the theoretical transfer function of Figure 7.6.

From Figure 5.8 we see that the simulation matches the theoretical estimation at least below the GBW. The simulated DC gain and GBW are slightly higher than the target. We observe a discrepancy at higher frequency with a simulated zero that is about two times lower than the theoretical estimation. This is due to a larger feedback capacitance. As explained above, this comes the intrinsic C_{GDi} which for a large transistor can not really be neglected despite the transistor is biased in saturation.

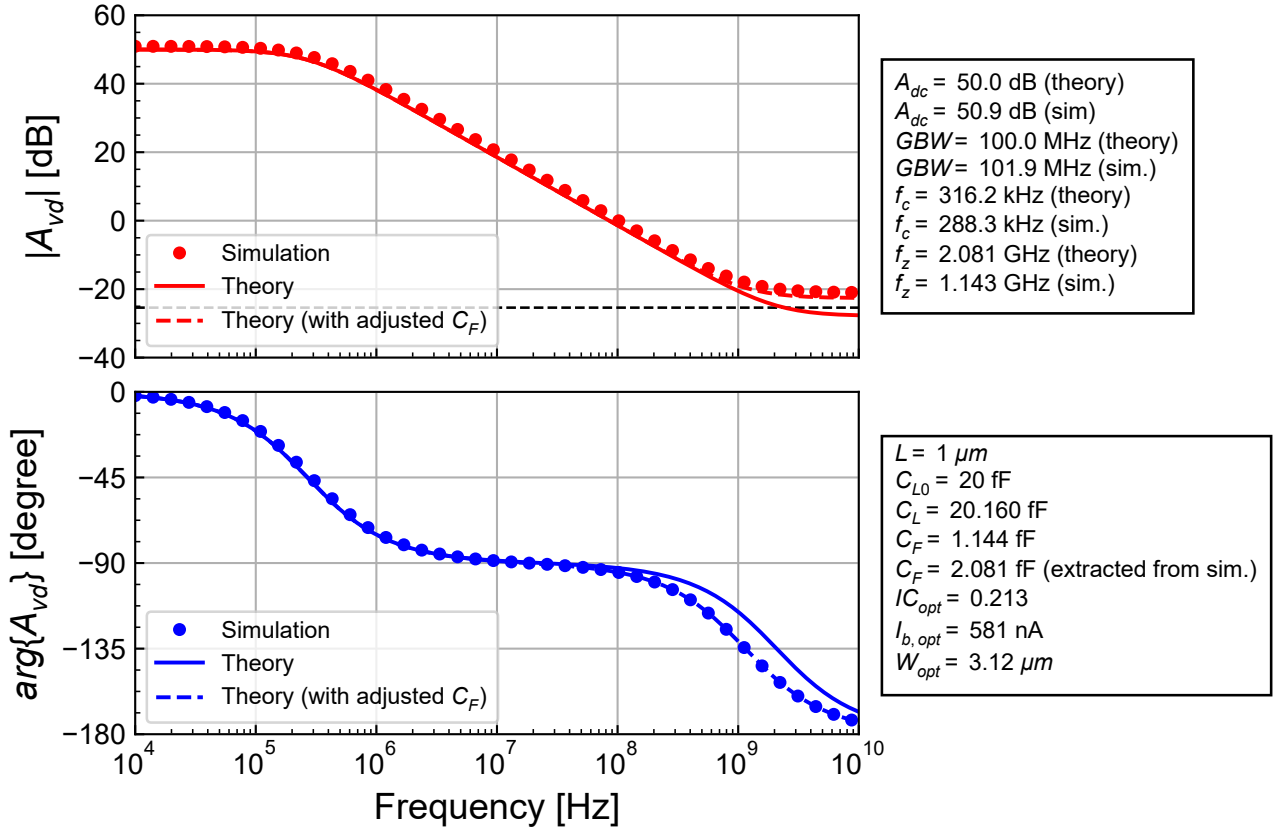

Figure 7.7: Simulated gain response compared to theoretical estimation.

8 Minimum current for a given input-referred thermal noise

In this section we want to answer the following question:

> **Question**
>
> What is the minimum current I_b and transistor size (aspect ratio W/L) in order for the OL CS gain stage to achieve a given input-referred thermal noise resistance?

The input-referred thermal noise resistance is given by

$$R_{n,th} = \frac{\gamma_n}{G_m}$$

For a long-channel transistor, the thermal noise excess factor γ_n can be considered as constant and $R_{n,th}$ decreases with IC as $1/IC$ in WI and $1/\sqrt{IC}$ in SI. However, when velocity saturation (VS) is considered, G_m will saturate in SI and the thermal noise excess factor γ_n increases with IC.

We first will consider the long-channel case (no VS).

8.1 Long-channel (no VS)

In this case the thermal noise excess factor γ_n can be considered as constant.

We then need to solve the following set of equation for I_b and W/L

$$\begin{aligned} R_{n,th} &= \frac{\gamma_n}{G_m}, \\ G_m &= \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \\ I_b &= I_{spec\square} \cdot \frac{W}{L} \cdot IC. \end{aligned}$$

This leads to the following normalized results

$$i_b \triangleq \frac{I_b \cdot R_{n,th}}{nU_T \cdot \gamma_n} = \frac{IC}{g_{ms}}, \tag{8.1}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{I_{spec\square} \cdot R_{n,th}}{nU_T \cdot \gamma_n}. \tag{8.2}$$

With this normalization, the normalized current i_b and aspect ratio AR are identical to the curve of the constant G_m case with $\lambda_c = 0$ shown in Figure 3.1.

8.2 Short-channel case (incl. VS)

When VS is present we need to account for the transconductance saturation in SI given by (6.1) and for the dependence of γ_n to IC which can be approximated by [6]

$$\gamma_n = \gamma_{nwi} \cdot (1 + \alpha_n \cdot IC) \tag{8.3}$$

where γ_{nwi} is normally the noise excess factor in WI given by $\gamma_{nwi} \cong n/2$. However in the empirical model (8.3) it is used as a fitting parameter which turns out to be very close to one. Parameter α_n depends on the VS parameter λ_c according to

$$\alpha_n = \frac{n}{2} \cdot \lambda_c^2. \tag{8.4}$$

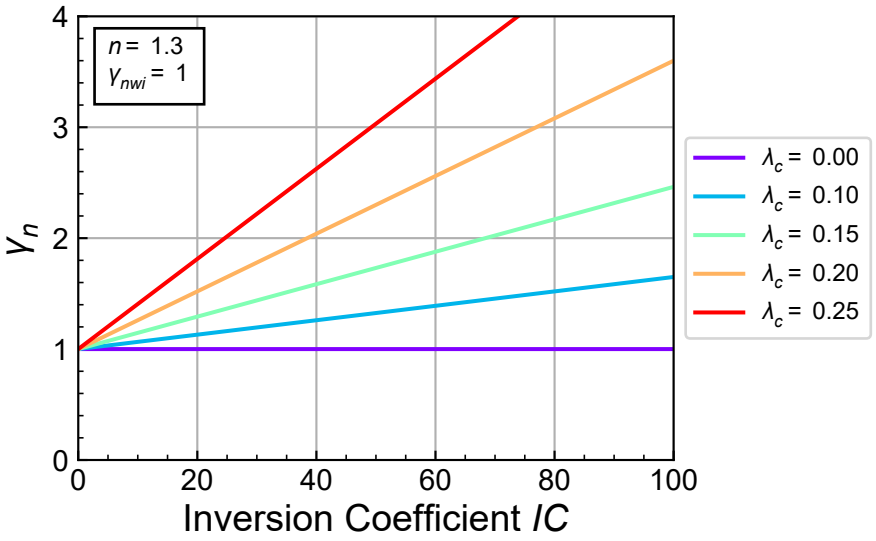

Figure 8.1: Thermal noise excess factor γ_n versus inversion coefficient IC including short-channel effects.

Eqn. (8.3) is plotted versus the inversion coefficient in Figure 8.1 for $n = 1.3$ and for different values of λ_c and hence of α_n.

The normalized input-referred thermal noise resistance can be defined as

$$r_n \triangleq R_{n,th} \cdot G_{spec} = \frac{\gamma_n}{g_m} \tag{8.5}$$

with $g_m \triangleq G_m/G_{spec}$.

To find the current for achieving a given input-referred thermal noise resistance, we need to solve the following set of equations for I_b and W/L

$$R_{nt} = \frac{\gamma_n}{G_m}, \tag{8.6}$$

$$\gamma_n = \gamma_{nwi} \cdot (1 + \alpha_n \cdot IC), \tag{8.7}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{8.8}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC, \tag{8.9}$$

This leads to the following normalized results

$$i_b \triangleq \frac{I_b \cdot R_{n,th}}{nU_T \cdot \gamma_{nwi}} = \frac{IC}{g_{ms}} \cdot (1 + \alpha_n \cdot IC), \tag{8.10}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{I_{spec\square} \cdot R_{n,th}}{nU_T \cdot \gamma_{nwi}} = \frac{1}{g_{ms}} \cdot (1 + \alpha_n \cdot IC). \tag{8.11}$$

i_b is plotted versus IC in Figure 8.2 for various values of λ_c. We see that things have become worse in SI. We need much more current to achieve the same input-referred thermal noise resistance as λ_c increases. As the inversion coefficient increases, the normalized source transconductance saturates to $1/\lambda_c$ and therefore the normalized current increase with IC according to

$$i_b \cong \lambda_c \cdot \alpha_n \cdot IC^2 = \frac{n}{2} \cdot \lambda_c^3 \cdot IC^2. \tag{8.12}$$

For example for $\lambda_c = 0.5$, this means that we need 100 times more current for $IC = 100$ compared to the long-channel case ($\lambda_c = 0$). Clearly, WI gives the smallest bias current. However this leads to a large transistor.

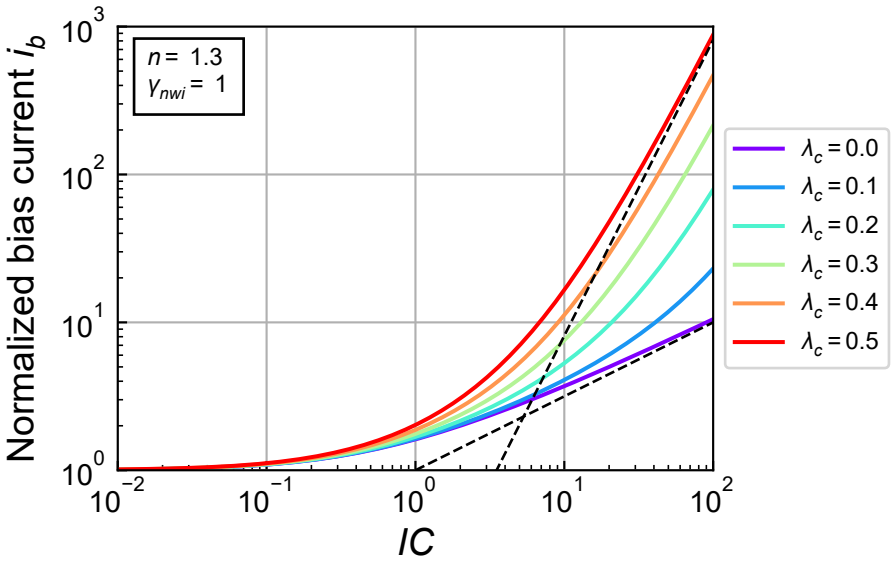

Figure 8.2: Normalized bias current i_b versus inversion coefficient IC.

This can be evaluated by looking at the normalized aspect ratio AR which is plotted versus IC in Figure 8.3 for the same values of λ_c. As for the long-channel case, we see that AR increases as $1/IC$ when moving to WI. In SI and under VS, AR increases instead of decreasing as $1/\sqrt{IC}$ as it does for $\lambda_c = 0$. In SI under VS $1/g_{ms} = \lambda_c$ and hence AR increases as

$$AR \cong \lambda_c \cdot \alpha_n \cdot IC = \frac{n}{2} \cdot \lambda_c^3 \cdot IC. \tag{8.13}$$

We also see that there is a minimum of AR and therefore a minimum width for a given length.

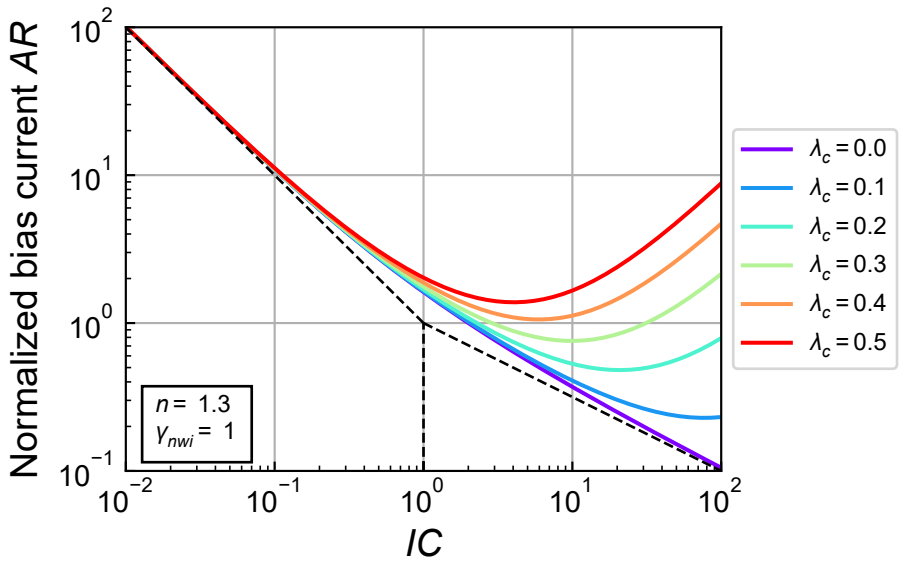

Figure 8.3: Normalized aspect ratio W/L versus inversion coefficient IC.

9 Minimum input-referred thermal noise (short-channel)

> **Note**
>
> Note that in this section we look at the input-referred thermal noise resistance versus the inversion coefficient instead of the bias current for a given input-referred thermal noise resistance.

We have seen that for a short-channel transistor the thermal noise excess factor increases with IC in SI. According to (8.3), in very SI under heavy VS the thermal noise excess factor is given by $\gamma_n \cong \gamma_{wi} \cdot \alpha_n \cdot IC$ and the normalized transconductance g_m saturates to $g_m \cong 1/(n\,\lambda_c)$ so that the normalized thermal noise resistance r_n now increases with IC according to

$$r_n \cong \gamma_{nwi} \cdot \frac{n^2}{2} \cdot \lambda_c^3 \cdot IC \cong \frac{n^2}{2} \cdot \lambda_c^3 \cdot IC \quad \text{in SI and sat.} \tag{9.1}$$

On the other hand, in WI, γ_{nwi} is constant (close to one) and g_m is proportionnal to IC according to $g_m \cong IC/n$. The normalized input-referred white noise resistance decreases with respect to IC improving the noise according to

$$r_n \cong \gamma_{nwi} \frac{n}{IC} \cong \frac{n}{IC} \quad \text{in WI and sat.} \tag{9.2}$$

Since the normalized input-referred white noise resistance r_n decreases as $1/IC$ in WI and inceases as IC in SI, it reaches a minimum in moderate inversion (MI). There is no simple closed form expression of the optimum IC for which r_n reaches a minimum. However we can find an approximation by equating the two asymptotes and solving for IC. This gives an approximate value of the optimum inversion coefficient

$$IC_{opt} \cong \sqrt{\frac{2}{n \cdot \lambda_c^3}}. \tag{9.3}$$

The normalized input-referred thermal noise resistance r_n in saturation is plotted versus the inversion coefficient IC for an nMOS transistor from a 40nm bulk CMOS technology in Figure 9.1. We clearly see that there is a minimum on the upper side of moderate inversion. The estimation of the optimum inversion coefficient is slightly lower than the value corresponding to the effective minimum. However, considering the log scale used for the x-axis and the empiricial model used, this estimation is good enough.

This result is particularly important for RF IC design where white noise is dominating in low-noise amplifiers (LNAs). Note that an additional gate resitance needs to be added to the input-referred noise resistance [7].

Now that we have found the optimum inversion coefficient for achieving a minimum input-referred thermal noise resistance, we can find the corresponding W/L and bias current I_b according to

$$\left.\frac{W}{L}\right|_{opt} = r_{n,min} \cdot \frac{U_T}{R_{n,th}\, I_{spec\square}}, \tag{9.4}$$

$$I_b = I_{spec\square} \cdot \left.\frac{W}{L}\right|_{opt} \cdot IC_{opt} = r_{n,min} \cdot \frac{U_T}{R_{n,th}} \cdot IC_{opt}. \tag{9.5}$$

where $r_{n,min} = r_n(IC_{opt})$.

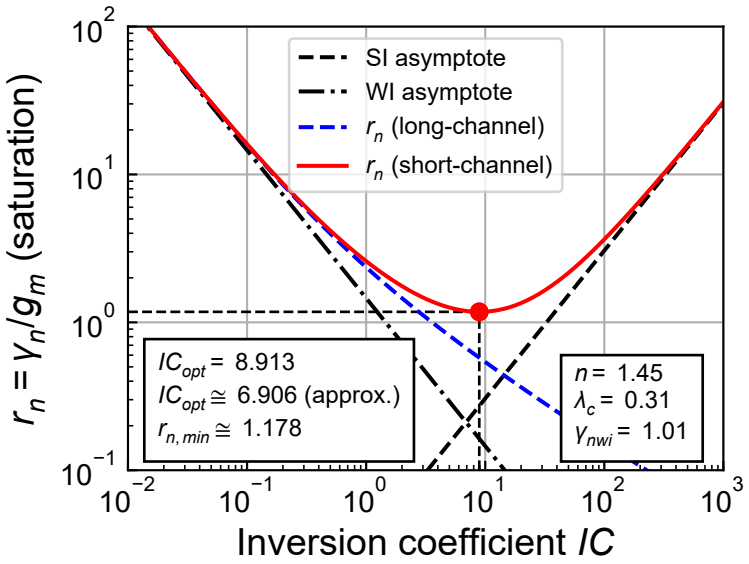

Figure 9.1: Normalized input-referred thermal noise resistance versus IC including VS.

> **Note**
>
> The fact that the input-referred thermal noise resistance (or white noise power spectral density or PSD) gets minimum for an optimum value of the inversion coefficient often located on the upper side of moderate inversion does not mean that it is achieved with a minimum bias current. It simply means that for a given current budget, we can find an optimum value of the inversion coefficient for which the input-referred thermal noise resistance gets minimum.

10 Minimum of F_{min} (short-channel)

It can be shown that the minimum noise factor accounting for the effects of the gate resistance and the induced-gate noise (but without the correlation) can be approximated by [7]

$$F_{min} \cong 1 + 2\frac{\gamma_n}{G_m}\,\omega\, C_{GS}\,\sqrt{\alpha_G + b_n}, \tag{10.1}$$

where C_{GS} is the gate-to-source capacitance, $b_n = 2/(5n^2)$ and α_G is the thermal noise contribution of the gate resistance normalized to that of the channel

$$\alpha_G \triangleq \frac{R_G}{\gamma_n/G_m}. \tag{10.2}$$

In RF we often use minimum length devices. In this case the gate-to-source capacitance is dominated by the extrinsic capacitance made of the overlap and fringing field capacitances. It scales with the width according to $C_{GS} \cong W \cdot C_{GeW}$ where C_{GeW} is the total extrinsic capacitance per unit width. We can then rewrite the minimum noise factor as

$$F_{min} \cong 1 + 2\frac{\gamma_n}{g_{ms}}\,\frac{\omega}{\omega_n}\,\sqrt{\alpha_G + b_n} \tag{10.3}$$

where

$$\omega_n \triangleq \frac{I_{spec\square}}{nU_T\, L_f\, C_{GeW}} \tag{10.4}$$

The minimum noise figure NF_{min} is plotted versus IC in Figure 10.1 for two different operating frequencies in the case of an nMOS transistor from a 40nm bulk CMOS process. The transistor is rather large since it is made of $M = 10$ devices with $N_f = 10$ fingers and a finger width $W_f = 1.8\,\mu m$ and a finger length $L_f = 40\,nm$. We clearly see the minimum which occurs for the same value of IC than the input-referred thermal noise resistance. The larger the frequency the larger the minimum figure.

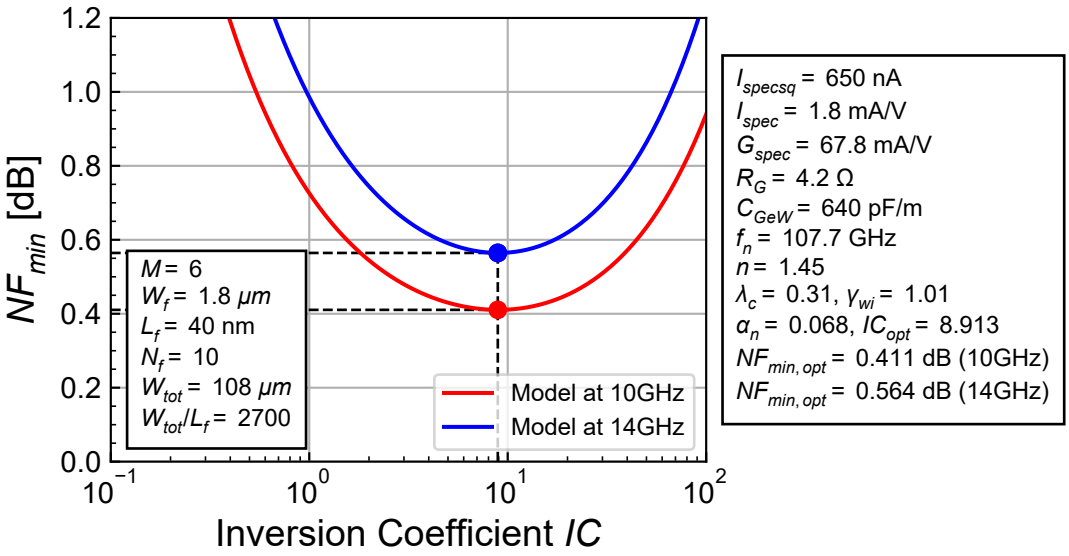

Figure 10.1: Minimum noise figure

11 Conclusion

In this notebook we have analyzed the basic common-source (CS) gain stage in open-loop (OL) configuration. We started by looking at the minimum current for achieving a given transconductance and gain-bandwidth product with a constant load capacitance, which turns out to be in weak inversion. Then we accounted for the self-loading capacitance at the drain which introduces a minimum in the bias current for achieving a given gain-bandwidth product for a given transistor length. We then used the additional degree of freedom, namely the transistor length, for at the time also achieving a given DC gain. We have shown that there is an optimum inversion coefficient leading to a minimum current for achieving at the same time a given DC gain and gain-bandwidth product. The theory was then illustrated by an example designed for a 180nm generic technology. The results have been validated by simulation with ngspice [1] using the EKV 2.6 compact model [2] [3].

We then looked at the bias current required for achieving a given input-referred thermal noise resistance, which again turns out to be in weak inversion. We also have seen that, for short-channel transistors, the required current increases significantly in strong inversion compared to the long-channel case because of the effect of velocity saturation.

Finally, we had a look at the input-referred thermal noise resistance versus the inversion coefficient for a short-channel device. We discovered that there is an optimum inversion coefficient for which the input-referred thermal noise resistance bcomes minimum. Similarly, we also have shown that there is an optimum inversion coefficient for which the minimum noise factor becomes minimum for a short-channel transistor at a given operating frequency.

> **Note**
>
> Note that CS gain stages are seldom used in open-loop configuration. They usually include some feedback such as a feedback capacitor like in switched-capacitor circuits. The above theory is extended in another notebook to a closed-loop gain stage with capacitive feedback.

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