Common-source Stage Optimization using the Inversion Coefficient

Input-referred white noise optimization (Version 1)

Christian Enz (christian.enz@epfl.ch)

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1 Introduction

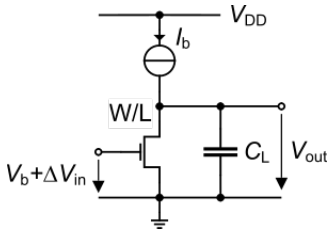

Figure 1.1: Schematic of the open-loop common-source (CS) gain stage.

The schematic of the common-source (CS) stage in open-loop configuration is shown in Figure 1.1. To size the transistor according to some specifications on the gain, bandwidth or noise, we need to find the bias current I_b and the aspect ratio W/L that satisfies the given specifications. In order to do this, we first need to analyze the circuit in terms of its key features. We will start with a small-signal analysis.

2 Small-signal analysis

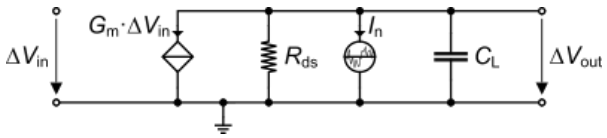

Figure 2.1: Small-signal schematic of the open-loop (OL) common-source (CS) gain stage including its noise source.

The small-signal schematic of the open-loop (OL) common-source (CS) stage is shown in Figure 2.1. Ignoring the noise source I_n, it is straightforward to show that the transfer function is given by

$$A(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = A_{dc} \cdot \frac{1}{1 + s/\omega_p}$$

where

$$A_{dc} = -G_m \cdot R_{ds},$$
$$\omega_p = \frac{R_{ds}}{C_L}.$$

$A_{dc} = -G_m \cdot R_{ds}$ is the DC voltage gain and ω_p the pole. The gain-bandwidth product (GBW)or unity gain frequency (ω_u)is then given by

$$GBW = \omega_u = |A_{dc}| \cdot \omega_p = \frac{G_m}{C_L}.$$

The transfer function magnitude is plotted in Figure 2.2.

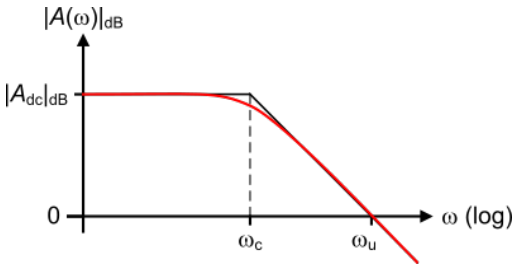

Figure 2.2: Small-signal transfer function of the OL CS amplifier.

3 Minimum current for a given transconductance

In this section we want to answer the following question:

> **Question**
>
> What is the minimum current I_b and transistor size (aspect ratio W/L) in order for the OL CS gain stage to achieve a given transconductance?

To answer this question we first rewrite the current as [1] [2] [3]

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC \tag{3.1}$$

and the transconductance as

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{3.2}$$

where $g_{ms}(IC)$ is the normalized source transconductance which only depends on IC according to [1] [2] [3]

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = \frac{n\,G_m}{G_{spec}} = \frac{\sqrt{4IC+1}-1}{2} \tag{3.3}$$

for a long-channel transistor and [1] [2] [3]

$$g_{ms} = \frac{\sqrt{4IC+1+(\lambda_c\,IC)^2}-1}{2+\lambda_c^2\,IC} \tag{3.4}$$

for a short-channel transistor accounting for velocity saturation with parameter λ_c. Note that, according to (3.4), g_{ms} saturates to $1/\lambda_c$ in very strong inversion.

We then need to solve the following set of equation for I_b and W/L

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{3.5}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{3.6}$$

This leads to the following normalized results

$$i_b \triangleq \frac{I_b}{G_m \cdot nU_T} = \frac{IC}{g_{ms}}, \tag{3.7}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{I_{spec\square}}{G_m \cdot nU_T} = \frac{1}{g_{ms}}. \tag{3.8}$$

i_b and AR are plotted below for various values of λ_c

From Figure 3.1, we see that we can reduce the current i_b when moving from strong inversion (SI) to moderate inversion (MI) reaching a minimum in weak inversion (WI). The loss of transconductance resulting from a reduction of IC is compensated by an increase of W/L as shown by the blue curves, resulting in a very large transistor and a drastic area increase. Moderate inversion turns out to be a good trade-off between low current and acceptable area for achieving a given transconductance.

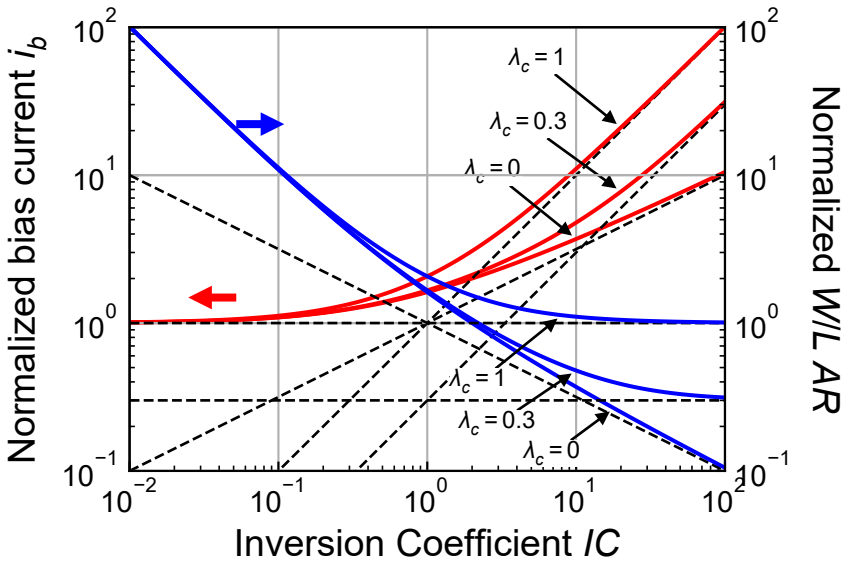

Figure 3.1: Normalized bias current i_b and aspect ratio AR versus inversion coefficient IC.

4 Minimum current for a given input-referred thermal noise

In this section we want to answer the following question:

> **Question**
>
> What is the minimum current I_b and transistor size (aspect ratio W/L) in order for the OL CS gain stage to achieve a given input-referred thermal noise resistance?

The input-referred thermal noise resistance is given by

$$R_{n,th} = \frac{\gamma_n}{G_m}$$

For a long-channel transistor, the thermal noise excess factor γ_n is constant and $R_{n,th}$ decreases with IC, as $1/IC$ in WI and $1/\sqrt{IC}$ in SI. However, when velocity saturation (VS) is considered, G_m will saturate in SI and the thermal noise excess factor γ_n increases with IC.

We first will consider the long-channel case (no VS).

4.1 Long-channel (no VS)

In this case the thermal noise excess factor γ_n can be considered as constant.

We then need to solve the following set of equation for I_b and W/L

$$\begin{aligned} R_{n,th} &= \frac{\gamma_n}{G_m}, \\ G_m &= \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \\ I_b &= I_{spec\square} \cdot \frac{W}{L} \cdot IC. \end{aligned}$$

This leads to the following normalized results

$$i_b \triangleq \frac{I_b \cdot R_{n,th}}{nU_T \cdot \gamma_n} = \frac{IC}{g_{ms}}, \tag{4.1}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{I_{spec\square} \cdot R_{n,th}}{nU_T \cdot \gamma_n}. \tag{4.2}$$

With this normalization, the normalized current i_b and aspect ratio AR are identical to the curve of the constant G_m case with $\lambda_c = 0$ shown in Figure 3.1.

4.2 Short-channel case (incl. VS)

When VS is present we need to account for the transconductance saturation in SI given by (3.4) and for the dependence of γ_n to IC which can be approximated by [4]

$$\gamma_n = \gamma_{nwi} \cdot (1 + \alpha_n \cdot IC) \tag{4.3}$$

where γ_{nwi} is normally the noise excess factor in WI given by $\gamma_{nwi} \cong n/2$. However in the empirical model (4.3) it is used as a fitting parameter which turns out to be very close to one. Parameter α_n depends on the VS parameter λ_c according to

$$\alpha_n = \frac{n}{2} \cdot \lambda_c^2. \tag{4.4}$$

The normalized input-referred thermal noise resistance can be defined as

$$r_n \triangleq R_{n,th} \cdot G_{spec} = \frac{\gamma_n}{g_m} \tag{4.5}$$

with $g_m \triangleq G_m/G_{spec}$.

To find the current for achieving a given input-referred thermal noise resistance, we need to solve the following set of equations for I_b and W/L

$$R_{nt} = \frac{\gamma_n}{G_m}, \tag{4.6}$$

$$\gamma_n = \gamma_{nwi} \cdot (1 + \alpha_n \cdot IC), \tag{4.7}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{4.8}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC, \tag{4.9}$$

This leads to the following normalized results

$$i_b \triangleq \frac{I_b \cdot R_{n,th}}{nU_T \cdot \gamma_{nwi}} = \frac{IC}{g_{ms}} \cdot (1 + \alpha_n \cdot IC), \tag{4.10}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{I_{spec\square} \cdot R_{n,th}}{nU_T \cdot \gamma_{nwi}} = \frac{1}{g_{ms}} \cdot (1 + \alpha_n \cdot IC). \tag{4.11}$$

i_b is plotted versus IC in Figure 4.1 for various values of λ_c. We see that things have become worse in SI. We need much more current to achieve the same input-referred thermal noise resistance as λ_c increases. As the inversion coefficient increases, the normalized source transconductance saturates to $1/\lambda_c$ and therefore the normalized current increase with IC according to

$$i_b \cong \lambda_c \cdot \alpha_n \cdot IC^2 = \frac{n}{2} \cdot \lambda_c^3 \cdot IC^2. \tag{4.12}$$

For example for $\lambda_c = 0.5$, this means that we need 100 times more current for $IC = 100$ compared to the long-channel case ($\lambda_c = 0$). Clearly, WI gives the smallest bias current. However this leads to a large transistor.

This can be evaluated by looking at the normalized aspect ratio AR which is plotted versus IC in Figure 4.2 for the same values of λ_c. As for the long-channel case, we see that AR increases as $1/IC$ when moving to WI. In SI and under VS, AR increases instead of decreasing as $1/\sqrt{IC}$ as it does for $\lambda_c = 0$. In SI under VS $1/g_{ms} = \lambda_c$ and hence AR increases as

$$AR \cong \lambda_c \cdot \alpha_n \cdot IC = \frac{n}{2} \cdot \lambda_c^3 \cdot IC. \tag{4.13}$$

We also see that there is a minimum of AR and therefore a minimum width for a given length.

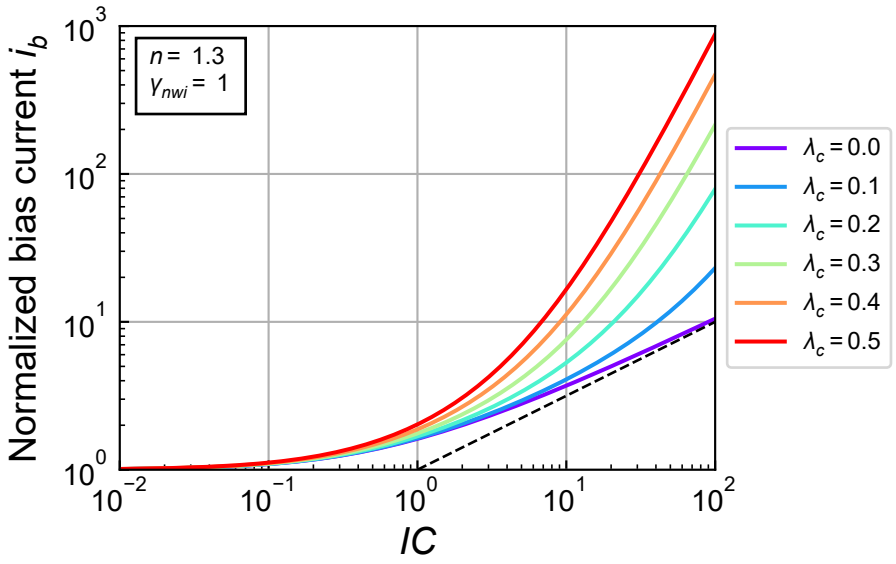

Figure 4.1: Normalized bias current i_b versus inversion coefficient IC.

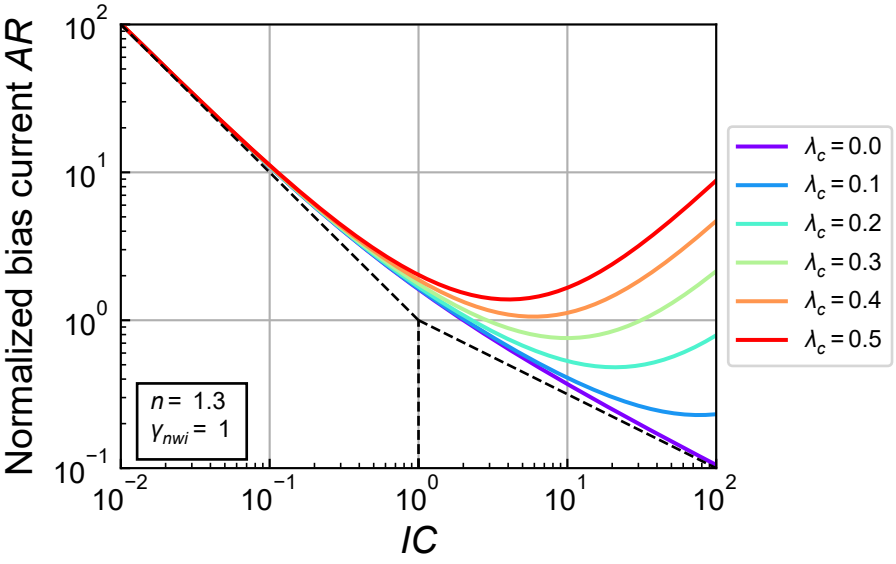

Figure 4.2: Normalized aspect ratio W/L versus inversion coefficient IC.

5 Minimum input-referred thermal noise (short-channel)

We have seen that for a short-channel transistor the thermal noise excess factor increases with IC in SI. According to (4.3), in very SI under heavy VS the thermal noise excess factor is given by $\gamma_n \cong \gamma_{wi} \cdot \alpha_n \cdot IC$ and the normalized transconductance g_m saturates to $g_m \cong 1/(n\,\lambda_c)$ so that the normalized thermal noise resistance r_n now increases with IC according to

$$r_n \cong \gamma_{nwi} \cdot \frac{n^2}{2} \cdot \lambda_c^3 \cdot IC \cong \frac{n^2}{2} \cdot \lambda_c^3 \cdot IC \quad \text{in SI and sat.} \tag{5.1}$$

On the other hand, in WI, γ_{nwi} is constant (close to one) and g_m is proportionnal to IC according to $g_m \cong IC/n$. The normalized input-referred white noise resistance decreases with respect to IC improving the noise according to

$$r_n \cong \gamma_{nwi} \frac{n}{IC} \cong \frac{n}{IC} \quad \text{in WI and sat.} \tag{5.2}$$

Since the normalized input-referred white noise resistance r_n decreases as $1/IC$ in WI and inceases as IC in SI, it reaches a minimum in moderate inversion (MI). There is no simple closed form expression of the optimum IC for which r_n reaches a minimum. However we can find an approximation by equating the two asymptotes and solving for IC. This gives an approximate value of the optimum inversion coefficient

$$IC_{opt} \cong \sqrt{\frac{2}{n \cdot \lambda_c^3}}. \tag{5.3}$$

The normalized input-referred thermal noise resistance r_n in saturation is plotted versus the inversion coefficient IC for an nMOS transistor from a 40nm bulk CMOS technology in Figure 5.1. We clearly see that there is a minimum on the upper side of moderate inversion. The estimation of the optimum inversion coefficient is slightly lower than the value corresponding to the effective minimum. However, considering the log scale used for the x-axis and the empiricial model used, this estimation is good enough.

This result is particularly important for RF IC design where white noise is dominating in low-noise amplifiers (LNAs). Note that an additional gate resitance needs to be added to the input-referred noise resistance [1].

Now that we have found the optimum inversion coefficient for achieving a minimum input-referred thermal noise resistance, we can find the corresponding W/L and bias current I_b according to

$$\left.\frac{W}{L}\right|_{opt} = r_{n,min} \cdot \frac{U_T}{R_{n,th}\, I_{spec\square}}, \tag{5.4}$$

$$I_b = I_{spec\square} \cdot \left.\frac{W}{L}\right|_{opt} \cdot IC_{opt} = r_{n,min} \cdot \frac{U_T}{R_{n,th}} \cdot IC_{opt}. \tag{5.5}$$

where $r_{n,min} = r_n(IC_{opt})$.

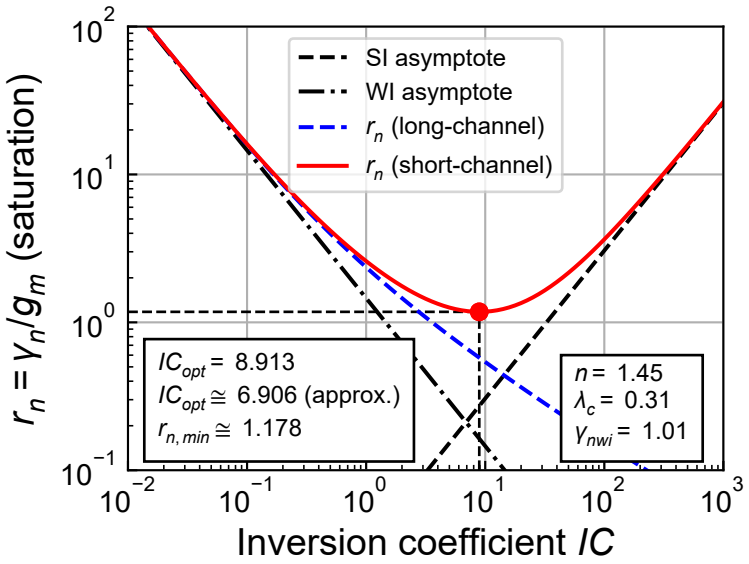

Figure 5.1: Normalized input-referred thermal noise resistance versus IC including VS.

> **Note**
>
> The fact that the input-referred thermal noise resistance (or white noise power spectral density or PSD) gets minimum for an optimum value of the inversion coefficient often located on the upper side of moderate inversion does not mean that it is achieved with a minimum bias current. It simply means that for a given current budget, we can find an optimum value of the inversion coefficient for which the input-referred thermal noise resistance gets minimum.

6 Minimum of F_{min} (short-channel)

It can be shown that the minimum noise factor accounting for the effects of the gate resistance and the induced-gate noise (but without the correlation) can be approximated by [1]

$$F_{min} \cong 1 + 2\frac{\gamma_n}{G_m}\,\omega\, C_{GS}\,\sqrt{\alpha_G + b_n}, \tag{6.1}$$

where C_{GS} is the gate-to-source capacitance, $b_n = 2/(5n^2)$ and α_G is the thermal noise contribution of the gate resistance normalized to that of the channel

$$\alpha_G \triangleq \frac{R_G}{\gamma_n/G_m}. \tag{6.2}$$

In RF we often use minimum length devices. In this case the gate-to-source capacitance is dominated by the extrinsic capacitance made of the overlap and fringing field capacitances. It scales with the width according to $C_{GS} \cong W \cdot C_{GeW}$ where C_{GeW} is the total extrinsic capacitance per unit width. We can then rewrite the minimum noise factor as

$$F_{min} \cong 1 + 2\frac{\gamma_n}{g_{ms}}\,\frac{\omega}{\omega_n}\,\sqrt{\alpha_G + b_n} \tag{6.3}$$

where

$$\omega_n \triangleq \frac{I_{spec\square}}{nU_T\, L_f\, C_{GeW}} \tag{6.4}$$

The minimum noise figure NF_{min} is plotted versus IC in Figure 6.1 for two different operating frequencies in the case of an nMOS transistor from a 40nm bulk CMOS process. The transisor is rather large since it is made of $M = 10$ devices with $N_f = 10$ fingers and a finger width $W_f = 1.8\,\mu m$ and a finger length $L_f = 40\,nm$. We clearly see the minimum which occurs for the same value of IC than the input-referred thermal noise resistance. The larger the frequency the larger the minimum figure.

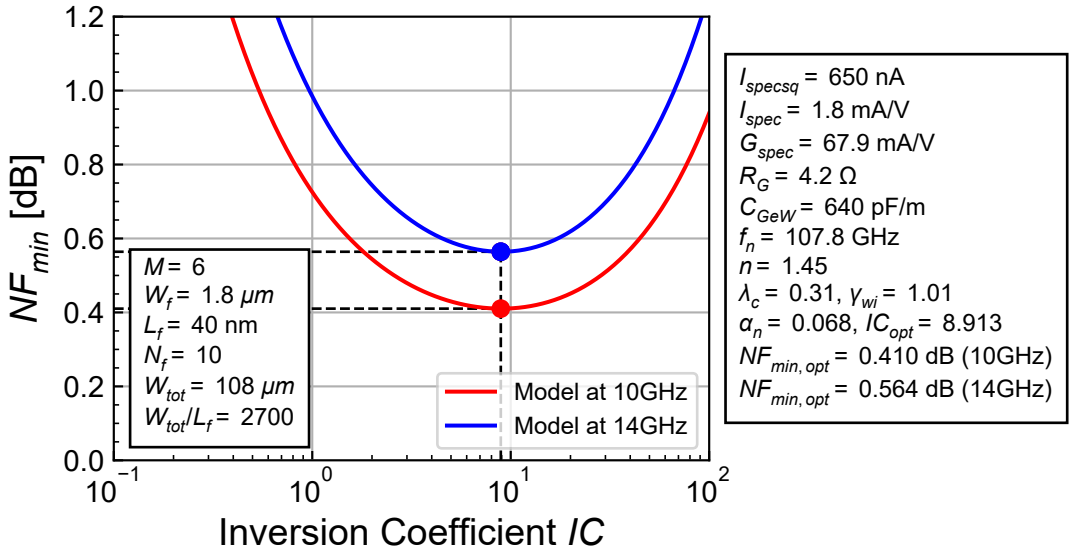

Figure 6.1: Minimum noise figure

7 Conclusion

In this notebook, we have analyzed the input-referred white noise or thermal noise resistance of a common-source nMOS gain stage. We first have investigated what is the minimum bias current for achieving a given input-referred thermal noise resistance. We have seen that the minimum current is achieved in WI at the cost of a larger transistor. The current reduction moving from SI to WI can be significant particularly for short-channel devices. We then have found that, for short-channel devices, there is an optimum inversion coefficient for which the input-referred thermal noise resistance becomes minimum. This does not mean it corresponds to a minimum current, but for a given current budget, choosing this optimum inversion coefficient garanties that we achieve a minimum input-referred thermal noise resistance. Finally, we also have seen that the minimum noise factor reaches a minimum in the upper side of moderate inversion.

References

[1] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design*, 1st ed. John Wiley, 2006.

[2] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 1: The Simplified EKV Model for the Design of Low-Power Analog Circuits," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 3, pp. 26–35, 2017.

[3] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 2: Using the Inversion Coefficient as the Primary Design Parameter," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 4, pp. 73–81, 2017.

[4] C. Enz, "Simple Expression of the Thermal Noise Excess Factor for LNA Design," in *2022 29th IEEE international conference on electronics, circuits and systems (ICECS)*, 2022, pp. 1–4.