Common-source Stage Optimization using the inversion coefficient

In Open-loop Configuration (Version 1)

Christian Enz (christian.enz@epfl.ch)

2025-08-28

Table of contents

1 Introduction

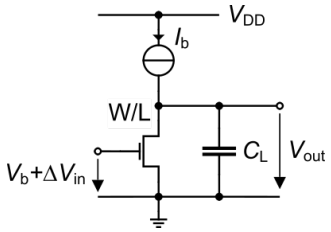

Figure 1.1: Schematic of the open-loop common-source (CS) gain stage.

The schematic of the common-source (CS) stage in open-loop (OL) configuration is shown in Figure 1.1. To size the transistor according to some specifications on the gain, bandwidth or noise, we need to find the bias current I_b and the aspect ratio W/L that satisfies the given specifications. In order to do this, we first need to analyze the circuit in terms of its key features. We will start with a small-signal analysis.

2 Small-signal analysis

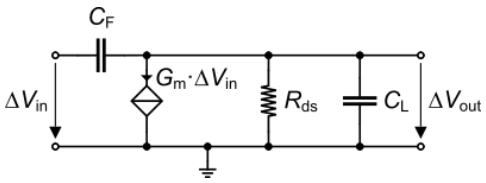

Figure 2.1: Small-signal schematic of the open-loop (OL) common-source (CS) gain stage including the feedback capacitance.

The small-signal schematic of the open-loop (OL) common-source (CS) stage of Figure 1.1 is shown in Figure 2.1. It is straightforward to show that the transfer function is given by

$$A(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = A_{dc} \cdot \frac{1 - s/\omega_z}{1 + s/\omega_p} \tag{2.1}$$

where

$$A_{dc} = -G_m \cdot R_{ds}, \tag{2.2}$$

$$\omega_z = \frac{G_m}{C_F}, \tag{2.3}$$

$$\omega_p = \frac{1}{R_{ds}\, C_{out}}, \tag{2.4}$$

with $A_{dc} = -G_m \cdot R_{ds}$ the DC voltage gain, ω_z the zero (in the right half plan), ω_p the pole and $C_{out} = C_L + C_F$ the total load capacitance at the output node including the feedback capacitance. The gain-bandwidth product (GBW) or unity gain frequency (ω_u) is then given by

$$GBW = \omega_u = |A_{dc}| \cdot \omega_p = \frac{G_m}{C_{out}}. \tag{2.5}$$

As illustrated in Figure 2.2, the gain magnitude at high frequency will settle to

$$\lim_{s \to \infty} A(s) = \frac{C_F}{C_L + C_F}, \tag{2.6}$$

and the phase will turn to -180° because of the positive zero.

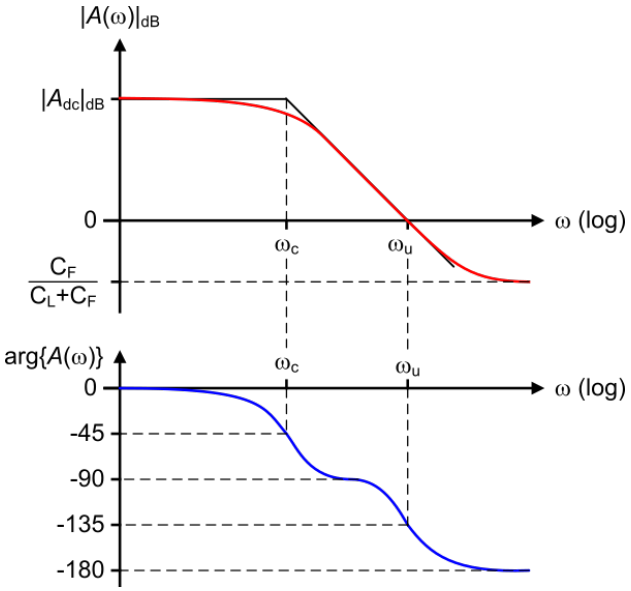

Figure 2.2: Bode plot of the small-signal transfer function of the CS OL amplifier.

3 Minimum current for a given transconductance

In this section we want to answer the following question:

> **Question**
>
> What is the minimum current I_b and transistor size (aspect ratio W/L) in order for the OL CS gain stage to achieve a given transconductance?

To answer this question we first rewrite the current as

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC \tag{3.1}$$

and the transconductance as

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{3.2}$$

where $g_{ms}(IC)$ is the normalized source transconductance which only depends on IC according to

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = \frac{n\,G_m}{G_{spec}} = \frac{\sqrt{4IC+1}-1}{2} \tag{3.3}$$

for a long-channel transistor and

$$g_{ms} = \frac{\sqrt{4IC+1+(\lambda_C\,IC)^2}-1}{2+\lambda_c^2\,IC} \tag{3.4}$$

for a short-channel transistor accounting for velocity saturation with parameter λ_c.

We then need to solve the following set of equation for I_b and W/L

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{3.5}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{3.6}$$

This leads to the following normalized results

$$i_b \triangleq \frac{I_b}{G_m \cdot nU_T} = \frac{IC}{g_{ms}}, \tag{3.7}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{I_{spec\square}}{G_m \cdot nU_T} = \frac{1}{g_{ms}}. \tag{3.8}$$

i_b and AR are plotted below for various values of λ_c

From Figure 3.1, we see that we can reduce the current i_b when moving from strong inversion to moderate inversion reaching a minimum in weak inversion. The loss of transconductance resulting from a reduction of IC is compensated by an increase of W/L as shown by the blue curves, resulting in a very large transistor and a drastic area increase. Moderate inversion turns out to be a good trade-off between low current and acceptable area for achieving a given transconductance.

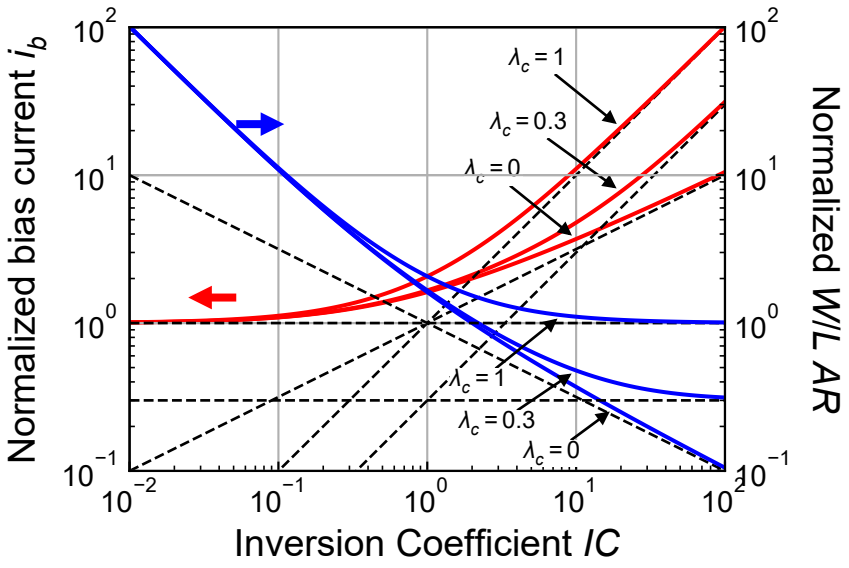

Figure 3.1: Normalized bias current i_b and aspect ratio AR versus inversion coefficient IC.

4 Minimum current for a given gain-bandwidth product (no self-loading)

We now will answer the question:

> **Question**
>
> What is the minimum bias current to achieve a given gain-bandwidth product for a given load capacitance neglecting the effect of self-loading?

We first rewrite the gain-bandwidth as

$$\omega_u = \frac{G_m}{C_L} = \omega_L \cdot \frac{W}{L} \cdot g_{ms}, \tag{4.1}$$

where

$$\omega_L \triangleq \frac{I_{spec\square}}{nU_T \cdot C_{out}}. \tag{4.2}$$

To answer this question we need to solve the following set of equations for I_b and W/L

$$\omega_u = \omega_L \cdot \frac{W}{L} \cdot g_{ms}, \tag{4.3}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{4.4}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{4.5}$$

Since the load capacitance C_L is assumed constant, the problem is similar to imposing a given transconductance With a slightly different normalization we get the same normalized functions as before

$$i_b \triangleq \frac{I_b}{G_m \cdot nU_T} \cdot \frac{1}{\Omega} = \frac{IC}{g_{ms}}, \tag{4.6}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{1}{\Omega} = \frac{1}{g_{ms}}. \tag{4.7}$$

with

$$\Omega \triangleq \frac{\omega_u}{\omega_L}. \tag{4.8}$$

A different normalization reduces to the same trade-off than constant G_m and hence the normalized bias current i_b and aspect AR are identical to the one plotted in Figure 3.1 for various values of λ_c. Moderate inversion again turns out to be a good trade-off between low current and acceptable area for achieving a given gain-bandwidth product.

When moving to moderate and weak inversion, the transistor can become very large. The parasitic capacitance at the transistor drain can then no more be ignored. We will analyze the impact of self-loading in the next section.

5 Minimum current for a given gain-bandwidth product including self-loading (long-channel)

5.1 Analysis

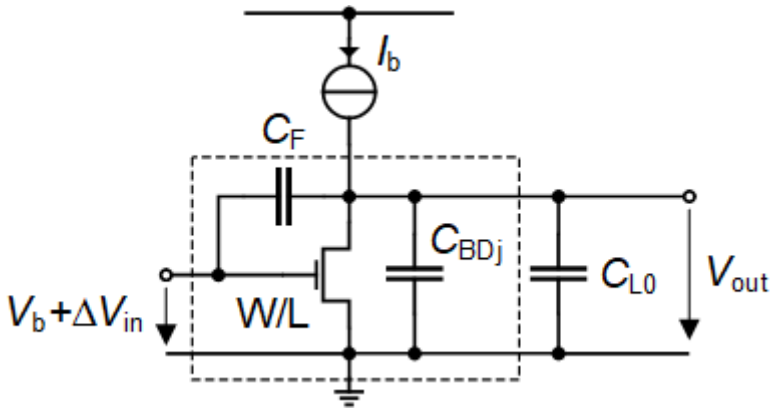

Figure 5.1: Schematic of the open-loop common-source (CS) gain stage including the self-loading capacitances at the drain.

When optimizing the OL CS amplifier for low current consumption, the transistor is often biased in moderate or even weak inversion leading to large transistor and therefore an increased output capacitance due to the self-loading from the parasitic capacitances connected to the drain. As shown in the above figure, the self-loading capacitances include the junction capacitance at the drain C_{BDj} and the feedback capacitance C_F. The junction capacitance C_{BDj} is given by

$$C_{BDj} = 2H_{dif} \cdot W \cdot C_J + 2(2H_{dif} + W) \cdot C_{JSW} = 4H_{dif} \cdot C_{JSW} + 2(H_{dif} \cdot C_J + C_{JSW}) \cdot W \quad (5.1)$$

where C_J is the bottom junction capacitance per area, C_{JSW} is the side-wall capacitance per unit length and H_{dif} is half the minimum diffusion width. Of course the junction capacitances per area and per length C_J and C_{JSW} are bias dependent since they depend on the drain-to-bulk voltage, but we consider their highest value obtained for a zero drain-to-bulk voltage (worst case).

The feedback capacitance is due to the overlap and fringing field capacitance

$$C_F = C_{GDe} \cdot W, \quad (5.2)$$

where C_{GDe} is the extrinsic capacitance per unit width.

The total transistor parasitic capacitance at the drain can then be written as

$$C_D = C_{D0} + C_{DW} \cdot W. \quad (5.3)$$

with

$$C_{D0} = 4H_{dif} \cdot C_{JSW}, \quad (5.4)$$
$$C_{DW} = 2(H_{dif} \cdot C_J + C_{JSW}) + C_{GDe}. \quad (5.5)$$

The part C_{D0} of the total parasitic capacitance at the drain C_D that doesn't scale with W needs to be added to C_{L0}

$$C_L = C_{L0} + C_{D0}. \tag{5.6}$$

In order to achieve a certain bandwidth we need to have a certain transconductance for a certain load capacitance. In order to maximize the current efficiency, we should bias the transistor in weak inversion. This leads to a large transistor and therefore large parasitic capacitances which will impact the bandwidth. Imposing the bandwidth, at some point the capacitance becomes so large that it is no more possible to achieve the required transconductance in weak inversion for the desired bandwidth.

> **Question**
>
> Does this mean that there is a minimum current for the OL CS amplifier to achieve a certain gain-bandwidth product?

To answer this question we need to solve the following set of equations for I_b and W assuming a given length L

$$\omega_u = \frac{G_m}{C_{out}}, \tag{5.7}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{5.8}$$

$$C_{out} = C_L + C_{DW} \cdot W, \tag{5.9}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{5.10}$$

Solving for I_b and W/L leads to the following normalized solutions

$$i_b \triangleq \frac{I_b}{I_{pec\square} \cdot \Omega} = \frac{IC}{g_{ms}(IC) - \Theta}, \tag{5.11}$$

$$AR \triangleq \frac{W/L}{\Omega} = \frac{1}{g_{ms} - \Theta}, \tag{5.12}$$

where

$$\Omega \triangleq \frac{\omega_u}{\omega_L}, \tag{5.13}$$

$$\omega_L \triangleq \frac{I_{spec\square}}{nU_T \cdot C_L}, \tag{5.14}$$

$$\Theta \triangleq \frac{\omega_u}{\omega_W}, \tag{5.15}$$

$$\omega_W \triangleq \frac{I_{spec\square}}{nU_T \cdot C_{DW} \cdot L}. \tag{5.16}$$

The normalized current i_b is plotted in Figure 5.2 versus IC for different values of Θ.

From Figure 5.2, we clearly see that there is a minimum current for a given value of parameter Θ. We can find the optimum inversion coefficient IC_{opt} which is given by

$$IC_{opt} = \left(\sqrt{\Theta \cdot (1+\Theta)} + \Theta + \frac{1}{2}\right)^2 - \frac{1}{4} = 2\Theta \cdot (1+\Theta) + (1+2\Theta) \cdot \sqrt{\Theta \cdot (1+\Theta)}. \tag{5.17}$$

For $\Theta \ll 1$, (5.17) reduces to

$$IC_{opt} \cong 2\Theta + \sqrt{\Theta}. \tag{5.18}$$

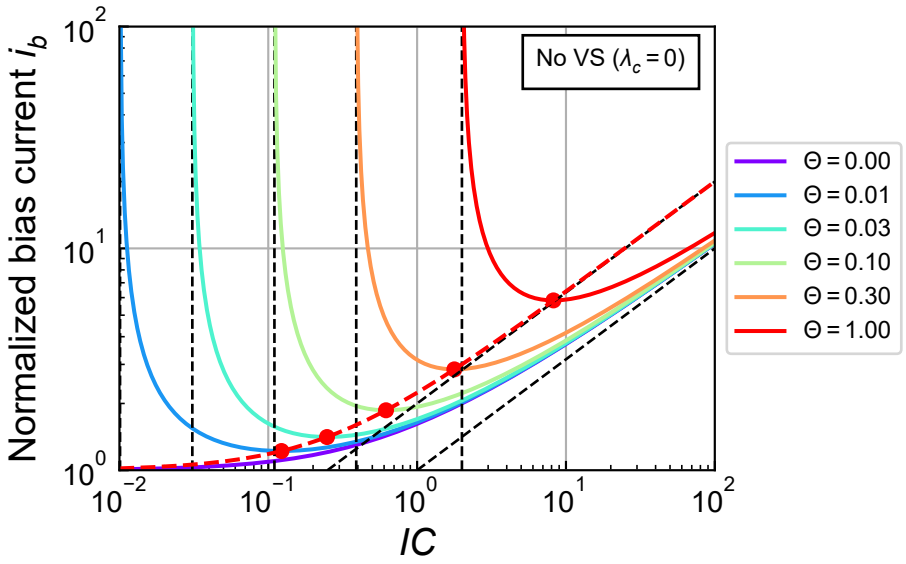

Figure 5.2: Normalized bias current i_b versus inversion coefficient IC.

From the above figure we also see that there is a minimum inversion coefficient IC_{lim} below which the desired gain-bandwidth product GBW can no more be achieved

$$IC_{lim} = \Theta \cdot (1 + \Theta) \cong \Theta, \tag{5.19}$$

which is about equal to Θ for small values of Θ.

The optimum normalized current is given by

$$i_{bopt} \triangleq i_b(IC_{opt}) = 1 + 2\Theta + 2\sqrt{\Theta \cdot (1 + \Theta)}. \tag{5.20}$$

Parameter Θ can be eliminated from equations (5.20) and (5.17) resulting in an expression of i_{opt} in terms of IC_{opt}

$$i_{bopt} = \sqrt{4IC_{opt} + 1} \tag{5.21}$$

which is plotted as a dashed red line in Figure 5.2.

The optimum current also corresponds an optimum transistor width W and hence and optimum normalized W/L given by

$$AR_{opt} \triangleq AR(IC_{opt}) = \frac{1}{\sqrt{\Theta \cdot (1 + \Theta)}}. \tag{5.22}$$

As above, parameter Θ can be eliminated between equations (5.17) and (5.22) giving an expression of AR_{opt} in terms of IC_{opt}

$$AR_{opt} = \frac{\sqrt{4IC_{opt} + 1}}{IC_{opt}}, \tag{5.23}$$

which is plotted as a dashed red line in Figure 5.3.

We see from Figure 5.3 that the transistor width increases first as $1/\sqrt{IC}$ in strong inversion and then as $1/IC$ in weak inversion making the transistor quickly very large until IC reaches IC_{lim} where the width becomes infinity. The dots correspond to the AR obtained for IC_{opt}.

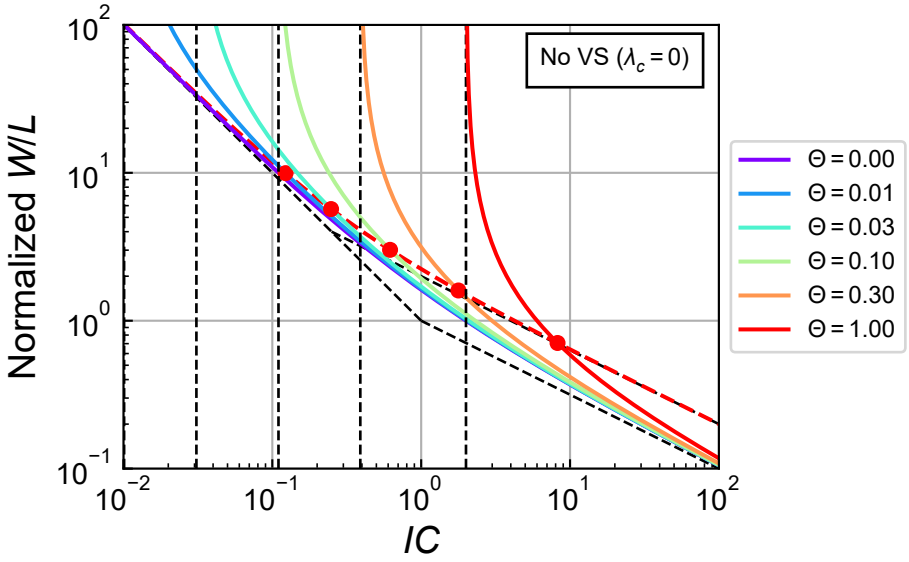

Figure 5.3: Normalized aspect ratio AR versus inversion coefficient IC.

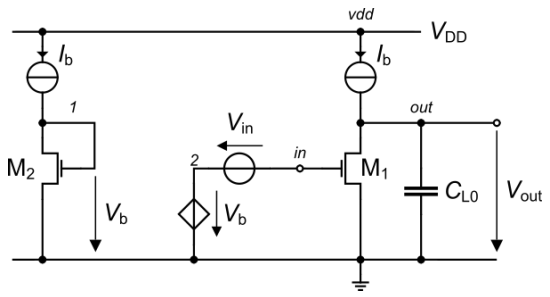

Figure 5.4: Schematic of the open-loop common-source (CS) gain stage used for simulation.

5.2 Design example

We want to size a CS SC amplifier for the specifications given in Table 5.1. We need to find the minimum current and size the transistor to achieve this specs. We will design the amplifier for a generic 180nm bulk CMOS process. The physical parameters are given in Table 5.2, the global process parameters in Table 5.3 and finally the MOSFET parameters in Table 5.4.

Table 5.1: CS amplifier specifications.

Specification	Symbol	Value	Unit
Gain bandwidth product	GBW	100	MHz
Load capacitance	C_{L0}	20	fF
Transistor length	L	1000	nm

Table 5.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 5.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 5.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	15	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	8.1e-24	J
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$

Table 5.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

For the chosen technology we get $C_{DW} = 1.167\ fF/\mu m$ and we get $C_{D0} = 0.160\ fF$. The total load capacitance is now $C_{out} = 20.160\ fF$.

Table 5.5: CS OL amplifier optimum parameters.

Parameter	Value	Unit
C_{DW}	1.167	$fF/\mu m$
C_{D0}	0.16	fF
C_{L0}	20	fF
C_L	20.16	fF
f_L	171.589	MHz
f_W	2.965	GHz
Ω	0.583	-
Θ	0.03372	-
IC_{opt}	0.269	-
$i_{b,opt}$	1.441	-
AR_{opt}	5.356	-
$(W/L)_{opt}$	3.121	-
$I_{b,opt}$	600	nA
W_{opt}	3.12	μm
$G_{m,opt}$	14.955	$\mu A/V$
$C_{D,opt}$	3.641	fF
AD	1.25	μm^2
PD	7.043	μm
C_{DBJ}	2.657	fF
C_F	1.144	fF
C_{out}	23.801	fF
GBW (check)	100	MHz
f_z	2.081	GHz
A_{dc}	51.449	dB

Table 5.6: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M1	3.12	1.00	600	2232	0.269	-22	107
M2	3.12	1.00	600	2232	0.269	-22	107

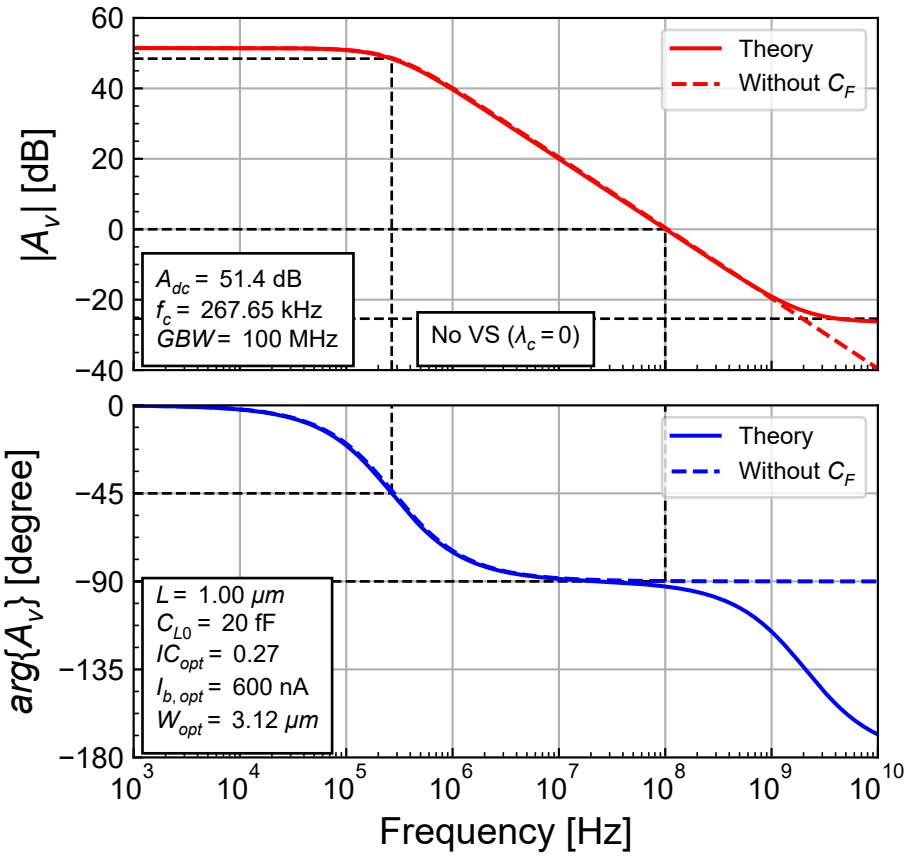

Figure 5.5: Theoretical transfer function.

Table 5.7: Transistor small-signal and thermal noise parameters.

Transistor	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M1	86.255	19.013	14.955	40.026	0.674
M2	86.255	19.013	14.955	40.026	0.674

The theoretical results can be validated by comparing them to the results obtained from simulations performed with ngspice. The cells below will run the simulations with ngspice. In order to run the simulations you need to have ngspice installed. Please refer to the ngspice instructions.

> **Note**
>
> The simulations are performed with ngspice [1] using the EKV 2.6 compact model [2]. For ngspice, we use the original Verilog-A implementation of EKV 2.6 [3] modified by C. Enz to get the operating point informations and available on the Gitub va-models site provided by D. Warning at [4]. The parameters correspond to a generic 180 nm bulk CMOS process [5].

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 5.8.

Table 5.8: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
in	0.443473
out	0.443473
1	0.443473
2	0.443473

Table 5.9: Operating point information extracted from ngspice .op file for each transistor.

Transistor	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC	n	$V_{Dsat}\ [mV]$
M1	600	2459	0.244	1.27	129
M2	600	2459	0.244	1.27	129

Table 5.10: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{mb}\ [\mu A/V]$	$G_{ds}\ [nA/V]$
M1	1.27	19.197	14.898	4.265	34.556
M2	1.27	19.197	14.898	4.265	34.556

The large-signal transistor bias information and the small-signal parameters extracted from the simulation are given in Table 5.9 and Table 5.10, respectively. We see that their values are very close to the theoretical values given in Table 5.6 and Table 5.7.

The simulated transfer function is shown in Figure 5.6 and compared to the theoretical transfer function of Figure 5.5. We see a good match between theory and simulation.

From Figure 5.6 we see that the simulation matches the theoretical estimation at least below the GBW. The simulated GBW is slightly higher than the target and the DC gain is slightly smaller. We observe a discrepancy at higher frequency with a simulated zero that is about two times lower than the theoretical estimation. This is due to a larger feedback capacitance. The origin of this larger feedback capacitance is unknown.

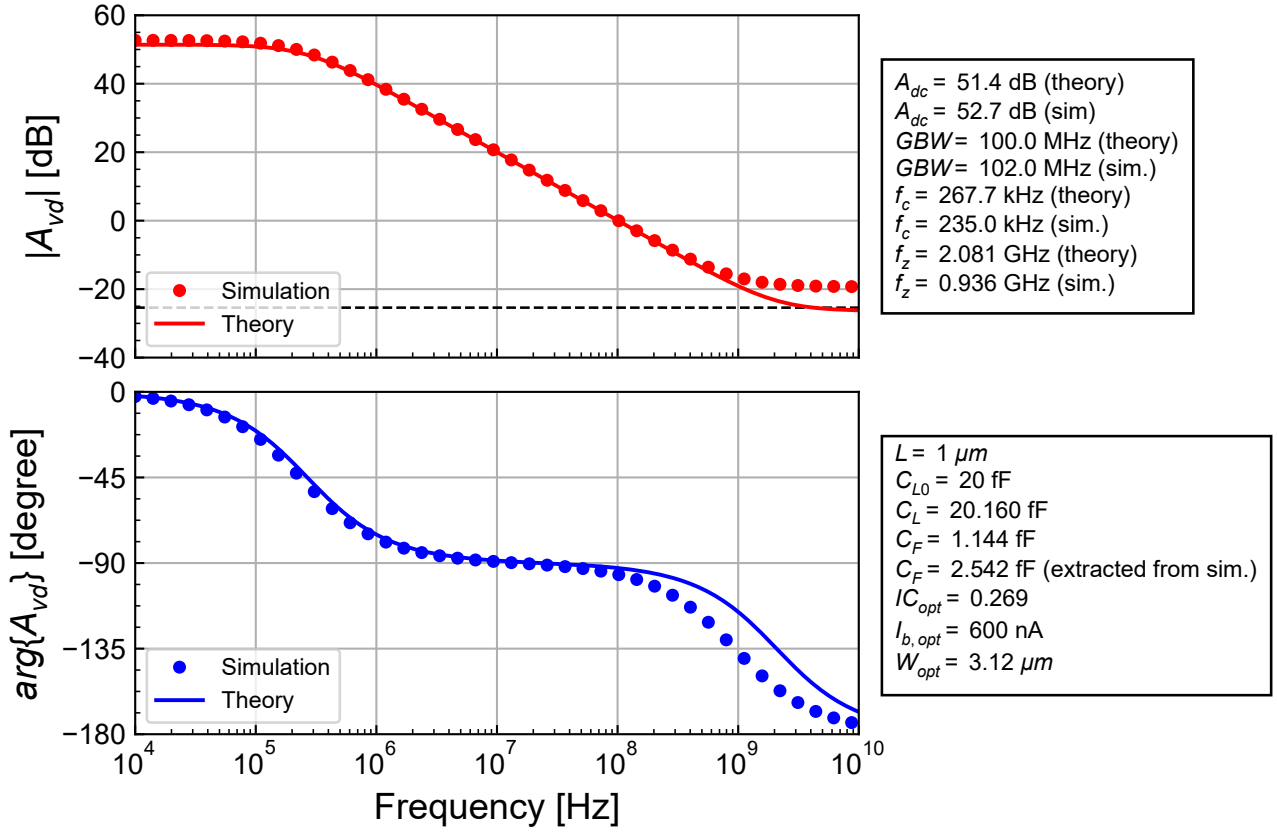

Figure 5.6: Simulated gain response compared to theoretical estimation.

6 Minimum current for given GBW and DC gain

6.1 Analysis

We can actually use the additional degree of freedom, namely the transistor length L (which has been arbitrarily set in the previous example), to set the DC gain. To this purpose we can use the simple output conductance model given by

$$G_{ds} \cong \frac{I_D}{\lambda \cdot L}. \tag{6.1}$$

We now need to solve the following set of equations

$$\omega_u = \frac{G_m}{C_L} = \frac{G_m}{C_{L0} + C_{DW} \cdot W}, \tag{6.2}$$

$$A_{dc} = \frac{G_m}{G_{ds}} = \frac{G_m \cdot \lambda \cdot L}{I_b}, \tag{6.3}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{6.4}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{6.5}$$

for I_b, W, L and G_m. This leads to the following normalized results

$$i_b \triangleq \frac{I_b}{I_{norm}} = \frac{g_{ms} \cdot IC}{g_{ms}^2 - \xi \cdot IC} = \frac{g_{ms}/IC}{(g_{ms}/IC)^2 - \xi/IC}, \tag{6.6}$$

$$w \triangleq \frac{W}{W_{norm}} = \frac{IC}{g_{ms}^2 - \xi \cdot IC}, \tag{6.7}$$

$$\ell \triangleq \frac{L}{L_{norm}} = \frac{IC}{g_{ms}}, \tag{6.8}$$

where

$$\xi \triangleq \frac{C_{DW} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} \cdot A_{dc} \cdot \omega_u, \tag{6.9}$$

$$I_{norm} \triangleq n\, U_T \cdot C_{L0} \cdot \omega_u, \tag{6.10}$$

$$W_{norm} \triangleq \frac{C_{L0} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} \cdot A_{dc} \cdot \omega_u, \tag{6.11}$$

$$L_{norm} \triangleq \frac{nU_T}{\lambda} \cdot A_{dc}. \tag{6.12}$$

6.2 Design example

We want to size a CS SC amplifier for the specifications given in Table 6.1. We need to find the minimum current and size the transistor to achieve this specs. We will design the amplifier for a generic 180nm bulk CMOS process. The physical parameters are given in Table 5.2, the global process parameters in Table 5.3 and finally the MOSFET parameters in Table 5.4.

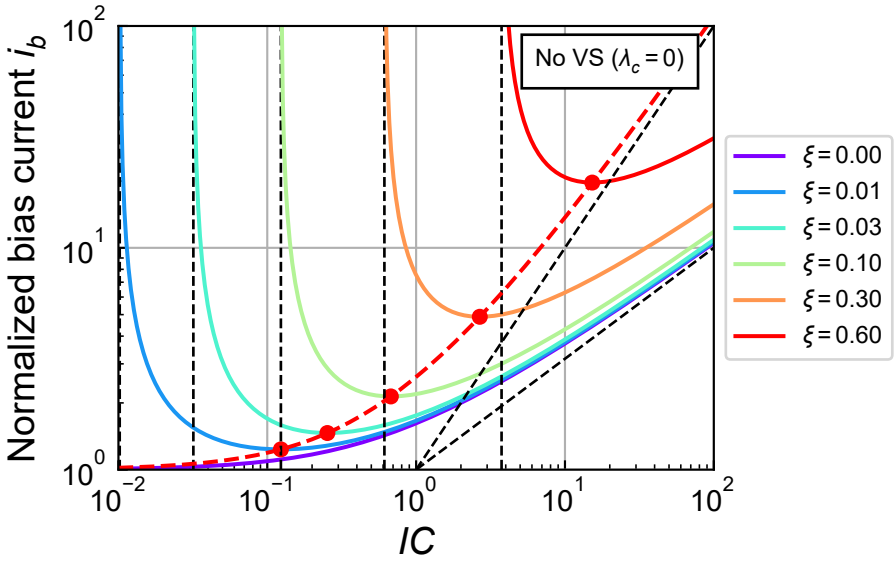

Figure 6.1: Normalized bias current i_b versus inversion coefficient IC for given gain-bandwidth product and DC gain.

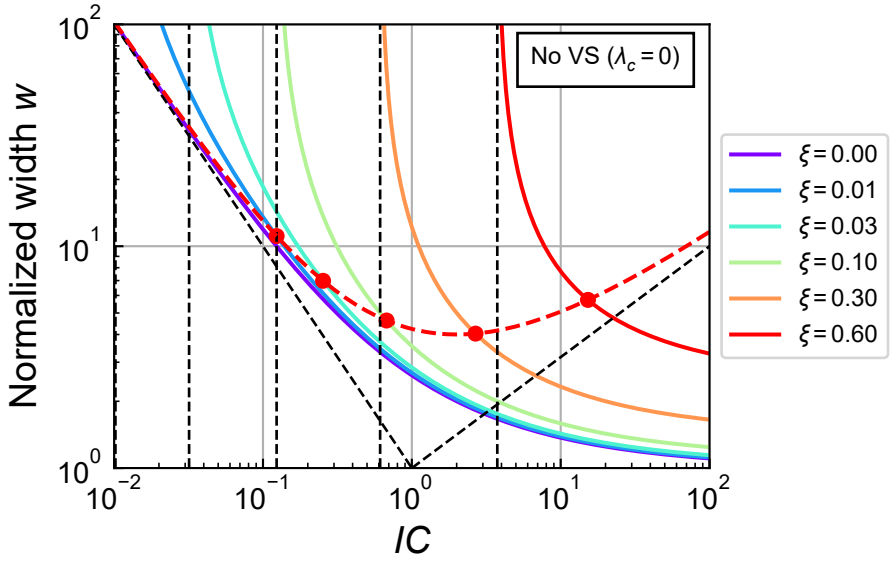

Figure 6.2: Normalized width w versus inversion coefficient IC for given gain-bandwidth product and DC gain.

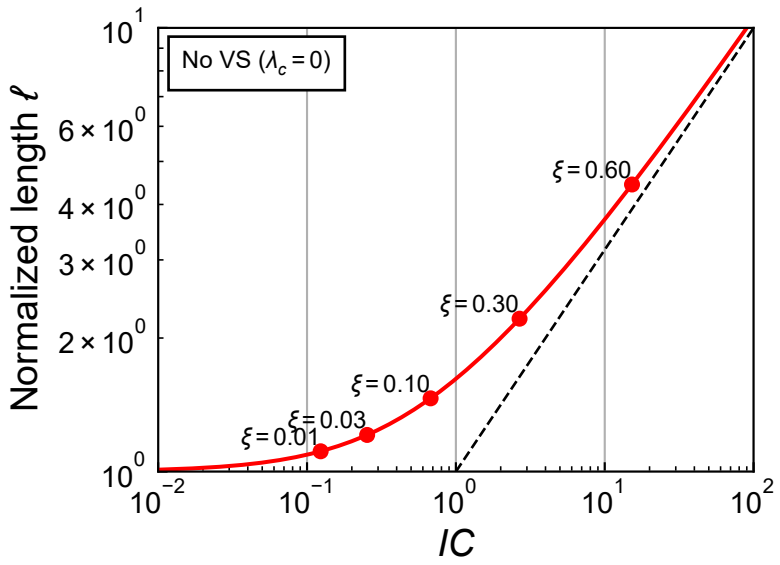

Figure 6.3: Normalized length ℓ versus inversion coefficient IC for given gain-bandwidth product and DC gain.

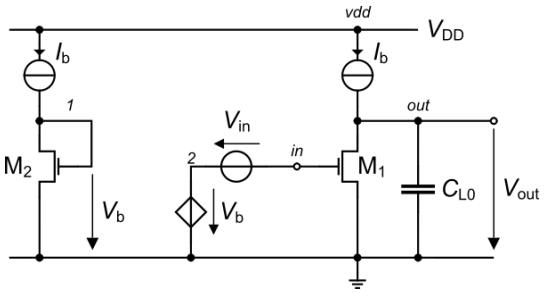

Figure 6.4: Schematic of the open-loop common-source (CS) gain stage used for simulation.

Table 6.1: CS SC amplifier specifications.

Specification	Symbol	Value	Unit
Gain bandwidth product	GBW	100	MHz
DC gain	A_{dc}	50	dB
Load capacitance	C_{L0}	20	fF

Table 6.2: CS OL amplifier optimum parameters.

Parameter	Value	Unit
C_{DW}	1.167	$fF/\mu m$
C_{D0}	0.16	fF
C_{L0}	20	fF
C_L	20.16	fF
ξ	0.023	-
IC_{opt}	0.213	-
$i_{b,opt}$	1.394	-
w_{opt}	7.72	-
ℓ_{opt}	1.181	-
$g_{m,opt}$	1.181	-
$I_{b,opt}$	581	nA
$(W/L)_{opt}$	3.121	-
I_{norm}	417	nA
W_{norm}	404	nm
L_{norm}	694	nm
$G_{m,norm}$	12.667	$\mu A/V$
$I_{b,opt}$	580.733	nA
W_{opt}	3.12	μm
L_{opt}	818.72	nm
$G_{m,opt}$	14.954	$\mu A/V$
$C_{D,opt}$	3.64	fF
AD	1.25	μm^2
PD	7.04	μm
C_{DBJ}	2.656	fF
C_F	1.144	fF
C_{out}	23.8	fF
GBW (check)	100	MHz
f_z	2.081	GHz
A_{dc}	50	dB

Table 6.3: Transistor size and bias information.

Transistor	W $[\mu m]$	L $[\mu m]$	I_D $[nA]$	I_{spec} $[nA]$	IC	$V_G - V_{T0}$ $[mV]$	V_{DSsat} $[mV]$
M1	3.12	0.82	581	2725	0.213	-27	106
M2	3.12	0.82	581	2725	0.213	-27	106

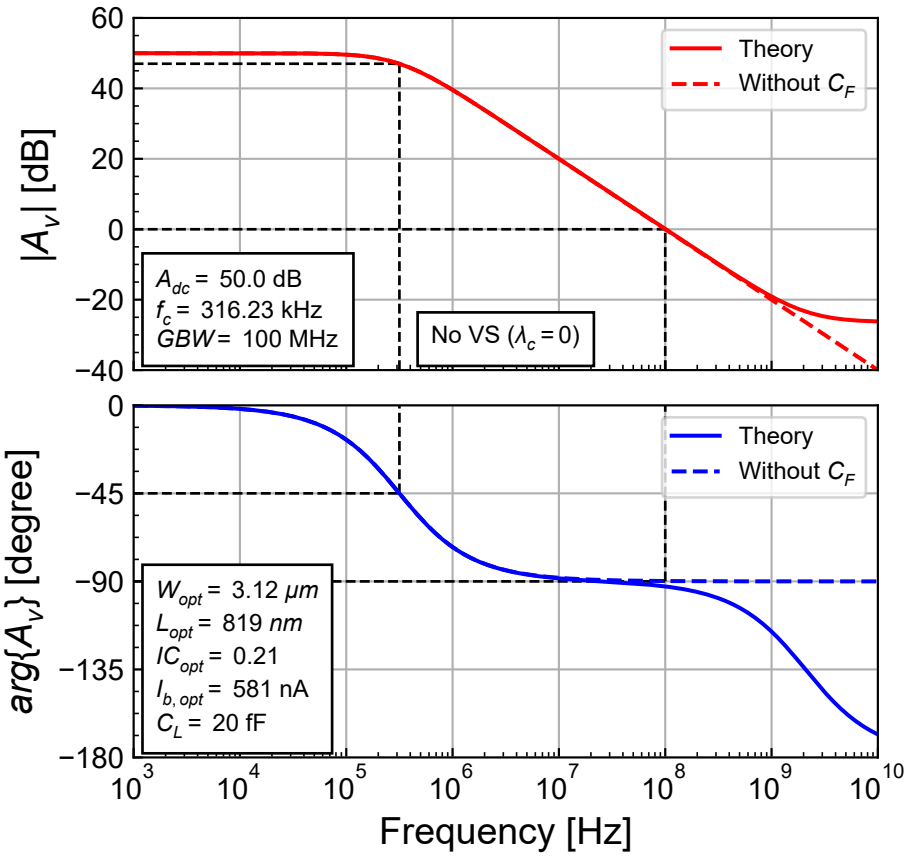

Figure 6.5: Theoretical transfer function.

Table 6.4: Transistor small-signal and thermal noise parameters.

Transistor	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M1	105.307	19.012	14.954	47.288	0.668
M2	105.307	19.012	14.954	47.288	0.668

The theoretical results can be validated by comparing them to the results obtained from simulations performed with ngspice. The cells below will run the simulations with ngspice. In order to run the simulations you need to have ngspice installed. Please refer to the ngspice instructions.

> **Note**
>
> The simulations are performed with ngspice [1] using the EKV 2.6 compact model [2]. For ngspice, we use the original Verilog-A implementation of EKV 2.6 [3] modified by C. Enz to get the operating point informations and available on the Gitub va-models site provided by D. Warning at [4]. The parameters correspond to a generic 180 nm bulk CMOS process [5].

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 6.5.

Table 6.5: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
in	0.438602
out	0.438602
1	0.438602
2	0.438602

Table 6.6: Operating point information extracted from ngspice .op file for each transistor.

Transistor	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC	n	$V_{Dsat}\ [mV]$
M1	581	3073	0.189	1.27	126
M2	581	3073	0.189	1.27	126

Table 6.7: Small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{mb}\ [\mu A/V]$	$G_{ds}\ [nA/V]$
M1	1.27	19.232	14.926	4.264	42.398
M2	1.27	19.232	14.926	4.264	42.398

The large-signal transistor bias information and the small-signal parameters extracted from the simulation are given in Table 6.6 and Table 6.7, respectively. We see that their values are very close to the theoretical values given in Table 6.3 and Table 6.4.

The simulated transfer function is shown in Figure 6.6 and compared to the theoretical transfer function of Figure 6.5. We see a good match between theory and simulation.

From Figure 5.6 we see that the simulation matches the theoretical estimation at least below the GBW. The simulated GBW is slightly lower than the target and the simulated DC gain is slightly higher than the target. We observe a discrepancy at higher frequency with a simulated zero that is about two times lower than the theoretical estimation. This is due to a larger feedback capacitance. The origin of this larger feedback capacitance is unknown.

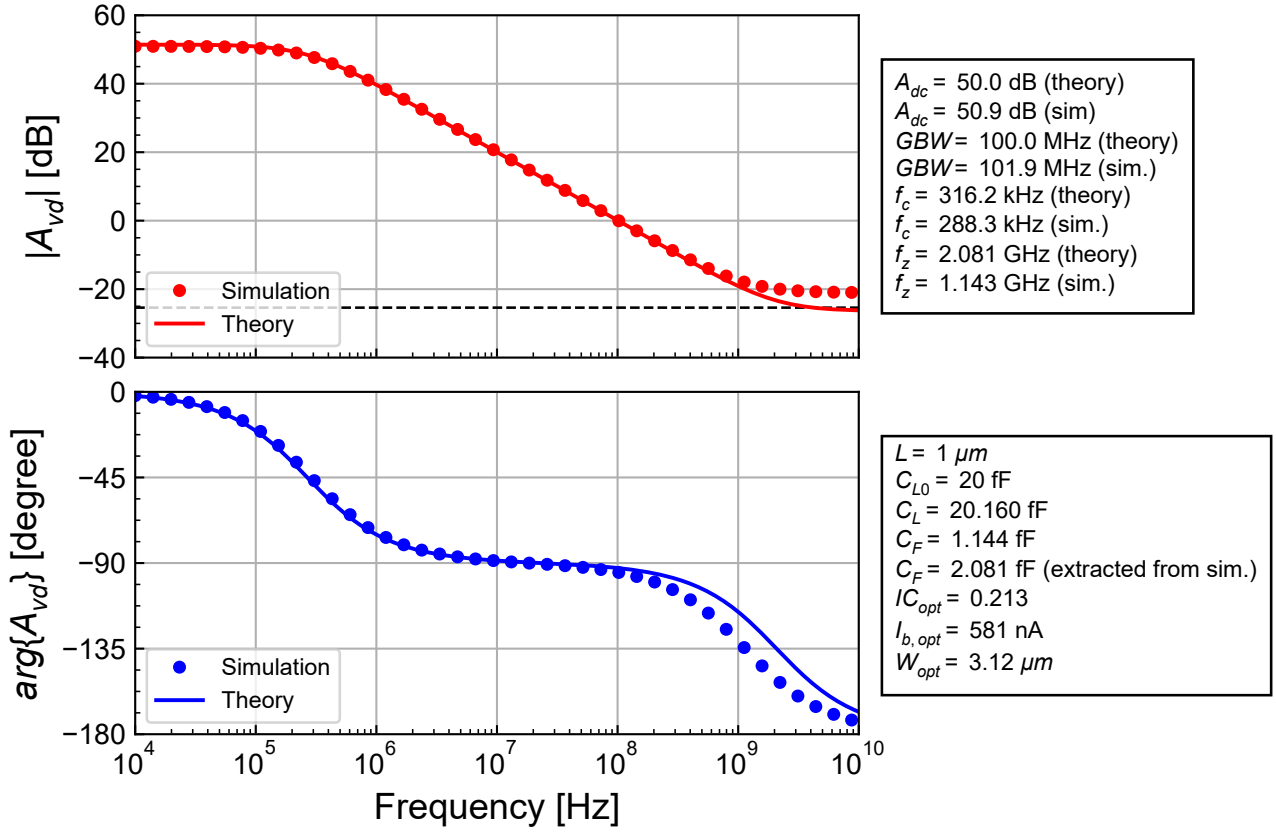

Figure 6.6: Simulated gain response compared to theoretical estimation.

7 Conclusion

In this notebook we have analyzed the basic common-source (CS) open-loop (OL) gain stage including the feedback capacitance C_F. We have seen that the minimum bias current for a achieving a given transconductance G_m or gain-bandwidth product GBW with a constant load capacitance is obtained in weak inversion at the cost of a large transistor. We then have seen that when we include the self-loading capacitance at the drain there is a minimum bias current to achieve a given GBW for a given transistor length L. The theory was then illustrated by an example designed for a 180nm generic technology. The results have been validated by simulation with ngspice [1] using the EKV 2.6 compact model [2] [3].

Finally, we have optimized the gain stage stage by finding the minimum bias current for achieving a given GBW and DC gain at the same time. The theory was then illustrated by an example designed for a 180nm generic technology and results succesfully validated by simulation.

The above theory is extended in another notebook to a closed-loop gain stage which are often found in switched-capacitor circuits.

References

[1] Holger Vogt, Giles Atkinson, Paolo Nenzi, "Ngspice User's Manual Version 43." https://ngspice.sourceforge.io/docs/ngspice-43-manual.pdf, 2024.

[2] M. Bucher, C. Lallement, C. Enz, F. Théodoloz, and F. Krummenacher, "The EPFL-EKV MOSFET Model Equations for Simulation." https://github.com/chrisenz/EKV/blob/main/EKV2.6/docs/ekv_v26_rev2.pdf, 1998.

[3] W. Grabinski *et al.*, "FOSS EKV2.6 verilog-a compact MOSFET model," in *European solid-state device research conference (ESSDERC)*, 2019, pp. 190–193. doi: 10.1109/ESSDERC.2019.8901822.

[4] Dietmar Warning, "Verilog-A Models for Circuit Simulation." https://github.com/dwarning/VA-Models, 2024.

[5] W. Grabinski *et al.*, "FOSS EKV 2.6 parameter extractor," in *2015 22nd international conference mixed design of integrated circuits & systems (MIXDES)*, 2015, pp. 181–186. doi: 10.1109/MIXDES.2015.7208507.