OTA with Capacitive Feedback

Small-signal Closed-loop Transfer Function (Version 1)

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1 Introduction

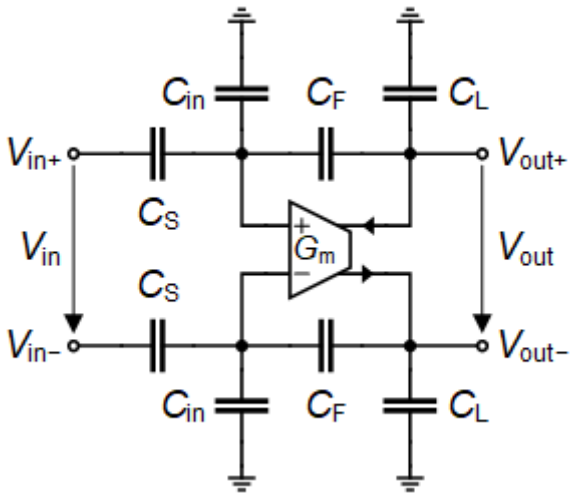

Figure 1.1: Schematic of a fully differential OTA with capacitive feedback.

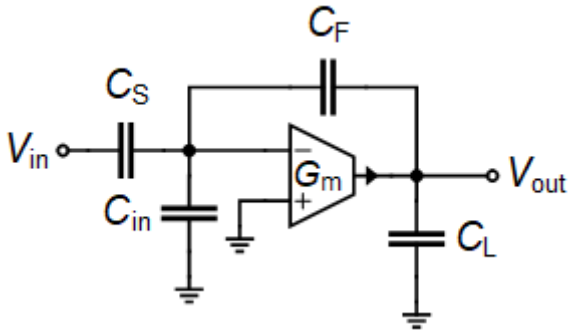

Figure 1.2: Equivalent circuit of the fully differential OTA of Figure 1.1 operating in differential mode.

In this notebook, we want to minimize the bias current of the fully differential OTA amplifier shown in Figure 1.1 for achieving a given gain and bandwidth. When the fully differential amplifier of Figure 1.1 is used in differential mode operation (assuming a perfect internal matching) it simplfies to the equivalent circuit shown in Figure 1.2.

Note that capacitance C_{in} represents the parasitic input capacitance of the fully differential OTA. Since the OTA input stage is a differential pair, when operated in differential mode, this input capacitance corresponds to the gate-to-source C_{GS} and gate-to-bulk C_{GB} capacitances of the input differential pair transistors.

> **Note**
>
> Of course the circuits of Figure 1.1 or Figure 1.2 cannot be used without periodically resetting the feedback capacitor C_F. They are usually implemented as switched-capacitor (SC) circuits as shown in Figure 1.3 which operate with two non-overlapping phases. During phase Φ_1, the sampling and feedback capacitors are reset. The amplification occurs during phase Φ_2

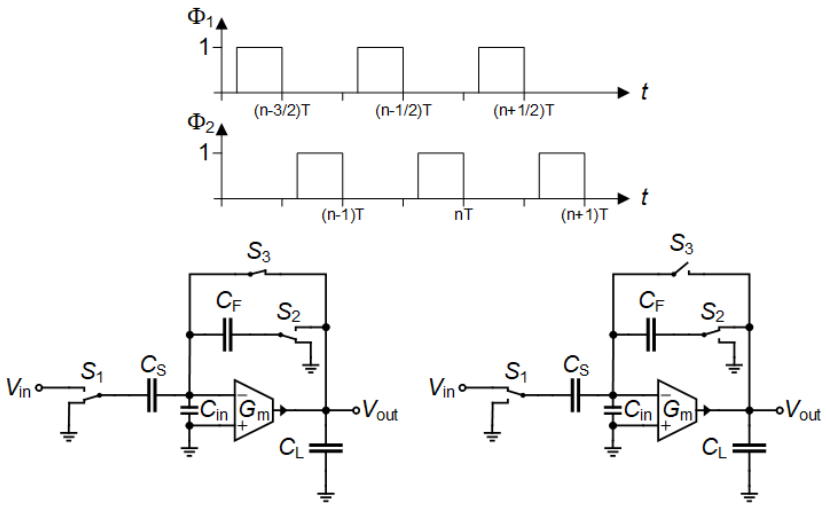

Figure 1.3: SC implementation of the amplifier (single-ended).

2 Linear Analysis

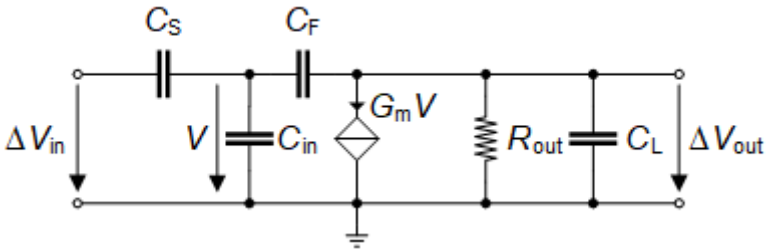

Figure 2.1: Equivalent linear circuit of the fully-differential circuit of Figure 1.1 operating in differential mode.

When operating in differential mode, the circuit of Figure 1.1 simplifies to the equivalent circuit shown in Figure 2.1. From Figure 2.1, it is then easy to show that the transfer function is given by

$$A(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = A_0 \cdot \frac{1 - s/\omega_z}{1 + s/\omega_p} \tag{2.1}$$

where A_0 is the amplifier DC gain, ω_p the cut-off frequency and ω_z the zero given by

$$A_0 = A_{0,ideal} \cdot \frac{\beta\, A_{dc}}{1 + \beta\, A_{dc}}, \tag{2.2}$$

$$A_{0,ideal} = -\frac{C_S}{C_F}, \tag{2.3}$$

$$\omega_p = \frac{1 + \beta\, A_{dc}}{R_{out}\, C_{out}}, \tag{2.4}$$

$$\omega_z = \frac{G_m}{C_F}. \tag{2.5}$$

$A_{dc} = G_m \cdot R_{out}$ is the OTA DC voltage gain, $\beta\, A_{dc}$ the DC loop gain, β the feedback gain and C_{out} the total capacitance seen at the output. If the loop-gain $\beta\, A_{dc} \gg 1$, the amplifier DC gain and cut-off frequency simplify to

$$A_0 \cong A_{0,ideal} = -\frac{C_S}{C_F}, \tag{2.6}$$

$$\omega_p \cong \frac{\beta\, A_{dc}}{R_{out}\, C_{out}} = \frac{\beta\, G_m}{C_{out}}. \tag{2.7}$$

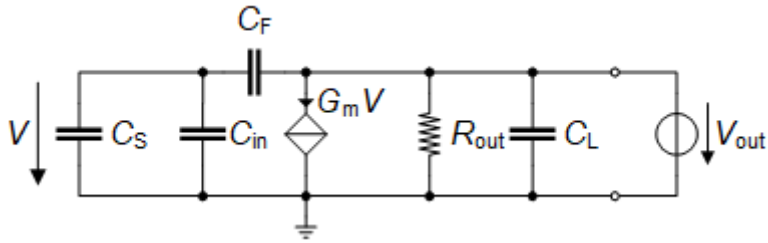

Figure 2.2: Small-signal circuit to evaluate the feedback gain β.

The feedback gain β can be calculated from the schematic shown in Figure 2.2 as

$$\beta \triangleq \frac{V}{V_{out}} = \frac{C_F}{C_F + C_S + C_{in}}. \tag{2.8}$$

The amplifier bandwidth is given by $\omega_c = \omega_p \cong \beta \cdot G_m/C_{out}$ where the total capacitance seen at the output C_{out} can be expressed as

$$C_{out} = C_L + \frac{C_S + C_{in}}{C_F + C_S + C_{in}} \cdot C_F, \tag{2.9}$$

which can also be written in terms of the feedback factor β as

$$C_{out} = C_L + \beta \cdot (C_S + C_{in}) = C_L + (1 - \beta) \cdot C_F. \tag{2.10}$$

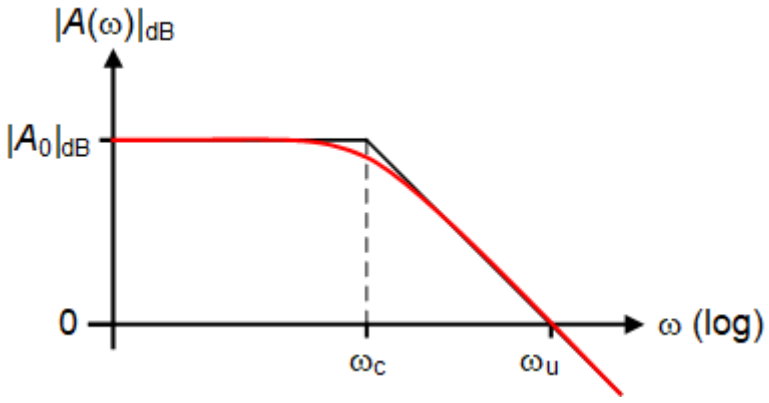

Figure 2.3: Small-signal transfer function of the amplifier.

In order to achieve some DC gain, C_F is smaller than C_S and usually also smaller than C_L. This means that the right-hand side (RHS) zero is located higher than the unity gain frequency which is then simply given by $\omega_u \cong G_m/C_{out}$. For frequencies below ω_u, the magnitude of the transfer function is shown in Figure 2.3.

At high-frequency (i.e. for $\omega_u < \omega_z \ll \omega$), the gain saturates to

$$A(s) \cong -A_0 \cdot \frac{\omega_p}{\omega_z} = \frac{C_F\, C_S}{C_L\,(C_{in} + C_S) + C_F\,(C_{in} + C_L + C_S)} \tag{2.11}$$

3 Minimum current for a given bandwidth (long-channel)

When optimizing the amplifier for low current consumption, the transistors of the differential pair are often biased in moderate or even weak inversion leading to large transistors and therefore an increased input capacitance. As mentioned above, in differential mode operation, this input capacitance is the sum of the gate-to-source and gate-to-bulk capacitances of the differential pair transistor

$$C_{in} = C_{GS} + C_{GB}. \tag{3.1}$$

Assuming the transistors of the differential pair are biased in saturation, we have

$$C_{GS} \cong W\,L\,C_{ox} \cdot c_{gsi} + C_{GSo} \cdot W \tag{3.2}$$

where c_{gsi} is the intrinsic gate-to-source capacitance normalized to the total oxide capacitance $W\,L\,C_{ox}$. c_{gsi} is typically equal to 2/3 in strong inversion and proportional to IC in weak inversion. C_{GSo} is the gate-to-source overlap capacitance per unit width.

The gate-to-bulk capacitance C_{GB} is given by

$$C_{GB} \cong W\,L\,C_{ox} \cdot c_{gbi} + C_{GBo} \cdot W, \tag{3.3}$$

where c_{gbi} is the gate-to-bulk intrinsic capacitance normalized to the total oxide capacitance $W\,L\,C_{ox}$. In strong inversion it is given by

$$c_{gbi} = \frac{n-1}{3n}. \tag{3.4}$$

C_{GBo} is the gate-to-bulk overlap capacitance per unit width.

For a given transistor length L, the input capacitance C_{in} scales with the transistor width W according to

$$C_{in} = C_{GW} \cdot W, \tag{3.5}$$

where C_{GW} is the gate-to-source and gate-to-bulk capacitance per unit width given by

$$C_{GW} = L\,C_{ox} \cdot (c_{gsi} + c_{gbi}) + C_{GSo} + C_{GBo}. \tag{3.6}$$

To achieve a certain bandwidth we need to have a certain transconductance for a given load capacitance. In order to maximize the current efficiency, we should bias the transistors of the differential pair in weak inversion. This leads to large transistors and therefore large parasitic capacitances which will impact the bandwidth. Imposing the bandwidth, at some point the capacitance becomes so large that it is no more possible to achieve the required transconductance in weak inversion for the desired bandwidth. Does this mean that there is a minimum current for the amplifier to achieve a certain bandwidth?

To answer this question we need to solve the following set of equations for I_b and W assuming a given length L

$$\omega_c = \beta \cdot \frac{G_m}{C_{out}}, \tag{3.7}$$

$$C_{out} = C_L + (1-\beta) \cdot C_F, \tag{3.8}$$

$$\beta = \frac{C_F}{C_F + C_S + C_{in}}, \tag{3.9}$$

$$C_{in} = W \cdot C_{GW}, \tag{3.10}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC, \tag{3.11}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{3.12}$$

where $g_{ms}(IC)$ is the long-channel normalized source transconductance given by

$$g_{ms} = \frac{\sqrt{4IC+1}-1}{2} = \frac{2IC}{\sqrt{4IC+1}+1}. \tag{3.13}$$

Solving for I_b and W/L leads to the following normalized solutions

$$i_b \triangleq \frac{I_b}{I_{pec\square} \cdot \Omega} = \frac{IC}{g_{ms}(IC) - \Theta}, \tag{3.14}$$

$$AR \triangleq \frac{W/L}{\Omega} = \frac{1}{g_{ms} - \Theta}, \tag{3.15}$$

where i_b is the bias current normalized to $I_{pec\square} \cdot \Omega$ and AR is the W/L ratio normalized to Ω with

$$\Omega \triangleq \frac{\omega_c}{\omega_L}, \tag{3.16}$$

$$\omega_L \triangleq \frac{I_{spec\square}}{nU_T} \cdot \frac{1}{(1 + C_S/C_L + C_S/C_F) \cdot C_L}, \tag{3.17}$$

$$\Theta \triangleq \frac{\omega_c}{\omega_W}, \tag{3.18}$$

$$\omega_W \triangleq \frac{I_{spec\square}}{nU_T} \cdot \frac{1}{(1 + C_L/C_F) \cdot C_{GW} \cdot L}. \tag{3.19}$$

Parameters Ω and Θ are proportionnal to the desired bandwidth ω_c and depend on the parameters ω_L and ω_W.

The normalized current i_b is plotted versus the inversion coefficient IC in Figure 3.1 for different values of Θ. Note that the curve for $\Theta = 0$ corresponds to the case where the input capacitance can be ignored ($C_{GW} = 0$).

From Figure 3.1, we clearly see that there is a minimum current for a given value of parameter Θ. We can find the optimum inversion coefficient IC_{opt} corresponding to this minimum which is given by

$$IC_{opt} = \left(\sqrt{\Theta \cdot (1+\Theta)} + \Theta + \frac{1}{2}\right)^2 - \frac{1}{4} \tag{3.20}$$

$$= 2\Theta \cdot (1+\Theta) + (1+2\Theta) \cdot \sqrt{\Theta \cdot (1+\Theta)} \tag{3.21}$$

$$\cong 2\Theta + \sqrt{\Theta} \quad \text{for } \Theta \ll 1. \tag{3.22}$$

We see that IC_{opt} only depends on the parameter Θ. We also see that there is a minimum inversion coefficient IC_{lim} below which the desired bandwidth ω_c can no more be achieved

$$IC_{lim} = \Theta \cdot (1+\Theta) \cong \Theta \quad \text{for } \Theta \ll 1, \tag{3.23}$$

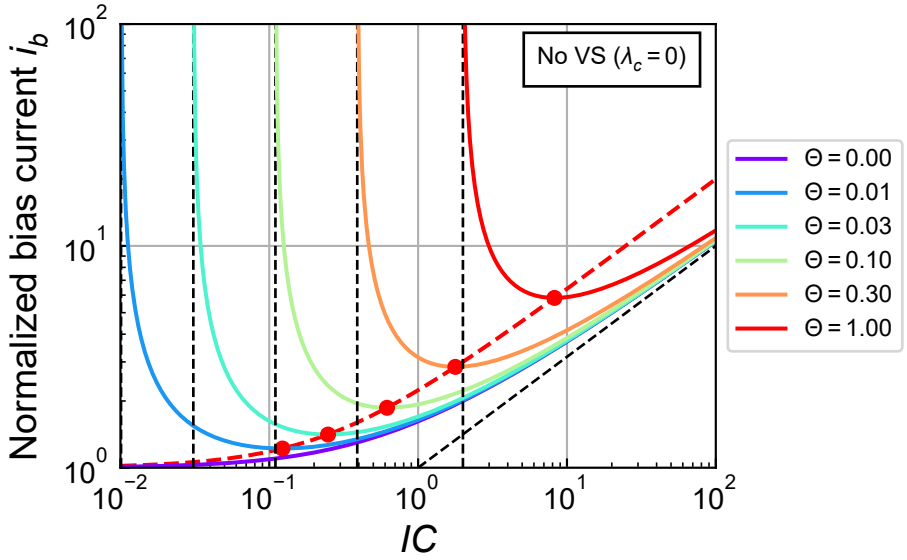

Figure 3.1: Normalized bias current i_b versus inversion coefficient IC.

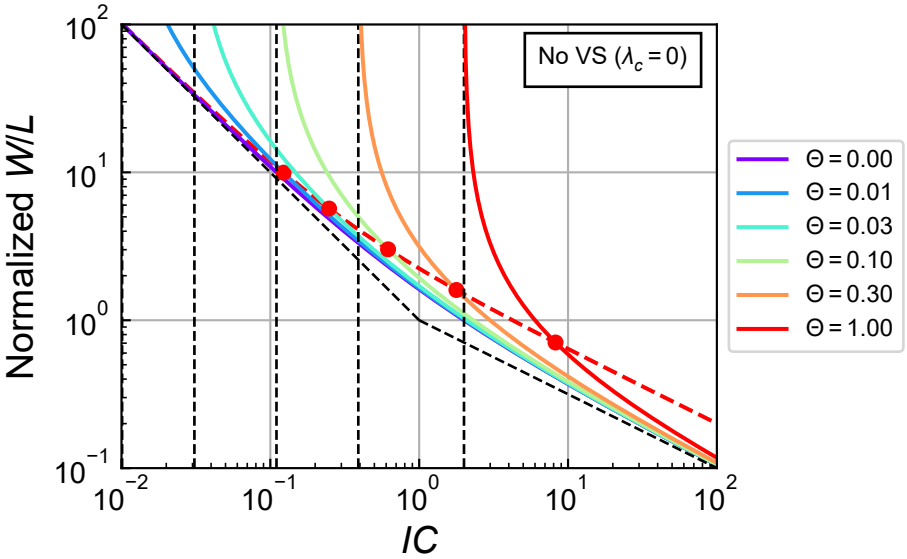

Figure 3.2: Normalized aspect ratio W/L versus inversion coefficient IC.

which is about equal to Θ for small values of Θ. The optimum normalized current is given by

$$i_{bopt} \triangleq i_b(IC_{opt}) = 1 + 2\Theta + 2\sqrt{\Theta \cdot (1+\Theta)}. \tag{3.24}$$

The normalized W/L is plotted versus IC in Figure 3.2 for the same values of Θ.

We see from Figure 3.2 that the transistor width increases first as $1/\sqrt{IC}$ in strong inversion and then faster as $1/IC$ in weak inversion making the transistor quickly very large until IC reaches IC_{lim} where the width becomes infinity. The optimum current also corresponds to an optimum transistor width W and hence and optimum normalized W/L given by

$$AR_{opt} \triangleq AR(IC_{opt}) = \frac{1}{\sqrt{\Theta \cdot (1+\Theta)}}. \tag{3.25}$$

The dots in Figure 3.2 correspond to the normalized aspect ratio AR obtained for IC_{opt}.

We now will illustrate the design of the fully differential capacitively coupled OTA for a given bandwidth with an example.

4 Design Example

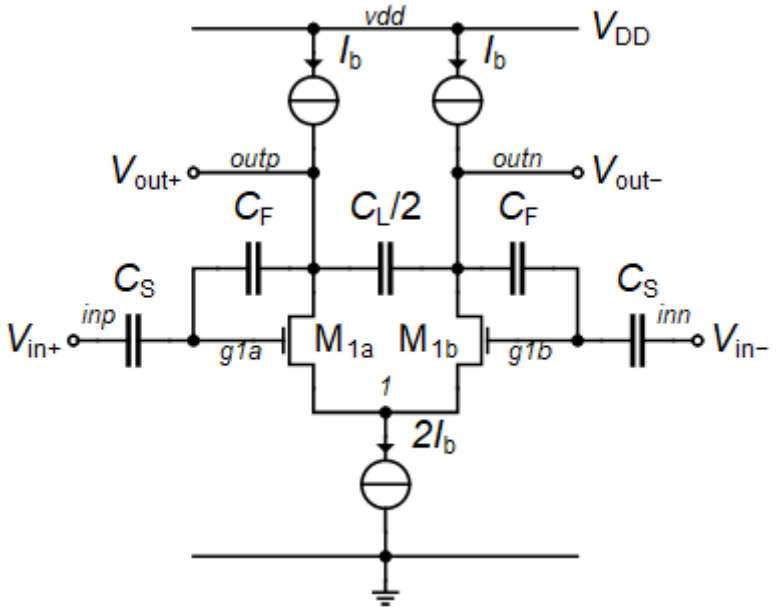

Figure 4.1: Schematic of the fully differential amplifier used for simulations.

For this example we have chosen the simplest fully differential OTA shown in Figure 4.1, namely a simple differential pair. Note that in reality the circuit of Figure 4.1 requires an additional common-mode feedback (CMFB) circuit to set and stabilize the common-mode output voltage. However, in simulation, the circuit is perfectly symmetrical and therefore the output common-mode voltage is well defined (by the input common-mode, the V_{GS} voltage and output conductance of M_{1a}-M_{1b}). In differential operation, the sources of M_{1a}-M_{1b} remain an AC ground and the circuit reduces to a common-source amplifier corresponding to a single current branch as shown in Figure 4.2. We can therefore use the above analysis to design the amplifier.

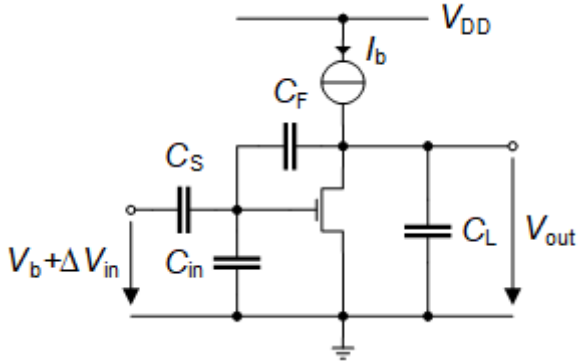

Figure 4.2: Equivalent schematic of the fully differential amplifier in differential operation.

We want to size the fully differential amplifier for the specifications given in Table 4.1. We need to find the minimum current and size the transistor to achieve these specs. We will design the amplifier for a generic 180nm bulk CMOS process. The physical parameters are given in Table 4.2, the global process parameters in Table 4.3 and finally the MOSFET parameters in Table 4.4.

Table 4.1: Fully-differential SC amplifier specifications.

Specification	Symbol	Value	Unit
DC gain	A_0	20	dB
Bandwidth	BW	0	MHz
Load capacitance	C_L	1	pF
Feedback capacitance	C_F	100	fF
Transistor length	L	1	μm

4.1 Process

We will design the fully-differential SC amplifier for a generic 180 nm bulk CMOS process. The physical parameters are given in Table 4.2, the global process parameters in Table 4.3 and finally the MOSFET parameters in Table 4.4.

Table 4.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.875	mV

Table 4.3: Global process parameters

Parameter	Value	Unit
V_{DD}	1.8	V
C_{ox}	8.443	$\frac{fF}{\mu m^2}$
W_{min}	200	nm
L_{min}	180	nm

Table 4.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
sEKV parameters			
n	1.27	1.31	-
$I_{spec\square}$	715	173	nA
V_{T0}	0.455	0.445	V
L_{sat}	26	36	nm
λ	20	20	$\frac{V}{\mu m}$
Overlap capacitances parameters			
C_{GDo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GSo}	0.366	0.329	$\frac{fF}{\mu m}$
C_{GBo}	0	0	$\frac{fF}{\mu m}$
Junction capacitances parameters			
C_J	1	1.121	$\frac{fF}{\mu m^2}$
C_{JSW}	0.2	0.248	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	8.1e-24	8.1e-24	J

Table 4.4: Transistor process parameters

Parameter	NMOS	PMOS	Unit
AF	1	1	-
ρ	0.05794	0.4828	$\frac{V \cdot m^2}{A \cdot s}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$
Source and drain sheet resistance parameter			
R_{sh}	600	2386	$\frac{\Omega}{\mu m}$
Width and length parameters			
ΔW	39	54	nm
ΔL	-76	-72	nm

We first need to estimate the parameter C_{GW} which is related to the transistor input capacitance C_{in}. Since we don't know the inversion coefficient we cannot estimate c_{gsi} and c_{gbi}. We therefore will take their values in strong inversion for the estimation of the input capacitance per width C_{GW}

$$C_{GW} \cong \left(1 - \frac{1}{3n}\right) \cdot C_{ox} \cdot L + C_{GSo} + C_{GBo}, \tag{4.1}$$

which depends on transistor length L. Since the above theory was developed for a long-channel device, we will choose $L = 1\ \mu m$.. We can now estimate the total gate capacitance per unit width for an n-channel transistor.

For the selected technology, we get $C_{GW} = 6.596\ fF/\mu m$.

From the DC gain specification $A_0 = 10$ and the chosen feedback capacitance $C_F = 100\ fF$, we get $C_S = 1\ pF$. We can compute the optimum inversion coefficient IC_{opt}, optimum width W_{opt}, optimum current $I_{b,opt}$ and aspect ratio $W/L|_{opt}$ which are given in Table 4.5.

Table 4.5: Fully differential OTA optimum parameters.

Parameter	Value	Unit
A_0	10	-
C_S	1	pF
f_L	288.269	kHz
f_W	47.679	MHz
Ω	0.347	-
θ	0.002097	-
IC_{opt}	0.05	-
$i_{b,opt}$	1.096	-
AR_{opt}	21.813	-
$(W/L)_{opt}$	7.567	-
$I_{b,opt}$	272	nA
$G_{m,opt}$	7.885	μA
W_{opt}	7.57	$\frac{\mu A}{V}$
C_{in}	49.908	fF
C_{GD}	2.773	fF
C_F	100	fF
C_{F0}	97.227	fF

Table 4.6: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M1a	7.57	1.00	272	5.410	0.050	-60	104
M1b	7.57	1.00	272	5.410	0.050	-60	104

Table 4.7: Transistor small-signal and thermal noise parameters.

Transistor	$G_{spec}\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{ds}\ [nA/V]$	γ_n
M1a	209.093	10.024	7.885	13.591	0.645
M1b	209.093	10.024	7.885	13.591	0.645

The transistor size and bias information are given in Table 4.6, while Table 4.7 gives the small-signal parameters.

The theoretical transfer function for this design is plotted in Figure 4.3.

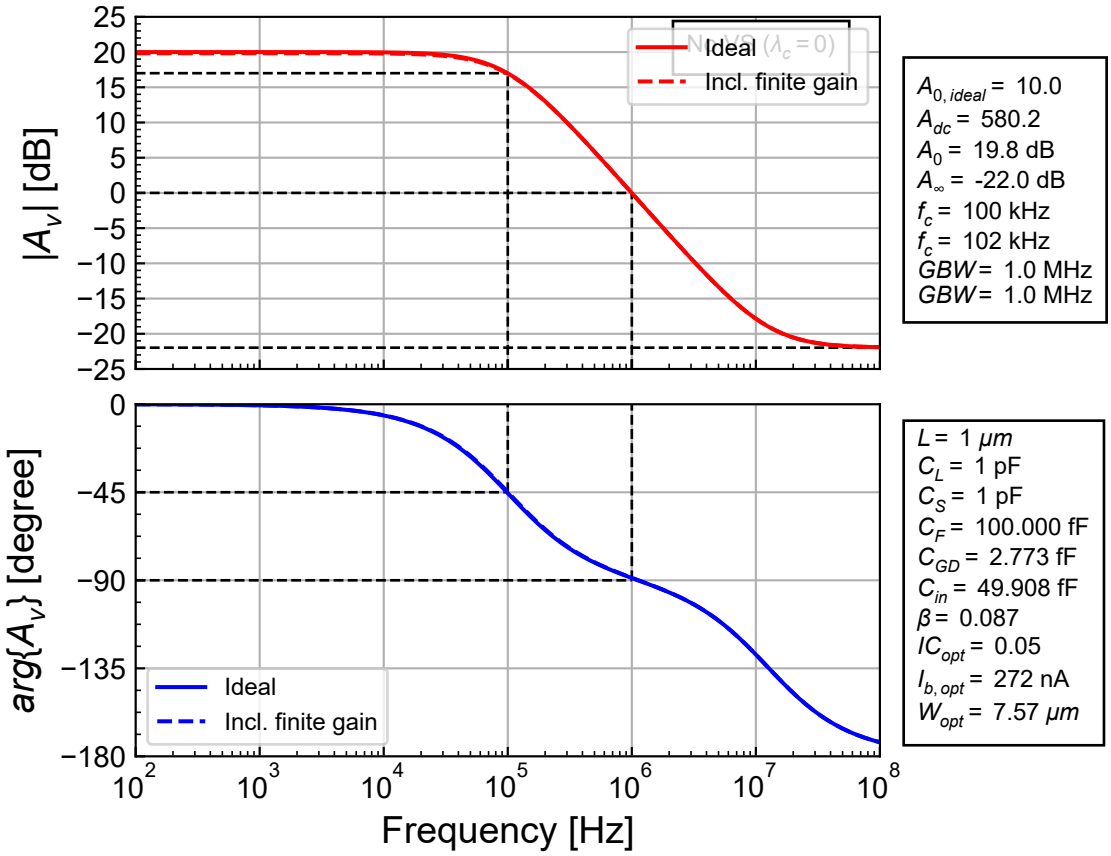

Figure 4.3: Theoretical transfer function.

We now will check the design with simulations.

4.2 Simulation results from ngspice

The theoretical results can be validated by comparing them to the results obtained from simulations performed with ngspice. In order to run the simulations you need to have ngspice installed. Please refer to the ngspice instructions.

> **Note**
>
> The simulations are performed with ngspice [1] using the EKV 2.6 compact model [2]. For ngspice, we use the original Verilog-A implementation of EKV 2.6 [3] modified by C. Enz to get the operating point informations and available on the Gitub va-models site provided by D. Warning at [4]. The parameters correspond to a generic 180 nm bulk CMOS process [5].

4.2.1 Operating point

Before running the AC simulation, we first need to check the quiescent voltages and currents and the operating point by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 4.8.

Table 4.8: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.8
ic	0.9
inp	0.9
inn	0.9
outp	0.966482
outn	0.966482
g1a	0.899979
g1b	0.899979
1	0.518367

Table 4.9: EKV 2.6 operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[nA]$	I_{spec} $[nA]$	IC	n	V_{Dsat} $[mV]$
M1a	272	6047	0.045	1.27	114
M1b	272	6047	0.045	1.27	114

Table 4.10: EKV 2.6 small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	n	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[nA/V]$
M1a	1.27	10.064	7.773	2.274	16.453
M1b	1.27	10.064	7.773	2.274	16.453

The EKV 2.6 large- and small-signal transistor bias information extracted from the simulation are given in Table 4.9 and Table 4.10, respectively. We see that their values are close to the theoretical values given in Table 4.6 and Table 4.7.

4.2.2 Transfer function

The simulated transfer function is shown in Figure 4.4 and compared to the theoretical transfer function of Figure 2.3. We see a perfect match between theory and simulation.

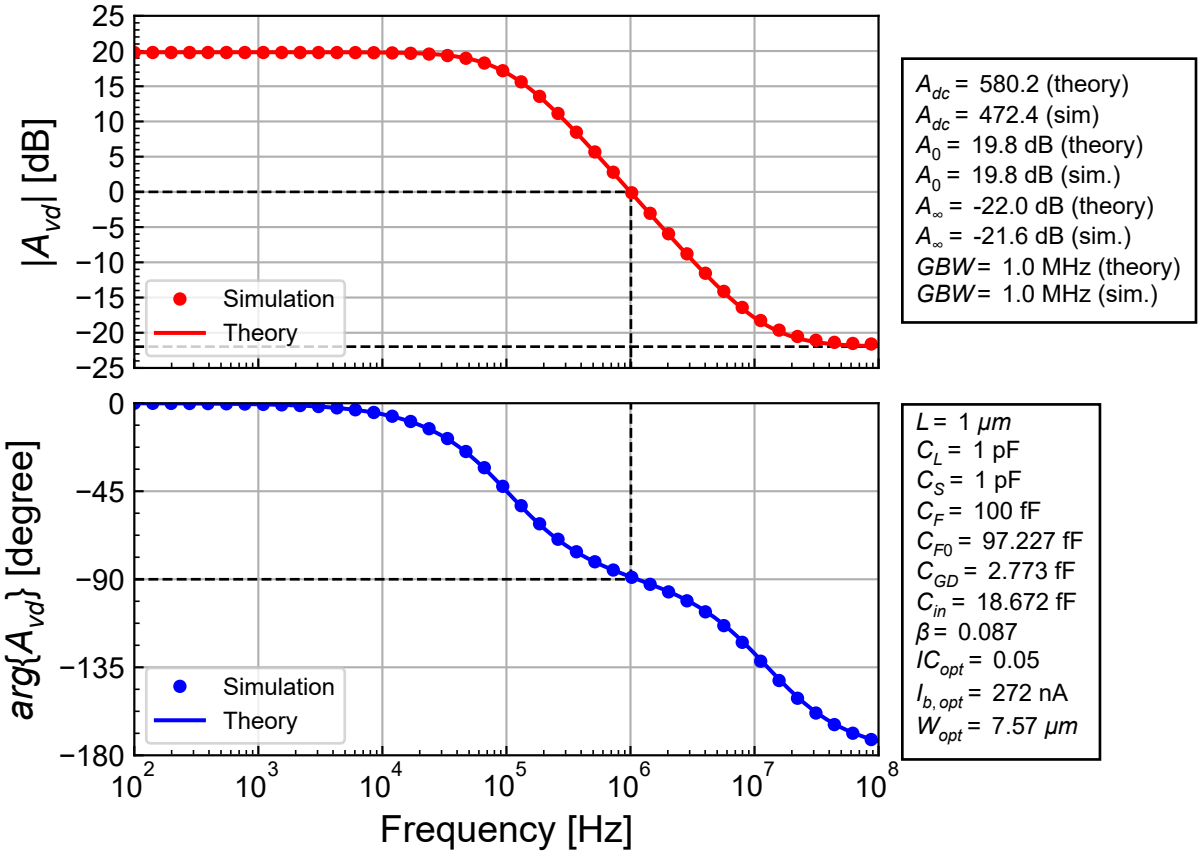

Figure 4.4: Simulated gain response compared to theoretical estimation.

5 Conclusion

In this notebook we have optimized a fully differential capacitiviely coupled OTA for achieving a certain DC gain and bandwidth with a minimum power consumption. We started to analyze the circuit accounting for the input parasitic capacitance which scales with the width of the transistor of the differential pair. We have found that there is an optimum transistor inversion coefficient and width for achieving a certain bandwidth with a minimum bias current. We then illustrated the theory with an example. The sized circuit was then simulated with ngspice using the EKV 2.6 compact model for a generic 180nm CMOS technology. The simulation results perfectly match the theory.

> **Note**
>
> An analysis of the small- and large-signal step response and the related settling times is performed in the companion notebook entitled “OTA with Capacitive Feedback – Step Response (Version 1)”.

References

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