Common-source Gain Stage Optimization

For IHP 130nm Process (Version 2)

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1 Introduction

This notebook presents the optimization of a common-source gain stage to minimize the power consumption for a given gain-bandwidth product and DC gain using the sEKV model and the inversion coefficient approach [1], [2], [3].

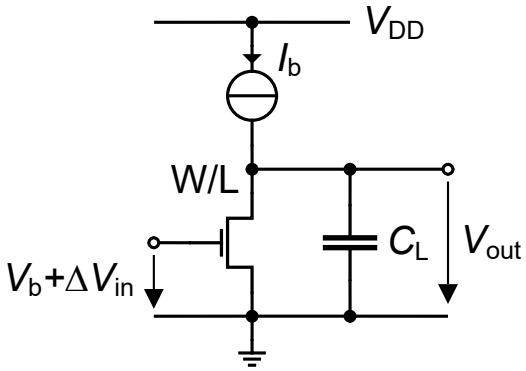

Figure 1.1: Schematic of the open-loop common-source (CS) gain stage.

The schematic of the common-source (CS) stage in open-loop configuration is shown in Figure 1.1. To size the transistor according to some specifications on the gain, bandwidth or noise, we need to find the bias current I_b and the aspect ratio W/L that satisfies the given specifications. In order to do this, we first need to analyze the circuit in terms of its key features. We will start with the small-signal analysis.

2 Small-signal analysis

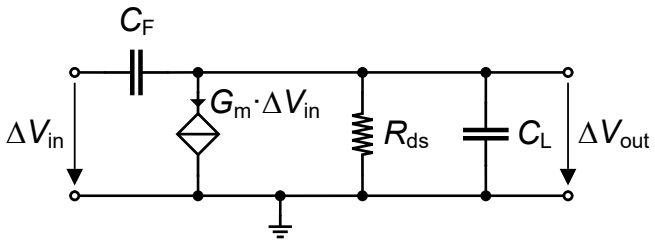

Figure 2.1: Small-signal schematic of the open-loop (OL) common-source (CS) gain stage including the feedback capacitance.

The small-signal schematic of the open-loop (OL) common-source (CS) stage is shown in Figure 2.1. It is straightforward to show that the transfer function is given by

$$A(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = A_{dc} \cdot \frac{1 - s/\omega_z}{1 + s/\omega_p} \tag{2.1}$$

where

$$A_{dc} = -G_m \cdot R_{ds}, \tag{2.2}$$

$$\omega_z = \frac{G_m}{C_F}, \tag{2.3}$$

$$\omega_p = \frac{1}{R_{ds}\, C_{Ltot}}, \tag{2.4}$$

with $A_{dc} = -G_m \cdot R_{ds}$ the DC voltage gain, ω_z the zero (in the right half plan), ω_p the pole and $C_{Ltot} = C_L + C_F$ the total load capacitance incldluing the feedback capacitance. The gain-bandwidth product (GBW) or unity gain frequency (ω_u) is then given by

$$GBW = \omega_u = |A_{dc}| \cdot \omega_p = \frac{G_m}{C_{Ltot}}. \tag{2.5}$$

As illustrated in Figure 2.2, the gain magnitude at high frequency will settle to

$$A_\infty \triangleq \lim_{s\to\infty} A(s) = \frac{C_F}{C_L + C_F}, \tag{2.6}$$

and the phase will turn to $-180°$ because of the positive zero.

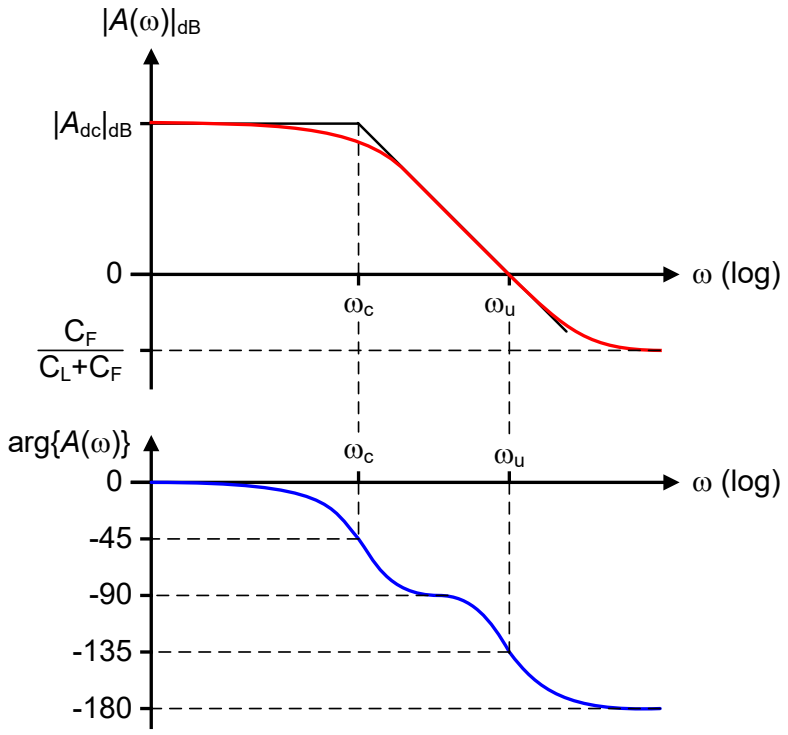

Figure 2.2: Bode plot of the small-signal transfer function of the CS OL amplifier.

3 Minimum current for a given transconductance

In this section we want to answer the following question:

> **Question**
>
> What is the minimum bias current I_b and transistor size (aspect ratio W/L) in order for the OL CS gain stage to achieve a given transconductance?

To answer this question we first rewrite the current as

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC \tag{3.1}$$

and the transconductance as

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{3.2}$$

where $g_{ms}(IC)$ is the normalized source transconductance which only depends on IC according to

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = \frac{n\,G_m}{G_{spec}} = \frac{\sqrt{4IC+1}-1}{2} \tag{3.3}$$

for a long-channel transistor and

$$g_{ms} = \frac{\sqrt{4IC+1+(\lambda_C\,IC)^2}-1}{2+\lambda_c^2\,IC} \tag{3.4}$$

for a short-channel transistor accounting for velocity saturation with parameter λ_c.

We then need to solve the following set of equation for I_b and W/L

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{3.5}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{3.6}$$

This leads to the following normalized results

$$i_b \triangleq \frac{I_b}{G_m \cdot nU_T} = \frac{IC}{g_{ms}}, \tag{3.7}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{I_{spec\square}}{G_m \cdot nU_T} = \frac{1}{g_{ms}}. \tag{3.8}$$

i_b and AR are plotted below for various values of λ_c

From Figure 3.1, we see that we can reduce the current i_b when moving from strong inversion to moderate inversion reaching a minimum in weak inversion. The loss of transconductance resulting from a reduction of IC is compensated by an increase of W/L as shown by the blue curves, resulting in a very large transistor and a drastic area increase. Moderate inversion turns out to be a good trade-off between low current and acceptable area for achieving a given transconductance.

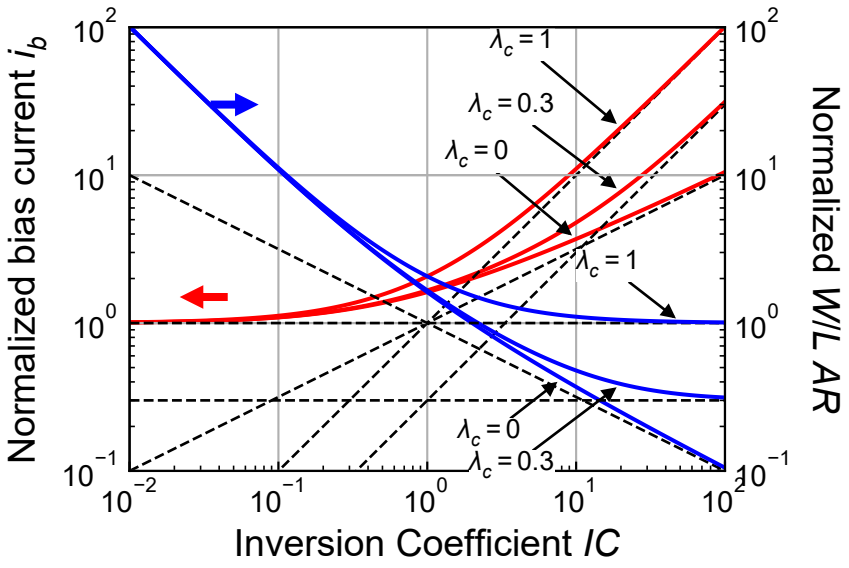

Figure 3.1: Normalized bias current and aspect ratio versus inversion coefficient.

4 Minimum current for a given gain-bandwidth product (no self-loading)

We now will answer the following question:

> **Question**
>
> What is the minimum bias current I_b and transistor size (aspect ratio W/L) in order for the OL CS gain stage to achieve a given gain-bandwidth product for a given load capacitance neglecting the effect of self-loading?

We first rewrite the gain-bandwidth as

$$\omega_u = \frac{G_m}{C_L} = \omega_L \cdot \frac{W}{L} \cdot g_{ms}, \tag{4.1}$$

where

$$\omega_L \triangleq \frac{I_{spec\square}}{nU_T \cdot C_{Ltot}}. \tag{4.2}$$

To answer this question we need to solve the following set of equations for I_b and W/L

$$\omega_u = \omega_L \cdot \frac{W}{L} \cdot g_{ms}, \tag{4.3}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{4.4}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{4.5}$$

Since the load capacitance C_L is assumed constant, the problem is similar to imposing a given transconductance With a slightly different normalization we get the same normalized functions as before

$$i_b \triangleq \frac{I_b}{G_m \cdot nU_T} \cdot \frac{1}{\Omega} = \frac{IC}{g_{ms}}, \tag{4.6}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{1}{\Omega} = \frac{1}{g_{ms}}. \tag{4.7}$$

with

$$\Omega \triangleq \frac{\omega_u}{\omega_L}. \tag{4.8}$$

i_b and AR are plotted Figure 3.1 for various values of λ_c. A different normalization reduces to the same trade-off than constant G_m. Moderate inversion again turns out to be a good trade-off between low current and acceptable area for achieving a given gain-bandwidth product.

When moving to moderate and weak inversion, the transistor can become very large. The parasitic capacitance at the transistor drain can then no more be ignored. We will analyze the impact of self-loading in the next section.

5 Minimum current for a given gain-bandwidth product including self-loading

5.1 Analysis

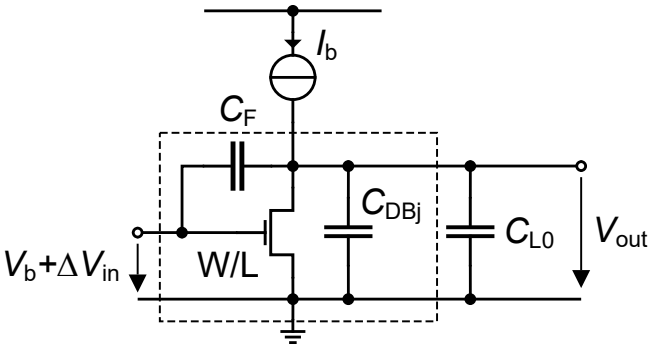

Figure 5.1: Schematic of the open-loop common-source (CS) gain stage including the self-loading capacitances at the drain.

When optimizing the OL CS amplifier for low current consumption, the transistor is often biased in moderate or even weak inversion leading to large transistor and therefore an increased output capacitance due to the self-loading from the parasitic capacitances connected to the drain. We now want to answer the following question:

> **Question**
>
> What is the minimum bias current I_b and transistor size (aspect ratio W/L) in order for the OL CS gain stage to achieve a given gain-bandwidth product accounting for the effect of self-loading?

As shown in Figure 5.1, the self-loading capacitances include the junction capacitance at the drain C_{BDj} and the feedback capacitance C_F. The junction capacitance C_{BDj} is given by

$$C_{DBJ} = AD \cdot C_J + (PD - W) \cdot C_{JSWSTI} + W \cdot C_{JSWGAT}, \tag{5.1}$$

where AD and PD are the drain diffusion area and perimeter, respectively, which are given by

$$AD = W \cdot Z_{dif}, \tag{5.2}$$
$$PD = 2\,(W + Z_{dif}), \tag{5.3}$$

with Z_{dif} the diffusion width (i.e. $Z_{dif} = 2\,H_{dif}$). Paramter C_J is the bottom junction capacitance, C_{JSWSTI} the side-wall junction capacitance along the STI edge and C_{JSWSTI} the side-wall junction capacitance along the gate edge. The latter are bias-dependent since they depend on the drain-to-bulk voltage, but we can approximate them by their zero-bias values $C_{JSWSTI0}$, C_{JSWSTI} and $C_{JSWGAT0}$ which are larger.

We can split the junction capacitance C_{DBJ} among a component that scales with W and another that remains constant

$$C_{DBJ} = C_{DBJW} \cdot W + C_{DBJ0}, \tag{5.4}$$

where

$$C_{DBJW} = Z_{dif} \cdot C_J + C_{JSWSTI} + C_{JSWGAT}, \tag{5.5}$$
$$C_{DBJ0} = 2\, Z_{dif} \cdot C_{JSWSTI}. \tag{5.6}$$

The feedback capacitance is due to the overlap and fringing field capacitance which scale with W

$$C_F = C_{GDe} \cdot W, \tag{5.7}$$

where C_{GDe} is the extrinsic capacitance per unit width which is given by

$$C_{GDe} = C_{GDo} + C_{GDf}. \tag{5.8}$$

where C_{GDo} is the overlap capacitance per unit width and C_{GDf} is the fringing field capacitance per unit width.

The total transistor parasitic capacitance at the drain can then be written as

$$C_D = C_{D0} + C_{DW} \cdot W. \tag{5.9}$$

with

$$C_{DW} = Z_{dif} \cdot C_J + C_{JSWSTI} + C_{JSWGAT} + C_{GDo} + C_{GDf}, \tag{5.10}$$
$$C_{D0} = C_{DBJ0} = 2\, Z_{dif} \cdot C_{JSWSTI}. \tag{5.11}$$

The total load capacitance at the output is then given by

$$C_{out} = C_{L0} + C_{DBJ} + C_F \tag{5.12}$$

which can be split into a compoenent that scales with W and a constant part

$$C_{out} = C_{DW} \cdot W + C_{out0} \tag{5.13}$$

with

$$C_{out0} = C_{L0} + C_{D0}. \tag{5.14}$$

In order to achieve a certain bandwidth we need to have a certain transconductance for a certain load capacitance. In order to maximize the current efficiency, we should bias the transistor in weak inversion. This leads to a large transistor and therefore large parasitic capacitances which will impact the bandwidth. Imposing the bandwidth, at some point the capacitance becomes so large that it is no more possible to achieve the required transconductance in weak inversion for the desired bandwidth. Does this mean that there is a minimum current for the OL CS amplifier to achieve a certain gain-bandwidth product?

To answer this question we need to solve the following set of equations for I_b and W assuming a given length L

$$\omega_u = \frac{G_m}{C_{out}}, \tag{5.15}$$
$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{5.16}$$
$$C_{out} = C_{DW} \cdot W + C_{out0}, \tag{5.17}$$
$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{5.18}$$

Solving for I_b and W/L, assuming a long-channel (i.e. $\lambda_c = 0$), leads to the following normalized solutions

$$i_b \triangleq \frac{I_b}{I_{pec\square} \cdot \Omega} = \frac{IC}{g_{ms}(IC) - \Theta}, \tag{5.19}$$

$$AR \triangleq \frac{W/L}{\Omega} = \frac{1}{g_{ms} - \Theta}, \tag{5.20}$$

where

$$\Omega \triangleq \frac{\omega_u}{\omega_L}, \tag{5.21}$$

$$\omega_L \triangleq \frac{I_{spec\square}}{nU_T \cdot C_{out0}}, \tag{5.22}$$

$$\Theta \triangleq \frac{\omega_u}{\omega_W}, \tag{5.23}$$

$$\omega_W \triangleq \frac{I_{spec\square}}{nU_T \cdot C_{DW} \cdot L}. \tag{5.24}$$

The normalized current i_b is plotted Figure 5.2 for different values of Θ.

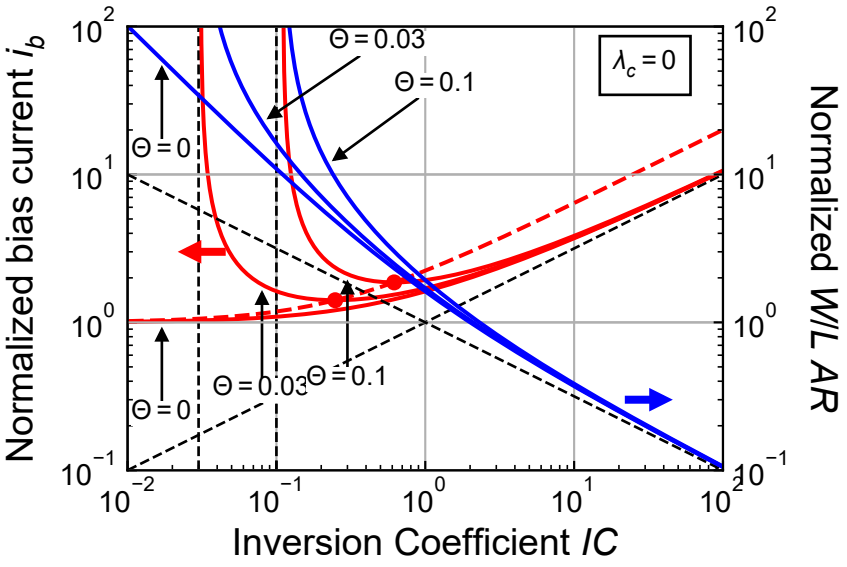

Figure 5.2: Normalized bias current and aspect ratio versus inversion coefficient including the self-loading capacitances at the drain.

From Figure 5.2 and Figure 5.3, we clearly see that there is a minimum current for a given value of parameter Θ. We can find the optimum inversion coefficient IC_{opt} which is given by

$$IC_{opt} = \left(\sqrt{\Theta \cdot (1+\Theta)} + \Theta + \frac{1}{2}\right)^2 - \frac{1}{4} = 2\Theta \cdot (1+\Theta) + (1+2\Theta) \cdot \sqrt{\Theta \cdot (1+\Theta)}. \tag{5.25}$$

Note that IC_{opt} only depends on parameter θ. Often $\Theta \ll 1$ and IC_{opt} simplifies to

$$IC_{opt} \cong 2\Theta + \sqrt{\Theta}. \tag{5.26}$$

From Figure 5.2 and Figure 5.3, we also see that there is a minimum inversion coefficient IC_{lim} below which the desired gain-bandwidth product GBW can no more be achieved

$$IC_{lim} = \Theta \cdot (1+\Theta) \cong \Theta, \tag{5.27}$$

which is about equal to Θ for small values of Θ.

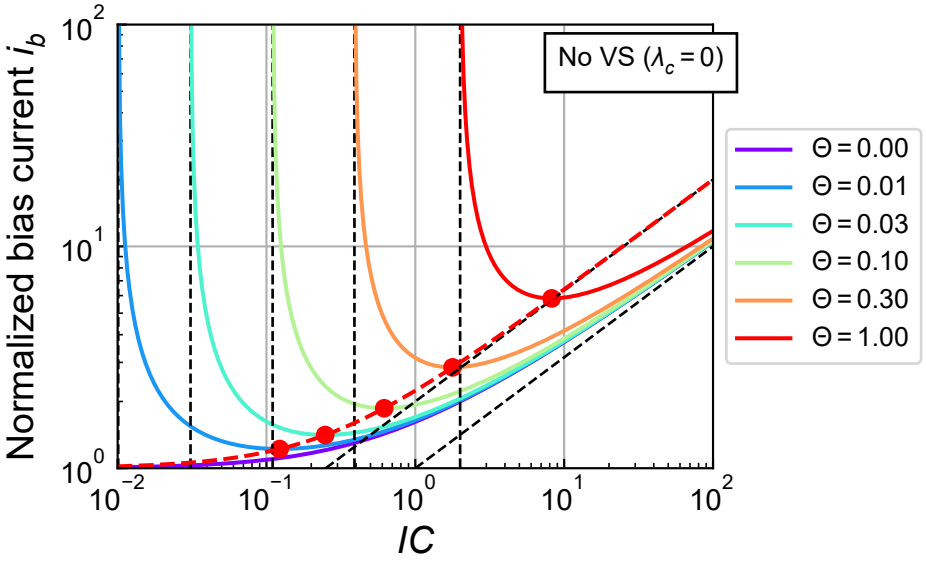

Figure 5.3: Normalized bias current versus inversion coefficient including the self-loading capacitances at the drain.

The optimum normalized current is given by

$$i_{bopt} \triangleq i_b(IC_{opt}) = 1 + 2\Theta + 2\sqrt{\Theta \cdot (1+\Theta)}. \tag{5.28}$$

Parameter Θ can be eliminated from equations (5.28) and (5.25) resulting in an expression of i_{bopt} in terms of IC_{opt}

$$i_{bopt} = \sqrt{4IC_{opt} + 1} \tag{5.29}$$

which is plotted in Figure 5.3 as a dashed red line.

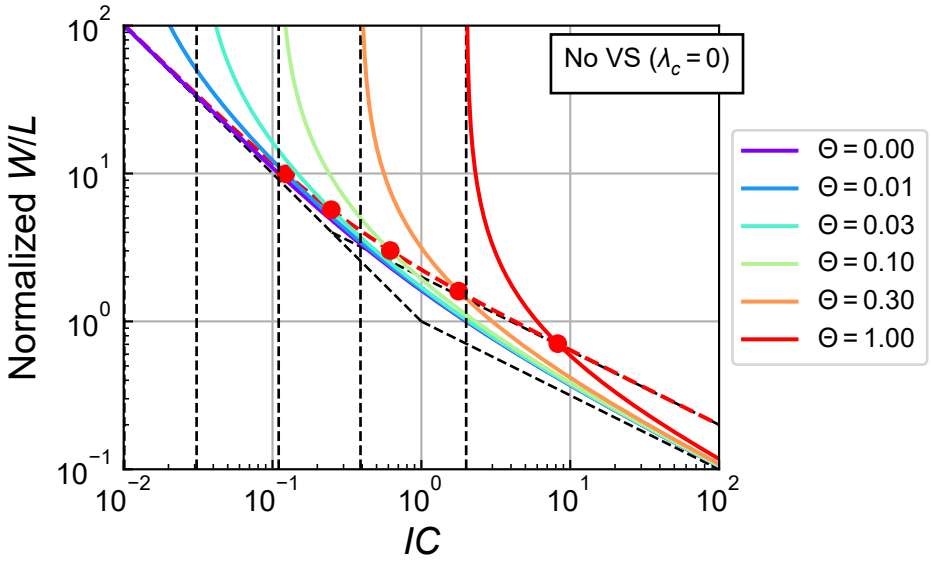

Figure 5.4: Normalized aspect ratio versus inversion coefficient including the self-loading capacitances at the drain.

From Figure 5.4, we see from the above plot that the transistor width increases first as $1/\sqrt{IC}$ in strong inversion and then as $1/IC$ in weak inversion making the transistor quickly very large until IC reaches IC_{lim} where the width becomes infinity. The dots correspond to the AR obtained for IC_{opt}.

The above analysis was done assuming a long-channel transistor (i.e. $\lambda_c = 0$). There is unfortunatly no closed form expression for the optimum inversion coefficient when including the short-channel effects (i.e. setting $\lambda_c > 0$). However we can plot the normalized bias current i_b versus IC accounting for the short-channel effects. The result is plotted in Figure 5.5. We can observe that the optimum inversion coefficient IC_{opt} corresponding to the minimum bias current does change significantly for λ_c varying from 0 to 1 (the latter value being beyond the usual values of λ_c). The optimum inversion coefficient IC_{opt} is plotted versus the parameter Θ in Figure 5.6 for λ_c ranging from 0 to 1. From Figure 5.6, we can obeserve that the impact of short-channel effects is rather limited particularly for reasonable values of λ_c (λ_c is rarely larger than 0.4). We can therefore use the long-channel expression of the optimum inversion coefficient IC_{opt} and get close to the minimum bias current even for short channel transistors.

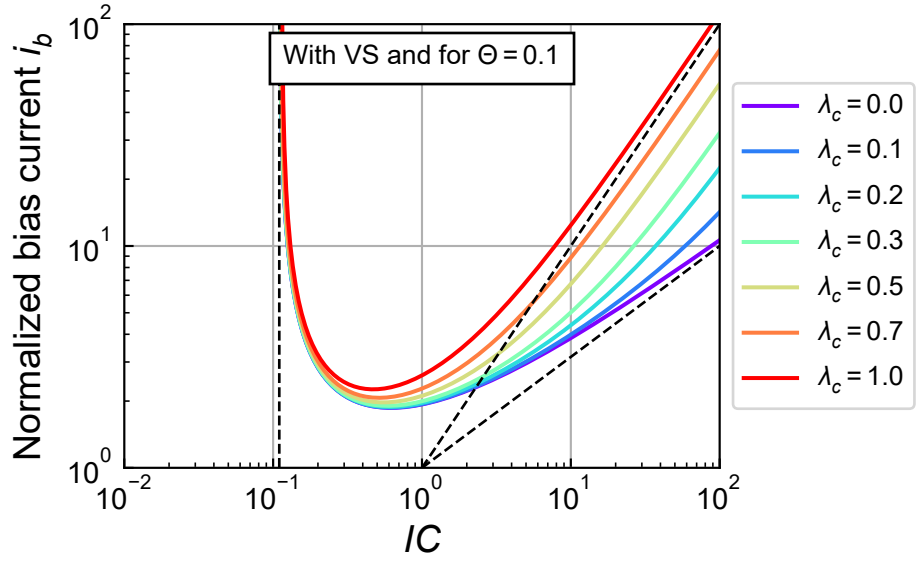

Figure 5.5: Normalized bias current versus inversion coefficient for various velocity saturation parameter λ_c.

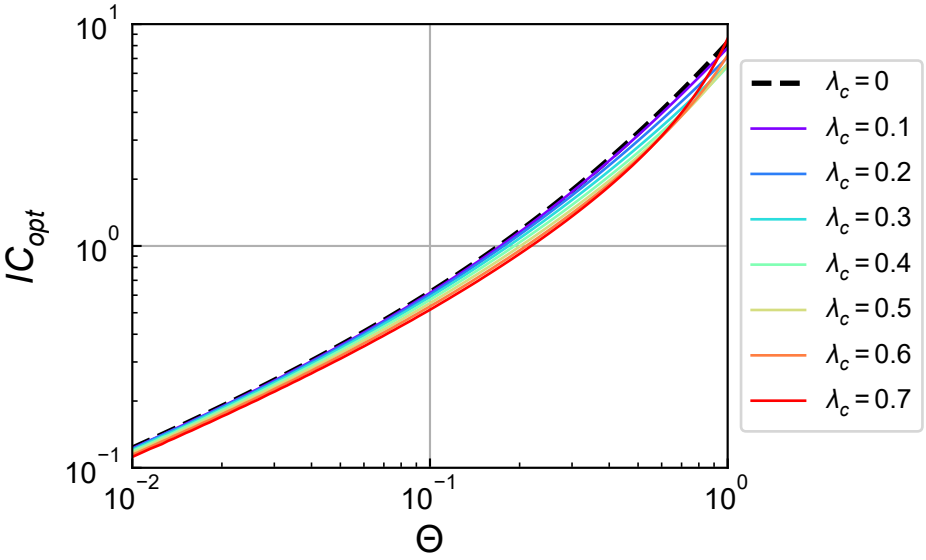

Figure 5.6: Optimum inversion coefficient versus Θ for different velocity saturation parameter λ_c.

5.2 Examples

5.2.1 Process

We want to size a CS gain stage to achieve a certain gain-bandwidth GBW for a given transistor length L and constant load capacitance C_{L0}. We select the open source IHP 130nm CMOS technology [4]. The PDK uses the PSP 103.6 MOSFET compact model for the MOS part of the technology [5]. The process parameters are given in Table 5.1 and the transistor parameters in Table 5.2.

> **Note**
>
> The parameters given in Table 5.2 are a mix of parameters taken from the PSP model library and others (mostly the sEKV parameters) extracted from I_D-V_G and I_D-V_D data (this is done in another notebook).

Table 5.1: Process parameters.

Parameter	Value	Unit	Comment
t_{ox}	2.24	nm	SiO_2 oxyde thickness
C_{ox}	15.413	$\frac{fF}{\mu m^2}$	Oxyde capacitance per unit area
V_{DD}	1.2	V	Nominal supply voltage
L_{min}	130	nm	Minimum drawn gate length
W_{min}	150	nm	Minimum drawn gate width
z_1	340	nm	Minimum outer diffusion width
z_2	389	nm	Minimum diffusion width between two fingers

Table 5.2: Transistors parameters.

Parameter	nMOS	pMOS	Unit
Length and width correction parameters for current			
DL	59	-46	nm
DW	-20	30	nm
Length and width correction for intrinsic and overlap capacitances			
$DLCV$	73	49	nm
$DWCV$	-10	15	nm
Length and width correction parameter for fringing capacitances			
$DLGCV$	14	-1	nm
$DWGCV$	10	-15	nm
Long-channel sEKV parameters parameters			
n	1.22	1.23	-
$I_{spec\square}$	708	245	nA
V_{T0}	246	365	mV
Short-channel sEKV parameters parameters			
L_{sat}	0	0	nm
λ	1.384	14.271	$\frac{V}{\mu m}$
Junction capacitances parameters			
C_J	0.976	0.863	$\frac{fF}{\mu m^2}$
C_{JSWSTI}	0.025	0.032	$\frac{fF}{\mu m}$
C_{JSWGAT}	0.03	0.027	$\frac{fF}{\mu m}$
Overlap capacitances parameters			

Table 5.2: Transistors parameters.

Parameter	nMOS	pMOS	Unit
C_{GSo}	0.453	0.443	$\frac{fF}{\mu m}$
C_{GDo}	0.453	0.443	$\frac{fF}{\mu m}$
C_{GBo}	0	0.022	$\frac{fF}{\mu m}$
Fringing capacitances parameters			
C_{GSf}	0.2	0.1	$\frac{fF}{\mu m}$
C_{GDf}	0.2	0.1	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	2.352e-24	8.508e-24	VAs
AF	1	1	-
ρ	0.009206	0.0333	$\frac{Vm^2}{As}$

We start below with the nMOS case.

5.2.2 nMOS

5.2.2.1 Design

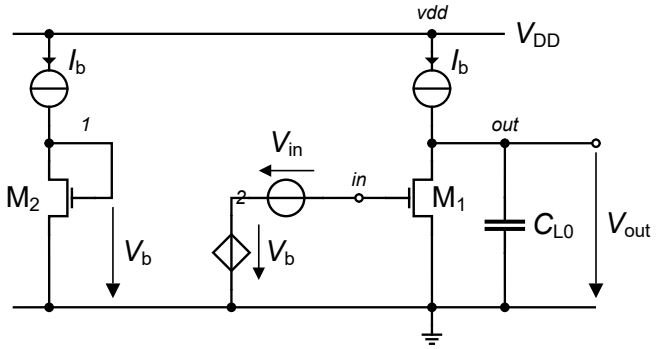

Figure 5.7: Schematic of the open-loop common-source (CS) gain stage used for simulation.

The schematic that is used for the simulations is shown in Figure 5.7. Note that a bias transistor M_2 has been added to correctly set the DC gate voltage of M_1 so that its drain current is equal to I_b by means of a VCVS as shown in Figure 5.7

Since the transistor is biased in saturation, the intrinsic gate-to-drain capacitance C_{GDi} can be considered as zero. The feedback capacitance C_F is therefore made of the overlap C_{GDo} and fringing capacitances C_{GDf}, so that $C_F \cong C_{GDo} + C_{GDf}$. Note that, since the DC gate voltage is constant it is an AC ground and hence C_F adds to the total load capacitance. Since both C_{GDo} and C_{GDf} scale with W, we need to add it to C_{DW} which is now given by

$$C_{DW} = Z_{dif} \cdot C_J + C_{JSWSTI} + C_{JSWGAT} + C_{GDo} + C_{GDf}. \tag{5.30}$$

Since we don't know the drain voltage across the junction capacitance, we will use its zero-bias values which is anyway larger than the actual value. The technology parameters we will need are summarized in Table 5.3. From Table 5.3, we observe that C_{D0} is actuall very small.

The specifications are given in Table 5.4, where we have chosen a long-channel transistor to be consistent with the theory and the resulting design equations. Note that, as shown in Figure 5.5 and Figure 5.6, short-channel effects like velocity saturation have a mˆlimited impact on the value of IC_{opt}. We can

therefore use the long-channel expressions even for short-channel transistors still getting close to the minimum bias current.

Table 5.3: Required process parameters (nMOS).

Parameter	Value	Unit
V_{DD}	1.2	V
n	1.22	-
$I_{spec\square}$	708	nA
C_{DW}	1.041	$\frac{fF}{um}$
C_{D0}	0.017	fF

Table 5.4: Specifications.

Parameter	Value	Unit
GBW	100	MHz
L	1	μm
C_{L0}	20	fF
C_L	20.017	fF

We can now calculate the optimum inversion coefficient, optimum bias current and optimum width. The calculated parameters are given in Table 5.5.

Table 5.5: Calculated parameters (nMOS).

Parameter	Value	Unit
f_L	178.394	MHz
f_W	3.431	GHz
Ω	0.561	-
θ	0.029	-
IC_{opt}	0.243	-
$i_{b,opt}$	1.405	-
AR_{opt}	5.774	-
$\left(\frac{W}{L}\right)_{opt}$	3.237	-
$I_{b,opt}$	557	nA
W_{opt}	3.24	μm
$G_{m,opt}$	14.694	$\frac{\mu A}{V}$
$C_{D,opt}$	3.369	fF
AD	1.1	μm^2
PD	7.153	μm
C_{DBJ}	1.271	fF
$C_{DBJ,bot}$	1.074	fF
$C_{DBJ,SWSTI}$	0.099	fF
$C_{DBJ,SWGAT}$	0.097	fF
C_{GDo}	1.468	fF
C_{GDf}	0.647	fF
C_{GDe}	2.115	fF
C_F	2.115	fF
C_{out}	23.386	fF
f_z	1.106	GHz

From Table 5.5, we see that the optimum inversion coefficient for a minimum bias current is in the lower side of moderate inversion. We also end-up with a large transistor, but still an acceptable value.

We can now estimate the output conductance as $G_{ds} = 402.802\ nA/V$. From the transconductance $G_m = 14.694\ \mu A/V$ we get the DC gain $A_{dc} = 36.479$ or in dB $A_{dc} = 31.2\ dB$. The CS estimated open-loop transfer function is shown in Figure 5.8.

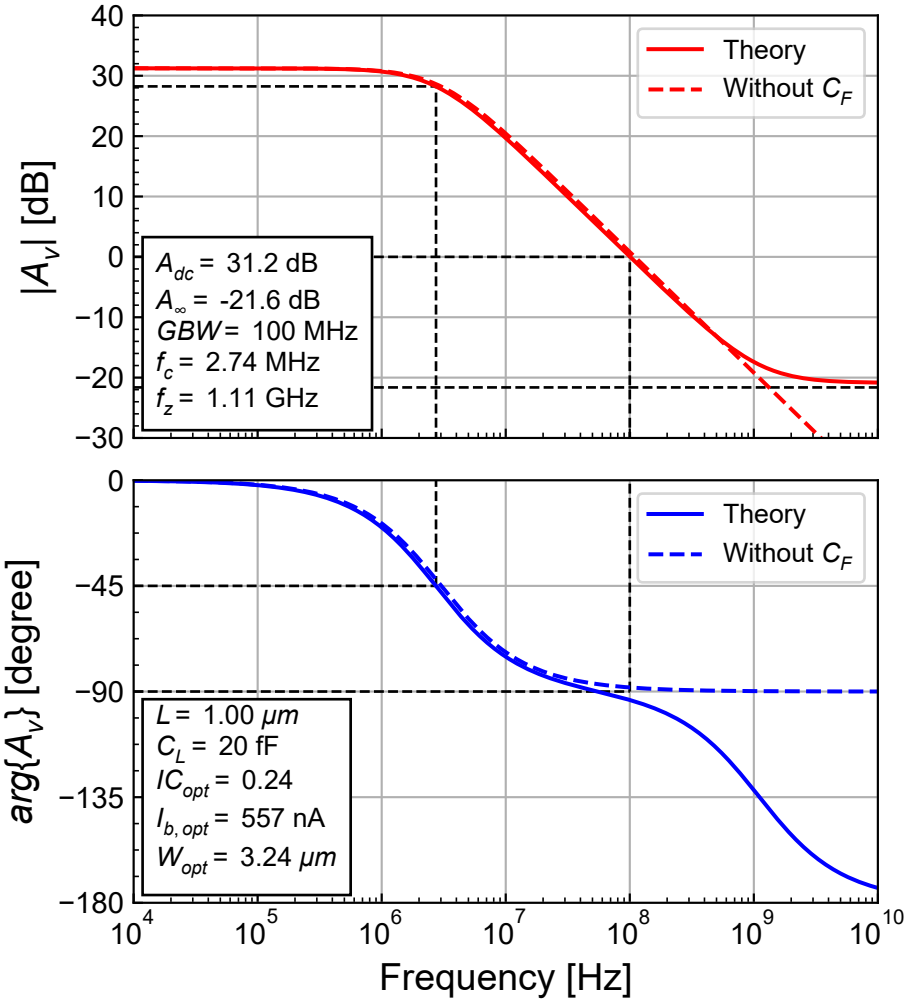

Figure 5.8: Transfer function (nMOS).

We can now proceed with the simulations.

5.2.2.2 ngspice simulations

We start checking the DC operating point by first looking at the drain current I_D, gate transconductance G_m, output conductance G_{ds} and DC gain A_{dc}. The values extracted from the simulation (PSP) are compared to the theoretical prediction in Table 5.6.

Table 5.6: Simulated drain current and small-signal parameter values compared to theoretical values.

	$I_D\,[nA]$	$G_m\,[\mu A/V]$	$G_{ds}\,[nA/V]$	A_v
Theory	557	14.694	402.802	31.241
PSP	557	14.712	633.288	27.321

From Table 5.6, we see that the values extracted from PSP are very close to the theoretical values, except for the output conductance. We now compare the simulated values of the overlap and fringing capacitances to the theoretical estimation in Table 5.7.

Table 5.7: Simulated overlap and fringing capacitances values compared to theoretical values.

	$C_{GSo}\,[fF]$	$C_{GDo}\,[fF]$	$C_{GSf}\,[fF]$	$C_{GDf}\,[fF]$	$C_{GSe}\,[fF]$	$C_{GDe}\,[fF]$
Theory	1.463	1.463	0.649	0.649	2.113	2.113
PSP	1.473	1.473	0.645	0.645	1.998	1.959

The two first columns C_{GSo} and C_{GDo} correspond to the zero-bias overlap capacitances, whereas the third and fourth columns C_{GSf} and C_{GDf} correspond to the zero-bias fringing capacitances. Finally, the theoretical C_{GSe} and C_{GDe} correspond to the sum of the zero-bias overlap and fringing capacitances, whereas for PSP it includes the bias dependence. We see that the estimated zero-bias values of the overlap and fringing capacitance are very close to those extracted from PSP, whereas the bias-dependent values of the total extrinsic capacitances extracted from PSP are slightly smaller and asymmetrical (this is certainly due to the bias dependence which is very different for the drain and the source).

We finally look at the junction capacitances. The theoretical values of the junction capacitances are compared to the values extracted from PSP in Table 5.8 and Table 5.9. Table 5.8 compares the zero-bias values whereas Table 5.9 compares the theoretical zero-bias values to the actual values accounting for the junction bias voltage extracted from PSP.

Table 5.8: Simulated zero-bias junction capacitances values compared to theoretical values.

	$C_{Jbot}(0)\,[fF]$	$C_{JSWSTI}(0)\,[fF]$	$C_{JSWGAT}(0)\,[fF]$	$C_{Jtot}(0)\,[fF]$
Theory	1.071	0.099	0.097	1.267
PSP	1.079	0.099	0.097	1.275

Table 5.9: Simulated actual junction capacitances values compared to theoretical zero-bias values.

	$C_{Jbot}\,[fF]$	$C_{JSWSTI}\,[fF]$	$C_{JSWGAT}\,[fF]$	$C_{Jtot}\,[fF]$
Theory	1.071	0.099	0.097	1.267
PSP	1.001	0.093	0.093	1.188

From Table 5.8, we see that the estimated zero-bias junction capacitances, including bottom and side-wall components, are very close to those extracted from PSP. As expected, the actual values including the effect of bias in PSP and shown in Table 5.9, are slightly lower than the zero-bias theoretical values.

From the values of the transconductance and capacitances, we can now estimate the GBW.

Table 5.10: Comparison of the simulated and predicted values of the gain-bandwidth and zero frequency.

	$G_m\,[\mu A/V]$	$C_{out}\,[fF]$	$C_F\,[fF]$	$GBW\,[MHz]$	$f_z\,[GHz]$	$A_\infty\,[dB]$
Theory	14.694	23.397	2.113	99.954	6.955	-21.637
PSP	14.712	23.164	1.959	101.083	7.5	-22.161

The theoretical and simulated values shown in Table 5.10 are very close. The theoretical GBW is almost on target as it should be (the slight difference comes from the recalculations of the effective

width). Because of the smaller capacitance values extracted from PSP, the GBW for PSP is larger than the estimated and the target values.

We can now proceed with the AC simulation.

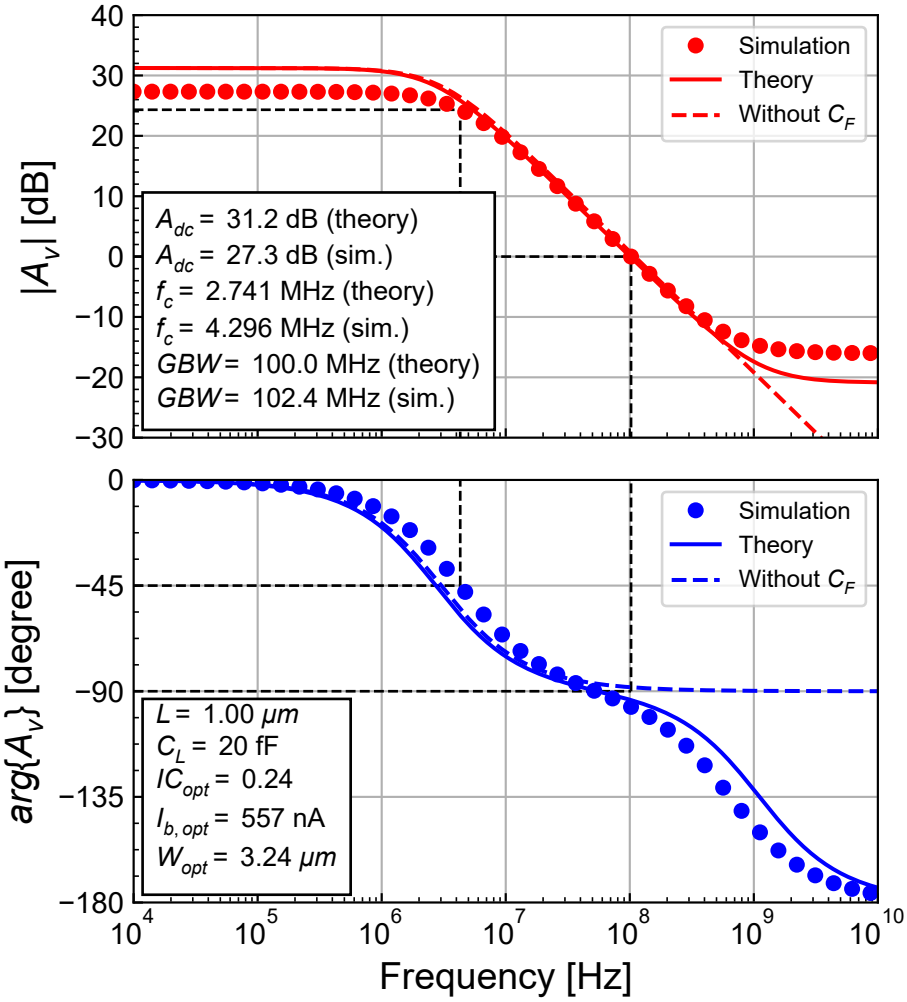

Figure 5.9: CS simulated open-loop transfer function compared to the theoretical prediction.

The result of the AC simulation is compared to the theoretical estimation in Figure 5.9. We see that the simulated GBW is slightly higher than the spec due to the lower extrinsic capacitances. We also see that the simulated DC gain is lower than the estimated one. This is due to the high output conductance of the nMOS transistor in this technology even for long-channel transistors. The zero is also lower than the theoretical value. This is a bit surpising because the simulated extrinsic capacitance that are extracted from the DC operating point is lower than the theoretical estimation. We will come back to this discrepancy in the next Section when looking at the pMOS implementation.

5.2.3 pMOS

5.2.3.1 Design

We now design the same CS gain stage but with a pMOS transistor. We use the same process with the pMOS parameters given in Table 5.2. C_{DW} and C_{D0} need to be recalculated for the pMOS transistor and are given in Table 5.11.

Table 5.11: Required process parameters (pMOS).

Parameter	Value	Unit
V_{DD}	1.2	V
n	1.23	-
$I_{spec\square}$	245	nA
C_{DW}	0.895	$\frac{fF}{um}$
C_{D0}	0.022	fF

The specifications are the same than for the nMOS case. They are recalled in Table 5.12.

Table 5.12: Specifications.

Parameter	Value	Unit
GBW	100	MHz
L	1	μm
C_{L0}	20	fF
C_L	20.022	fF

We can now calculate the optimum inversion coefficient, optimum bias current and optimum width. The calculated parameters are given in Table 5.13.

Table 5.13: Calculated parameters (pMOS).

Parameter	Value	Unit
f_L	61.217	MHz
f_W	1.369	GHz
Ω	1.634	-
θ	0.073	-
IC_{opt}	0.478	-
$i_{b,opt}$	1.706	-
AR_{opt}	3.572	-
$\left(\frac{W}{L}\right)_{opt}$	5.834	-
$I_{b,opt}$	683	nA
W_{opt}	5.83	μm
$G_{m,opt}$	15.862	$\frac{\mu A}{V}$
$C_{D,opt}$	5.224	fF
AD	1.984	μm^2
PD	12.349	μm
C_{DBJ}	2.08	fF
$C_{DBJ,bot}$	1.937	fF
$C_{DBJ,SWSTI}$	0.165	fF
$C_{DBJ,SWGAT}$	0.175	fF
C_{GDo}	2.582	fF
C_{GDf}	0.583	fF
C_{GDe}	3.166	fF
C_F	3.166	fF
C_{out}	25.246	fF
f_z	0.797	GHz

Because of the smaller $I_{spec\square}$ of the pMOS, we get a larger bias current and wider transistor than for the nMOS case.

We can now estimate the output conductance as $G_{ds} = 47.846\ nA/V$. From the transconductance $G_m = 15.862\ \mu A/V$ we get the DC gain $A_{dc} = 331.531$ or in dB $A_{dc} = 50.4\ dB$. We see that the DC gain of the pMOS is much higher than what we obtained for the nMOS. The CS estimated open-loop transfer function for the pMOS implementation is shown in Figure 5.10.

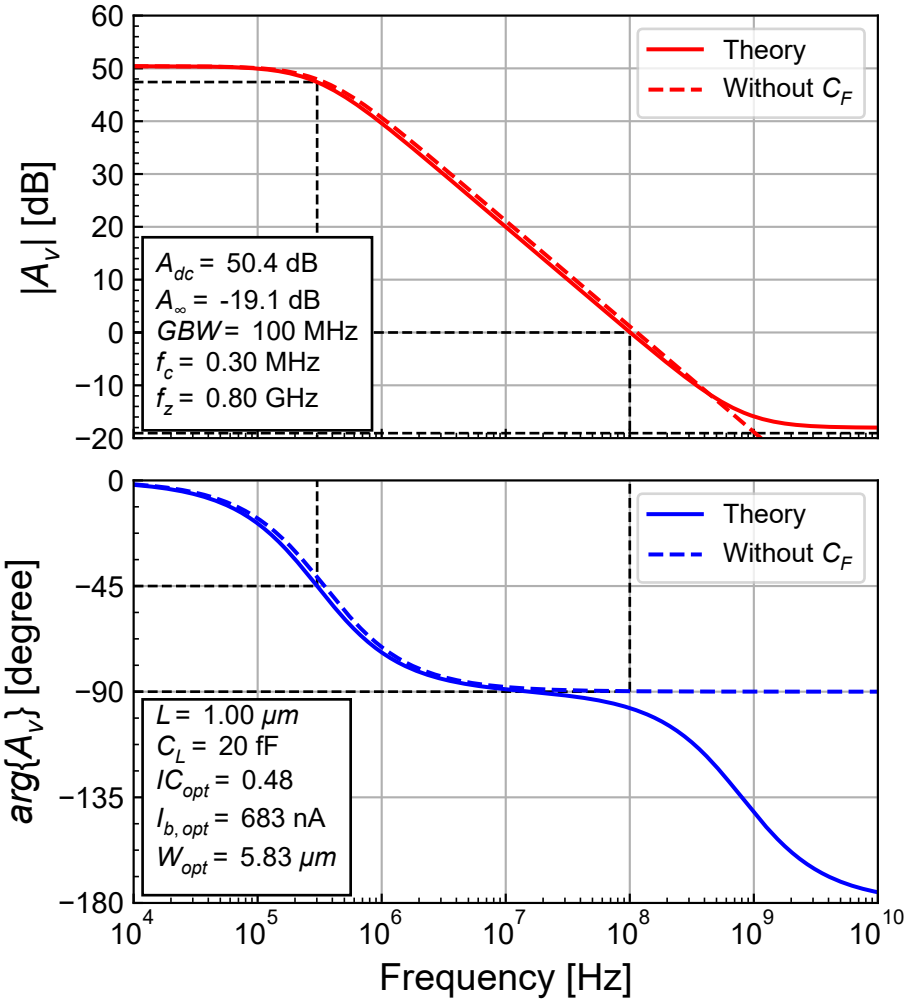

Figure 5.10: Theoretical transfer function (pMOS).

We can now proceed with the simulations.

5.2.3.2 ngspice simulations

We start checking the DC operating point by first looking at the drain current I_D, gate transconductance G_m, output conductance G_{ds} and DC gain A_{dc}. The values extracted from the simulation (PSP) are compared to the theoretical prediction in Table 5.14.

Table 5.14: Simulated drain current and small-signal parameter values compared to theoretical values (pMOS).

	$I_D\,[nA]$	$G_m\,[\mu A/V]$	$G_{ds}\,[nA/V]$	A_v
Theory	683	15.862	47.846	50.41
PSP	683	15.484	71.751	46.681

From Table 5.14, we see that the values extracted from PSP are very close to the theoretical values, even for the output conductance. We now compare the simulated values of the overlap and fringing capacitances to the theoretical estimation in Table 5.15.

Table 5.15: Simulated overlap and fringing capacitances values compared to theoretical values (pMOS).

	$C_{GSo}\,[fF]$	$C_{GDo}\,[fF]$	$C_{GSf}\,[fF]$	$C_{GDf}\,[fF]$	$C_{GSe}\,[fF]$	$C_{GDe}\,[fF]$
Theory	2.589	2.589	0.582	0.582	3.171	3.171
PSP	2.575	2.575	0.585	0.585	2.964	2.826

We see that the estimated zero-bias values of the overlap and fringing capacitance are very close to the values extracted from PSP, whereas the bias-dependent values of the total extrinsic capacitances extracted from PSP are slightly smaller and asymmetrical (this is due to the bias dependence which is very different for the drain and the source).

We finally look at the junction capacitances. The theoretical values of the junction capacitances are compared to the values extracted from PSP in Table 5.16 and Table 5.17. Table 5.16 compares the zero-bias values whereas Table 5.17 compares the theoretical zero-bias values to the actual values accounting for the junction bias voltage extracted from PSP.

Table 5.16: Simulated zero-bias junction capacitances values compared to theoretical values.

	$C_{Jbot}(0)\,[fF]$	$C_{JSWSTI}(0)\,[fF]$	$C_{JSWGAT}(0)\,[fF]$	$C_{Jtot}(0)\,[fF]$
Theory	1.716	0.208	0.16	2.085
PSP	1.721	0.208	0.16	2.09

Table 5.17: Simulated actual junction capacitances values compared to theoretical zero-bias values.

	$C_{Jbot}\,[fF]$	$C_{JSWSTI}\,[fF]$	$C_{JSWGAT}\,[fF]$	$C_{Jtot}\,[fF]$
Theory	1.716	0.208	0.161	2.086
PSP	1.511	0.2	0.139	1.85

From Table 5.16 and Table 5.17, we observe that the estimated values of the zero-bias junction capacitances, including bottom and side-wall components, are almost equal to the values extracted from PSP. As expected, the actual values including the effect of bias in PSP are slightly lower than the zero-bias zero-bias theoretical values.

From the values of transconductance and capacitances, we can now estimate the GBW.

Table 5.18: Comparison of the simulated and predicted values of the gain-bandwidth and zero frequency.

	$G_m\,[\mu A/V]$	$C_{out}\,[fF]$	$C_F\,[fF]$	$GBW\,[MHz]$	$f_z\,[GHz]$	$A_\infty\,[dB]$
Theory	15.862	25.278	3.171	99.873	5.003	-19.058
PSP	15.484	24.698	2.826	99.778	5.612	-19.77

The theoretical and simulated values shown in Table 5.18 are very close. The theoretical GBW is almost on target as it should be (the slight difference comes from the recalculations of the effective width).

We can now proceed with the AC simulation.

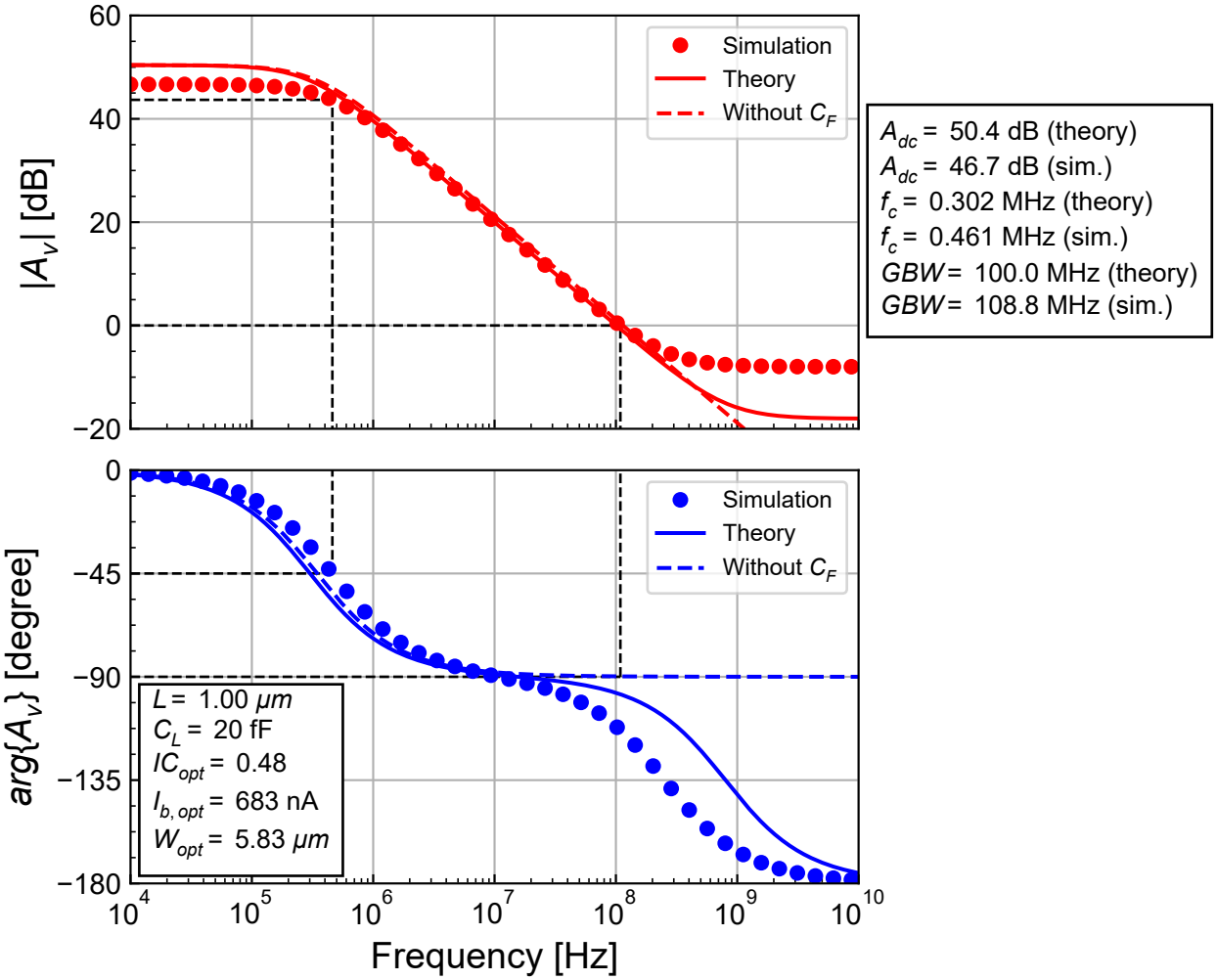

Figure 5.11: CS simulated open-loop transfer function compared to the theoretical prediction (pMOS).

From Figure 5.11, we see that the simulated GBW is slightly higher than the estimated value and the spec. This is probably due to the effect of the nearby zero and the lower extrinsic capacitances. We also see that the simulated DC gain is slightly lower than the estimated one. The zero is also lower than the theoretical value. This is coming from the fact that we have a rather long pMOS transistor and therefore the quasi-static frequency, which is scaling like $1/L^2$, is probably at the level of the zero introduced by the feedback capacitor. We can have a better estimation of the transfer function accounting for the quasi-static time constant by replacing G_m by

$$Y_m(s) = G_m \cdot (1 - s \cdot \tau_{qs}) = G_m \cdot \left(1 - \frac{s}{\omega_{qs}}\right), \tag{5.31}$$

where $\tau_{qs} = 1/\omega_{qs}$ is the quasi-static time constant and ω_{qs} the quasi-static frequency which delimits the frequency range above which the operation of the transistor can no more be considered as quasi-static, but becomes non-quasi-static (NQS). The quasi-static time constant τ_{qs} is given by

$$\tau_{qs} = \frac{C_m}{G_m}, \tag{5.32}$$

where C_m is the gate transcapacitance which is a fraction of the total gate capacitance $W\,L\,C_{ox}$ given by

$$\frac{C_m}{W\,L\,C_{ox}} = \frac{q_s - q_d}{15} \cdot \frac{4q_s^2 + 4q_d^2 + 12q_sq_d + 10q_s + 10q_d + 5}{(q_s + q_d + 1)^3}. \tag{5.33}$$

In saturation $q_d = 0$ and C_m reduces to

$$\frac{C_m}{W\,L\,C_{ox}} = \frac{q_s}{15}\,\frac{4q_s^2 + 10q_s + 5}{(q_s + 1)^3} \tag{5.34}$$

In strong inversion $q_s \gg 1$ and C_m saturates to

$$\frac{C_m}{W\,L\,C_{ox}} \cong \frac{4}{15}, \tag{5.35}$$

whereas in weak inversion $q_s \ll 1$ and C_m simplifies to

$$\frac{C_m}{W\,L\,C_{ox}} \cong \frac{q_s}{3}. \tag{5.36}$$

Since the transconductance in weak inversion is given by

$$G_m = \frac{G_{spec}}{n} \cdot q_s, \tag{5.37}$$

the quasi-static time constant τ_{qs} in weak inversion becomes bias independent

$$\tau_{qs} \cong \frac{L^2}{6\mu\,U_T} \tag{5.38}$$

and scales as L^2 and is inversely proportionnal to the mobility μ. This explains why for a long-channel pMOS transistor, the quasi-static frequency may become low.

We can now estimate the transcapacitance for this particular design as $C_m = 7.715\ fF$ and the corresponding quasi-static frequency as $f_{qs} = 327.251\ MHz$. We see that C_m is even larger than the extrinsic feedback capacitance and therefore cannot be neglected. The quasi-static frequency is just 3 times the target GBW and hence the transcapacitance cannot be neglected.

The transfer function accounting for the transcapacitance is still given by the same expression, which is repeated below

$$A(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = A_{dc} \cdot \frac{1 - s/\omega_z}{1 + s/\omega_p}. \tag{5.39}$$

However ω_z now includes the effect of the transcapacitance according to

$$A_{dc} = -G_m \cdot R_{ds}, \tag{5.40}$$

$$\omega_z = \frac{G_m}{C_F + C_m}, \tag{5.41}$$

$$\omega_p = \frac{1}{R_{ds}\,(C_F + C_L)}. \tag{5.42}$$

We see that C_m directly adds to C_F. This of course changes the position of the zero, but also the asymptotic high frequency value which now becomes

$$A_\infty \triangleq \lim_{s\to\infty} A(s) = \frac{C_F + C_m}{C_L + C_F} = \frac{1 + C_m/C_F}{1 + C_L/C_F}, \tag{5.43}$$

A_∞ can be estimated as A_∞ = 3.829e-01 or in dB A_∞ = -8.337 dB. We can now compare the simulations to the improved model accounting for the transcapacitance. The result is shown in Figure 5.12.

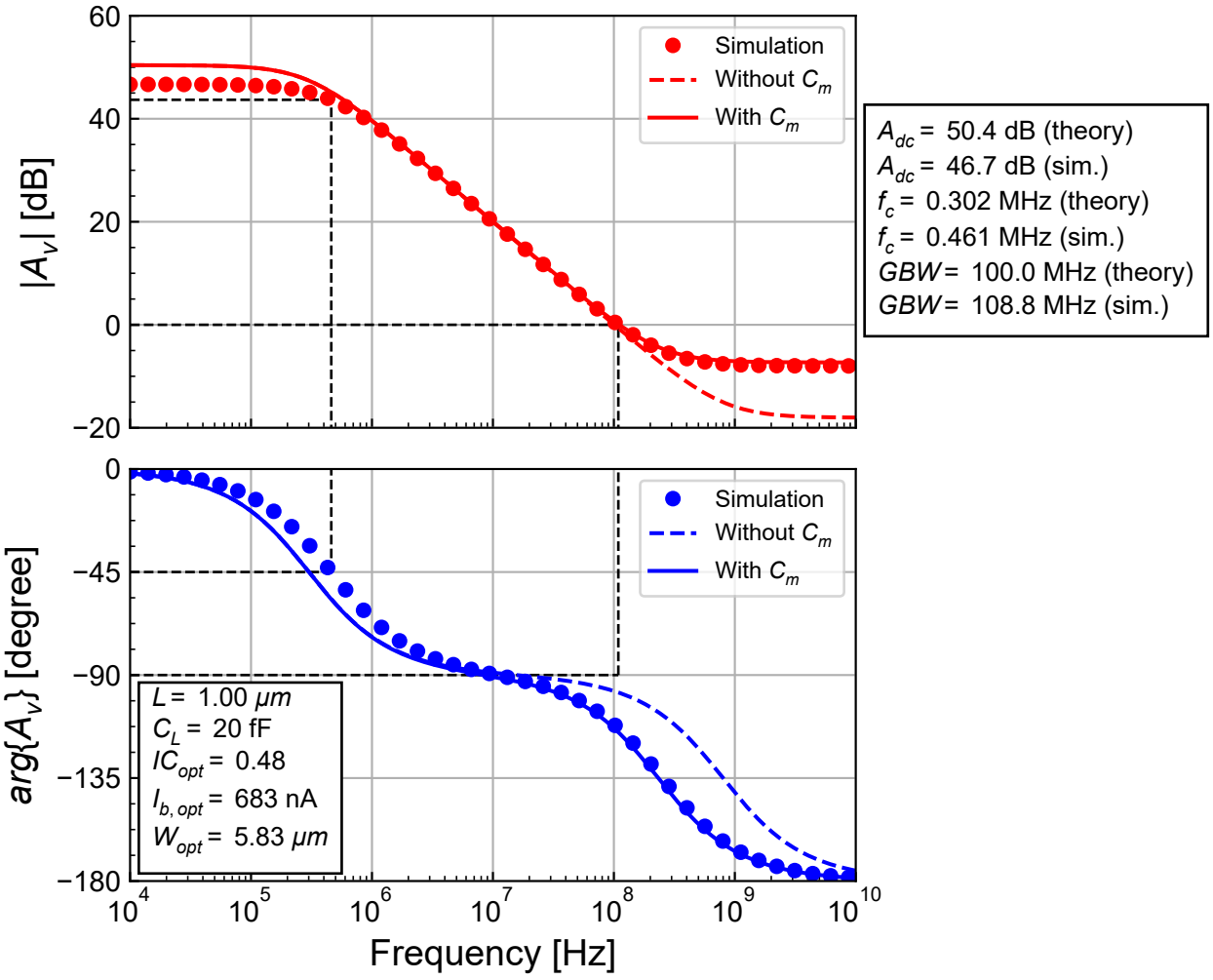

Figure 5.12: CS simulated open-loop transfer function compared to the theoretical prediction including the transcapacitance C_m.

From Figure 5.12, we see that we have now an almost perfect fit between the theoretical estimation including the effect of the transcapacitance C_m and the simulation.

It is worth mentioning that even if we have a good fit between theory and simulation, in reality the non-quasi-static (NQS) effects make the magnitude of the transadmittance Y_m to decrease fast and its

phase to turn quickly with respect to frequency above ω_{qs}. As $Y_m \to 0$, the gain then tends to

$$\lim_{s\to\infty} A(s) = \frac{C_F}{C_L + C_F}. \tag{5.44}$$

This can be verified by simulation by turning on the NQS model in PSP by setting $rfmode = 1$.

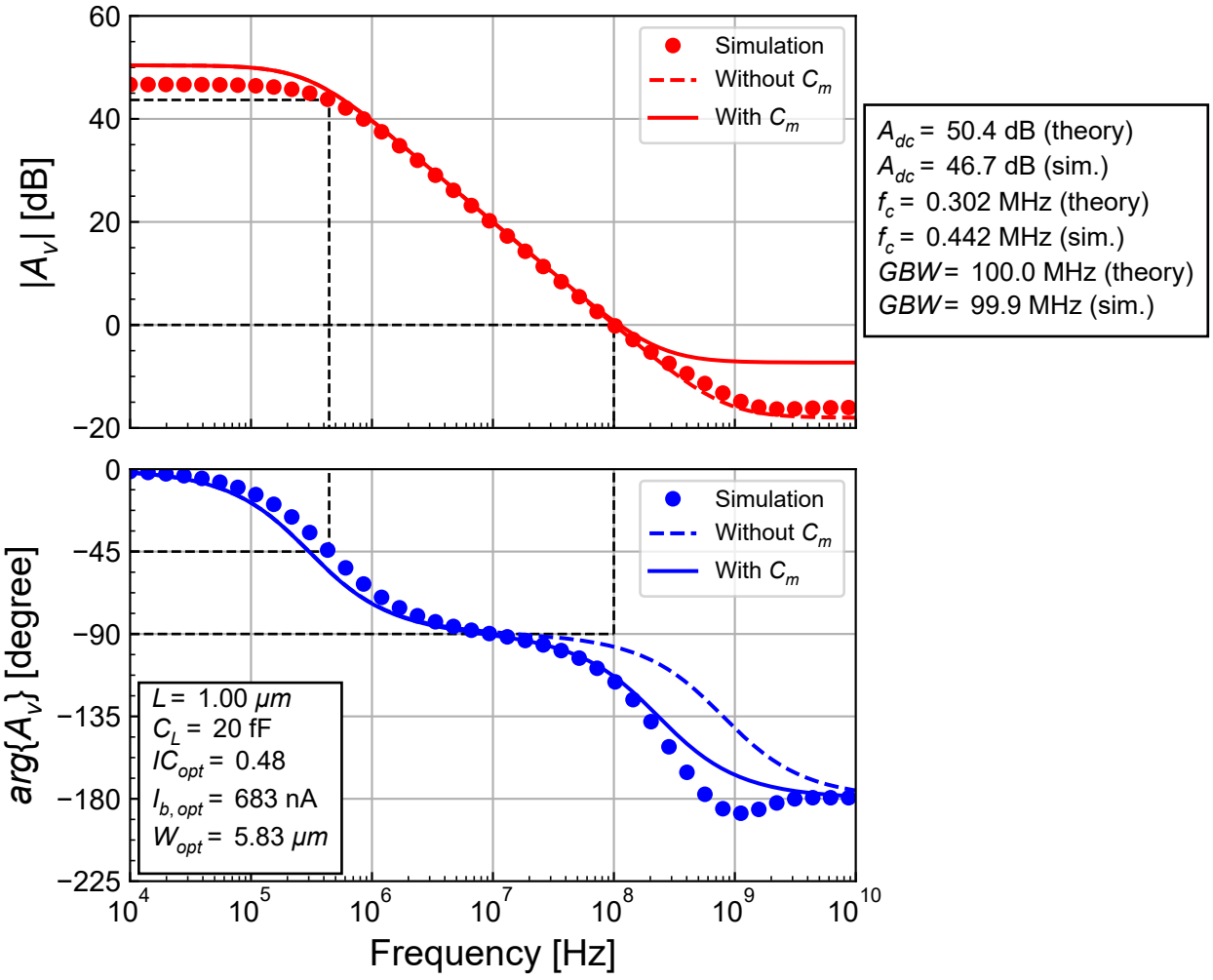

Figure 5.13: CS open-loop transfer function simulated with the NQS option in PSP and compared to the theoretical prediction with and without the transcapacitance C_m.

Figure 5.13 shows that now the magnitude tends indeed to $C_F/(C_F + C_L)$ as predicted by the initial model without C_m. We also see that the phase is quickly turning and then tending to $-180°$. In reality, the phase would continue to turn. This example shows that the PSP compact model without turning on the NQS option, does not give a correct result above ω_{qs}. To evaluate the impact of NQS we need to turn on the NQS option which approximates the NQS effect by splitting the channel into several pieces. This example shows the limit of the quasi-static model.

6 Minimum current for given GBW and DC gain

6.1 Analysis

We can actually use the additional degree of freedom, namely the transistor length L (which has been chosen arbitrarily in the previous example), to set the DC gain. To this purpose we can use the simple output conductance model (actually corresponding to channel length modulation only) given by

$$G_{ds} \cong \frac{I_D}{\lambda \cdot L}. \tag{6.1}$$

We now need to solve the following set of equations

$$\omega_u = \frac{G_m}{C_L} = \frac{G_m}{C_{L0} + C_{DW} \cdot W}, \tag{6.2}$$

$$A_{dc} = \frac{G_m}{G_{ds}} = \frac{G_m \cdot \lambda \cdot L}{I_b}, \tag{6.3}$$

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{6.4}$$

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{6.5}$$

for I_b, W, L and G_m. This leads to the following normalized results

$$i_b \triangleq \frac{I_b}{I_{norm}} = \frac{g_{ms} \cdot IC}{g_{ms}^2 - \xi \cdot IC} = \frac{g_{ms}/IC}{(g_{ms}/IC)^2 - \xi/IC}, \tag{6.6}$$

$$w \triangleq \frac{W}{W_{norm}} = \frac{IC}{g_{ms}^2 - \xi \cdot IC}, \tag{6.7}$$

$$\ell \triangleq \frac{L}{L_{norm}} = \frac{IC}{g_{ms}}, \tag{6.8}$$

where

$$\xi \triangleq \frac{C_{DW} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} \cdot A_{dc} \cdot \omega_u, \tag{6.9}$$

$$I_{norm} \triangleq n\, U_T \cdot C_{L0} \cdot \omega_u, \tag{6.10}$$

$$W_{norm} \triangleq \frac{C_{L0} \cdot (nU_T)^2}{I_{spec\square} \cdot \lambda} \cdot A_{dc} \cdot \omega_u, \tag{6.11}$$

$$L_{norm} \triangleq \frac{nU_T}{\lambda} \cdot A_{dc}. \tag{6.12}$$

The normalized current i_b, width w and length ℓ are plotted versus the inversion coefficient IC in Figure 6.1, Figure 6.2 and Figure 6.3, respectively. From Figure 6.1, we observe that similarly to the previous case, there is an optimium IC for which the bias current is minimum.

6.2 Examples

We now will design a CS stage imposing the GBW and the DC gain at the same time. We use the same technology with the parameters given in Table 5.1 and Table 5.2. We start with the case where the CS transistor is implemented with an nMOS transistor.

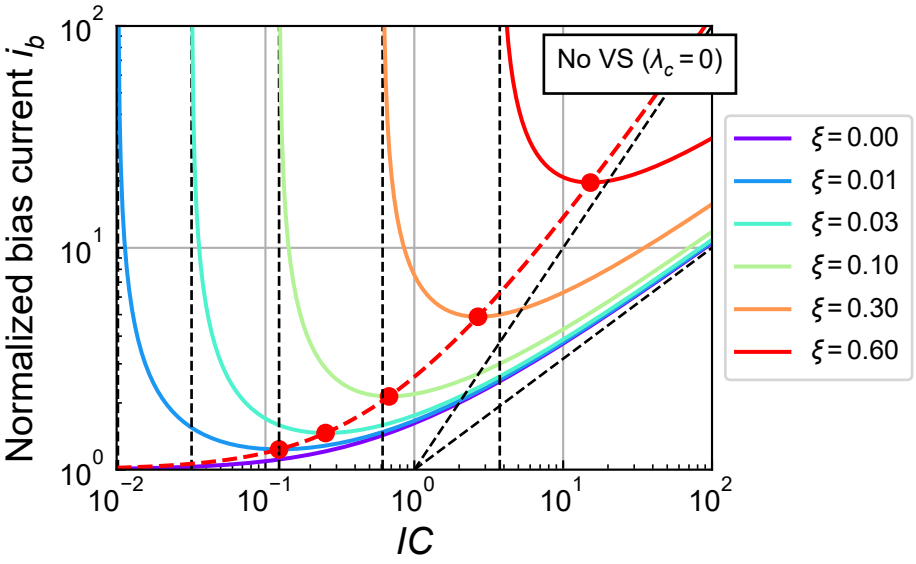

Figure 6.1: Normalized bias current versus inversion coefficient including the self-loading capacitances at the drain.

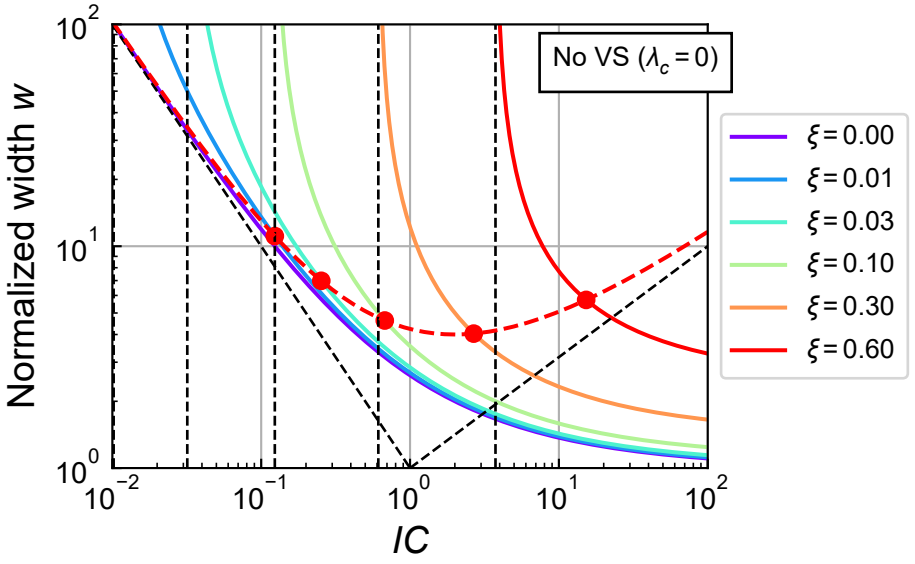

Figure 6.2: Normalized width versus inversion coefficient including the self-loading capacitances at the drain.

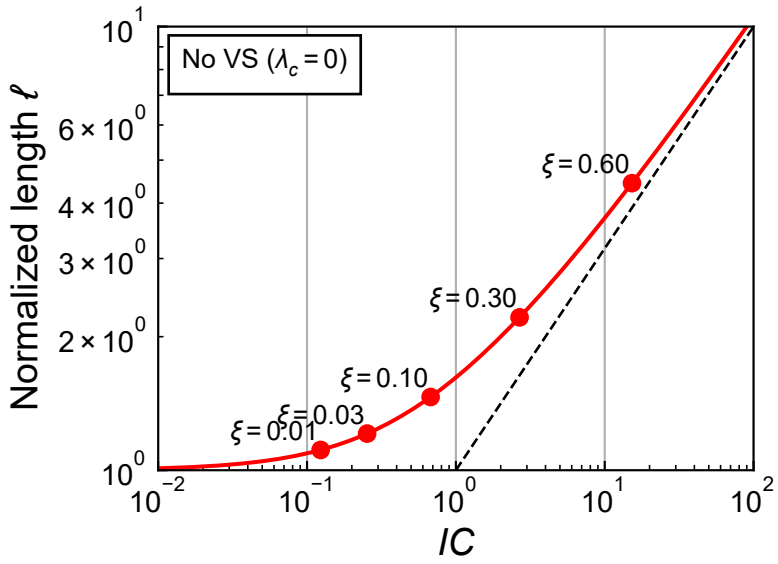

Figure 6.3: Normalized length versus inversion coefficient including the self-loading capacitances at the drain.

6.2.1 nMOS

6.2.1.1 Design

The process parameters that are needed to achieve the specifications given in Table 6.2 are given in Table 6.1. Notice that because of the high output conductance of nMOS transistors in this particular technology, we have chosen a moderate DC gain. The optimum inversion coefficient, optimum bias current, optimum width and optimum length are calculated in Table 6.3.

Table 6.1: Required process parameters (nMOS).

Parameter	Value	Unit
V_{DD}	1.2	V
n	1.22	-
$I_{spec\square}$	708	nA
λ	1.38	$\frac{V}{\mu m}$
C_{DW}	1.041	$\frac{fF}{um}$
C_{D0}	0.017	fF

Table 6.2: Specifications.

Parameter	Value	Unit
GBW	100	MHz
A_{dc}	25	dB
C_{L0}	20	fF
C_L	20.017	fF

Table 6.3: Calculated parameters (nMOS).

Parameter	Value	Unit
ξ	0.012	-
IC_{opt}	0.137	-
$i_{b,opt}$	1.259	-
w_{opt}	10.321	-
ℓ_{opt}	1.122	-
$g_{m,opt}$	1.122	-
I_{norm}	396.875	nA
W_{norm}	0.227	μm
L_{norm}	0.405	μm
$G_{m,norm}$	12.577	$\frac{\mu A}{V}$
$I_{b,opt}$	499.587	nA
W_{opt}	2.346	μm
L_{opt}	0.455	μm
$G_{m,opt}$	14.111	$\frac{\mu A}{V}$
$C_{D,opt}$	2.441	fF
AD	0.798	μm^2
PD	5.372	μm
C_{DBJ}	0.926	fF
$C_{DBJ,bot}$	0.779	fF
$C_{DBJ,SWSTI}$	0.076	fF
$C_{DBJ,SWGAT}$	0.07	fF
C_{GDo}	1.064	fF
C_{GDf}	0.469	fF
C_{GDe}	1.533	fF
C_F	1.533	fF
C_{out}	22.459	fF
f_z	1.465	GHz

We can now estimate the output conductance as $G_{ds} = 793.527\ nA/V$. From the transconductance $G_m = 14.111\ \mu A/V$, we get the DC gain $A_{dc} = 1.778\text{e+}01$ or in dB $A_{dc} = 25.0\ dB$, which is expected! The CS estimated open-loop transfer function is shown in Figure 6.4.

6.2.1.2 ngspice simulations

We now simulate the above design to check whether the design meets the specifications. We use the ngspice open source simulator [6].

Similarly to the previous design, we can first check the operating point informations. The drain current, transconductance and output conductance are given in Table 6.4 and the various capacitances are shown in Table 6.5, Table 6.6 and Table 6.7. Finally, the gain-bandwidth, zero frequency are given in Table 6.8. We observe that the estimated and simulated values are close.

Table 6.4: Simulated drain current and small-signal parameter values compared to theoretical values.

	$I_D\,[nA]$	$G_m\,[\mu A/V]$	$G_{ds}\,[nA/V]$	A_v
Theory	499.587	14.111	793.527	25
PSP	500	13.77	751.631	25.259

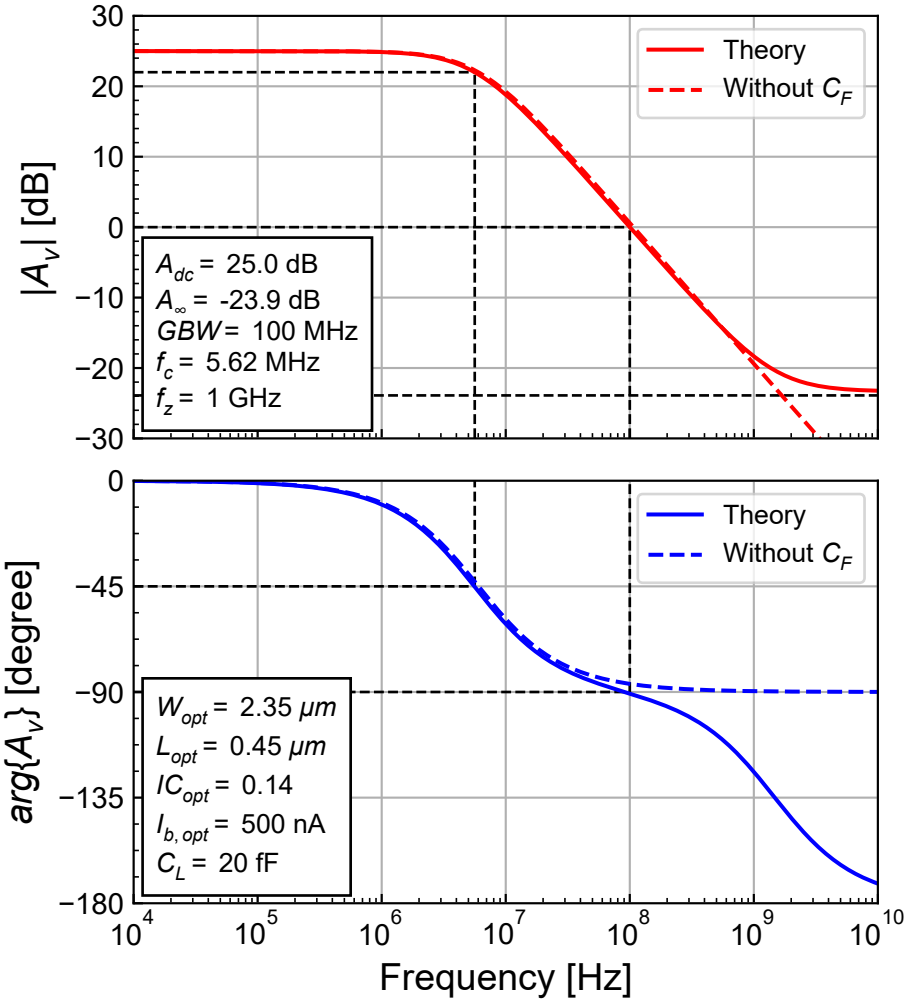

Figure 6.4: Transfer function (nMOS).

Table 6.5: Simulated overlap and fringing capacitances values compared to theoretical values.

	$C_{GSo}\,[fF]$	$C_{GDo}\,[fF]$	$C_{GSf}\,[fF]$	$C_{GDf}\,[fF]$	$C_{GSe}\,[fF]$	$C_{GDe}\,[fF]$
Theory	1.059	1.059	0.471	0.471	1.53	1.53
PSP	1.068	1.068	0.467	0.467	1.451	1.42

Table 6.6: Simulated zero-bias junction capacitances values compared to theoretical values.

	$C_{Jbot}(0)\,[fF]$	$C_{JSWSTI}(0)\,[fF]$	$C_{JSWGAT}(0)\,[fF]$	$C_{Jtot}(0)\,[fF]$
Theory	0.775	0.076	0.07	0.922
PSP	0.782	0.076	0.071	0.929

Table 6.7: Simulated actual junction capacitances values compared to theoretical zero-bias values.

	$C_{Jbot}\,[fF]$	$C_{JSWSTI}\,[fF]$	$C_{JSWGAT}\,[fF]$	$C_{Jtot}\,[fF]$
Theory	0.775	0.076	0.07	0.922
PSP	0.721	0.072	0.067	0.859

Table 6.8: Comparison of the simulated and predicted values of the gain-bandwidth and zero frequency.

	$G_m\,[\mu A/V]$	$C_{out}\,[fF]$	$C_F\,[fF]$	$GBW\,[MHz]$	$f_z\,[GHz]$	$A_\infty\,[dB]$
Theory	14.111	22.469	1.53	99.952	9.22	-23.908
PSP	13.77	22.297	1.42	98.293	9.935	-24.453

We can now proceed with the AC simulation. The simulation result is compared to the theoretical prediction in Figure 6.5. We see that the simulated GBW is slightly lower than the spec. This is due to the lower transconductance of PSP compared to sEKV. On the other hand the simulated DC gain and gain at high frequency are perfectly matching the theoretical estimations.

6.2.2 pMOS

We now design the same CS gain stage but with a pMOS transistor. Note that all the design equations remain the same.

6.2.2.1 Design

The process parameters that are needed to achieve the specifications given in Table 6.10 are given in Table 6.9. The optimum inversion coefficient, optimum bias current, optimum width and optimum length are calculated in Table 6.11.

Table 6.9: Required process parameters (nMOS).

Parameter	Value	Unit
V_{DD}	1.2	V
n	1.23	-
$I_{spec\square}$	245	nA
λ	14.27	$\frac{V}{\mu m}$

Table 6.9: Required process parameters (nMOS).

Parameter	Value	Unit
C_{DW}	0.895	$\frac{fF}{um}$
C_{D0}	0.022	fF

Table 6.10: Specifications.

Parameter	Value	Unit
GBW	100	MHz
A_{dc}	50	dB
C_{L0}	20	fF
C_L	20.022	fF

Table 6.11: Calculated parameters (nMOS).

Parameter	Value	Unit
ξ	0.052	-
IC_{opt}	0.38	-
$i_{b,opt}$	1.673	-
w_{opt}	5.7	-
ℓ_{opt}	1.294	-
$g_{m,opt}$	1.294	-
I_{norm}	400.218	nA
W_{norm}	1.152	μm
L_{norm}	0.705	μm
$G_{m,norm}$	12.58	$\frac{\mu A}{V}$
$I_{b,opt}$	669.689	nA
W_{opt}	6.564	μm
L_{opt}	0.912	μm
$G_{m,opt}$	16.273	$\frac{\mu A}{V}$
$C_{D,opt}$	5.878	fF
AD	2.232	μm^2
PD	13.808	μm
C_{DBJ}	2.338	fF
$C_{DBJ,bot}$	2.179	fF
$C_{DBJ,SWSTI}$	0.183	fF
$C_{DBJ,SWGAT}$	0.197	fF
C_{GDo}	2.905	fF
C_{GDf}	0.656	fF
C_{GDe}	3.562	fF
C_F	3.562	fF
C_{out}	25.899	fF
f_z	0.727	GHz

We can now estimate the output conductance as $G_{ds} = 51.460\ nA/V$. From the transconductance $G_m = 16.273\ \mu A/V$, we get the DC gain $A_{dc} = 3.162\text{e+}02$ or in dB $A_{dc} = 50.0\ dB$, which is expected! The CS estimated open-loop transfer function is shown in Figure 6.6.

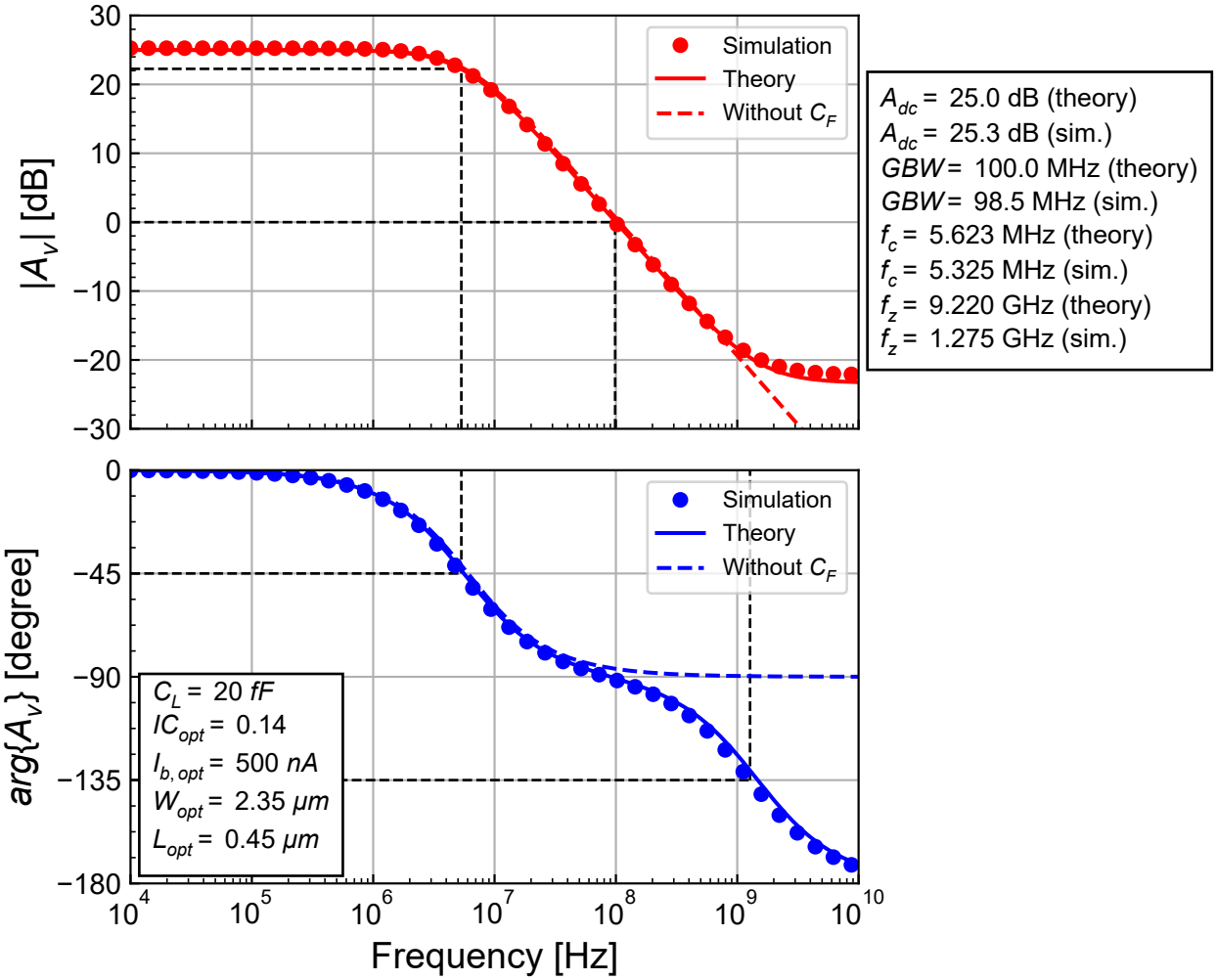

Figure 6.5: CS simulated open-loop transfer function compared to the theoretical prediction.

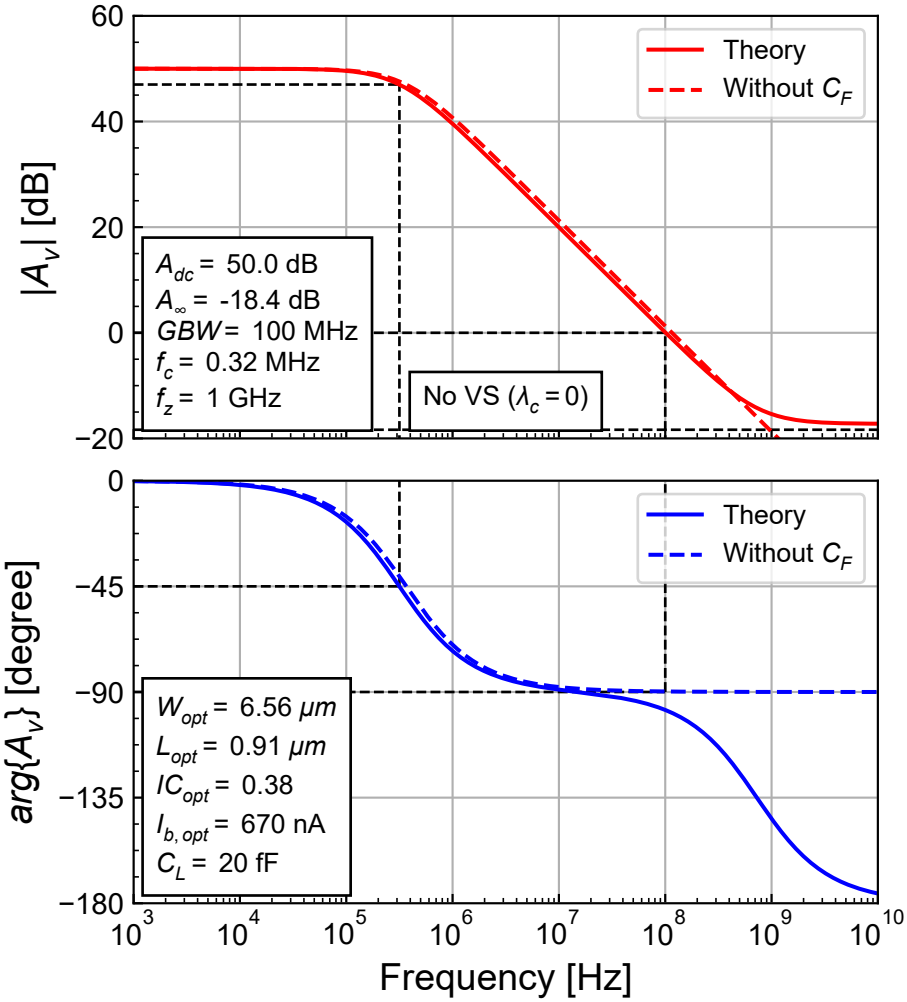

Figure 6.6: Transfer function (pMOS).

6.2.2.2 ngspice simulations

We now simulate the above design to check whether the design meets the specifications. We now simulate the above design to check whether the design meets the specifications.

Similarly to the previous design, we can first check the operating point informations. The drain current, transconductance and output conductance are given in Table 6.12 and the various capacitances are shown in Table 6.13, Table 6.14 and Table 6.15. Finally, the gain-bandwidth, zero frequency are given in Table 6.16. We observe that the estimated and simulated values are close.

Table 6.12: Simulated drain current and small-signal parameter values compared to theoretical values.

	$I_D\,[nA]$	$G_m\,[\mu A/V]$	$G_{ds}\,[nA/V]$	A_v
Theory	670	16.273	51.46	50
PSP	670	15.938	71.905	46.914

Table 6.13: Simulated overlap and fringing capacitances values compared to theoretical values (pMOS).

	$C_{GSo}\,[fF]$	$C_{GDo}\,[fF]$	$C_{GSf}\,[fF]$	$C_{GDf}\,[fF]$	$C_{GSe}\,[fF]$	$C_{GDe}\,[fF]$
Theory	2.912	2.912	0.655	0.655	3.567	3.567
PSP	2.898	2.898	0.658	0.658	3.333	3.181

Table 6.14: Simulated zero-bias junction capacitances values compared to theoretical values.

	$C_{Jbot}(0)\,[fF]$	$C_{JSWSTI}(0)\,[fF]$	$C_{JSWGAT}(0)\,[fF]$	$C_{Jtot}(0)\,[fF]$
Theory	1.931	0.232	0.18	2.343
PSP	1.937	0.232	0.18	2.348

Table 6.15: Simulated actual junction capacitances values compared to theoretical zero-bias values.

	$C_{Jbot}\,[fF]$	$C_{JSWSTI}\,[fF]$	$C_{JSWGAT}\,[fF]$	$C_{Jtot}\,[fF]$
Theory	1.931	0.232	0.181	2.343
PSP	1.704	0.223	0.157	2.085

Table 6.16: Comparison of the simulated and predicted values of the gain-bandwidth and zero frequency.

	$G_m\,[\mu A/V]$	$C_{out}\,[fF]$	$C_F\,[fF]$	$GBW\,[MHz]$	$f_z\,[GHz]$	$A_\infty\,[dB]$
Theory	16.273	25.931	3.567	99.876	4.562	-18.35
PSP	15.938	25.287	3.181	100.314	5.116	-19.037

We can now proceed with the AC simulation. The simulation result is compared to the theoretical prediction in Figure 6.7.

From Figure 6.7, we see that the simulated GBW is higher than the target. This is due to the influence of the zero which is very low due to the low quasi-static frequency related to the transcapacitance, similarly to the pMOS case in the previous optimization. We can estimate the transcapacitance for this particular design as $C_m = 6.907\ fF$ and the corresponding quasi-static frequency as $f_{qs} = 374.971\ MHz$. We see that C_m is much larger than the extrinsic feedback capacitance and almost equal to the

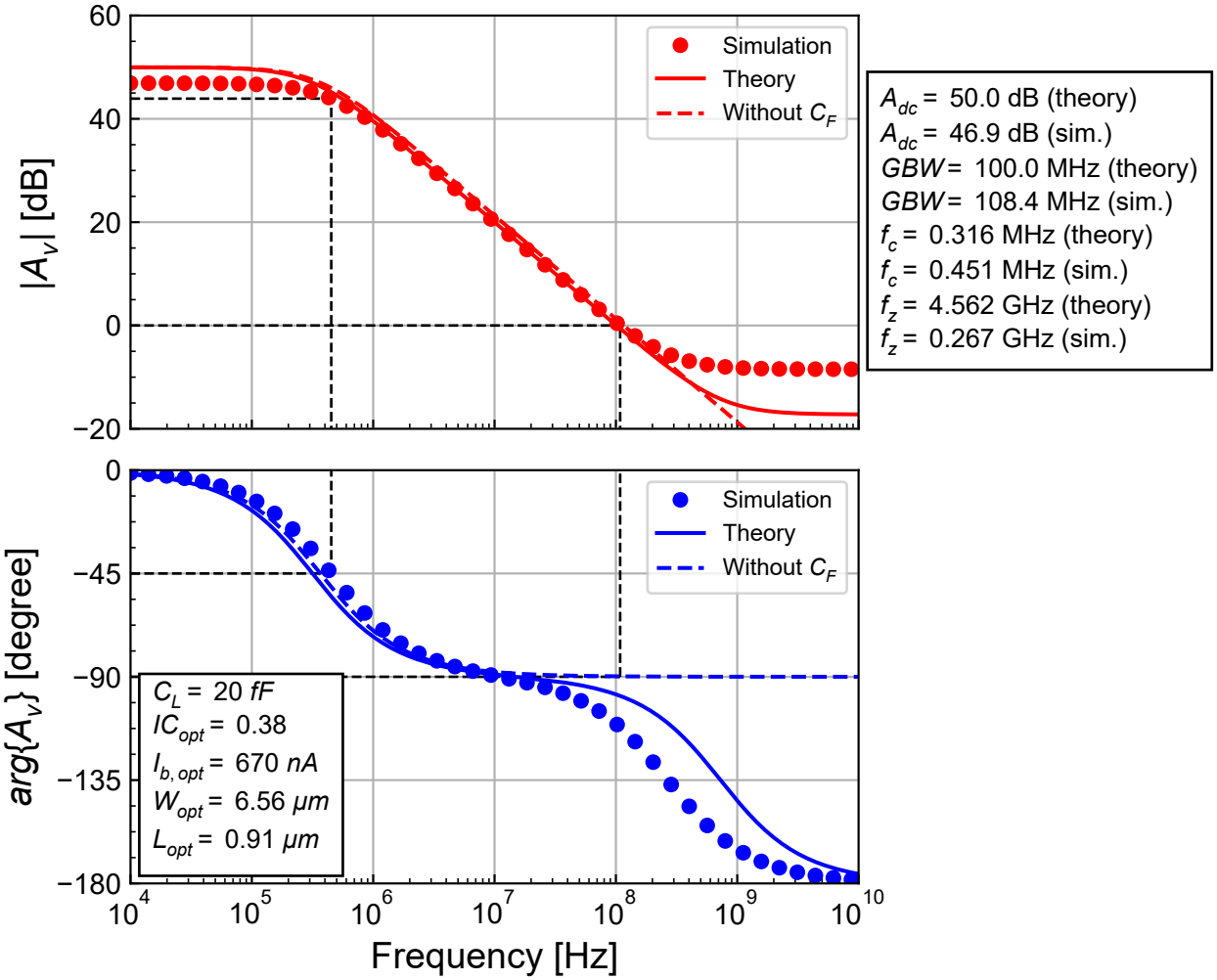

Figure 6.7: CS simulated open-loop transfer function compared to the theoretical prediction.

load capacitance. The quasi-static frequency is slightly above the target GBW. We can also estimate the asymptotic high frequency gain A_∞ as A_∞ = 3.553e-01 or in dB A_∞ = -8.987 dB.

Figure 6.8 compares the simulated transfer function to the theoretical estimations with and without the transcapacitance C_m. We now have an almost perfect fit between the theoretical prediciton including the transcapacitance and the simulation.

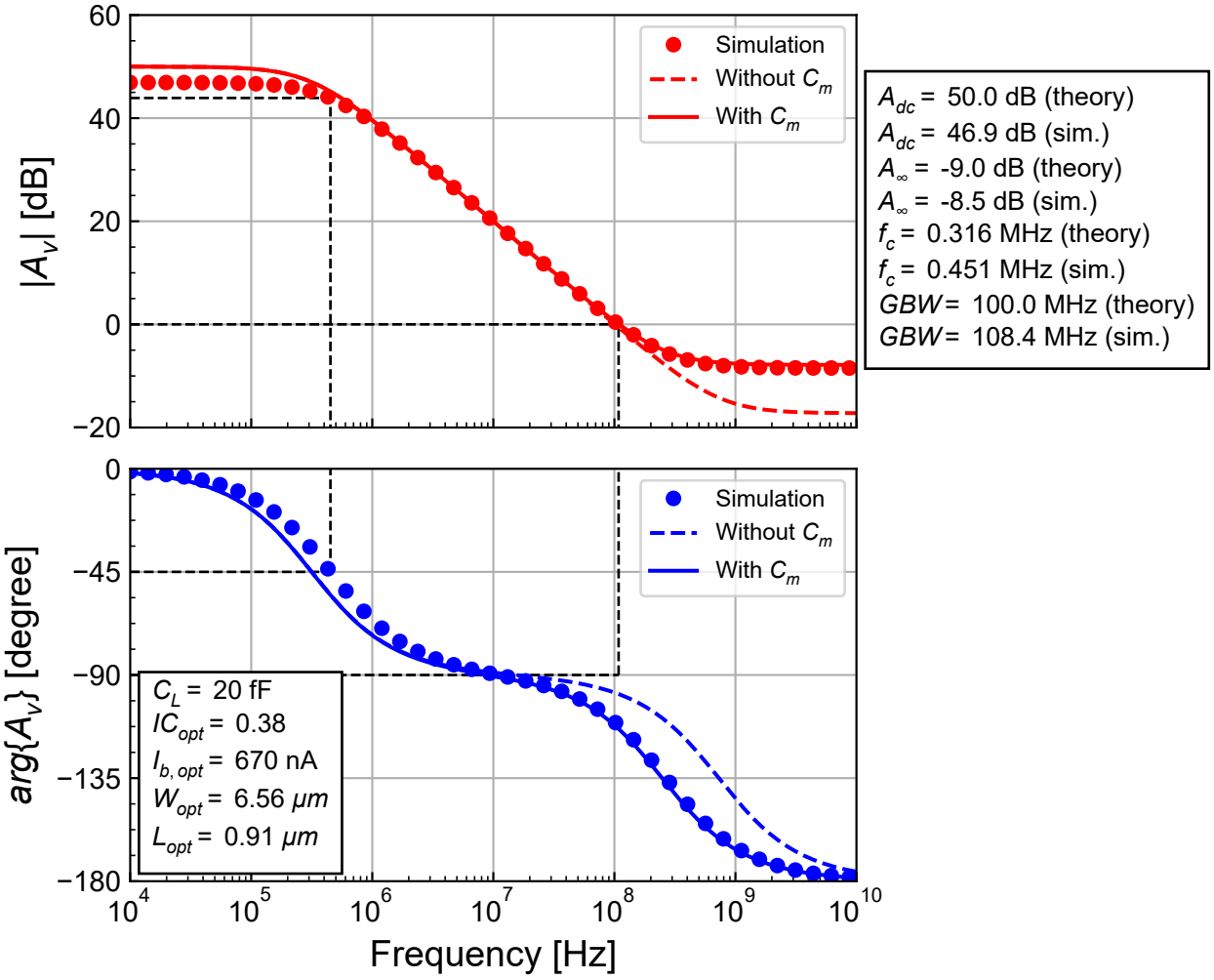

Figure 6.8: CS simulated open-loop transfer function compared to the theoretical prediction including the transcapacitance C_m.

7 Conclusion

In this notebook we have analyzed the common-source gain stage and found the minimum current to achieve certain specifications such as transconductance and gain-bandwidth. We first had a look at the case with a constant load capacitance for which the minimum current is in weak inversion. Optimizing the CS in weak inversion usually leads to fairly large transistor increasing the parasitic load capacitance which can no more be ignored. We then accounted for the junction, overlap and fringing capacitances which are all scaling with the transistor width. We then have shown that the self-loading capacitance introduces a true minimum current for achieving a given gain-bandwidth product for a given transistor length. The theoretical prediction were then validated by simulations done for the IHP 130nm process using the open source libary with the PSP compact model in ngspice. Despite the transistor model in the simulations is not the EKV model, the design approach using the inversion coefficient and the sEKV model parameters gave results that are very close to the simulations for the nMOS case. When implementing the CS gain stage with a pMOS device having a long channel length, we have discovered a strong deviation between the simulation and theoretical predictions at high frequency (above the gain-bandwidth product frequency). We have explained that this discrepancy came from the gate transcapacitance C_m which could no more be neglected. We could estimate the quasi-static frequency, which was close to the target gain-bandwidth product. Adding the transcapacitance, we then obtained a theoretical prediction that is very close to the simulation. We then used the additional degree of freedom, namely the transistor length (which was set arbitrarily in the previous case) to set the DC gain in addition to the gain-bandwidth product. The predicted results were again very close to the simulation except for the pMOS case. Since the resulting gate length is fairly long, we need to account for the transcapacitance as we did for the gain-bandwidth optimization. After adding the transcapacitance, we get an almost perfect fit between the theoretical prediction and the simulation.

This simple example of designing an elementary CS stage for gain-bandwidth and DC gain specifications has shown that the inversion coefficient approach can succesfully be used provided the sEKV parameters are correctly extracted for the target technology. It also has sown that the resulting design can be validated by simulation even if the compact model used in the simulator is not the EKV model.

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