sEKV Parameter Extraction for the IHP 130nm Process

pMOS (long-channel)

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1 Introduction

In this notebook we will extract the sEKV parameters [1] [2] for a long-channel pMOS transistors from the 130nm bulk CMOS process of IHP [3]. The extraction is done with data generated using the PSP compact model [4] from the PDK of the IHP 130nm process [3] for the typical-typical (t-t) case.

The easiest way to extract the sEKV parameters is to use the python tool developed by H.C. Han and available on GitLab [5]. The tool and the extraction procedure are described in [6]. In this notebook we will detail the extraction procedure and show how the parameters can be extracted manually.

We start by looking at the channel width and length corrections for the drain current and for the capacitances. Then we will extract the sEKV parameter using a direct extraction methodology with the velocity parameter $\lambda_c = 0$. We then will extract the additional parameter λ_c using a direct extraction methodology. Then we will extract all the sEKV parameters by optimization using nonlinear curve fitting.

We also will extract the output conductance due to channel-length modulation (CLM) and the related parameter.

Finally, we will check the white noise model and extract the EKV flicker noise parameters.

The extracted parameters are then all saved in an Excel worksheet.

2 Transistor geometry parameters

2.1 Effective length and width for current

Before we start the extraction we need to account for the geometry dependence. With PSP you can choose between geometry scaling rules or binning rules with parameter $SWGEO$. If $SWGEO = 1$, the scaling rules are chosen. This is the case in the IHP 130nm G2 PDK. The geometrical parameters are defined in Figure 2.1 [4].

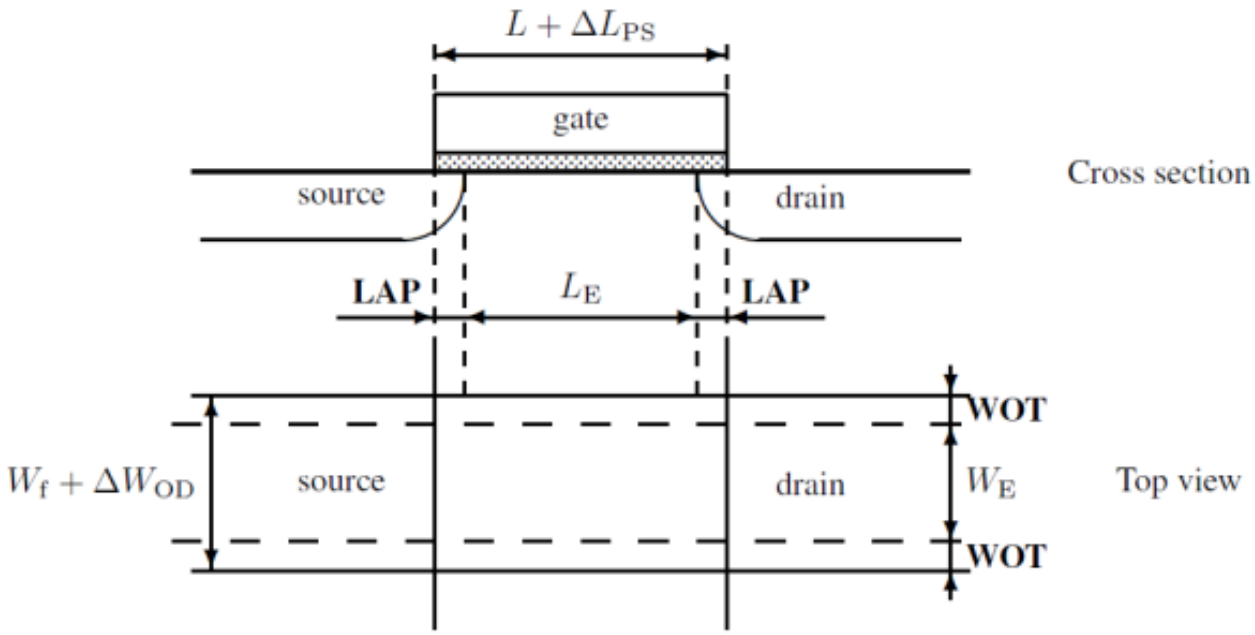

Figure 2.1: Definition of transistor geometrical parameters [4].

The effective length and width are defined as

$$L_{eff} = L - \Delta L, \tag{2.1}$$
$$W_{eff} = W_f - \Delta W, \tag{2.2}$$

where W_f is the width of one finger defined as

$$W_f = \frac{W}{NF}. \tag{2.3}$$

In our case we will assume that the number of fingers $NF = 1$ and hence that $W_f = W$. ΔL and ΔW are given by

$$\Delta L = 2\,LAP - \Delta L_{PS}, \tag{2.4}$$
$$\Delta W = 2\,WOT - \Delta W_{OD}, \tag{2.5}$$

with

$$\Delta L_{PS} = LVARO \cdot \left(1 + LVARL \cdot \frac{L_{EN}}{L}\right) \cdot \left(1 + LVARW \cdot \frac{W_{EN}}{W_f}\right), \tag{2.6}$$

$$\Delta W_{OD} = WVARO \cdot \left(1 + WVARL \cdot \frac{L_{EN}}{L}\right) \cdot \left(1 + WVARW \cdot \frac{W_{EN}}{W_f}\right). \tag{2.7}$$

Contrary to nMOS, for pMOS $LVARO \neq 0$ and $WVARO \neq 0$ and therefore $\Delta L_{PS} \neq 0$ and $\Delta W_{OD} \neq 0$. This means that the length and width reduction actually depend on the length L and width W. However, we can ignore this scaling of ΔL_{PS} and ΔW_{OD} with W and L and approximate ΔL_{PS} and ΔW_{OD} by taking the value for $L \to \infty$ and for $W \to \infty$ corresponding to

$$\Delta L_{PS} \cong LVARO, \tag{2.8}$$

$$\Delta W_{OD} \cong WVARO, \tag{2.9}$$

resulting in

$$\Delta L \cong 2\,LAP - LVARO, \tag{2.10}$$

$$\Delta W \cong 2\,WOT - WVARO. \tag{2.11}$$

Table 2.1: Length and width corrections.

Definition	ΔW [nm]	ΔL [nm]	Comment
For current	30.000	-46.442	extracted from PDK

The channel length and width reduction are then given in Table 2.1. Note that, contrary to the nMOS devices, for pMOS ΔL = -46.442 nm is negative wich leads to an effective length that is longer than the drawn length. On the other hand $\Delta W = 30.000$ nm is positive which results in an effective width that is smaller than the drawn width. The width and length for the selected pMOS transistor are given by $W = 10$ μm and $L = 10$ μm and the effective width and length are given by $W_{eff} = 9.970$ μm and $L_{eff} = 10.046$ μm. They are summarized in Table 2.2.

Table 2.2: Selected transistor width and length.

Type	W [μm]	W_{eff} [μm]	L [μm]	L_{eff} [μm]
pMOS	10	9.970	10	10.046

3 DC Transfer Characteristic Parameters

3.1 Generating and importing the data

The data used for the sEKV parameters extraction is generated by simulation using the PSP CM [4] from the PDK of the IHP 130nm process [3] for the typical-typical (t-t) case. We present the I_D-V_G and G_m-V_G data below.

3.1.1 I_D and G_m versus V_G

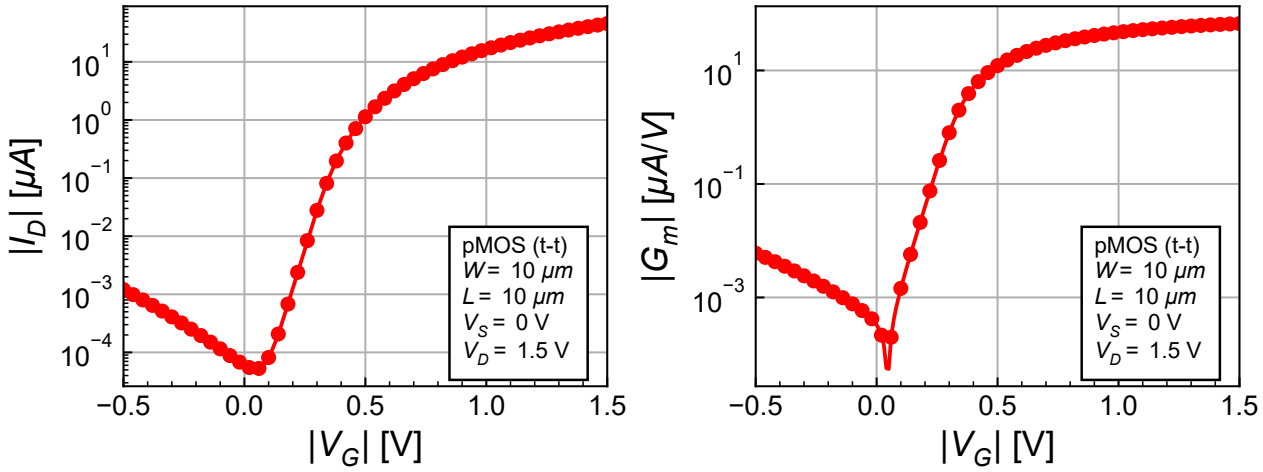

Figure 3.1: Imported I_D-V_G and G_m-V_G.

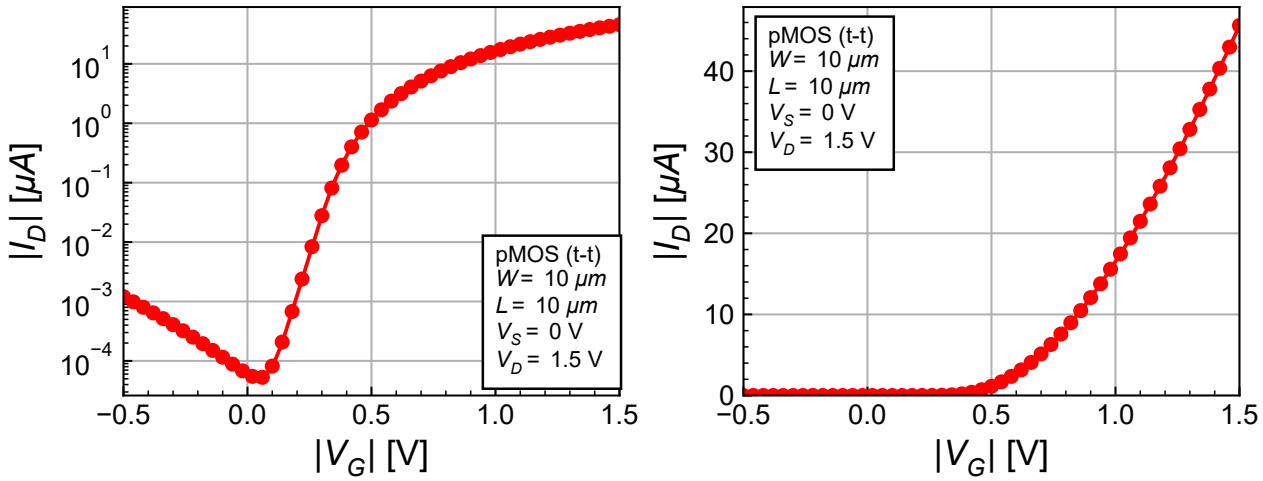

Figure 3.2: Imported I_D-V_G.

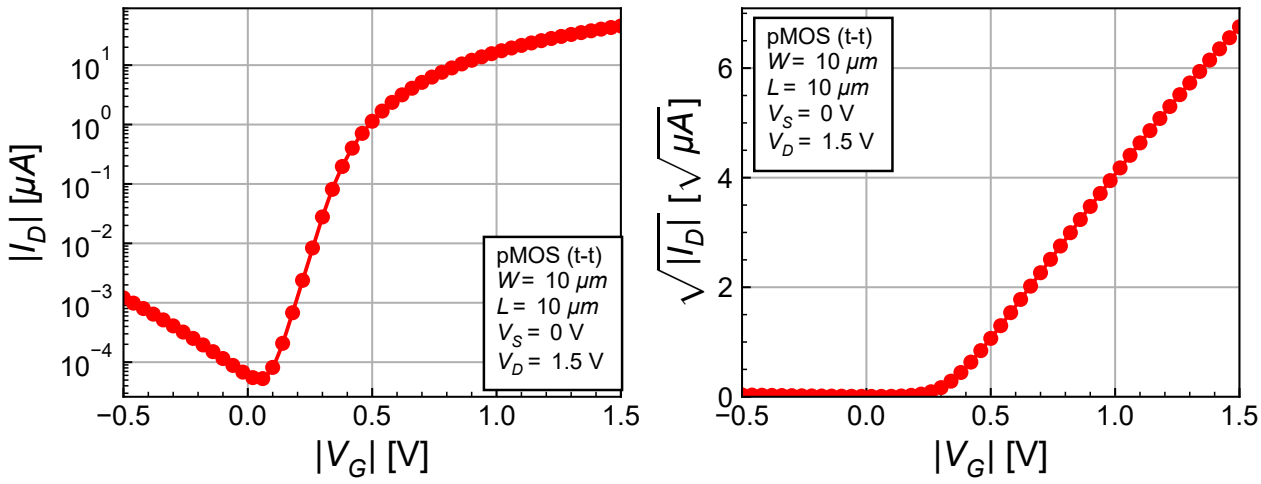

Figure 3.3: Imported I_D-V_G.

3.1.2 G_m-V_G and G_m-I_D

We now will check the derivative namely the gate transconductance obtained from the simulator and compare it to the numerical differentiation of the large-signal I_D-V_G characteristic.

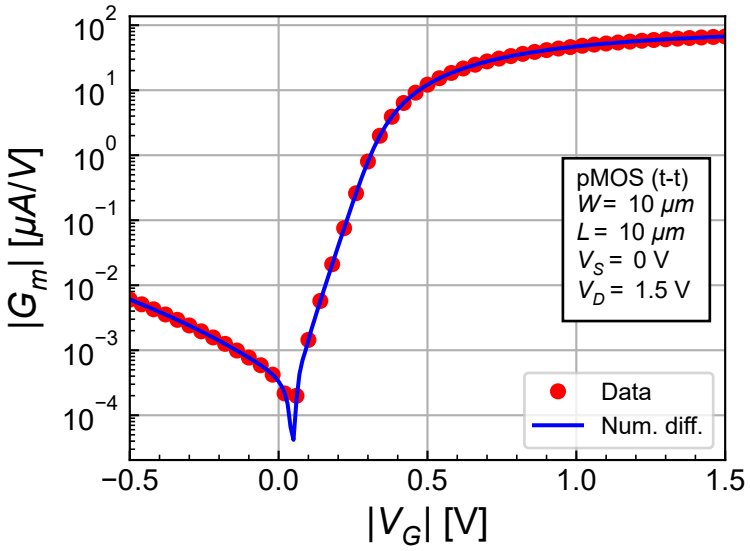

Figure 3.4: Check of the G_m-V_G consistency.

We see that the transconductance obtained by differentiating the large-signal I_D-V_G characteristic is equal to the transconductance extracted from the PSP model. We will keep the value extracted from the PSP model.

3.2 Filtering the outliers

Since the sEKV model [2] doesn't account for leakage currents such as gate induced drain leakage (GIDL) that appears at very low current, we need to filter the outlier points. This is done below with the outlier points shown in blue and the points used for the extraction shown in red.

We can now proceed with the parameter extraction, starting with the direct extraction approach.

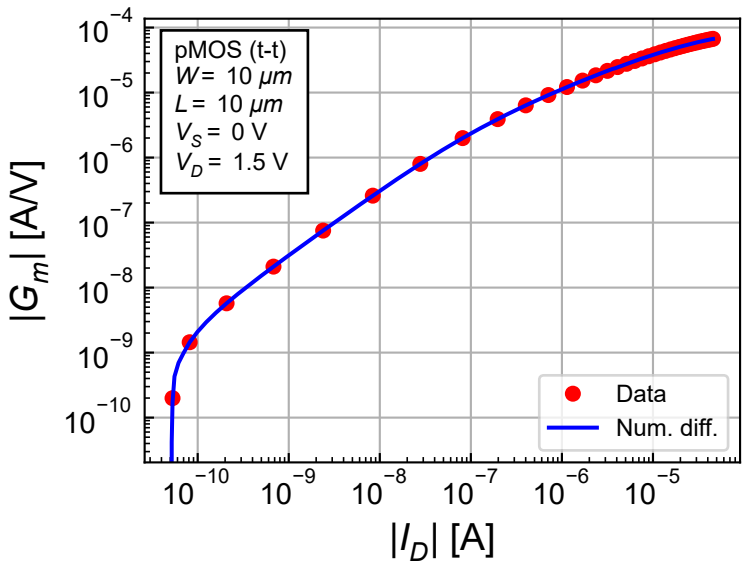

Figure 3.5: Check of the G_m-I_D consistency.

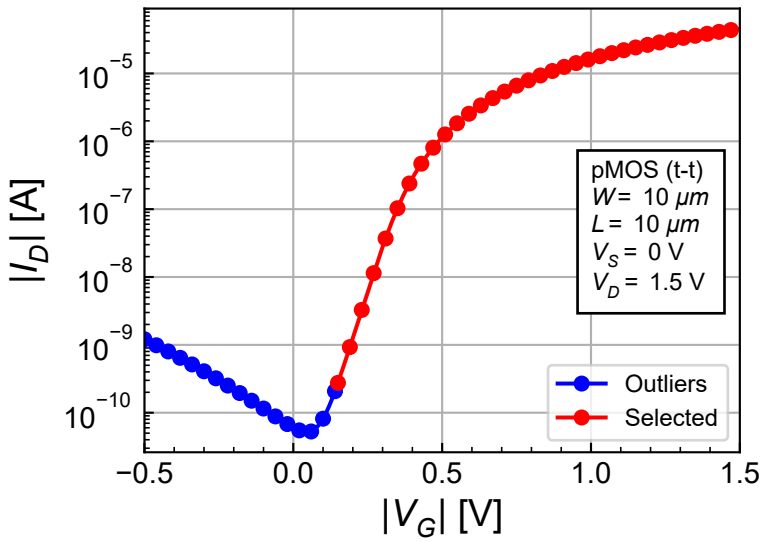

Figure 3.6: Filtering the outliers from the I_D-V_G characersitic.

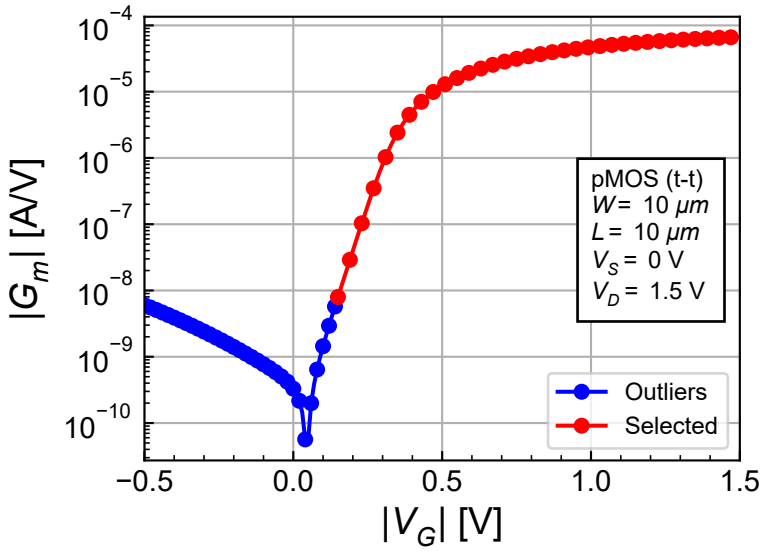

Figure 3.7: Filtering the outliers from the G_m-V_G characersitic.

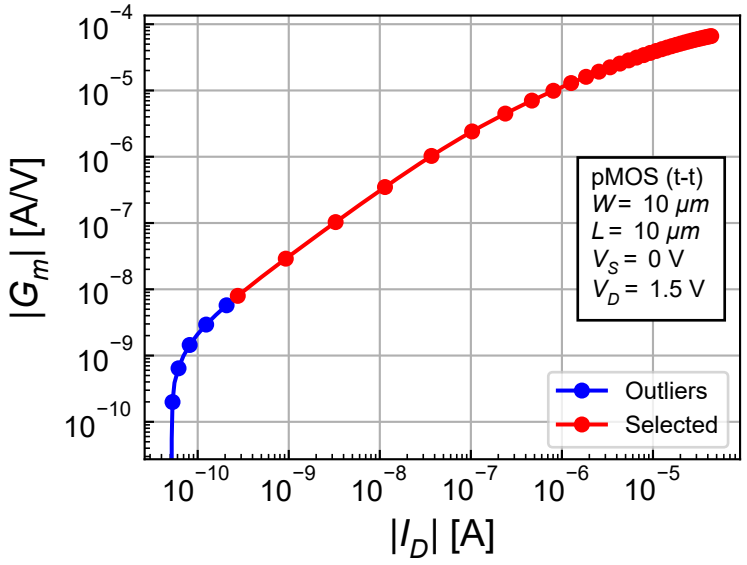

Figure 3.8: Filtering the outliers from the G_m-I_D characersitic.

3.3 Direct extraction with $\lambda_c = 0$

In the direct extraction approach, we avoid using curve fitting or optimization and manipulate the data to extract a given parameter in a certain data range.

3.3.1 Slope factor n and I_{spec} extraction

The gate transconductance in weak inversion and saturation is given by [1]

$$G_m = \frac{I_D}{n\,U_T}. \tag{3.1}$$

So if we plot $I_D/(G_m\,U_T)$ we should see a plateau in weak inversion the value of which is equal to the slope factor n.

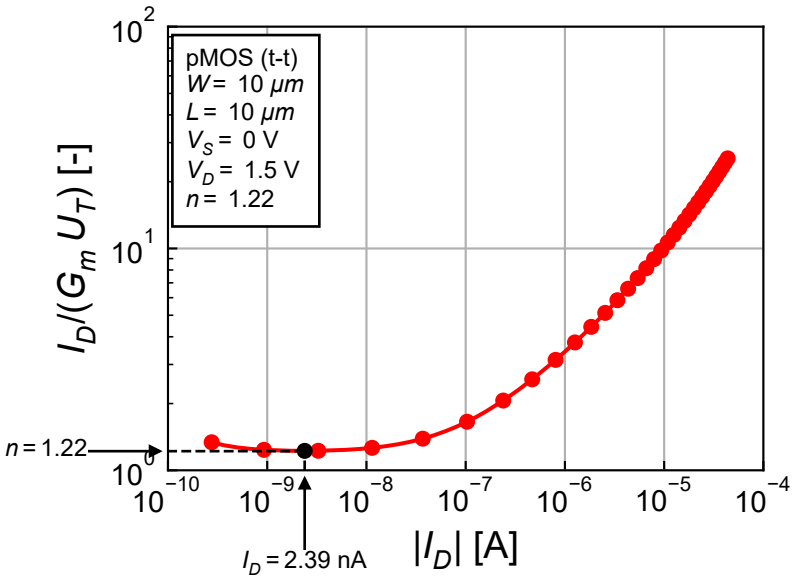

Figure 3.9: Slope factor extraction.

This is illustrated in Figure 3.9 resulting in $n = 1.22$. On the other hand the normalized G_m/I_D function for a long-channel transistor in strong inversion and saturation is given by [1]

$$\frac{G_m\,n\,U_T}{I_D} = \frac{1}{\sqrt{IC}} = \sqrt{\frac{I_{spec}}{I_D}}. \tag{3.2}$$

We can then plot $(G_m\,n\,U_T)^2/I_D$ which should find a maximum value equal to I_{spec}.

This is illustrated in Figure 3.10 resulting in $I_{spec} = 149\ nA$ corresponding to $I_{spec\square} = 150\ nA$. We can now plot $I_D/(G_m\,U_T)$ versus I_D as shown in Figure 3.11. We clearly see the two asymptotes in weak (i.e. $I_D < I_{spec}$) and strong inversion (i.e. $I_D > I_{spec}$).

Having extracted n and I_{spec}, we can now plot the normalized G_m/I_D function versus IC which is shown in Figure 3.12.

The fit is reasonable over the entire IC span. There is some discrepancy in the moderate inversion region which is due to the mobility reduction due to the vertical field appearing for $IC > 10^2$. The latter can be accounted for by using the λ_c parameter which is normally used for modeling the effect of velocity saturation in short-channel transistor but can also be used to correct the effect of mobility reduction due to the vertical field appearing in long-channel transistors. We will not do this here since we want to extract the long-channel parameters keeping $\lambda_c = 0$, but since we are mostly interested in

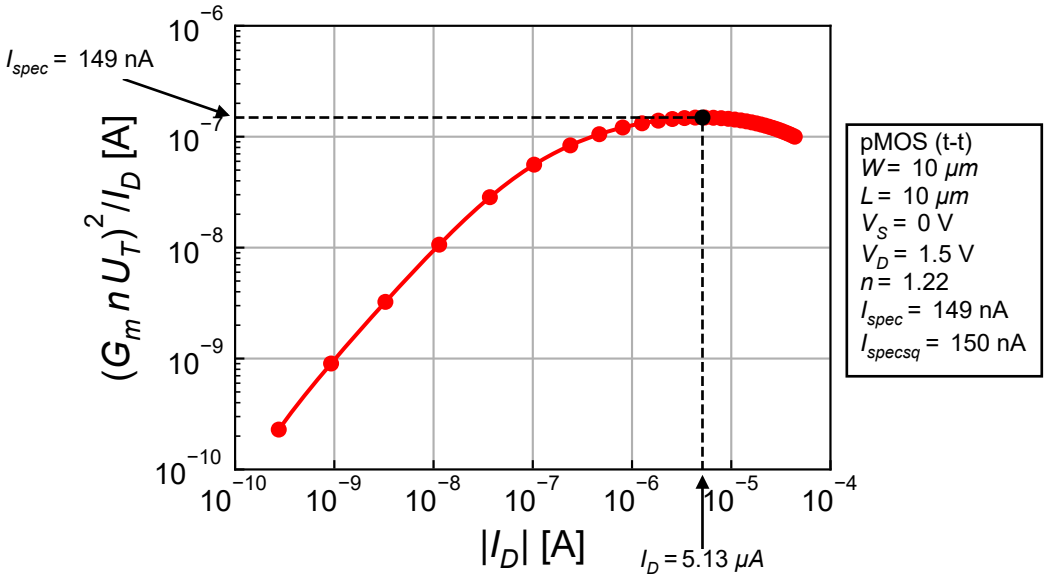

Figure 3.10: I_{spec} extraction.

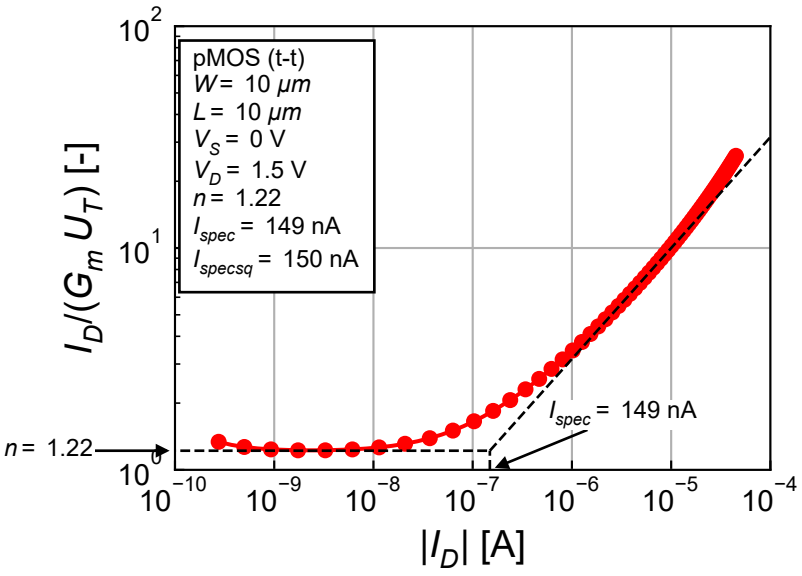

Figure 3.11: n and I_{spec} check.

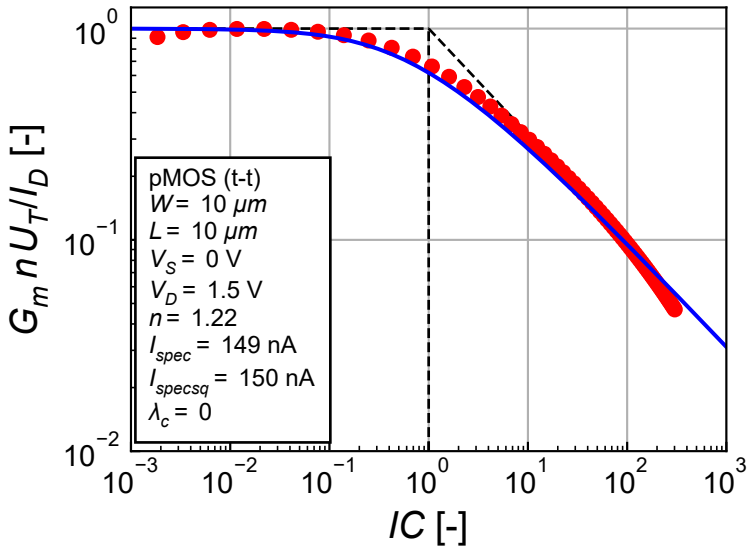

Figure 3.12: n and I_{spec} check.

the moderate inversion region, we can slightly increase I_{spec} to improve the fit in moderate inversion at the cost of a degradation in strong inversion. This results in the normalized G_m/I_D function versus IC shown in Figure 3.13.

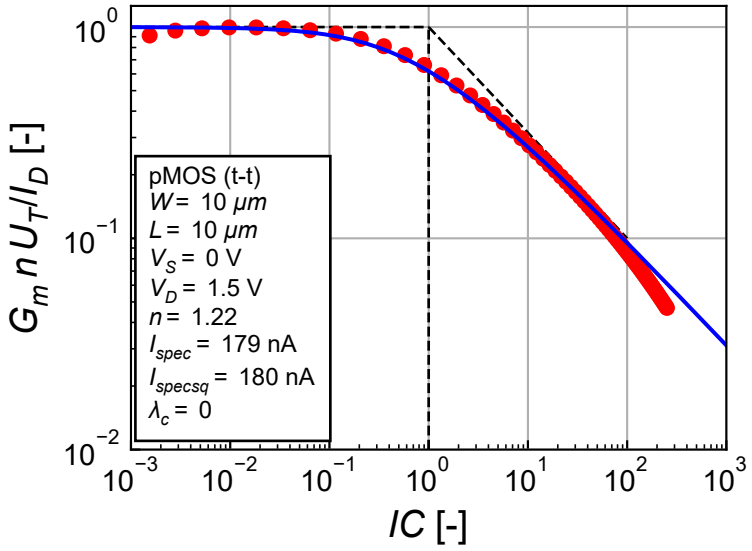

Figure 3.13: Fine tuning of the normalized G_m/I_D function versus IC in moderate inversion.

The fit is now much better in moderate inversion but less in strong inversion. This is due to mobility reduction due to the vertical field which is an effect that is not accounted for in the model. However, it offers a good trade-off between moderate inversion (where the curve is slightly below the simulations) and strong inversion up to $IC = 100$ (where the simulation points are slightly below the curve). We therefore will keep the new value of $I_{spec\square}$, namely $I_{spec\square} = 180\ nA$.

3.3.2 Threshold voltage extraction

We can extract the threshold voltage in weak inversion (assuming $V_S = 0$) from the normalized current (inversion coefficient) given by [1]

$$IC = e^{\frac{V_G - V_{T0}}{nU_T}}. \tag{3.3}$$

We can now plot

$$V_{T0} = V_G - nU_T \ln(IC) \tag{3.4}$$

to extract the threshold voltage. This results in the plot shown in Figure 3.14.

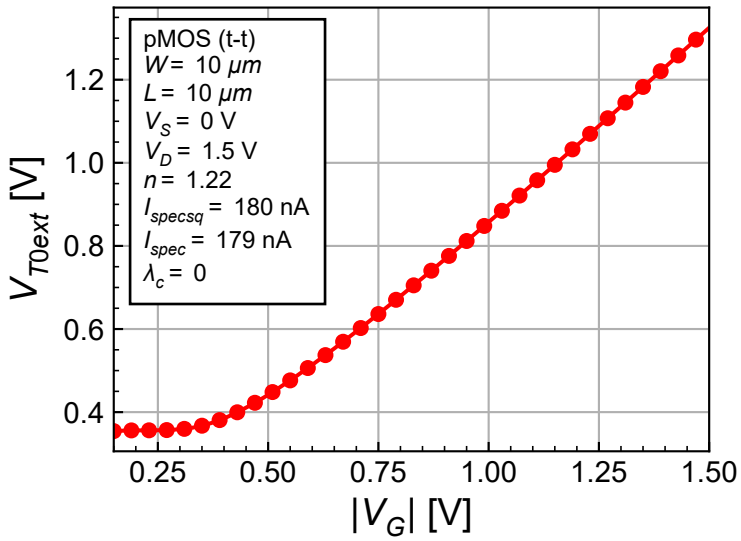

Figure 3.14: Threshold voltage extraction.

We see a plateau in weak inversion where we can average its value to get the threshold voltage in weak inversion which we can zoom into as shown in Figure 3.15.

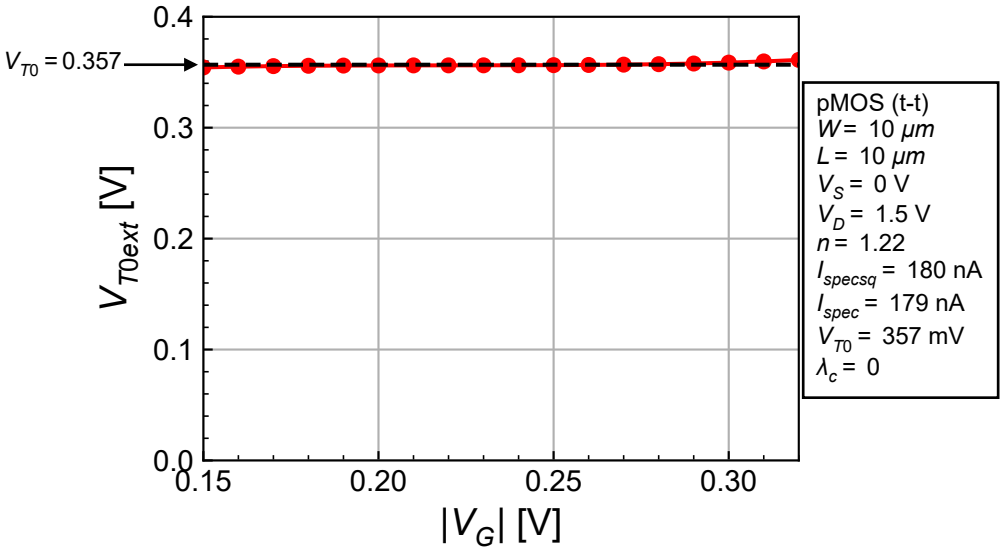

Figure 3.15: Threshold voltage extraction in weak inversion.

The average value of $V_{T0} =$ in this range is given by $V_{T0} = 357\ mV$.

We can now plot the I_D-V_G for the extracted parameters which is shown in Figure 3.16.

We get a reasonable fit with some deviations in strong inversion, which is expected since we focused on the moderate inversion and kept $\lambda_c = 0$.

We can also extract the threshold voltage in strong inversion by plotting $\sqrt{I_D}$ versus V_G as shown in Figure 3.17.

We can then fit the linear portion and extract the intersection point on the V_G axis as shown in Figure 3.18 which results in $V_{T0} = 294\ mV$. We get a very small threshold voltage even smaller than

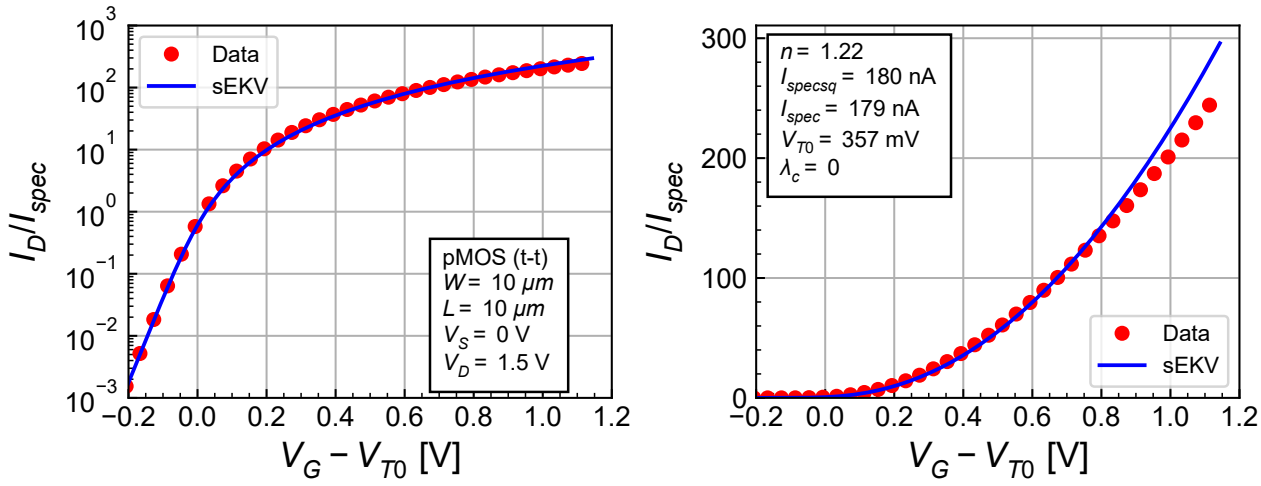

Figure 3.16: I_D-V_G for the extracted parameters.

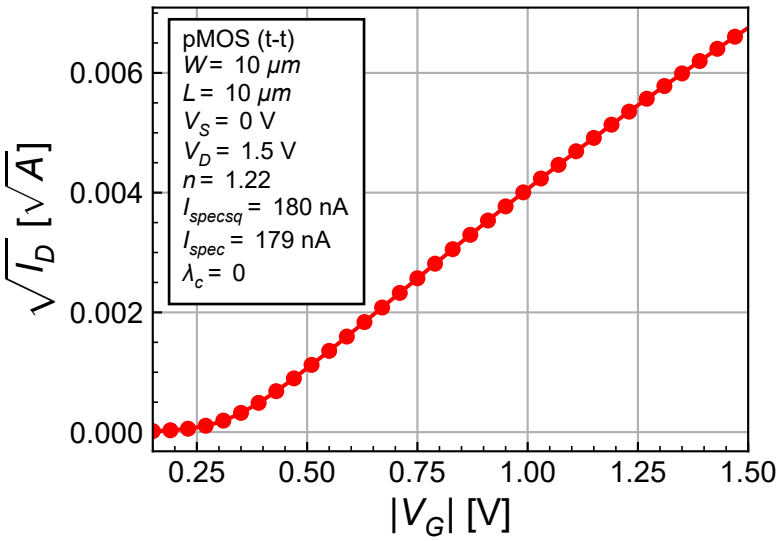

Figure 3.17: $\sqrt{I_D}$-V_G for the extracted parameters.

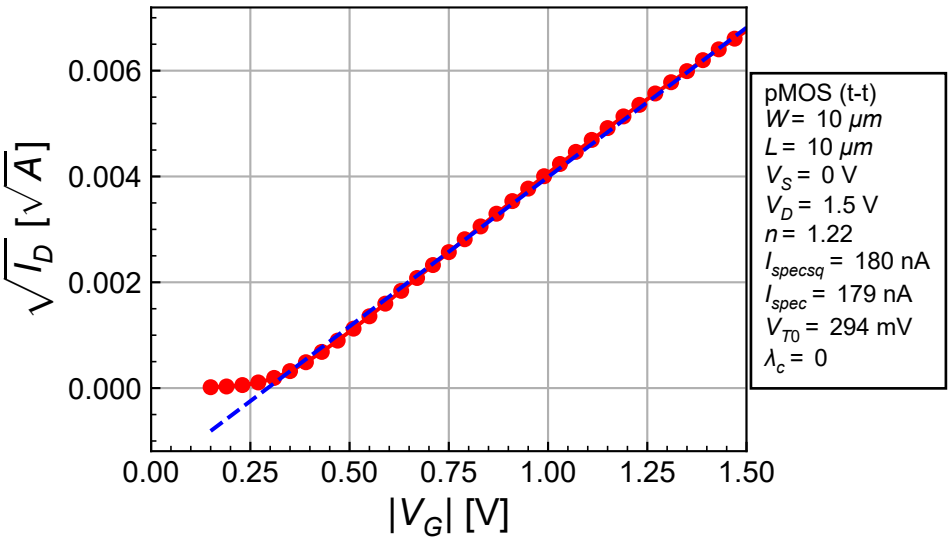

Figure 3.18: Threshold voltage extraction from $\sqrt{I_D}$-V_G in strong inversion.

the value extracted in weak inversion. We can check the I_D-V_G charactersitic with this extracted threshold voltage in Figure 3.19.

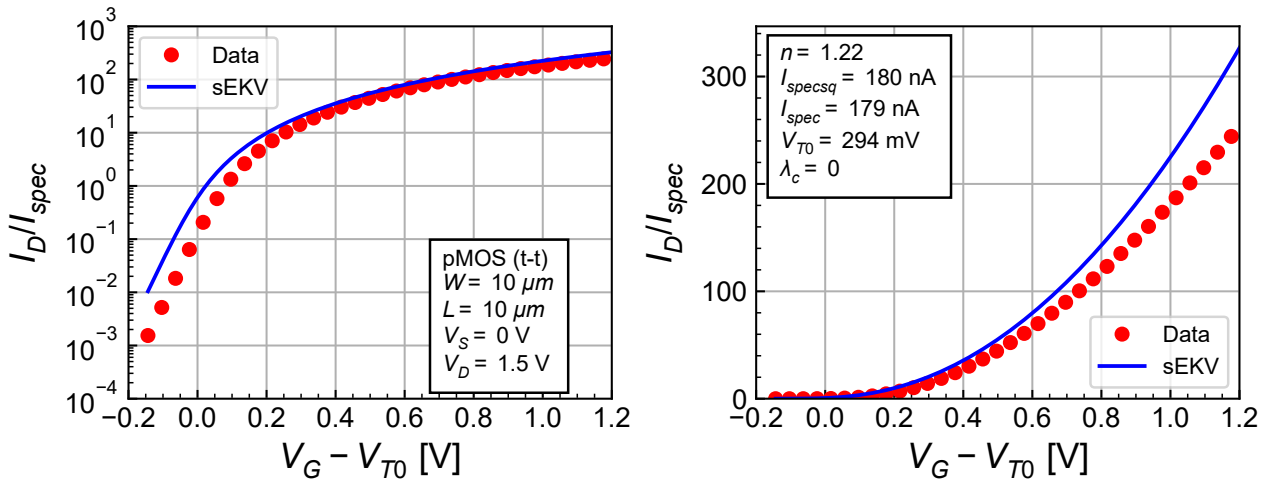

Figure 3.19: I_D-V_G for the extracted threshold voltage.

As expected, we get a less good fit in weak inversion. We therefore keep the value of the threshold voltage extracted in weak inversion, namely $V_{T0} = 357\ mV$.

3.3.3 Summary

The results of the direct extraction method is shown in Figure 3.20, which includes the large-signal $IC = I_D/I_{spec}$ versus $V_G - V_{T0}$ on the left and the small-signal parameters G_{ms}/G_{spec} versus IC and $G_m\, n\, U_T/I_D$ versus IC on the right. We see an very good fit of the large- and small-signal parameters except in very strong inversion (i.e. $100 < IC$). The extracted parameters are summarized in Table 3.1.

Table 3.1: Direct extraction of the sEKV parameters with $\lambda_c = 0$.

Type	n	$I_{spec\square}\ [nA]$	$V_{T0}\ [mV]$	λ_c	$L_{sat}\ [nm]$	Comment
pMOS	1.22	180	357	0	0	direct with $\lambda_c = 0$

3.4 Extraction using curve fitting with $\lambda_c = 0$

3.4.1 Slope factor n and I_{spec} extraction

We can try to extract n and I_{spec} for a long-channel directly from the normalized G_m/I_d function using curve fitting. The result is shown in Figure 3.21.

We get a reasonable fit and values that are similar to what we got from the direct extraction. We can keep the value of n extracted from the direct extraction above and optimize for I_{spec} only. This reults in Figure 3.22.

The fit is good in weak and moderate inversion, but we still have some discrepancies in strong inversion which is due to mobility reduction due to the vertical field. We will keep the last extracted values for I_{specsq}, namely $I_{spec\square} = 192\ nA$.

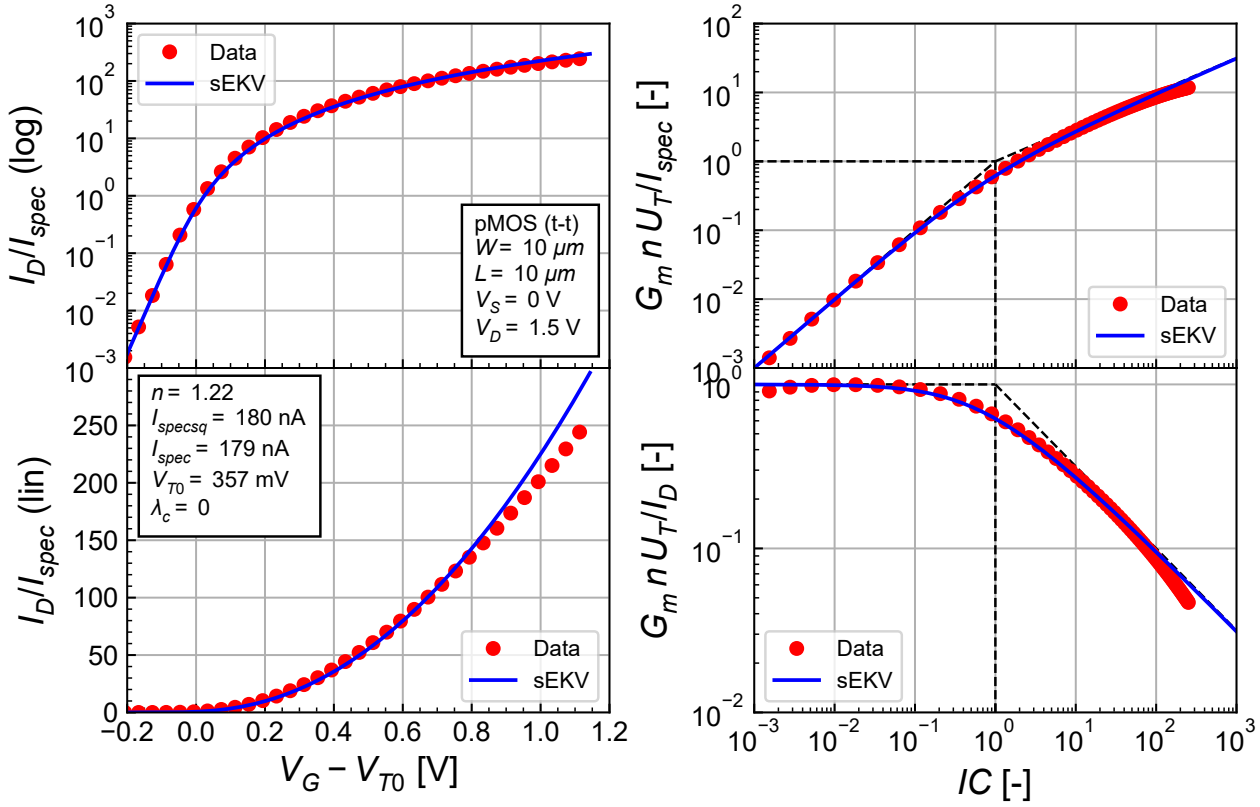

Figure 3.20: Summary of direct extraction with $\lambda_c = 0$.

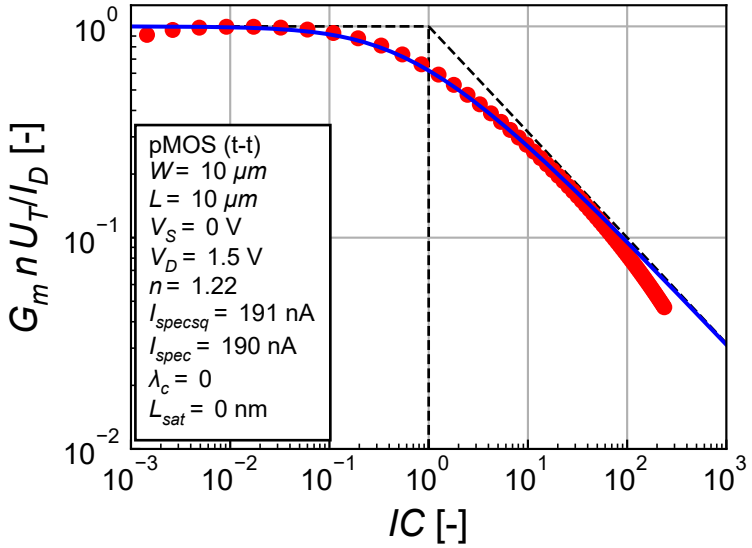

Figure 3.21: Extraction of n and I_{spec} by curve fitting.

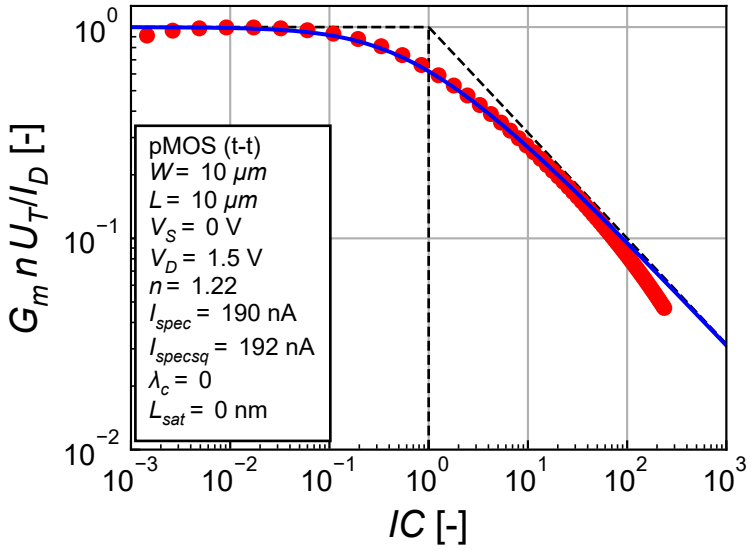

Figure 3.22: Extraction of I_{spec} by curve fitting.

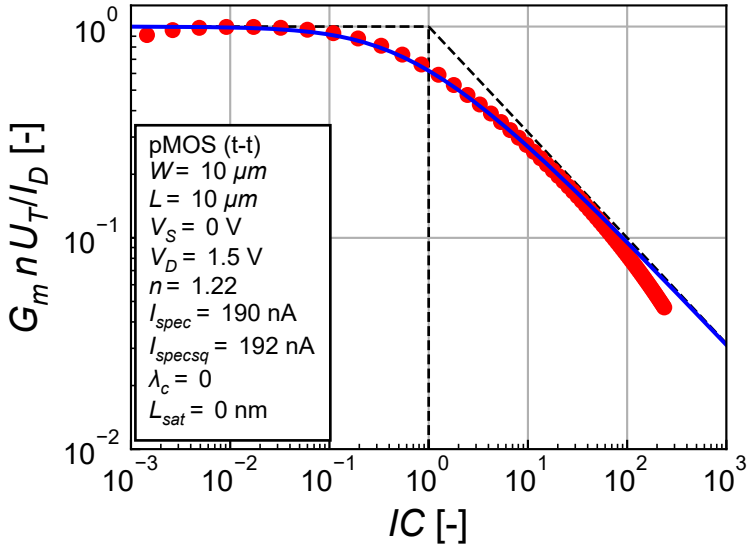

Figure 3.23: Extraction of I_{spec} by curve fitting.

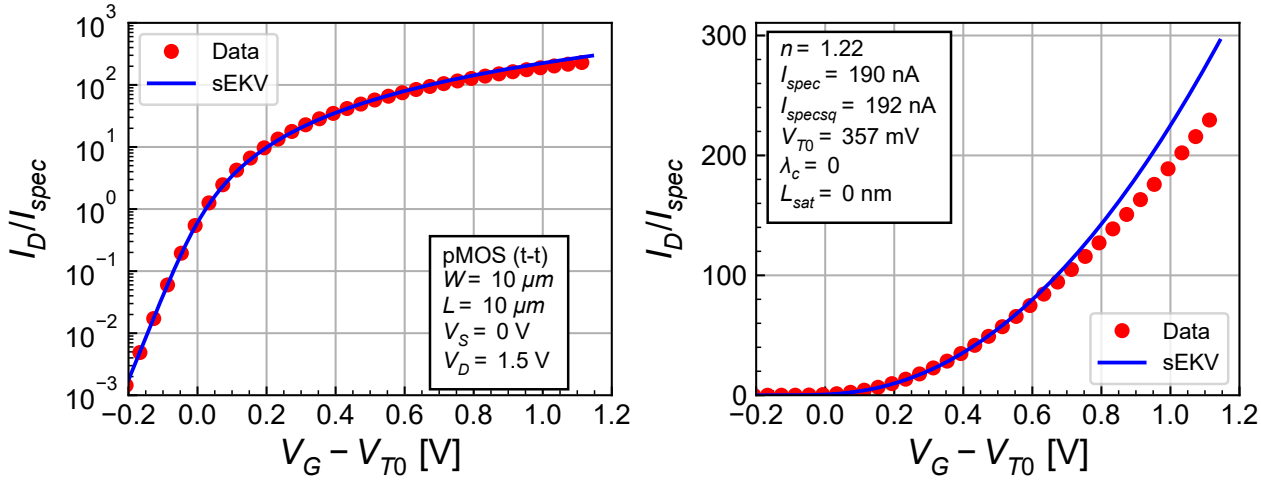

Figure 3.24: Check of the I_D-V_G obtained by curve fitting.

3.4.2 Threshold voltage extraction

We can also extract the threshold voltage using curve fitting which results in $V_{T0} = 357\ mV$ which is almost identical to the value obtained from the direct extraction. We can plot I_D-$V_G - V_{T0}$ in Figure 3.24. We see a reasonable fit except in strong inversion. This is expected since we optimized the moderate inversion region.

3.4.3 Summary

The results of the curve fitting extraction method with $\lambda_c = 0$ is shown in Figure 3.25. We see a good fit of the large- and small-signal parameters except in very strong inversion (i.e. $100 < IC$). The extracted parameters are summarized in Table 3.2.

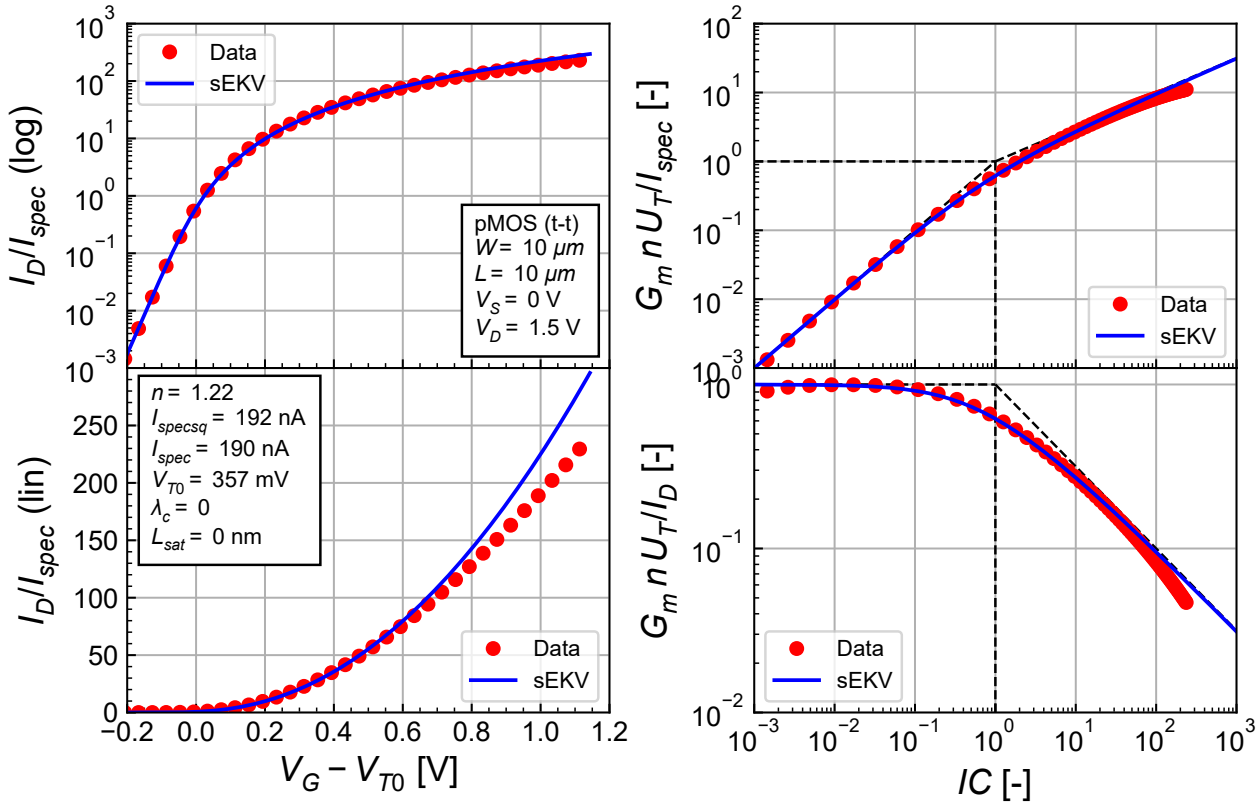

Figure 3.25: Summary of extraction by curve fitting with $\lambda_c = 0$.

The extraction using curve-fitting gives a better fit in moderate inversion but less in strong inversion.

Table 3.2: Extraction of the sEKV parameters using curve fitting with $\lambda_c = 0$.

Type	n	$I_{spec\square}\ [nA]$	$V_{T0}\ [mV]$	λ_c	$L_{sat}\ [nm]$	Comment
pMOS	1.22	180	357	0	0	direct with $\lambda_c = 0$
pMOS	1.22	192	357	0	0	curve fitting with $\lambda_c = 0$

3.5 Extraction using curve fitting with $\lambda_c > 0$

We will now extract n, I_{spec} and λ_c using curve fitting on the normalized G_m/I_D characteristic. This results in the normalized G_m/I_D characteristic shown in Figure 3.26.

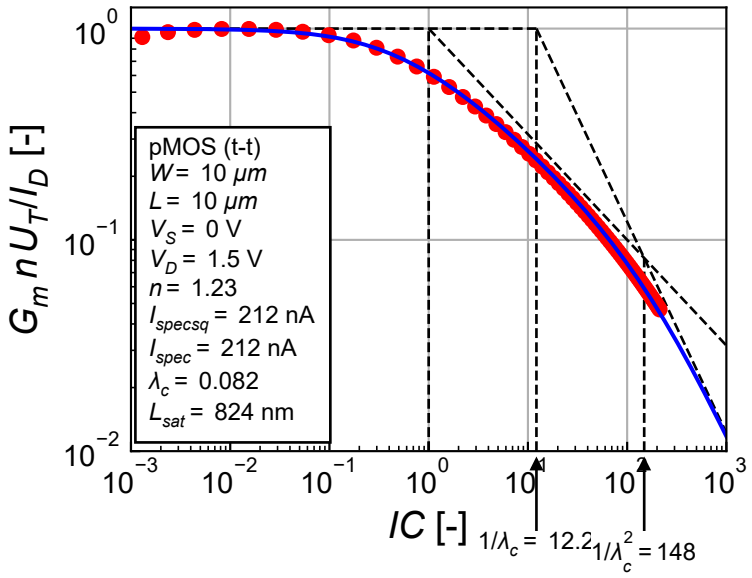

Figure 3.26: Extraction of n, I_{spec} and λ_c by curve fitting.

We now have a good fit in all regions including strong inversion. However the values of $I_{spec\square}$ and λ_c look a bit too large. We can slightly reduce them resulting in Figure 3.27.

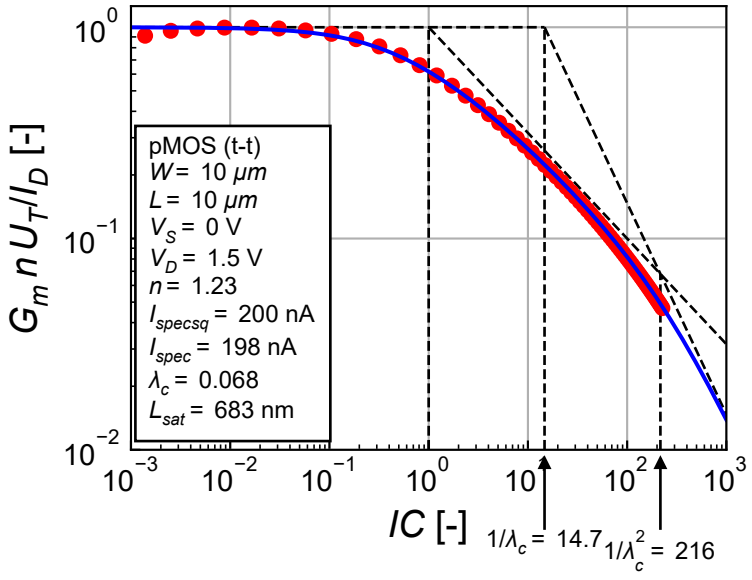

Figure 3.27: Fine tuning of I_{spec} and λ_c.

We now have an almost perfect fit in all regions of operation.

3.5.1 Summary

The results of the curve fitting extraction method with $\lambda_c = 0$ is shown in Figure 3.25 where we have kept the threshold voltage extracted earlier. We see a very good fit of the large- and small-signal parameters including in very strong inversion (i.e. $100 < IC$). The extracted parameters are summarized in Table 3.3.

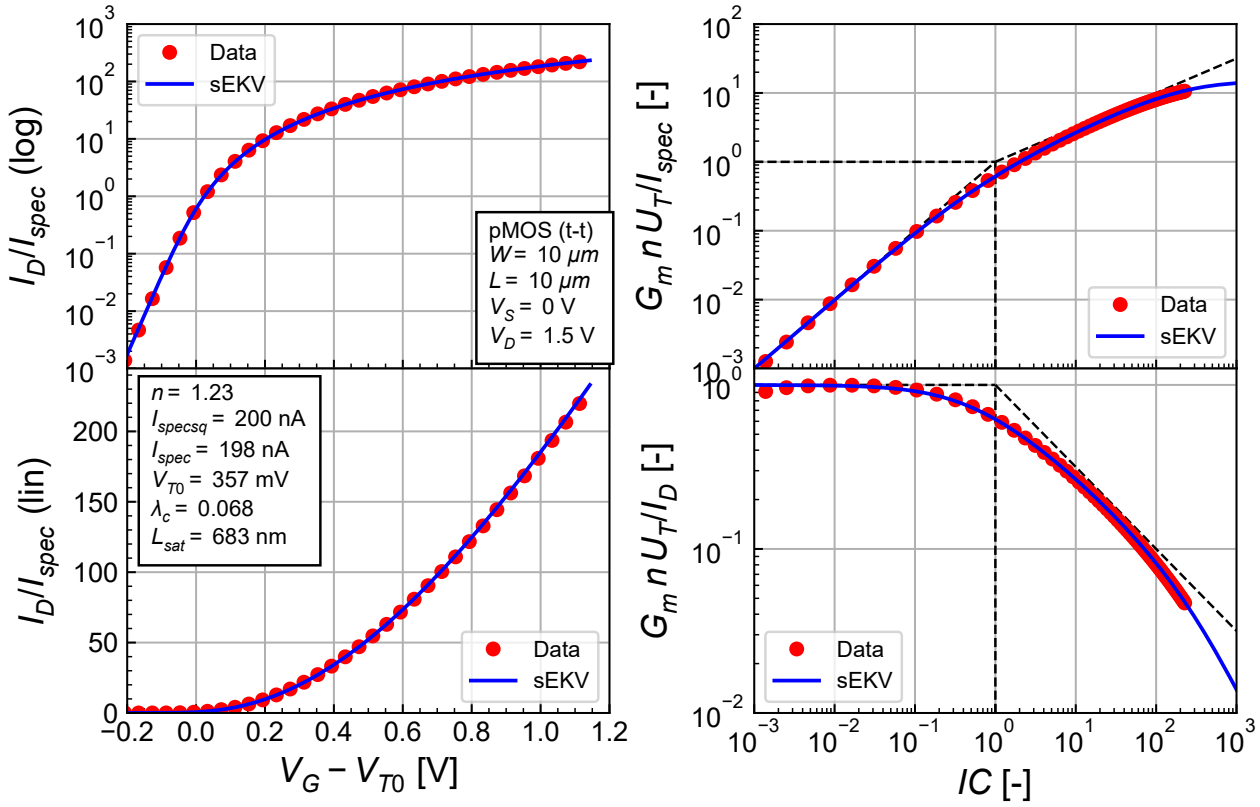

Figure 3.28: Summary of extraction by curve fitting with $\lambda_c = 0$.

Table 3.3: Extraction of the sEKV parameters using curve fitting with $\lambda_c > 0$.

Type	n	$I_{spec\square}$ $[nA]$	V_{T0} $[mV]$	λ_c	L_{sat} $[nm]$	Comment
pMOS	1.22	180	357	0.000	0	direct with $\lambda_c = 0$
pMOS	1.22	192	357	0.000	0	curve fitting with $\lambda_c = 0$
pMOS	1.23	200	357	0.068	683	curve fitting with $\lambda_c > 0$

4 Output characteristic

4.1 Generating and importing the data

In order to extract the CLM parameter in saturation, we will now filter out the points that correspond to the linear region. We can do this easily by looking at the G_{ds} versus V_D characteristic as shown in Figure 4.3. This done below where we will drop the blue points and keep the red points for the extraction.

4.1.1 I_D and G_{ds} versus V_D

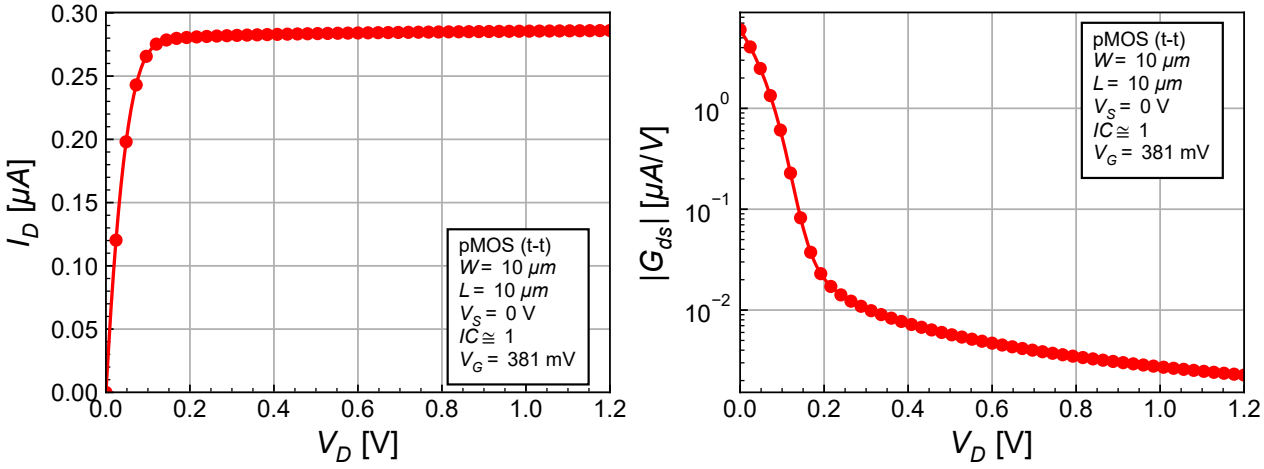

Figure 4.1: Imported I_D-V_D and G_{ds}-V_D.

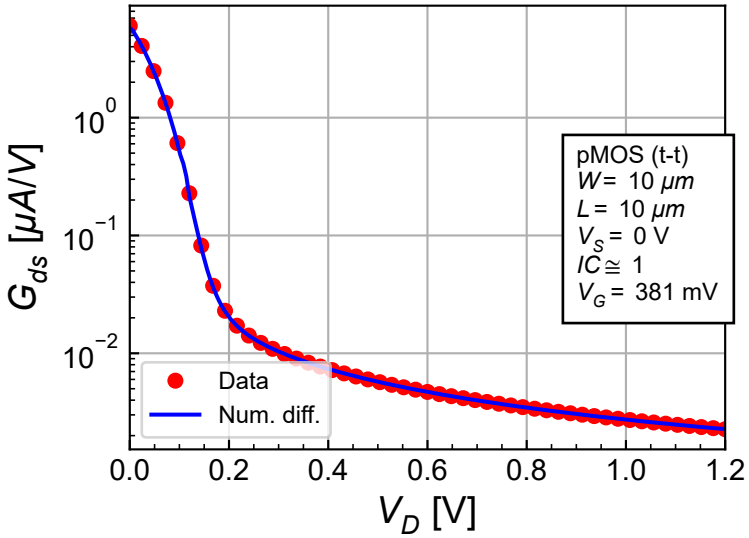

Figure 4.2: Check imported G_{ds} against computed G_{ds}.

The output conductance calculated by differentiating the large-signal I_D-V_D matches the value extracted from the PSP model. We will keep the value from PSP.

4.1.2 Filtering the outliers

In order to extract the CLM parameter in saturation, we will now filter out the points that correspond to the linear region. We can do this easily by looking at the G_{ds} versus V_D characteristic as shown in Figure 4.3.

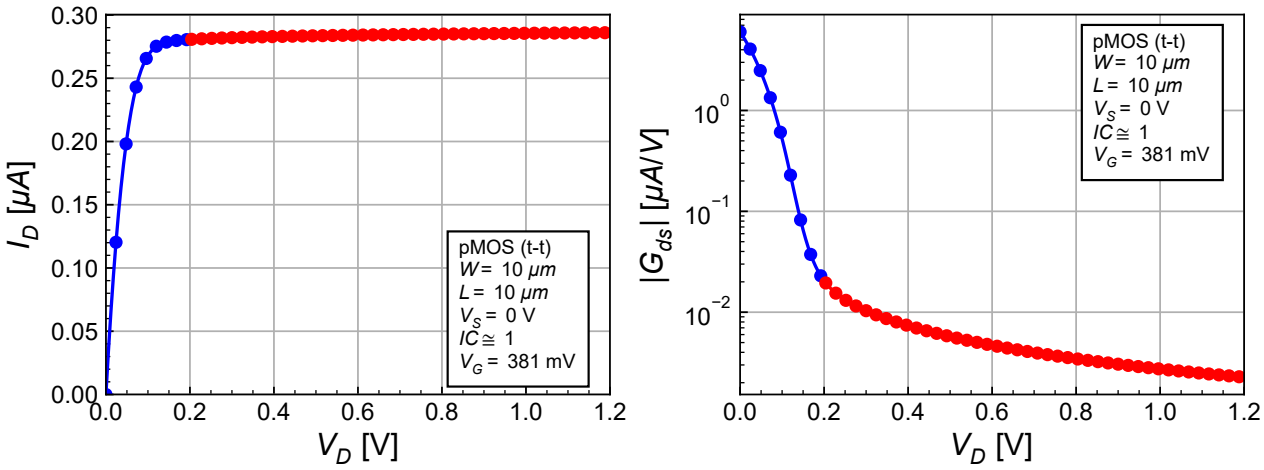

Figure 4.3: Filtering the outliers from I_D-V_G and G_{ds}-V_D.

4.2 Extracting the CLM parameter

The simple channel length modulation (CLM) of the output conductance in saturation is approximated by

$$G_{ds} = \frac{I_{D,sat}}{V_E} \tag{4.1}$$

where $I_{D,sat}$ is the drain current in saturation and

$$V_E = \lambda \cdot L_{eff} \tag{4.2}$$

is the Early voltage or CLM voltage which is proportionnal to the effectve length. This corresponds to a linear approximation of the drain current in saturation given by

$$I_{D,sat} \cong G_{ds} \cdot (V_D - V_E) \tag{4.3}$$

The value I_{D0} corresponds to the intercept

$$I_{D0} = -G_{ds} \cdot V_E \tag{4.4}$$

which is positive since V_E is negative.

Contrary to the nMOS transistor, the long-channel pMOS transistor has a smaller output conductance $G_{ds} = 4.623\ nA/V$ and a larger value of the λ parameter. This will lead to a better intrinsic gain for the pMOS.

As shown in the right plot of Figure 4.4, the output conductance is approximated by a constant value represented by the dashed black line. It is a poor approximation of the output conductance but good enough for starting a design. Note that, in analog circuit design, having a good fit of the

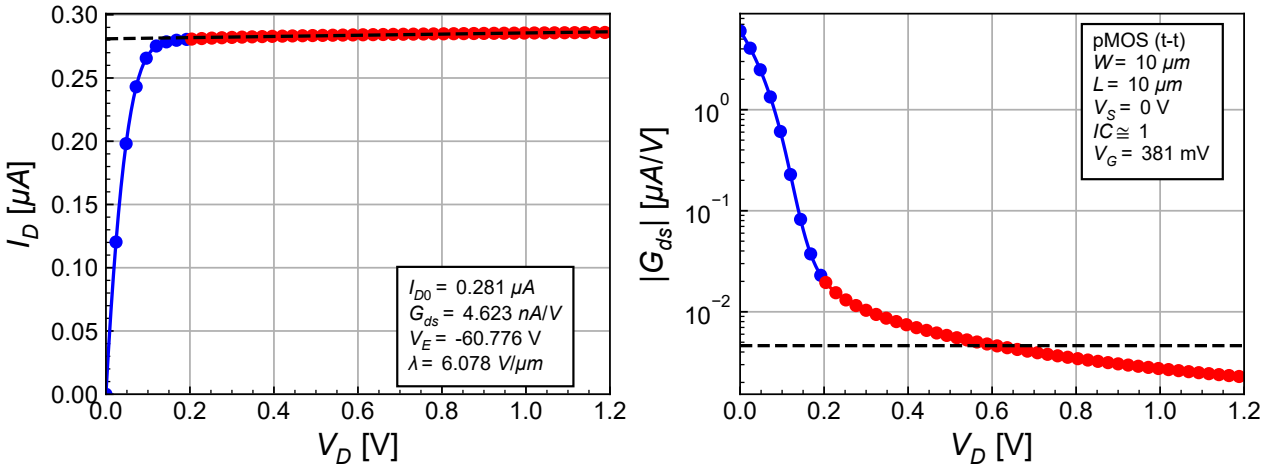

Figure 4.4: Extraction of the CLM parameter λ.

output conductance is less important than having a good fit of the transconductance because often we just need the intrinsic voltage gain to be large enough for the circuit to perform correctly, while we want to have a good estimation of the parameters depending on the transconductance, such as the gain-bandwidth product or the thermal noise.

Table 4.1: CLM parameters extracted in moderate inversion.

Type	L_{eff} [μm]	IC	G_{ds} [nA/V]	I_{D0} [μA]	V_E [V]	λ [$V/\mu m$]	Comment
pMOS	10.046	1	4.623	0.281	-60.776	6.078	moderate

5 Noise

In this section we will extract the flicker noise parameters to be used with sEKV and check the white noise power spectral desnity (PSD). We reuse the flicker noise model from EKV 2.6, where the input (gate) referred PSD is given by [7]

$$S_{nin,fl}(f) = \frac{KF}{W_{eff}\, L_{eff}\, C_{ox}\; f^{AF}} \tag{5.1}$$

In this model the flicker noise is assumed to scale as $1/C_{ox}$, which is correct if the noise follows the the Hooge model (i.e. originates from mobility fluctuations). In the case of the Mc Worther model (i.e. flicker noise originating from traps in Si-SiO_2 interface and in the oxyde), the PSD scales as C_{ox}^2. Despite the flicker noise is usually domanted by the trapping mechanism, we will keep the above model with a $1/C_{ox}$ scaling.

In EKV , we like to rewrite the flicker noise PSD like the thermal noise in terms of a input-referred noise resistance

$$S_{nin,fl}(f) = 4kT\, R_{nin,fl}(f) \tag{5.2}$$

where

$$R_{nin,fl}(f) = \frac{\rho}{W_{eff}\, L_{eff}\, f^{AF}} \tag{5.3}$$

with

$$\rho = \frac{KF}{4kT\, C_{ox}} \tag{5.4}$$

Note that the flicker noise parameter have some weird units. Indeed, KF is in $A \cdot V \cdot s^{2-AF}$ and ρ is in $V \cdot m^2/(A \cdot s^{AF})$. If $AF = 1$, like it is often the case, then KF is in $A \cdot V \cdot s$ and ρ is in $V \cdot m^2/(A \cdot s)$.

To extract the noise parameters, we use a common-source stage loaded by a noiseless resistor. We first will set the bias condition in terms of IC and calculate the input-referred white noise to compare it to the result obtained from the PSP simulations.

5.1 Setting the bias conditions

Having extracted n, $I_{spec\square}$ and V_{T0}, we can impose the inversion coefficient and calculate the corresponding gate voltage V_G. We nee to make sure the transistor remains in saturation.

We need to check that the transistor is biased in saturation. Setting the inversion coefficient to $IC = 1$ we get a drain current $I_D = 198\ nA$ corresponding to a gate voltage $V_G = 381\ mV$. The gate transconductance is estimated at $G_m = 3.865\ \mu A/V$. Setting the voltage gain to $A_v = G_m \cdot R_L = 10$ we get $R_L = 2587.329\ k\Omega$. For $V_{DD} = 1.2\ V$ we have $V_{DS} = 686\ mV$. With a saturation voltage $V_{DSsat} = 116\ mV$, the transistor is biased in the saturation region.

We can now proceed with the noise simulation and extract the PSP parameters and the PSD.

5.2 Extract operating point information

We can now check the operating point and extract the PSP noise parameters. The PSP operating point information are given in Table 5.1 and the PSP noise parameters are given in Table 5.2.

Table 5.1: PSP operating point.

Transistor	W_{eff} $[\mu m]$	L_{eff} $[\mu m]$	I_{DS} $[nA]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	Comment
Mp	9.970	10.046	199.477	3.929	2.754	extracted from PSP

Table 5.2: MOS PSP noise parameters.

Transistor	$\sqrt{S_{ninth}}$ $[nV/\sqrt{Hz}]$	$\sqrt{S_{ninfl}(1kHz)}$ $[nV/\sqrt{Hz}]$	f_k $[kHz]$	Comment
Mp	74.4	75.2	1.022	extracted from PSP

We see that the simulated bias current $I_D = 199\ nA$ is very close to the desired current $I_D = 198\ nA$ resulting in a predicted transconductance $G_m = 3.86\ \mu A/V$ that is also very close to the simulated transconductance $G_m = 3.93\ \mu A/V$.

5.3 Simulating noise PSD

We can now simulate the PSD and check against the EKV model. The square roots of the PSD are plotted versus frequency in Figure 5.1.

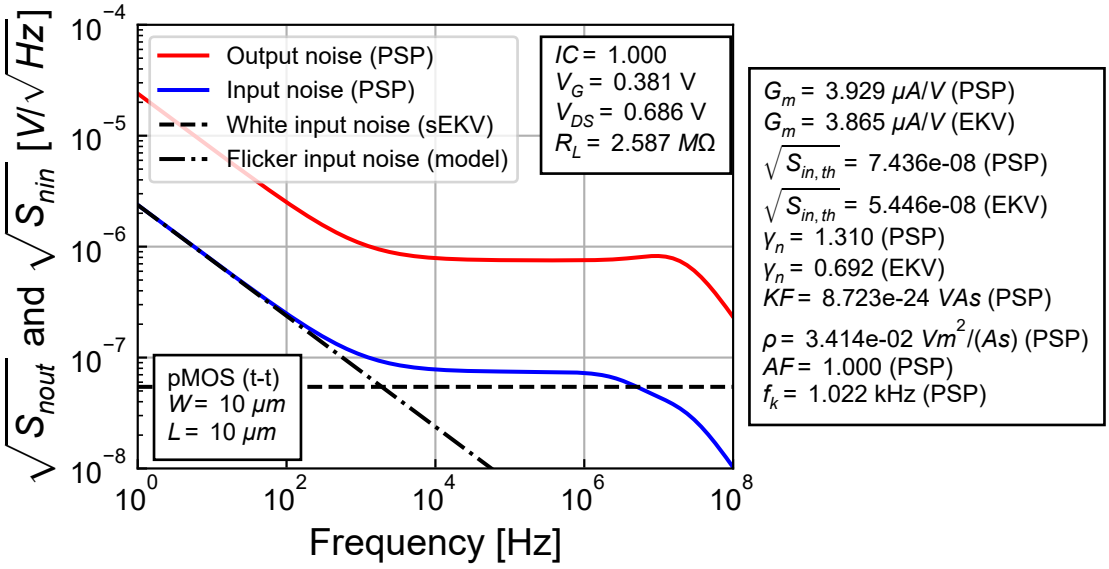

Figure 5.1: Output and input-referred PSD.

We see that the simulated white noise is sligthly higher than the sEKV estimation. This comes from the thermal noise exces factor which is significantly higher in PSP with $\gamma_n = 1.310$ compared to the sEKV value $\gamma_n = 0.692$. On the other hand the sEKV input-referred flicker noise estimation is right on top of PSP. The extracted sEKV flicker noise parameters are given in Table 5.3.

Table 5.3: Extraction of the sEKV flicker noise parameters.

Transistor	W_{eff} [μm]	L_{eff} [μm]	IC [-]	KF [J]	AF [-]	ρ_n $\left[\frac{V\,m^2}{A\,s}\right]$	Comment
Mn	9.970	10.046	1	8.723e-24	1.000	3.414e-02	moderate

6 Conclusion

This notebook presented different approaches to extract the sEKV parameters for a long-channel pMOS transistor for the 130nm IHP BiCMOS technology. The data was first obtained by simulations using the PSP compact model and the IHP PDK.

The sEKV parameters were first extracted using a direct extraction methodology with $\lambda_c = 0$. This results in a good fit over all regions of operation except in very strong inversion because effect of mobility reduction due to the vertical field is not included in the sEKV model. Things can be improved by using the λ_c parameter to account for this effect although this is a very long-channel transistor.

We also have checked the noise in moderate inversion and shown that the thermal noise which is slightly higher for the PSP model compared to the sEKV mode despite the transconductance being almost equal between PSP and sEKV. This comes from a larger thermal noise excess factor in PSP compared to sEKV. We have finally also extracted the flicker noise parameters.

Overall we have shown that sEKV can fit the large- and small-signal data of this is a long-channel pMOS transistor very well except for white noise which is higher in PSP compared to sEKV.

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