sEKV Parameter Extraction for the IHP 130nm Process

pMOS Extrinsic Capacitances

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1 Introduction

In this notebook we will extract the extrinsic capacitances, including junction, overlap and fringing capacitances for pMOS transistors of the 130nm bulk CMOS process from IHP [1]. The parameters is extracted from the PDK of the IHP 130nm process [1].

2 Transistor geometry parameters

2.1 Effective length and width for current

Before we start the extraction we need to account for the geometry dependence. With PSP you can choose between geometry scaling rules or binning rules with parameter $SWGEO$. If $SWGEO = 1$, the scaling rules are chosen. This is the case in the IHP 130nm G2 PDK. The geometrical parameters are defined in Figure 2.1 [2].

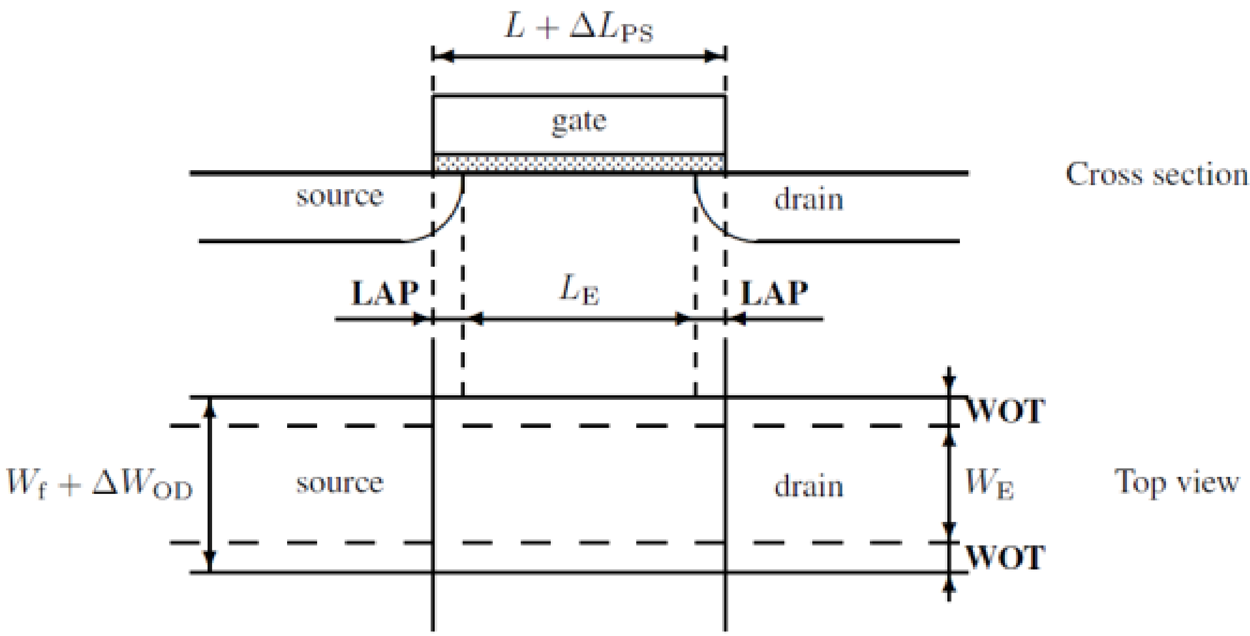

Figure 2.1: Definition of transistor geometrical parameters [2].

The effective length and width are defined as

$$L_{eff} = L - \Delta L, \tag{2.1}$$
$$W_{eff} = W_f - \Delta W, \tag{2.2}$$

where W_f is the width of one finger defined as

$$W_f = \frac{W}{NF}. \tag{2.3}$$

In our case we will assume that the number of fingers $NF = 1$ and hence that $W_f = W$. ΔL and ΔW are given by

$$\Delta L = 2\,LAP - \Delta L_{PS}, \tag{2.4}$$
$$\Delta W = 2\,WOT - \Delta W_{OD}, \tag{2.5}$$

with

$$\Delta L_{PS} = LVARO \cdot \left(1 + LVARL \cdot \frac{L_{EN}}{L}\right) \cdot \left(1 + LVARW \cdot \frac{W_{EN}}{W_f}\right), \tag{2.6}$$

$$\Delta W_{OD} = WVARO \cdot \left(1 + WVARL \cdot \frac{L_{EN}}{L}\right) \cdot \left(1 + WVARW \cdot \frac{W_{EN}}{W_f}\right). \tag{2.7}$$

Contrary to nMOS, for pMOS $LVARO \neq 0$ and $WVARO \neq 0$ and therefore $\Delta L_{PS} \neq 0$ and $\Delta W_{OD} \neq 0$. This means that the length and width reduction actually depend on the length L and width W. However, we can ignore this scaling of ΔL_{PS} and ΔW_{OD} with W and L and approximate ΔL_{PS} and ΔW_{OD} by taking the value for $L \to \infty$ and for $W \to \infty$ corresponding to

$$\Delta L_{PS} \cong LVARO, \tag{2.8}$$

$$\Delta W_{OD} \cong WVARO, \tag{2.9}$$

resulting in

$$\Delta L \cong 2\,LAP - LVARO, \tag{2.10}$$

$$\Delta W \cong 2\,WOT - WVARO. \tag{2.11}$$

The channel length and width reduction are then given in Table 2.1. Note that ΔL is negative which means that the effective length is longer than the drawn length.

2.2 Effective length and width for capacitances

The effective length and width are slightly different for the calculation of the capacitances. The effective length and width for the calculation of the intrinsic and overlap capacitances are defined as

$$L_{E,CV} = L - \Delta L_{CV}, \tag{2.12}$$

$$W_{E,CV} = W - \Delta W_{CV}, \tag{2.13}$$

where

$$\Delta L_{CV} = 2\,LAP - \Delta L_{PS} - DLQ, \tag{2.14}$$

$$\Delta W_{CV} = 2\,WOT - \Delta W_{OD} - DWQ. \tag{2.15}$$

Similarly to the length and width reduction for the current, the length and width reduction for the capacitance in the case of pMOS transistors depends on the transistor width W and length L. We can ignore this scaling of ΔL_{PS} and ΔW_{OD} by approximating them by the values obtained for for $W \to \infty$ and for $L \to \infty$ which leads to

$$\Delta L_{CV} \cong 2\,LAP - LVARO - DLQ, \tag{2.16}$$

$$\Delta W_{CV} \cong 2\,WOT - WVARO - DWQ. \tag{2.17}$$

The effective length and width for the calculation of the fringing field capacitances are defined as

$$L_{G,CV} = L - \Delta L_{G,CV}, \tag{2.18}$$

$$W_{G,ov} = W - \Delta W_{G,CV}, \tag{2.19}$$

where

$$\Delta L_{G,CV} = -\Delta L_{PS} - DLQ, \tag{2.20}$$

$$\Delta W_{G,CV} = -\Delta W_{OD} - DWQ, \tag{2.21}$$

which can be approximated in the same way by

$$\Delta L_{G,CV} \cong -LVARO - DLQ, \tag{2.22}$$

$$\Delta W_{G,CV} \cong -WVARO - DWQ. \tag{2.23}$$

Table 2.1: Length and width corrections.

Definition	ΔL [nm]	ΔW [nm]	Comment
For current	-46.442	30	extracted from PDK
For intrinsic and overlap capacitances	49.480	15	extracted from PDK
For fringing-field capacitances	-1.028	-15	extracted from PDK

3 Extrinsic capacitances

3.1 Junction capacitances

The calculation of the junction capacitances depends on the value used for the **SWJUNCAP** parameter. In this PDK **SWJUNCAP** is equal to 3 for which the junction area AB, junction length of side-wall capacitance along the STI edge LS and junction length of the side-wall capacitance along the gate edge LG are calculated according to

$$AB = AS, \tag{3.1}$$
$$LS = PS - W_E, \tag{3.2}$$
$$LG = W_E, \tag{3.3}$$
$$\tag{3.4}$$

where AS is the source junction area and PS the total source junction perimeter and

$$AB = AD, \tag{3.5}$$
$$LS = PD - W_E, \tag{3.6}$$
$$LG = W_E, \tag{3.7}$$
$$\tag{3.8}$$

where AD is the drain junction area and PD the total drain junction perimeter.

The total junction capacitance on the source CJS and drain side CJD are then given by

$$CJS = AS \cdot CJORBOT + (PS - W_E) \cdot CJORSTI + W_E \cdot CJORGAT, \tag{3.9}$$
$$CJD = AD \cdot CJORBOT + (PD - W_E) \cdot CJORSTI + W_E \cdot CJORGAT, \tag{3.10}$$

where:

- **CJORBOT** is the zero-bias bottom capacitance per unit-area,
- **CJORSTI** is the zero-bias capacitance per unit-of-length along the STI-edge,
- **CJORGAT** is the zero-bias capacitance per unit-of-length along the gate-edge.

The above junction capacitance parameters are extracted directly from the PDK. We will use the the zero-bias bias value of th various junctions capacitances.

If AS, PD, AD and PD are not specified, they are calculated automatically in the sg13g2_moslv_mod.lib file.

In the circuit examples, we will calculate AS, PD, AD and PD for avoiding the automatic cal.culation

Table 3.1: Extraction of the junction capacitance parameters.

Definition	Zero-bias junction capacitance	Unit	Comment
Bottom cap per area	8.631e-04	$\frac{F}{m^2}$	extracted from PDK
Side-wall cap per unit length (along STI)	3.192e-11	$\frac{F}{m}$	extracted from PDK
Side-wall cap per unit length (along gate)	2.747e-11	$\frac{F}{m}$	extracted from PDK

3.2 Overlap capacitances

In PSP, the gate-to-source and gate-to-drain overlap capacitances are equal and given by

$$CGOV = \epsilon_{ox} \cdot \frac{W_{E,CV} \cdot LOV}{TOXOV}, \tag{3.11}$$

where the effective length $L_{E,CV}$ and width $W_{E,CV}$ for the calculation of the intrinsic and overlap acacitances are defined as

$$L_{E,CV} = L + \Delta L_{CV}, \tag{3.12}$$

$$W_{E,CV} = W + \Delta W_{CV}, \tag{3.13}$$

where

$$\Delta L_{CV} = 2\,LAP - \Delta L_{PS} - DLQ \cong 2\,LAP - LVARO - DLQ, \tag{3.14}$$

$$\Delta W_{CV} = 2\,WOT - \Delta W_{OD} - DWQ \cong 2\,WOT - WVARO - DWQ. \tag{3.15}$$

3.3 Fringing capacitances

In PSP, the fringing field capacitance is given by

$$CFR = CFRW \cdot \frac{W_{G,CV}}{W_{EN}}, \tag{3.16}$$

where

$$W_{G,CV} = W_f + \Delta W_{OD} + DWQ \cong W_f + WVARO + DWQ \tag{3.17}$$

The values of the overlap and fringing capacitances per effective unit width for C_{GS} and C_{GD} and per effective unit length for C_{GB} are summarized in Table 3.2. We see that $CGBOn$ is almost negligible.

Table 3.2: Overlap and fringing capacitances per effective unit width for C_{GS} and C_{GD} and per effective unit length for C_{GB}.

Definition	C_{GS}	C_{GD}	C_{GB}	Unit	Comment
Overlap	4.426e-10	4.426e-10	2.186e-11	$\frac{F}{m}$	extracted from PDK
Fringing	1.000e-10	1.000e-10	-	$\frac{F}{m}$	extracted from PDK
Total	5.426e-10	5.426e-10	2.186e-11	$\frac{F}{m}$	extracted from PDK

4 Conclusion

The parameters of the extrinsic capacitances, including junction, overlap and fringing capacitances have been extracted from the PDK of the IHP 130nm process for the for pMOS transistors.

References

[1] IHP, "IHP SG13G2 Open Source PDK." https://github.com/IHP-GmbH/IHP-Open-PDK, 2025.

[2] G.D.J. Smit, A.J. Scholten, D.B.M. Klaassen, O. Rozeau, S. Martinie, T. Poiroux and J.C. Barbé, "PSP 103.6 - The PSP model is a joint development of CEA-Leti and NXP Semiconductors." https://www.cea.fr/cea-tech/leti/pspsupport/Documents/psp103p6_summary.pdf, 2017.