Design of the Telescopic OTA

Version 1

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2025-05-19

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1 Introduction

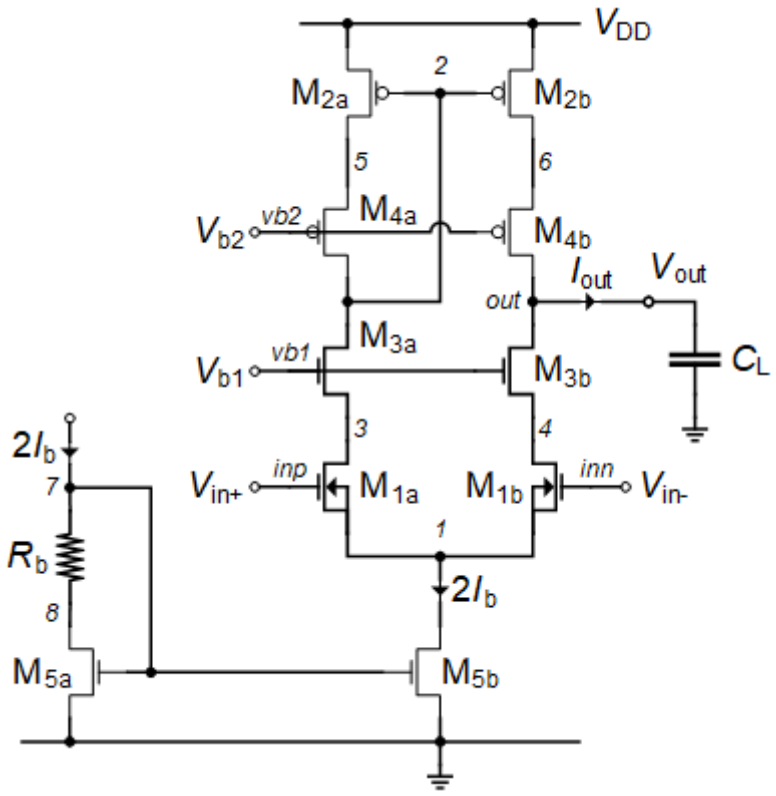

Figure 1.1: Schematic of the telescopic differential OTA.

> **Note**
>
> Note that all nMOS transistors in Figure 1.1 have an odd number and all the pMOS transistors an even number which explains the numbering process.

This notebook presents the analysis, design and simulation of the telescopic cascode OTA which schematic is presented in Figure 1.1 [1]. The design phase is using the sEKV model and the inversion coefficient approach [2], [3], [4]. The telescopic OTA is similar to the simple OTA except that four cascode transistors, namely M_{3a}-M_{3b} and M_{4a}-M_{4b}, have been added to decrease the output conductance and hence increase the DC gain. The GBW and hence the power consumption however remain almost unchanged.

Because of the stacked transistors, this OTA is a bit tricky to design particularly at low-voltage and presents a reduced output voltage swing. In order to save some voltage, we have put M_{1a}-M_{1b} in a separate well. This makes $V_{SB1a} = V_{SB1b} = 0$ and reduces V_{GS1a} and V_{GS1b} to a minimum. When designing the circuit, we particularly need to be careful when sizing the cascode transistors in weak inversion avoiding taking minimum length which would degrade their output conductance and hence the DC gain. This is explained in more details below.

As suggested in [1], we also have added the resistance R_b that will be sized in order for M_{5a} and M_{5b} to have about the same V_{DS} voltage. This makes sure that the current through M_{5a} and M_{5b} are about equal, despite the effect of the output conductance.

We will start with a detailed analysis of the OTA which will allow to derive all the design equations that will be used in the design phase. The OTA is then designed for a given set of specifications for the chosen IHP SG13G2 130nm BiCMOS technology [5]. We have selected this technology because IHP provides an open source PDK which is then used for the validation of the design by simulation with ngspice [6] using the PSP compact model [7] provided by the open source PDK [5].

2 Analysis

2.1 Small-signal analysis

We start with the small-signal analysis. The small-signal schematic of the telescopic OTA is shown in Figure 2.1. The analysis of the telescopic OTA is similar to the simple OTA, except that there are now additional nodes due to the cascode transistors.

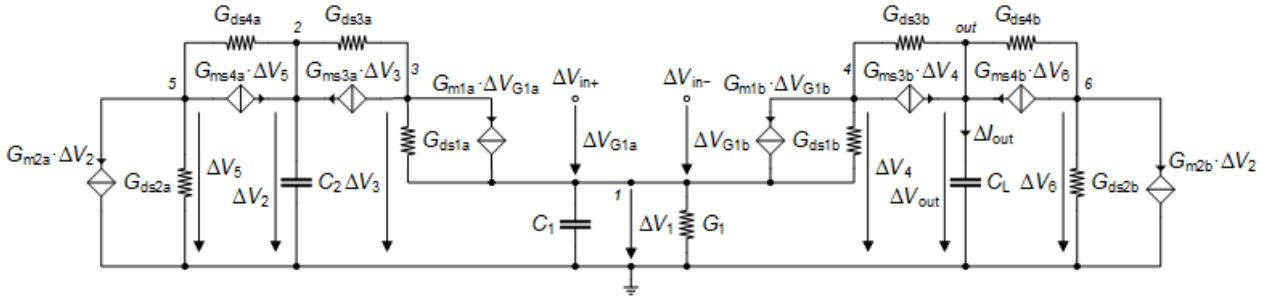

Figure 2.1: Small-signal schematic of the telescopic OTA.

For a differential input voltage, assuming a perfect matching between the transistors in the left and right current branches, the common-source node 1 of the differential pair M_{1a}-M_{1b} remains zero and the small-signal schematic of Figure 2.1 simplifies to the schematic shown in Figure 2.2.

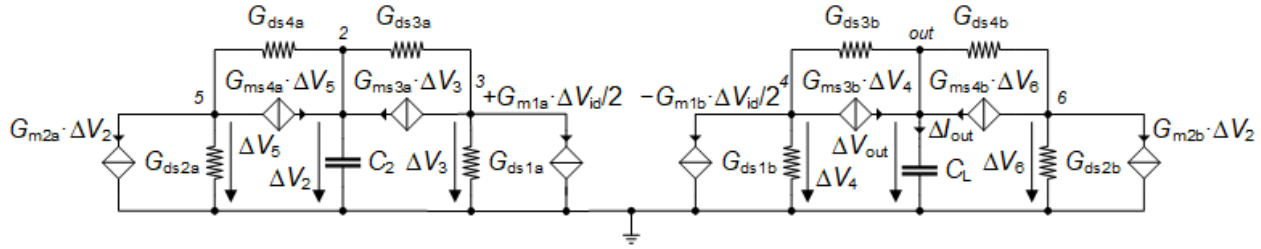

Figure 2.2: Simplified small-signal schematic of the telescopic OTA.

In a 1st-order analysis, we can neglect the capacitances at the low impedance cascode nodes 3, 4, 5 and 6 and only account for the capacitances at high impedance nodes 2 and out. The circuit becomes similar to that of the simple OTA, with the dominant pole ω_0 at the output node (out) and the non-dominant pole ω_p at the current mirror node 2. The transfer function also has a pole-zero doublet. Its transfer function is then given by

$$A_{dm}(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} \cong A_{dc} \cdot \frac{1 + s/\omega_z}{(1 + s/\omega_0)(1 + s/\omega_p)} \cong \frac{A_{dc}}{1 + s/\omega_0} \cong \frac{\omega_u}{s}, \tag{2.1}$$

where

$$A_{dc} \cong \frac{G_{m1}}{G_o}, \tag{2.2}$$

$$G_o \cong \frac{G_{ds1}\, G_{ds3}}{G_{ms3}} + \frac{G_{ds2}\, G_{ds4}}{G_{ms4}}, \tag{2.3}$$

$$\omega_0 \cong \frac{G_o}{C_L}, \tag{2.4}$$

$$\omega_p \cong \frac{G_{m2}}{C_2}, \tag{2.5}$$

$$\omega_z = 2\,\omega_p, \tag{2.6}$$

$$\omega_u = A_{dc} \cdot \omega_0 \cong \frac{G_{m1}}{C_L}. \tag{2.7}$$

We now anlyze the OTA noise in the next section.

2.2 Noise Analysis

At low-frequency the noise of the cascode transistors M_{3a}-M_{3b} and M_{4a}-M_{4b} can be neglected and the noise analysis is then identical to that of the simple OTA. The PSD of the output noise current is given by

$$S_{nout} \cong 2\,(S_{I_{n1}} + S_{I_{n2}}) \tag{2.8}$$

which can be expressed in terms of the output noise conductance as

$$S_{nout} = 4kT \cdot G_{nout}, \tag{2.9}$$

where

$$G_{nout} \cong 2\,(G_{n1} + G_{n2}), \tag{2.10}$$

with

$$G_{ni} = \gamma_{ni} \cdot G_{mi} + G_{mi}^2 \cdot \frac{\rho_i}{W_i\, L_i\, f} \quad \text{for } i = 1, 2. \tag{2.11}$$

The input-referred noise resistance is then given by

$$R_{nin} \triangleq \frac{G_{nout}}{G_{m1}^2} = \frac{2\,(G_{n1} + G_{n2})}{G_{m1}^2} = \frac{2\,G_{n1}}{G_{m1}^2} \cdot \left(1 + \frac{G_{n2}}{G_{n1}}\right) \tag{2.12}$$

which we rewrite as

$$R_{nin} = \frac{2\,G_{n1}}{G_{m1}^2} \cdot (1 + \eta) \tag{2.13}$$

with

$$\eta = \frac{G_{n2}}{G_{n1}}. \tag{2.14}$$

η represents the contribution of the current mirror referred to the input and normalized to the contribution of the differential pair. Of course during the design phase we will try to minimize η.

2.2.1 Input-referred thermal noise

The input-referred thermal noise resistance is given by

$$R_{nth} = \frac{2\,\gamma_{n1}}{G_{m1}} \cdot (1 + \eta_{th}), \tag{2.15}$$

where

$$\eta_{th} = \frac{\gamma_{n2}}{\gamma_{n1}} \cdot \frac{G_{m2}}{G_{m1}} \tag{2.16}$$

represents the contribution to the input-referred thermal noise of the current mirror M_{2a}-M_{2b} relative to that of the differential pair M_{1a}-M_{1b}. In case $G_{m1} \gg G_{m2}$ then $\eta_{th} \ll 1$ and the thermal noise is dominated by the input differential pair. Eqn. (2.16) can then be simplified to

$$R_{nth} \cong \frac{2\,\gamma_{n1}}{G_{m1}}. \tag{2.17}$$

The OTA thermal noise excess factor is then given by

$$\gamma_{ota} \triangleq G_m \cdot R_{nth} \tag{2.18}$$

with $G_m = G_{m1}$ is the OTA equivalent tranbsconductance. The OTA thermal noise excess factor then writes

$$\gamma_{ota} = 2\,\gamma_{n1} \cdot (1 + \eta_{th}). \tag{2.19}$$

In the case $G_{m1} \gg G_{m2}$ then $\eta_{th} \ll 1$ and the noise is dominated by the input differential pair M_{1a}-M_{1b}. The OTA thermal noise excess factor can then be simplified as

$$\gamma_{ota} \cong 2\,\gamma_{n1}. \tag{2.20}$$

2.2.2 Input-referred flicker noise

The input-referred flicker noise is given by

$$R_{nfl} = \frac{2}{f}\ \left[\frac{\rho_n}{W_1\,L_1} + \left(\frac{G_{m2}}{G_{m1}}\right)^2\ \frac{\rho_p}{W_2\,L_2}\right] \tag{2.21}$$

which can be rewritten as

$$R_{nfl} = \frac{2\rho_n}{W_1\,L_1\,f} \cdot (1 + \eta_{fl}) \tag{2.22}$$

where

$$\eta_{fl} = \frac{\rho_p}{\rho_n}\ \left(\frac{G_{m2}}{G_{m1}}\right)^2\ \frac{W_1\,L_1}{W_2\,L_2} \tag{2.23}$$

represents the contribution to the input-referred flicker noise of the current mirror M_{2a}-M_{2b} relative to that of the differential pair M_{1a}-M_{1b}. If M_{1a}-M_{1b} and M_{2a}-M_{2b} have about the same gate area, then η_{fl} can be made small by making $G_{m1} \gg G_{m2}$.

The corner frequency is the frequency at which the flicker noise becomes equal to the thermal noise

$$R_{nfl}(f = f_k) = R_{nth} \tag{2.24}$$

which is given by

$$f_k = \frac{1}{R_{nth}} \cdot \frac{2\rho_n}{W_1\,L_1} \cdot (1 + \eta_{fl}) = \frac{G_{m1}\,\rho_n}{\gamma_{n1}\,W_1\,L_1} \cdot \frac{1 + \eta_{fl}}{1 + \eta_{th}}. \tag{2.25}$$

The transconductance G_{m1} is set by the constraints either on thermal noise or on bandwidth (GBW product). The corner frequency f_k can be reduced by increasing $W_1\,L_1$ and $W_2\,L_2$ at the same time to conserve the same η_{fl} factor. Assuming that $G_{m2}/G_{m1} \ll 1$, as required by the constraints on minimizing the contribution of the current mirror to the input-referred offset and thermal noise, then $\eta_{th} \ll 1$ and $\eta_{fl} \ll 1$ and the corner frequency f_k is then mainly set by the differential pair transconductance and gate transistor area

$$f_k \cong \frac{G_{m1}\,\rho_n}{\gamma_{n1}\,W_1\,L_1}. \tag{2.26}$$

2.3 Input-referred offset voltage

The offset analysis is identical to that of the simple OTA because the contribution of the mismatch of the cascode transistors can be neglected. The random offset current is then mainly due to the mismatch between M_{1a} and M_{1b} and between M_{2a} and M_{2b}. The variance of the output offset current is then given by

$$\sigma^2_{I_{os}} \cong \sigma^2_{\Delta I_{D1}} + \sigma^2_{\Delta I_{D2}} = I_b^2 \cdot \left(\sigma^2_{\frac{\Delta I_{D1}}{I_{D1}}} + \sigma^2_{\frac{\Delta I_{D2}}{I_{D2}}} \right), \tag{2.27}$$

with

$$\sigma^2_{\frac{\Delta I_{Di}}{I_{Di}}} = \sigma^2_{\beta_i} + \left(\frac{G_{mi}}{I_b} \right)^2 \sigma^2_{V_{Ti}} \quad \text{for } i = 1, 2, \tag{2.28}$$

where

$$\sigma^2_{\beta_i} = \frac{A^2_\beta}{W_i\, L_i} \quad \text{for } i = 1, 2 \tag{2.29}$$

is the β-mismatch and

$$\sigma^2_{V_{Ti}} = \frac{A^2_{V_T}}{W_i\, L_i} \tag{2.30}$$

is the V_T-mismatch.

The variance of the output offset current then becomes

$$\sigma^2_{I_{os}} = I_b^2 \cdot (\sigma^2_{\beta_1} + \sigma^2_{\beta_2}) + G^2_{m1} \cdot \sigma^2_{V_{T1}} + G^2_{m2} \cdot \sigma^2_{V_{T2}}. \tag{2.31}$$

The variance of the input-referred offset voltage is obtained by dividing the variance of the output offset current by G^2_{m1} resulting in

$$\sigma^2_{V_{os}} = \left(\frac{I_b}{G_{m1}} \right)^2 (\sigma^2_{\beta_1} + \sigma^2_{\beta_2}) + \sigma^2_{V_{T1}} + \left(\frac{G_{m2}}{G_{m1}} \right)^2 \sigma^2_{V_{T2}} \tag{2.32}$$

which can be written as

$$\sigma^2_{V_{os}} = \sigma^2_{V_{T1}} \cdot (1 + \xi_{V_T}) + \left(\frac{I_b}{G_{m1}} \right)^2 \cdot \sigma^2_{\beta_1} \cdot (1 + \xi_\beta), \tag{2.33}$$

where ξ_{V_T} represents the V_T-mismatch contribution to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_{V_T} = \left(\frac{G_{m2}}{G_{m1}} \right)^2 \cdot \frac{\sigma^2_{V_{T2}}}{\sigma^2_{V_{T1}}} \tag{2.34}$$

and ξ_β represents the β-mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_\beta = \frac{\sigma^2_{\beta_2}}{\sigma^2_{\beta_2}} \tag{2.35}$$

with

$$\sigma_{V_{T1}} = \frac{A^2_{V_{Tn}}}{W_1\, L_1}, \tag{2.36}$$

$$\sigma_{V_{T2}} = \frac{A^2_{V_{Tp}}}{W_2\, L_2} \tag{2.37}$$

and

$$\sigma^2_{\beta_1} = \frac{A^2_{\beta_n}}{W_1\, L_1}, \tag{2.38}$$

$$\sigma^2_{\beta_2} = \frac{A^2_{\beta_p}}{W_2\, L_2}. \tag{2.39}$$

Replacing in (2.34) and (2.35) results in

$$\xi_{V_T} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \cdot \left(\frac{A_{V_{T_p}}}{A_{V_{T_p}}}\right)^2 \cdot \frac{W_1\, L_1}{W_2\, L_2} \tag{2.40}$$

and

$$\xi_\beta = \left(\frac{A_{\beta_p}}{A_{\beta_n}}\right)^2 \cdot \frac{W_1\, L_1}{W_2\, L_2}. \tag{2.41}$$

Assuming that the V_T-mismatch parameters $A_{V_{Tn}}$ and $A_{V_{Tp}}$ and the area $W_1\, L_1$ and $W_2\, L_2$ are of the same order of magnitude, the contribution of the current mirror M_{2a}-M_{2b} to the V_T-mismatch represented by the ξ_{V_T} parameter can be made small by choosing $G_{m1} \gg G_{m2}$. If this does not suffice, we can increase the area of M_{2a}-M_{2b} keeping its W/L ratio.

The contribution of M_{2a}-M_{2b} to the β-mismatch, represented by the ξ_β factor, is not weighted by the G_m ratio. Assuming that the β-mismatch parameters A_{β_n} and A_{β_p} are of the same order of magnitude, ξ_β can be reduced by increasing the area of M_{2a}-M_{2b} keeping its W/L ratio.

3 Design

3.1 Specifications

The OTA specifications are given in Table 3.1.

> **Warning**
>
> An important limitation of the IHP SC13G2 BiCMOS technology [5] is the high output conductance and hence limited intrinsic gain of nMOS transistors. Because of this and voltage constraint inherent to the telescopic OTA [1], the specification on the DC gain has been set to 60 dB.

> **Note**
>
> The specifications given in Table 3.1 are simplified specifications. They are mainly targeting the achievement of a certain gain-bandwidth product GBW and DC gain at lowest current consumption. The GBW sets the differential pair transconductance while the DC gain sets the output conductance. There is an additional specification on the random input-referred offset voltage which, if not met, might eventually require to increase the transistors area. There are no specifications on thermal noise since the transconductance is set by the GBW. There are no specifications on the flicker noise but if the corner frequency was set lower this would required to increase the transistors area. There are also no specifications on the slew-rate, which might be small because of the low-power objective. Finally, there are many more specifications such as CMRR, PSRR, input common-mode voltage range, output-voltage swing, etc... that are not discussed in this example.

Table 3.1: OTA specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	60	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF
Maximum input-referred random offset voltage	V_{os}	10	mV
Phase margin	PM	60	$^\circ$
Corner frequency	f_k	100	kHz

3.2 Process

We will design the cascode gain stage for the open source IHP 13G2 BiCMOS process [5]. The physical parameters are given in Table 3.2, the global process parameters in Table 3.3 and finally the MOSFET parameters in Table 3.4.

> **Warning**
>
> The matching parameters for IHP 130nm are unknown. We will use those from a generic 180nm technology.

Table 3.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.865	mV

Table 3.3: Process parameters.

Parameter	Value	Unit	Comment
t_{ox}	2.24	nm	SiO_2 oxyde thickness
C_{ox}	15.413	$\frac{fF}{\mu m^2}$	Oxyde capacitance per unit area
V_{DD}	1.2	V	Nominal supply voltage
L_{min}	130	nm	Minimum drawn gate length
W_{min}	150	nm	Minimum drawn gate width
z_1	340	nm	Minimum outer diffusion width
z_2	389	nm	Minimum diffusion width between two fingers

Table 3.4: Transistors parameters.

Parameter	nMOS	pMOS	Unit
Length and width correction parameters for current			
DL	59	51	nm
DW	-20	30	nm
Length and width correction for intrinsic and overlap capacitances			
$DLCV$	93	146	nm
$DWCV$	-10	15	nm
Length and width correction parameter for fringing capacitances			
$DLGCV$	34	96	nm
$DWGCV$	10	-15	nm
Long-channel sEKV parameters parameters			
n	1.22	1.23	-
$I_{spec\square}$	708	245	nA
V_{T0}	246	365	mV
Short-channel sEKV parameters parameters			
L_{sat}	7.1	24.9	nm
λ	1.375	6.078	$\frac{V}{\mu m}$
Junction capacitances parameters			
C_J	0.976	0.863	$\frac{fF}{\mu m^2}$
C_{JSWSTI}	0.025	0.032	$\frac{fF}{\mu m}$
C_{JSWGAT}	0.03	0.027	$\frac{fF}{\mu m}$
Overlap capacitances parameters			
C_{GSo}	0.453	0.443	$\frac{fF}{\mu m}$
C_{GDo}	0.453	0.443	$\frac{fF}{\mu m}$
C_{GBo}	0	0.022	$\frac{fF}{\mu m}$

Table 3.4: Transistors parameters.

Parameter	nMOS	pMOS	Unit
Fringing capacitances parameters			
C_{GSf}	0.2	0.1	$\frac{fF}{\mu m}$
C_{GDf}	0.2	0.1	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	2.208e-24	1.2e-23	VAs
AF	1	1	-
ρ	0.008642	0.04697	$\frac{Vm^2}{As}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$

3.3 Design procedure

> **!** Important
>
> For this process, the transistor dimensions are rounded to 10nm. We also will ignore the length and width reduction parameters DL and DW. The main reason is that most of the transistor length and width are sufficiently large that ignoring these parameters has little impact.

3.4 Sizing of M_{1a}-M_{1b}

M_{1a}-M_{1b} are biased in weak inversion in order to minimize the input-referred offset. They are sized according to the specification on the GBW and the load capacitance and the required slew-rate.

Recalling that

$$GBW = \frac{G_{m1}}{2\pi C_{out}}, \tag{3.1}$$

where C_{out} is the total output capacitance which includes the parasitic capacitance and the load capacitance C_L. Since we do not yet know the sizes of M_{1a} and M_{2b}, we cannot estimate the total output capacitance. We will start assuming $C_{out} = C_L$.

G_{m1} is the gate transconductance of M_{1a} and M_{1b} which in deep weak inversion is given by

$$G_{m1} = \frac{I_b}{nU_T}. \tag{3.2}$$

The bias current I_b is the current flowing in each transistor M_{1a} and M_{1b} when the input differential voltage is zero. The bias current provided by M_{3b} is therefore $2I_b$. The bias current must satisfy the following inequality

$$I_b \geq 2\pi n_{0n} U_T C_L GBW_{min}. \tag{3.3}$$

which for the given specifications gives $I_{b,min} = 198\ nA$. The corresponding slew-rate is given by $SR_{min} = 198\ mV/\mu s$, which we will consider as sufficient.

> **!** Important
>
> If the slew-rate is not sufficient, the bias current I_b should be increased resulting in a higher current and power consumption. Other options include the use of a class AB OTA [8] or a

dynamic/adaptive biasing OTA [9].

Because the cascode transistors M_{3b} and M_{4b} will be rather large, they will add a significant parasitic capacitance to the ouput node that add to the load capacitance C_L. We therefore need to take some margin to account for these additional parasitic capacitances at the output by setting the bias current to $I_b = 250\ nA$ and the inversion coefficient to $IC_1 = 0.1$. The transconductance G_{m1} of M_{1a}-M_{1b} can be calculated from the G_m/I_D function as $G_{m1} = 7.258\ \mu A/V$. This leads to the following gain-bandwidth product $GBW = 1.2\ MHz$, which is slightly higher than the target specification offering some margin. Knowing the drain current I_D and the inversion coefficient IC, we can calculate $I_{spec1} = 2.5\ \mu A$ and $W_1/L_1 = 3.5$. The degree of freedom left (W_1 or L_1) can be determined from the specification on the maximum flicker noise corner frequency

$$f_k = \frac{\rho_n\, G_{m1}}{W_1\, L_1\, \gamma_{n1}} \cdot \frac{1+\eta_{fl}}{1+\eta_{th}} \cong \frac{\rho_n\, G_{m1}}{W_1\, L_1\, \gamma_{n1}}, \tag{3.4}$$

where we have assumed that $\eta_{th} \ll 1$ and $\eta_{fl} \ll 1$. We can then deduce the gate area of M_{1a}-M_{1b} as

$$W_1\, L_1 = \frac{\rho_n\, G_{m1}}{f_k\, \gamma_{n1}} \cdot \frac{1+\eta_{fl}}{1+\eta_{th}} \cong \frac{\rho_n\, G_{m1}}{f_k\, \gamma_{n1}}. \tag{3.5}$$

This leads to $W_1\, L_1 = 1.00\ \mu m^2$ and $W_1 = 1.88\ \mu m$ and $L_1 = 0.53\ \mu m$. Although the length of M_{1a}-M_{1b} is 4.077 times longer than the minimum, it might not be long enough in order to reach the desired DC gain.

We therefore choose $L_1 = 1.30\ \mu m$ and keeping the same W/L we get $W_1 = 1.88\ \mu m$. The transistor is larger and the corner frequency should be lower than the specs.

We have finalized the sizing of the differential pair M_{1a}-M_{1b}. We can now size the pMOS current mirror M_{2a}-M_{2b}.

3.5 Sizing of M_{2a}-M_{2b}

Because of the transistors stacking, the design of the telescopic OTA becomes tricky at low voltage. The current mirror M_{2a}-M_{2b} should be biased as much in strong inversion as the voltage constraint allows for. In order to leave enough voltage headroom for the nMOS transistors, we choose to set the quiescent output voltage a bit hgiher than $V_{DD}/2$ to $V_{outq} = 0.700\ V$. The V_{SG2} voltage will set the open-loop quiescent output voltage and is therefore equal to $V_{SG2} = V_{DD} - V_{outq} = 500\ mV$. This corresponds to an inversion coefficient equal to $IC_2 = 5.1$ and a saturation voltage $V_{SDsat2} = 156\ mV$. Having set the inversion coefficient and bias current we can derive $I_{spec2} = 48.63\ nA$ and $W_2/L_2 = 0.199$. Having IC and I_D, we can deduce $G_{m2} = 2.785\ \mu A/V$.

We will now have to make sure that the non-dominant pole f_p at node 2 is sufficiently higher than the gain-bandwidth product GBW to insure the desired phase margin. The non-dominant pole is given by

$$\omega_p = \frac{G_{m2}}{C_2}, \tag{3.6}$$

where C_2 is given by

$$C_2 = 2(C_{GS2} + C_{GB2}) \tag{3.7}$$

Assuming M_{2a}-M_{2b} are biased in saturation, we have

$$C_{GS2} \cong W_2\, L_2\, C_{ox} \cdot c_{gsi} + (C_{GSop} + C_{GSfp}) \cdot W_2 \tag{3.8}$$

where c_{gsi} is the normalized intrinsic gate-to-source capacitance which is typically equal to 2/3 in strong inversion and is proportionnal to IC in weak inversion. The gate-to-bulk capacitance C_{GB2} is given by

$$C_{GB2} \cong\ W_2\, L_2\, C_{ox} \cdot c_{gbi} + C_{GBop} \cdot W_2, \tag{3.9}$$

where c_{gbi} is the normalized gate-to-bulk intrinsic capacitance given by

$$c_{gbi} = \frac{n-1}{n} \cdot c_{gsi}. \tag{3.10}$$

The capacitance at node 2 scales with W_2 and L_2 according to

$$C_2 = C_{WL} \cdot W_2 L_2 + C_W \cdot W_2, \tag{3.11}$$

with

$$C_{WL} = 2\, C_{ox} \cdot (c_{gsi} + c_{gbi}), \tag{3.12}$$
$$C_W = 2(C_{GSop} + C_{GSfp} + G_{GBop}). \tag{3.13}$$

Since the W/L has already been set by the transconductance and the current, we can derive W_2 and L_2 for achieving a given capacitance C_2 according to

$$W_2 = \frac{-C_W \cdot W_2/L_2 + \sqrt{W_2/L_2} \cdot \sqrt{4\, C_2\, C_{WL} + C_W^2 \cdot W_2/L_2}}{2\, C_{WL}}, \tag{3.14}$$

$$L_2 = \frac{W_2}{W_2/L_2}. \tag{3.15}$$

Setting the non-dominant pole f_p to 10 times the GBW, we get $C_2 = 38$ fF, $L_2 = 3.20\ \mu m$ and $W_2 = 640\ nm$.

We can now check the resulting corner frequency which is given by $f_k = 54.165\ kHz$, which is lower than the specification $f_k = 100.000\ kHz$, which is fine.

3.6 Sizing of M_{3a}-M_{3b} and M_{4a}-M_{4b}

The cascode transistors are sized according to the desired DC gain given by

$$A_{dc} = \frac{G_{m1}}{G_o} \tag{3.16}$$

where G_o is the conductance at the output node given by

$$G_o \cong G_{o1} + G_{o2} \tag{3.17}$$

with

$$G_{o1} = \frac{G_{ds1b} \cdot G_{ds3b}}{G_{ms3b}}, \tag{3.18}$$

$$G_{o2} = \frac{G_{ds2b} \cdot G_{ds4b}}{G_{ms4b}}. \tag{3.19}$$

To have some margin on the DC gain we will design for a minimum DC gain higher than the specification given by $A_{dc} = 70$ dB or $A_{dc} = 3.162\text{e+}03$. We can then deduce the output conductance as $G_o = G_{m1}/A_{dc} = 2.295\ nA/V$. We will split the output conductance G_o equally between the nMOS and pMOS cascodes.

To minimize the saturation voltage and maximize the current efficiency, the cascode transistors M_{3a}-M_{3b} and M_{4a}-M_{4b} are biased in weak inversion. We choose their inversion coefficient as $IC_4 = IC_3 = 0.1$, which gives a saturation voltage $V_{DSsat4} = 105\ mV$. Having set the IC and knowing the bias current, we can deduce $I_{spec3} = 2.5\ \mu A$ and $W_3/L_3 = 3.530$ for M_{3a}-M_{3b} and $I_{spec4} = 2.5\ \mu A$ and $W_4/L_4 = 10.221$ for M_{4a}-M_{4b}. We can now calculate the G_{ms} that is needed for the calculation of

the output conductances $G_{ms3} = 8.854\ \mu A/V$ and $G_{ms4} = 8.854\ \mu A/V$. Having already the length of M_{2a}-M_{2b}, we can estimate its output conductance G_{ds2} as $G_{ds2} = 12.854\ nA/V$. We can then deduce the output conductance G_{ds4} of M_{4a}-M_{4b} as $G_{ds4} = 790.5\ nA/V$, which corresponds to a cascode gain $G_{ms4}/G_{ds4} = 11.2$. We can deduce the length of M_{4a}-M_{4b} from G_{ds4} as $L_4 = 50\ nm$, which is smaller than L_{min}.

In order not to degrade the output conductance, we choose $L_4 = 10$ times L_{min} resulting in $L_4 = 1.30\ \mu m$, which gives a width equal to $W_4 = 13.29\ \mu m$. We can re-estimate the output conductances $G_{o2} = 0.046\ nA/V$ giving $G_{o1} = 2.249\ nA/V$.

Since we already know the length $L_1 = 1.30\ \mu m$ and the current $I_b = 250\ nA$ for M_{1a}-M_{1b}, we can estimate its output conductance $G_{ds1} = 139.860\ nA/V$. The output conductance of M_{3a}-M_{3b} is then given by $G_{ds3} = 142.045\ nA/V$ from which we can deduce its length $L_3 = 1.28\ \mu m$ and its width $W_3 = 4.51\ \mu m$.

In order to maximize the DC gain we will choose $L_3 = 2.60\ \mu m$. Keeping the same W/L results in $W_3 = 9.18\ \mu m$. The DC gain is now $A_{dc} = 75.998$ dB.

3.7 Sizing M_{5a}-M_{5b}

The sizing of M_{5a}-M_{5b} is conditioned by the minimum input common-mode voltage keeping M_{5a}-M_{5b} in saturation

$$V_{ic,min} = V_{GS1} + V_{DSsat5} \tag{3.20}$$

The gate-to-source voltage V_{GS1} is given by

$$V_{GS1} = V_{T0n} + (n_{0n} - 1)\, V_{S1} + n_{0n}\, U_T\, (v_p - v_s) \tag{3.21}$$

Since M_{1a}-M_{1b} are in a separate well $V_{SB1} = 0$. Additionally in weak inversion we can consider $v_p - v_s \cong 0$. V_{GS1} can therefore be approximated by $V_{GS1} \cong V_{T0n}$. This gives $V_{GS1} = 246\ mV$, which for $V_{ic} = V_{DD}/2 = 600\ mV$ leaves $V_{DS3} = 354\ mV$. If we set the saturation voltage of M_{5a}-M_{5b} to $V_{DSsat5} = 150\ mV$, this corresponds to an inversion coefficient $IC_5 = 4.4$. Having the IC and the current we can derive $I_{spec5} = 113\ nA$ and $W_5/L_5 = 0.160$. Since W_5/L_5 is small, we need to set W_5 to $W_5 = W_{min} = 150\ nm$ resulting in $L_5 = 0.94\ \mu m$. Note that the minimum input common-mode voltage is then given by $V_{ic,min} = 396\ mV$.

We still need to calculate the required bias voltages V_{b1} for M_{3a}-M_{3b} and V_{b2} for M_{4a}-M_{4b} which is done in the next section.

3.8 Bias voltages V_{b1} and V_{b2}

We start calculating the maximum bias voltage $V_{b2,max}$ still keeping M_{2a}-M_{2b} in saturation

$$V_{b2,max} = V_{DD} - V_{SG4} - V_{SDsat2} \tag{3.22}$$

with $V_{SG4} = 295\ mV$ and $V_{SDsat2} = 156\ mV$, we get $V_{b2,max} = 0.749\ V$.

We also want to make sure that the V_{SD} voltage across M_{4a}-M_{4b} is large enough not to degrade its output conductance

$$V_{b2,min} = V_{SD4} - V_{SG4} + V_{DD} - V_{SG2} \tag{3.23}$$

Setting the source-to-drain voltage of M_{4a}-M_{4b} to $V_{SD4} = 200\ mV$, we get $V_{b2,min} = 0.605\ V$.

Similarly, we can calculate the maximum bias voltage $V_{b1,max}$ still keeping M_{3a}-M_{3b} in saturation

$$V_{b1,max} = V_{GS3} - V_{DSsat3} - V_{SG2} + V_{DD}. \tag{3.24}$$

With $V_{GS3} = 176\ mV$, $V_{DSsat3} = 105\ mV$ and $V_{SG2} = 500\ mV$, we get $V_{b1,max} = 0.772\ V$. If we want to have $V_{DS3} = 200\ mV$ in order not to degrade the output conductance of M_{3a}-M_{3b}, the corresponding V_{b1} is given by $V_{b1} = 0.676\ V$. The input common-mode voltage V_{ic} corresponding to this V_{b1} bias voltage, allocating also $V_{DS1} = 200\ mV$ for M_{1a}-M_{1b} in order not to degrade its output conductance, is given by $V_{ic} = 0.546\ V$.

We will choose $V_{b1} = 0.700\ V$ and $V_{b2} = 0.600\ V$ and eventually will need to fine tune these values from simulations.

The design is now finalized. The transistor sizes and bias are summarized below.

3.9 Summary

3.9.1 Specifications

The specifications are recalled in Table 3.5.

Table 3.5: OTA specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	60	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF
Maximum input-referred random offset voltage	V_{os}	10	mV
Phase margin	PM	60	$^\circ$
Corner frequency	f_k	100	kHz

3.9.2 Bias

The bias information are summarized in Table 3.6.

Table 3.6: OTA bias.

Bias voltage or current	Symbol	Value	Unit
Supply voltage	V_{DD}	1.2	V
Bias current	I_b	250.0	nA
Cascode bias voltage	V_{b1}	0.7	V
Cascode bias voltage	V_{b2}	0.6	V

3.9.3 Transistor information

The transistor sizes and large-signal variables are summarized in Table 3.7, whereas Table 3.8 gives the small-signal and thermal noise parameters. An Excel table is generated with more information (e.g. all the parasitic capacitances).

Table 3.7: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M1a	1.88	1.30	250	1024	0.2	-25	107
M1b	1.88	1.30	250	1024	0.2	-25	107

Table 3.7: Transistor size and bias information.

Transistor	$W\ [\mu m]$	$L\ [\mu m]$	$I_D\ [nA]$	$I_{spec}\ [nA]$	IC	$V_G - V_{T0}\ [mV]$	$V_{DSsat}\ [mV]$
M2a	0.64	3.20	250	49	5.1	89	156
M2b	0.64	3.20	250	49	5.1	89	156
M3a	9.18	2.60	250	2501	0.1	-47	105
M3b	9.18	2.60	250	2501	0.1	-47	105
M4a	13.29	1.30	250	2501	0.1	-46	105
M4b	13.29	1.30	250	2501	0.1	-46	105
M5a	0.15	0.94	500	113	4.4	81	150
M5b	0.15	0.94	500	113	4.4	81	150

Table 3.8: Transistor small-signal and thermal noise parameters.

Transistor	$G_{spec}\ [\mu A/V]$	$G_{ms}\ [\mu A/V]$	$G_m\ [\mu A/V]$	$G_{ds}\ [nA/V]$	γ_n
M1a	39.602	8.035	6.586	139.860	0.644
M1b	39.602	8.035	6.586	139.860	0.644
M2a	1.891	3.433	2.791	12.854	0.747
M2b	1.891	3.433	2.791	12.854	0.747
M3a	96.689	8.855	7.258	69.930	0.627
M3b	96.689	8.855	7.258	69.930	0.627
M4a	96.678	8.855	7.199	31.640	0.632
M4b	96.678	8.855	7.199	31.640	0.632
M5a	4.370	7.262	5.953	386.847	0.737
M5b	4.370	7.262	5.953	386.847	0.737

4 OTA Characteristics

In this section, we check whether the specs are achieved.

4.1 Open-loop gain

We can calculate the various OTA features related to the open-loop transfer function, which are given in Table 4.1.

Table 4.1: OTA gain variables.

Symbol	Theoretical Value	Unit
A_{dc}	75.155	dB
G_{m1}	6.586	$\mu A/V$
G_{ds1}	139.860	nA/V
G_{m2}	2.791	$\mu A/V$
G_{ds2}	12.854	nA/V
G_{ms3}	8.855	$\mu A/V$
G_{ds3}	69.930	nA/V
G_{ms4}	8.855	$\mu A/V$
G_{ds4}	31.640	nA/V
C_2	38.509	fF
f_0	179.665	Hz
GBW	1.029	MHz
f_p	11.536	MHz
f_z	23.073	MHz

The gain-bandwidth product from the specifications is repeated here

$GBW = 1.000$ MHz (from spec).

The estimate value assuming that all the non-dominant poles are much higher than the GBW is given by

$GBW_{est} = 1.029$ MHz (estimation).

The GBW accounting for the effect of the additional non-dominant poles is given by

$GBW_{the} = 1.026$ MHz (theory).

We see that there is only a small difference between GBW_{est} and GBW_{the}, which confirms that the non-dominant poles are sufficiently far from GBW as stated in Table 4.1.

We can now plot the gain response Using the variables given in Table 4.1. It is shown in Figure 4.1.

From Figure 4.1, we see that the GBW is right on target and the DC gain is much larger than the specification.

We can now have a look at the input-referred noise PSD.

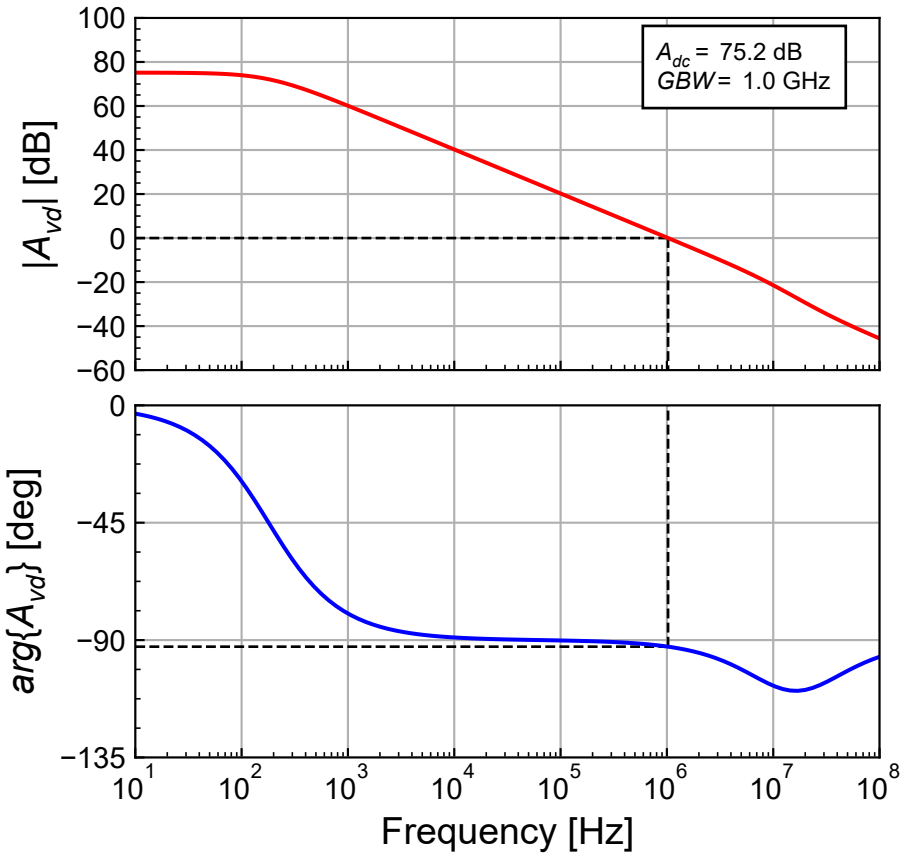

Figure 4.1: OTA theoretical transfer function.

4.2 Input-referred noise

We can compute all the parameters needed for the calculation of the OTA thermal noise excess factor and its input-referred thermal noise PSD and resistance. They are given in Table 4.2.

Table 4.2: OTA thermal noise parameters.

Symbol	Theoretical Value	Unit
G_{m1}	6.586	$\mu A/V$
G_{m2}	2.791	$\mu A/V$
G_{m1}/G_{m2}	2.360	-
γ_{n1}	0.644	-
γ_{n2}	0.747	-
η_{th}	0.491	-
γ_{ota}	1.922	-
R_{nt}	291.806	$k\Omega$
$\sqrt{S_{ninth}}$	69.548	$nV/\sqrt{Hz}$
$10 \cdot \log(S_{ninth})$	-143.154	$dBv/\sqrt{Hz}$

From Table 4.2, we see that the OTA thermal noise excess factor $\gamma_{ota} = 1.922$ is only slightly larger than that of the differential pair $2\,\gamma_{n1} = 1.289$. This is due to the low value of $\eta_{th} = 0.491$ indicating that the current mirror M_{2a}-M_{2b} is contributing about half the contribution of the differential pair M_{1a}-M_{1b}.

We can now compute all the parameters needed for the calculation of the input-referred flicker noise and the corner frequency. They are given in Table 4.3.

Table 4.3: OTA flicker noise parameters.

Symbol	Theoretical Value	Unit	Comment
$(G_{m1}/G_{m2})^2$	5.568	-	
ρ_p/ρ_n	5.435	-	
$\frac{W_1 \cdot L_1}{W_2 \cdot L_2}$	1.161	-	
η_{fl}	1.133	-	
$\sqrt{S_{ninfl}(1\,Hz)}$	15.549	$\mu V/\sqrt{Hz}$	
$10 \cdot \log(S_{ninfl}(1\,Hz))$	-96.166	$dBv/\sqrt{Hz}$	
$(1+\eta_{fl})/(1+\eta_{th})$	1.430	-	
f_k	36.149	kHz	Differential pair only
f_k	51.693	kHz	

From Table 4.3, we see that $\eta_{fl} = 1.133$, which means that the contribution of the current mirror M_{2a}-M_{2b} to the input-referred flicker noise is about the same as the differential pair M_{1a}-M_{1b} despite the flicker of pMOS transistor is higher by a factor $\rho_p/\rho_n = 5.435$ for the same gate area. We also see that the corner frequency is lower than the specification due to the fact that we have increased the length of M_{1a}-M_{1b} for achieving the DC gain.

We can plot the input-referred noise which is shown in Figure 4.2.

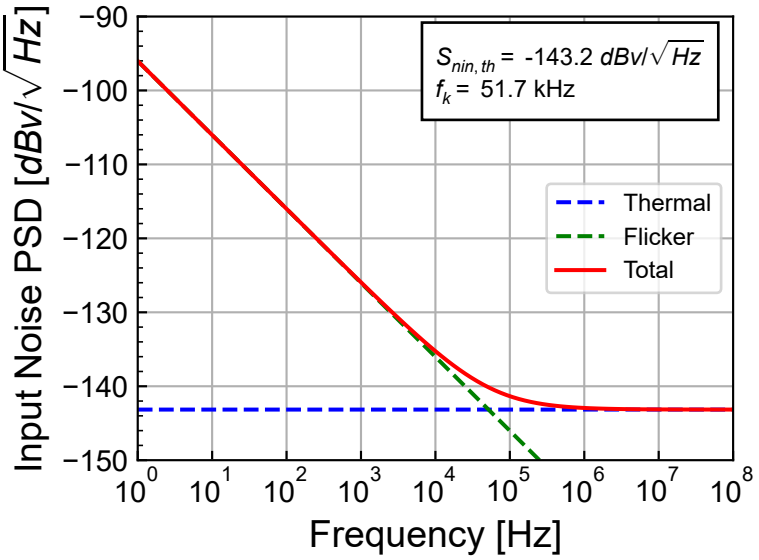

Figure 4.2: OTA theoretical input-referred noise PSD.

4.3 Input-referred offset

The variance of the input-referred offset voltage is given by (2.33), which is repeated below

$$\sigma^2_{V_{os}} = \sigma^2_{V_T} + \sigma^2_{\beta}, \tag{4.1}$$

where

$$\sigma^2_{V_T} = \sigma^2_{V_{T1}} \cdot (1 + \xi_{V_T}) \tag{4.2}$$

is the V_T-mismatch and

$$\sigma_\beta^2 = \left(\frac{I_b}{G_{m1}}\right)^2 \cdot \sigma_{\beta_1}^2 \cdot (1 + \xi_\beta) \tag{4.3}$$

is the β-mismatch with

$$\sigma_{V_{T1}} = \frac{A_{V_{Tn}}^2}{W_1\, L_1} \tag{4.4}$$

and

$$\sigma_{\beta_1}^2 = \frac{A_{\beta_n}^2}{W_1\, L_1}. \tag{4.5}$$

ξ_{V_T} represents the V_T-mismatch contribution to the input-referred offset of the current mirror relative to that of the differential pair. It is given by (2.40) which is repeated below

$$\xi_{V_T} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \cdot \left(\frac{A_{V_{Tp}}}{A_{V_{Tp}}}\right)^2 \cdot \frac{W_1\, L_1}{W_2\, L_2}. \tag{4.6}$$

ξ_β represents the β-mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair. It is given by (2.41) which is repeated below

$$\xi_\beta = \left(\frac{A_{\beta_p}}{A_{\beta_n}}\right)^2 \cdot \frac{W_1\, L_1}{W_2\, L_2}. \tag{4.7}$$

The parameter for calculating the standard deviation of the input-referred offset voltage are given in Table 4.4.

Table 4.4: OTA input-referred offset parameters.

Symbol	Theoretical Value	Unit
σ_{VT1}	3.198	mV
σ_{VT2}	3.494	mV
$\sigma_{\beta 1}$	0.640	%
$\sigma_{\beta 2}$	0.699	%
ξ_{VT}	0.214	-
ξ_β	1.193	-
$\sigma_{V_T}^2$	12.422	mV^2
σ_{V_T}	3.524	mV
σ_β^2	0.129	mV^2
σ_β	0.360	mV
σ_{Vos}	3.543	mV

From Table 4.4, we see that the β-mismatch is negligible and that the input-referred offset voltage is dominated by the contribution of the V_T-mismatch from the differential pair.

4.4 Current and power consumption

The total current consumption, ignoring the current drawn by M_{5a}, is $I_{tot} = 2I_b = 0.5\ \mu A$. Assuming the input differential pair M_{1a}-M_{1b} is biased in deep weak inversion, the minimum bias current is directly related to the gain-bandwidth product GBW according to

$I_{b,min} \cong nU_T \cdot C_L \cdot \omega_u = nU_T \cdot C_L \cdot 2\pi\, GBW = 198\ nA.$

The minimum total current consumption can then be estimated as $I_{tot,min} \cong 2I_{b,min} = 397\ nA$. The actual current consumption accounting for some margin taken on the GBW is therefore 26% higher than the minimum.

> **Note**
>
> Note that the telescopic OTA is the differential OTA that has the minimum power consumption for similar gain-bandwidth product, DC gain and phase margin specifications. Of course it has the smallest input and output voltage swings.

The above design will now be checked against simulations.

5 Simulation results from ngspice

The theoretical results can be validated with the results obtained from simulations performed with ngspice. In order to run the simulations you need to have ngspice correctly installed. Please refer to the installation instructions.

> **Note**
>
> The simulations are performed with the PSP 103.6 compact model [7] using the parameters from the IHP open source PDK [5]. For ngspice, we use the Verilog-A implementation given in the IHP package [5] and compiled the OSDI file with OpenVAF [10] to run with ngspice [11]. In addition to the PSP user manual [7] a documentation of PSP and other MOSFET compact models and their parameter extraction can be found in [12].

5.1 Operating point

We first write the parameter file for this specific design for running the ngspice simulations. Before running the AC and NOISE simulations, we first need to check the quiescent voltages and currents and the operating points of all transistors by running a .OP simulation.

Table 5.1: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.200
vb1	0.700
vb2	0.600
inp	0.450
inn	0.450
out	0.707
ic	0.450
id	0.000
1	0.207
2	0.708
3	0.500
4	0.500
5	0.948
6	0.948
7	0.368
8	0.208

We can extract the OTA quiescent node voltages from the ngspice .ic file. They are presented in Table 5.1. We see that the simulated quiescent output voltage $V_{outq} = 707\ mV$ is close to the desired value set at $V_{outq} = 700\ mV$. This means that the OTA is biased in the high gain region and we actually don't need to extract any offset voltage at this point and can proceed with the simulation of the large-signal characteristic.

The operating point information for all transistors are extracted from the ngspice .op file. The data is split into the large-signal operating informations in Table 5.2, the small-signal operating point informations in Table 5.3 and the noise operating point informations in Table 5.4.

Table 5.2: Operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[nA]$	V_{GS} $[mV]$	V_{DS} $[mV]$	V_{SB} $[mV]$	$V_{GS} - V_T$ $[mV]$	V_{Dsat} $[mV]$
M1a	249.830	243	294	207	-23	112
M1b	249.826	243	294	207	-23	112
M2a	249.830	492	252	-0	151	173
M2b	249.830	492	252	-0	151	173
M3a	249.829	200	207	500	-44	109
M3b	249.826	200	207	500	-44	109
M4a	249.826	348	241	252	-42	105
M4b	249.826	348	241	252	-42	105
M5a	499.999	368	208	0	149	171
M5b	499.656	368	207	0	149	171

Table 5.3: PSP small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[nA/V]$
M1a	6.691	0.821	265.957
M1b	6.691	0.821	265.957
M2a	2.744	0.510	30.170
M2b	2.744	0.510	30.170
M3a	7.553	0.771	276.868
M3b	7.553	0.771	276.951
M4a	7.299	1.228	19.905
M4b	7.299	1.228	19.860
M5a	5.929	0.800	235.806
M5b	5.925	0.800	238.023

Table 5.4: PSP noise operating point information extracted from ngspice .op file for each transistor.

Transistor	$S_{ID,th}$ $[A^2/Hz]$	$S_{ID,fl}$ at 1Hz $[A^2/Hz]$
M1a	7.113e-26	3.178e-21
M1b	7.113e-26	3.178e-21
M2a	6.463e-26	2.594e-21
M2b	6.463e-26	2.594e-21
M3a	7.498e-26	4.464e-22
M3b	7.498e-26	4.466e-22
M4a	1.417e-25	1.639e-21
M4b	1.417e-25	1.639e-21
M5a	7.230e-26	5.128e-20
M5b	7.229e-26	5.118e-20

Table 5.5: sEKV parameters calculated from the values extracted from the simulation to compare with Table 3.7.

Transistor	W_{eff} $[\mu m]$	L_{eff} $[\mu m]$	W_{eff}/L_{eff}	I_{spec} $[\mu A]$	IC
M1a	1.900	1.241	1.531	1.084	0.230
M1b	1.900	1.241	1.531	1.084	0.230
M2a	0.610	3.245	0.188	0.046	5.434
M2b	0.610	3.245	0.188	0.046	5.434
M3a	9.200	2.541	3.620	2.564	0.097
M3b	9.200	2.541	3.620	2.564	0.097
M4a	13.260	1.344	9.867	2.413	0.104
M4b	13.260	1.344	9.867	2.413	0.104
M5a	0.170	0.881	0.193	0.137	3.659
M5b	0.170	0.881	0.193	0.137	3.656

Table 5.6: sEKV small-signal parameters calculated from the values extracted from the simulation to compare with Table 3.8.

Transistor	G_{spec} $[\mu A/V]$	n	G_m $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_{ds} $[nA/V]$
M1a	41.921	1.123	6.691	7.513	265.957
M1b	41.921	1.123	6.691	7.513	265.957
M2a	1.777	1.186	2.744	3.254	30.170
M2b	1.777	1.186	2.744	3.254	30.170
M3a	99.143	1.102	7.553	8.325	276.868
M3b	99.143	1.102	7.553	8.325	276.951
M4a	93.310	1.168	7.299	8.528	19.905
M4b	93.310	1.168	7.299	8.528	19.860
M5a	5.283	1.135	5.929	6.730	235.806
M5b	5.283	1.135	5.925	6.725	238.023

Table 5.7: sEKV noise parameters calculated from the values extracted from the simulation to compare with Table 4.2.

Transistor	$\sqrt{S_{nin,th}}$ $[nV/\sqrt{Hz}]$	$R_{nin,th}$ $[k\Omega]$	γ_n $[-]$	$\sqrt{S_{nin,fl}}$ $[nV/\sqrt{Hz}]$
M1a	39.858	95.840	0.641	8425.328
M1b	39.858	95.841	0.641	8425.375
M2a	92.652	517.879	1.421	18561.435
M2b	92.652	517.879	1.421	18561.434
M3a	36.252	79.283	0.599	2797.184
M3b	36.252	79.284	0.599	2797.802
M4a	51.569	160.437	1.171	5546.874
M4b	51.568	160.431	1.171	5546.716
M5a	45.349	124.064	0.736	38190.572
M5b	45.380	124.237	0.736	38185.625

Table 5.8: Bias voltages and operating regions extracted from ngspice for each transistor.

Trans.	Type	Funct.	V_G $[V]$	V_S $[V]$	V_D $[V]$	V_{DS} $[mV]$	V_{DSsat} $[mV]$	Reg.	Sat.
M1a	n	DP	0.450	0.207	0.500	294	112	MI	sat

Table 5.8: Bias voltages and operating regions extracted from ngspice for each transistor.

Trans.	Type	Funct.	V_G [V]	V_S [V]	V_D [V]	V_{DS} [mV]	V_{DSsat} [mV]	Reg.	Sat.
M1b	n	DP	0.450	0.207	0.500	294	112	MI	sat
M2a	p	CM	0.492	0.000	0.252	252	173	MI	sat
M2b	p	CM	0.492	0.000	0.252	252	173	MI	sat
M3a	n	CA	0.700	0.500	0.708	207	109	WI	sat
M3b	n	CA	0.700	0.500	0.707	207	109	WI	sat
M4a	p	CA	0.600	0.252	0.492	241	105	MI	sat
M4b	p	CA	0.600	0.252	0.493	241	105	MI	sat
M5a	n	CM	0.368	0.000	0.208	208	171	MI	sat
M5b	n	CM	0.368	0.000	0.207	207	171	MI	sat

From Table 5.1, we see that all transistors have a V_{DS} voltage between 200 mV and 250 mV and are therefore biased in saturation. Additionnally we see that all the saturation voltages are summing up to 671 mV leaving an output voltage swing equal to $V_{out,swing} = 0.529\ V$.

The data extracted from the operating point simulation can be translated into sEKV parameters. Table 5.5 presents the effective width and length, the specific current and the resulting inversion coefficient which can be compared to the values resulting from the design given in Table 3.7. We observe that the values are close.

Table 5.6 presents the sEKV parameters including the specific conductance G_{spec}, slope factor n, gate transconductance G_m, source transconductance G_{ms} and output conductance G_{ds}. They can be compared to the results of the design presented in Table 3.8. Again, we see that the simulated values of the transconductances are close to the theoretical estimation. However, the simulated values of the output conductances are much larger thamn the estimated values, explaining why the estimated DC gain is much larger than the simulated value.

Table 5.7 presents the sEKV noise parameters. We can observe that the thermal noise excess factors of pMOS transistors are larger than the estimated values shown in Table 4.2.

Finally we can check whether all transistors are biased in saturation. From Table 5.8, we see that all transistors are biased in saturation. The operating points look fine. We can now proceed with the simulation of the open-loop large-signal transfer characteristic.

5.2 Large-signal differential transfer characteristic

We now simulate the DC differential transfer characteristic. The simulation of the large-signal input-output characteristic is presented in Figure 5.1.

We can now zoom into the high gain region in order to extract the offset voltage that is needed to bring the output voltage back to $V_{outq} = 0.700\ V$. The simulation results are presented in Figure 5.2.

We can now save the extracted offset voltage V_{os} = -9.163 μV that is required to bring the output voltage to $V_{outq} = 0.700\ V$ and that will be used for the following .AC and .NOISE simulations.

5.3 Open-loop gain

After having checked the operating point information and making sure that the OTA output is not saturated by extracting the required offset voltage for bringing the output operating point to the desired value $V_{outq} = 0.700\ V$, we can now perform the AC simulation.

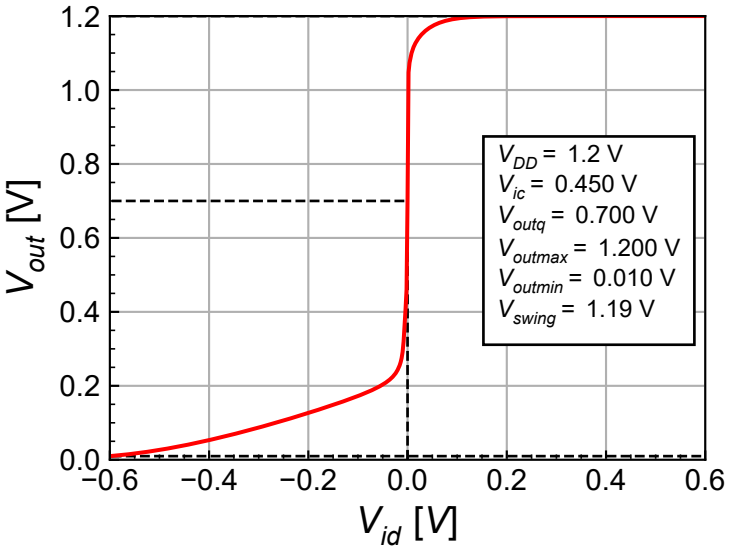

Figure 5.1: Simulated large-signal input-output characteristic.

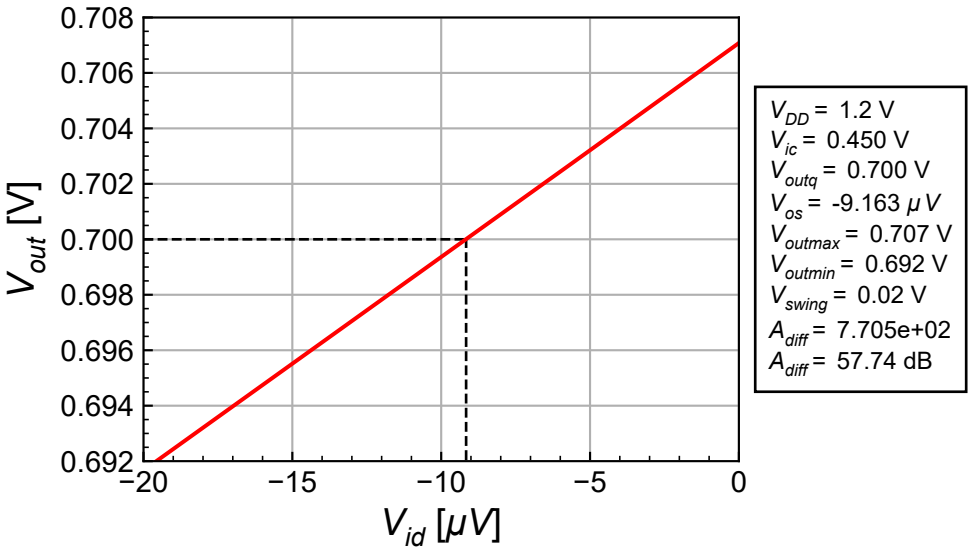

Figure 5.2: Zoom of the simulated large-signal input-output characteristic in the gain region.

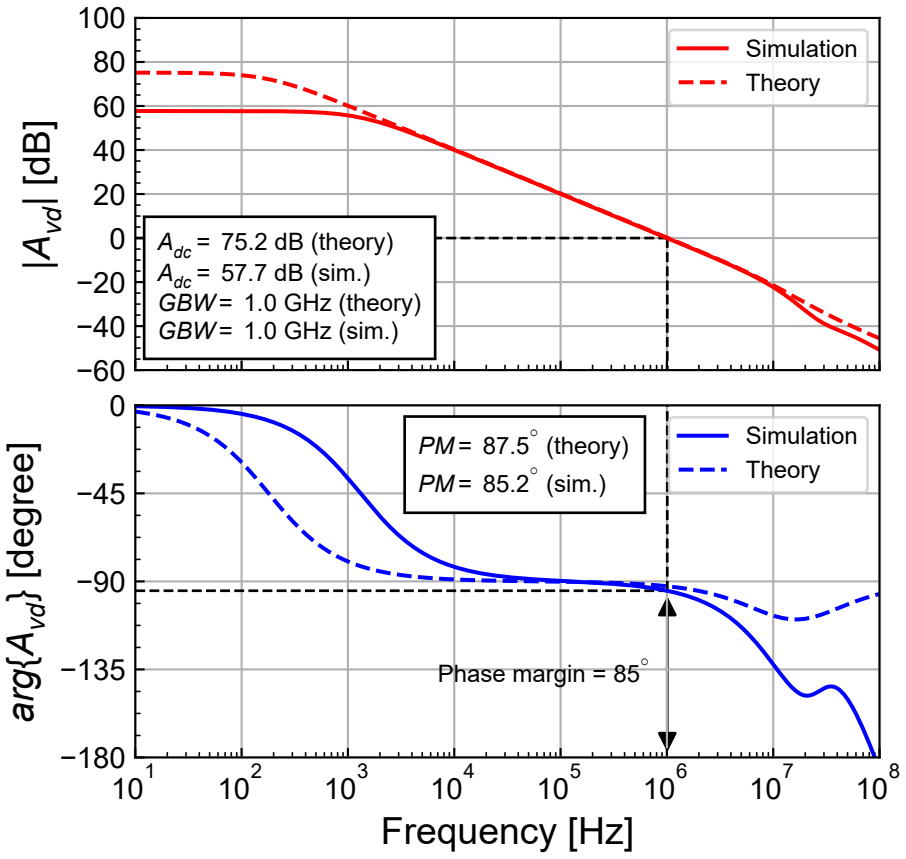

Figure 5.3: Simulated gain response compared to theoretical estimation.

From Figure 5.3, we see that the GBW is right on target, but the DC gain is way lower than the estimated DC gain and slihtly lower than the specifications. It is actually very hard to achieve a high DC gain for the telescopic OTA with this technology, despite the cascode stages and despite the longer transistor length we have chosen for the nMOS transistors. This is obviously due to the poor output conductance of the nMOS transistors and the low voltage constraint.

5.4 Input-referred noise

The simulated input-referred noise PSD is presented in Figure 5.4 and compared to the theoretical estimation.

From Figure 5.4, we see that the simulated input-referred noise PSD is very close to the theoretical prediction. The simulated flicker noise is exactly equal to the theoretical estimation, while the simulated white noise is slightly higher. We can have a closer look at the contributions of the various transistors to the input-referred white noise PSD.

The contributions of M_{1a}-M_{1b}, M_{2a}-M_{2b}, M_{3a}-M_{3b} and M_{4a}-M_{4b} to the input-referred white noise PSD are detailed in Figure 5.5 and compared to the theoretical white noise. We can observe that the contributions of the differential pair M_{1a}-M_{1b} and of the current mirror M_{2a}-M_{2b} are about equal. As expected, the contributions of the cascode transistors is more than 30 dB lower and can therefore be neglected. The total simulated white noise is slightly higher than the theoretical estimation, which is acceptable. This results in an OTA thermal noise excess factor $\gamma_{n,ota} = 2.516$ that is slightly larger than the predicted value $\gamma_{n,ota} = 1.922$.

Figure 5.6 presents the breakdown of the contributions of the various transistors to the input-referred flicker noise. We see that M_{2a}-M_{2b} contribute about the same than M_{1a}-M_{1b} and that the contributions

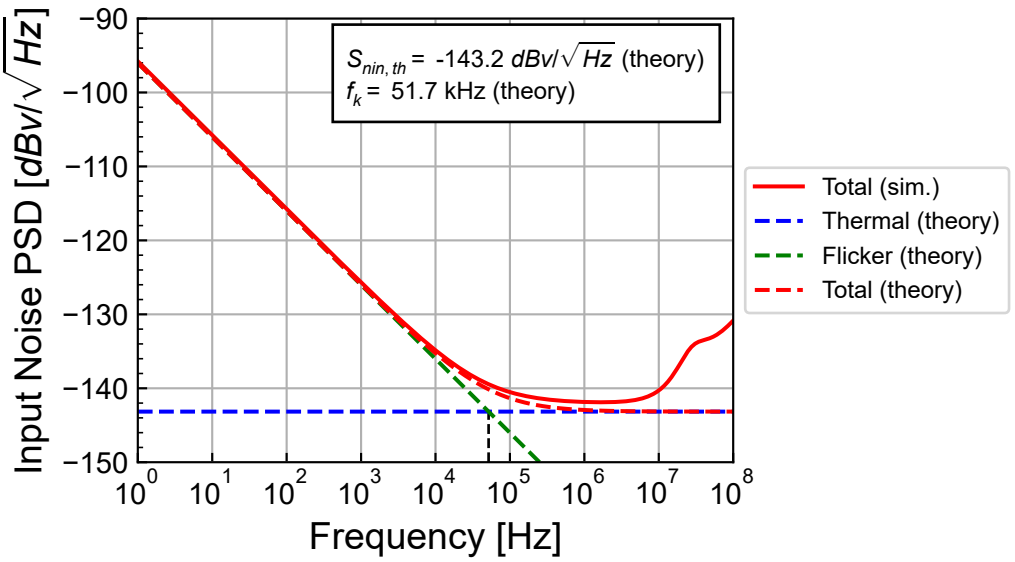

Figure 5.4: Simulated input-referred noise PSD compared to theoretical estimation.

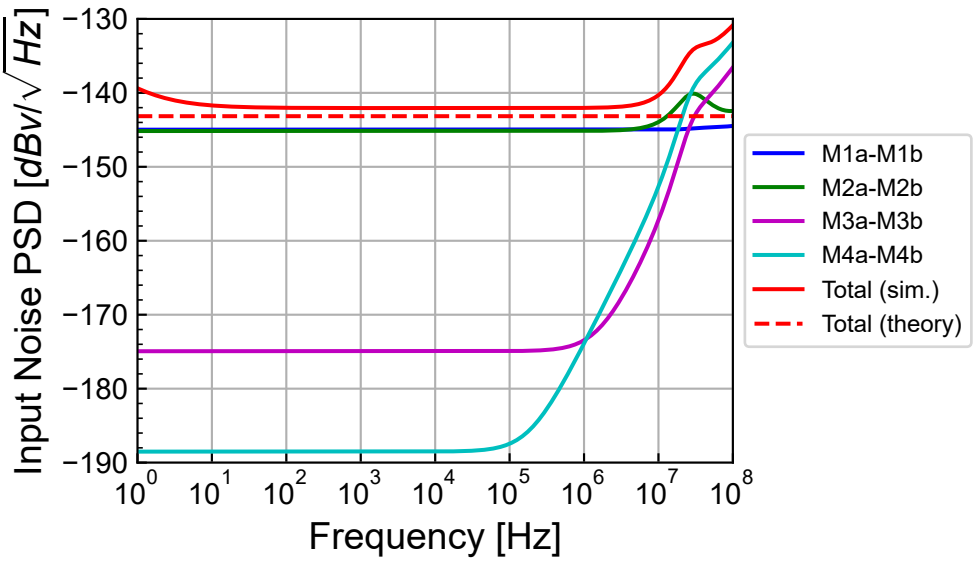

Figure 5.5: Breakdown of the contributions to the simulated input-referred white noise PSD.

of the cascode transistors M_{3a}-M_{3b} and M_{4a}-M_{4b} are negligible.

The breakdown of the contributions of the various transistors to the total input-referred noise is presented in Figure 5.6. We can observe that the simulation is close to the theoretical estimation.

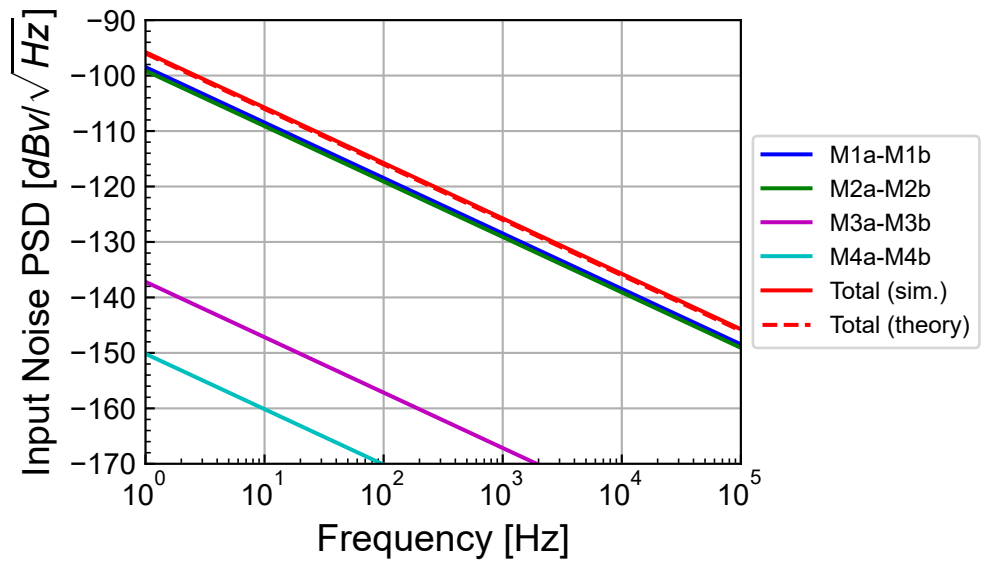

Figure 5.6: Breakdown of the contributions to the simulated input-referred flicker noise PSD.

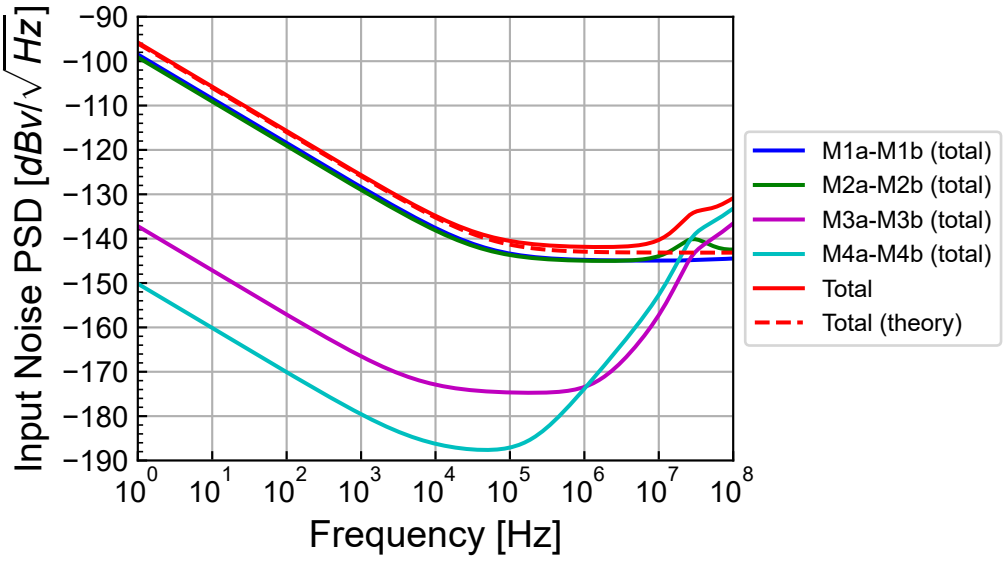

Figure 5.7: Breakdown of the contributions to the simulated input-referred noise PSD.

5.5 Input common-mode voltage range

We can check the input common-mode voltage range by connecting the OTA as a voltage follower and sweeping the positive input. As shown in Figure 5.8, the output follows the input voltage up to $0.8\,V$. So the input common-mode voltage range is about $0.8\,V$.

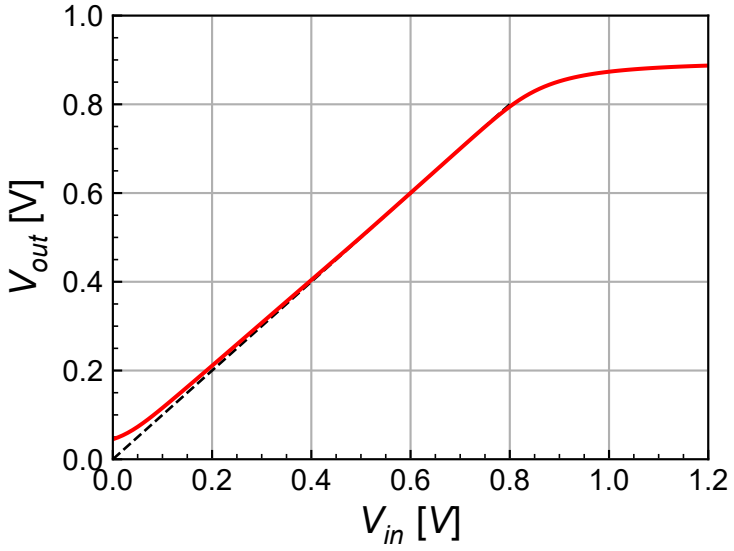

Figure 5.8: Simulated input common-mode voltage range.

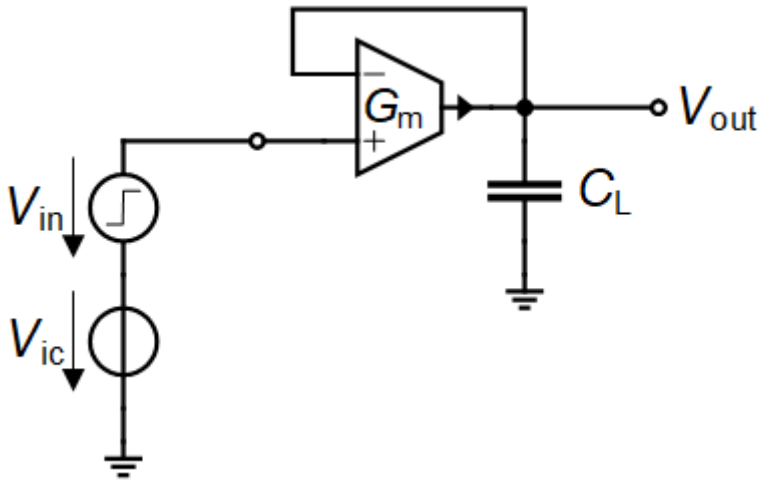

Figure 5.9: Schematic of the OTA connected as a voltage follower.

5.6 Step-response

In this section we will check the step response of the OTA operating as a voltage follower as shown in Figure 5.9 with its output connected to the negative input and with the same load capacitance $C_L = 1$ pF.

5.6.1 Small-step

According to the input common-mode voltage range established above, we will set the input common-mode voltage to $V_{ic} = 0.600$ V to make sure that the OTA is in the high gain region. We start by imposing a small step $\Delta V_{in} = 10$ mV on top of a common mode voltage $V_{ic} = 0.600$ V. The simulation results are shown in Figure 5.10 where $\Delta V_{in}(t) \triangleq V_{in+}(t) - V_{ic}$ and $\Delta V_{out}(t) \triangleq V_{out}(t) - V_{outq}$ with $V_{outq} \cong V_{ic}$ is the quiescent output voltage. ΔV_{in} and ΔV_{out} are compared to the response of a single pole circuit having a cut-off frequency equal to the GBW. From Figure 5.10, we see that the simulation result is very close to the first-order response.

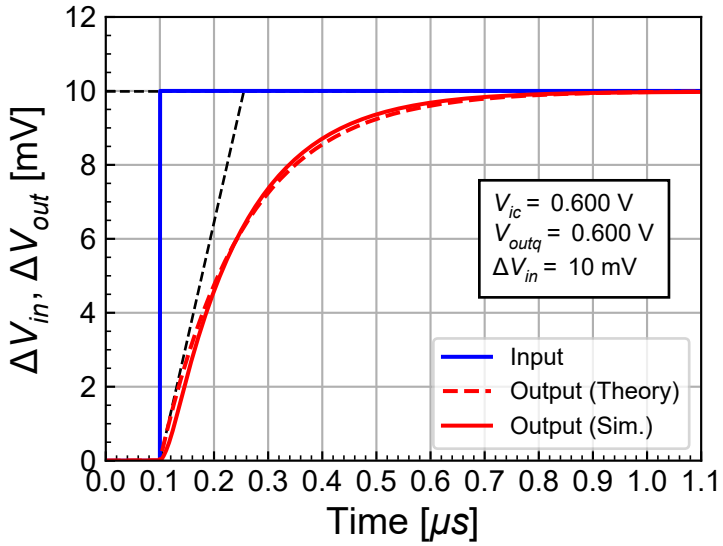

Figure 5.10: Step response of the OTA connected as a voltage follower for a small input step.

5.6.2 Large step

Since we now impose a larger step $\Delta V_{in} = 300$ mV, we need to lower the input common-mode voltage to $V_{ic} = 400$ mV, to make sure that after the step the OTA remains in the high gain region and correctly settles to the right voltage. The simulation results are shown in Figure 5.11 where $\Delta V_{in}(t) \triangleq V_{in+}(t) - V_{ic}$ and $\Delta V_{out}(t) \triangleq V_{out}(t) - V_{outq}$ with $V_{outq} \cong V_{ic}$ is the quiescent output voltage. ΔV_{in} and ΔV_{out} are compared to the response of a single pole circuit having a cut-off frequency equal to the GBW. We now observe the effect of slew-rate which increases the settling time.

5.7 Power consumption

The total current consumption, ignoring the current drawn by M_{5a}, is $I_{tot} = 2I_b = 0.5$ μA and the total power consumption is then $P = 0.6$ μW. Assuming the input differential pair M_{1a}-M_{1b} is biased in deep weak inversion, the minimum bias current is directly related to the gain-bandwidth product GBW according to

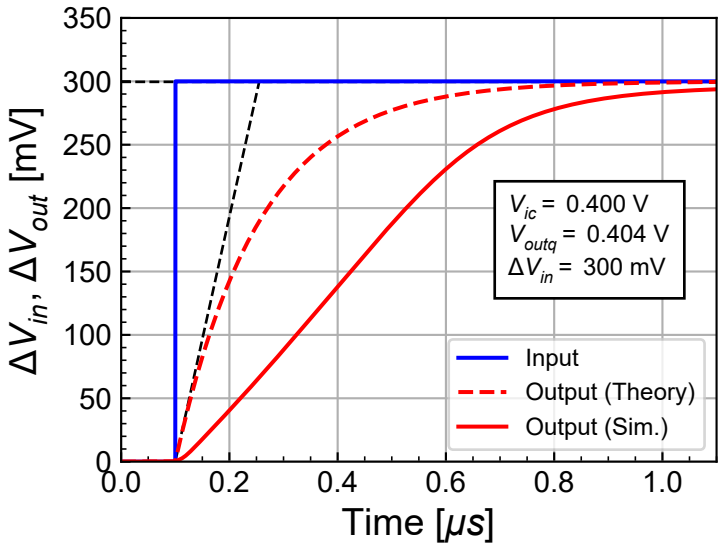

Figure 5.11: Step response of the OTA connected as a voltage follower for a large input step highlighting the slew-rate effect.

$I_{b,min} \cong nU_T \cdot C_L \cdot \omega_u = nU_T \cdot C_L \cdot 2\pi\, GBW = 198\ nA.$

The minimum total current consumption can then be estimated as $I_{tot,min} \cong 2I_{b,min} = 397\ nA$. The actual current consumption accounting for some margin taken on the GBW is therefore 26% higher than the absolute minimum. Note that this increased current consumption is necessary to fight against the paraistic capciatnces at the OTA output.

> **Note**
>
> Note that the telescopic OTA is the differential OTA that has the minimum power consumption for similar gain-bandwidth product, DC gain and phase margin specifications. Of course it has the smallest input and output voltage swings and the DC gain equivalent to the two-stage OTA is hard to achieve.

6 Conclusion

This notebook presented the detailed analysis, design and verification by simulation of the telescopic OTA [1]. The analysis allowed to derive the design equations to achieve the target specifications. The OTA has been designed for specifications on the gain-bandwidth product and DC gain in the IHP SG13G2 130nm BiCMOS technology [5] using the inversion coefficient approach with the sEKV model and parameters [2] [3] [4]. The design has been validated by simulations with the ngspice simulator [6] using the PSP compact model [7] and the parameters provided by the open source IHP [5].

The simulations have shown that the target gain-bandwidth product GBW was achieved. However the DC gain was not, despite the increase of the nMOS transistor length in the design phase. The estimated DC gain was $A_{dc} \cong 75.2\ dB$, way above the simulated value of $A_{dc} \cong 57.7\ dB$ which is slightly lower than the $A_{dc} = 60.0\ dB$ specification. The noise simulations on the other hand match the theoretical values very well prooving the negligible contributions of the cascode transistors and showing that the corner frequency was slightly below the specification.

The telescopic OTA is the most power efficient differential OTA among those we have studied. This efficiency comes at the cost of a reduced input and output voltage swing and lower DC gain.

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