sEKV Parameter Extraction for the IHP 130nm Process

pMOS

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Table of contents

1 Introduction

In this notebook we will extract the sEKV parameters for pMOS transistors of the IHP SG2 130nm CMOS process from IHP. The extraction is done with data generated by PSP for the typical-typical (t-t) case. The parameters are extracted first for a long and wide transistor, then for a medium transistor and finally for a short and wide transistor. In addition to the basic sEKV paramaters n, $I_{spec\square}$, V_{T0} and L_{sat}, we also extract the flicker noise parameters K_F and AF, the junction, overlap and fringing capacitances. All the parameters are saved into an Excel file.

2 Transistor geometry parameters

2.1 Effective length and width for current

Before we start the extraction we need to account for the geometry dependence. With PSP you can choose between geometry scaling rules or binning rules with parameter $SWGEO$. If $SWGEO = 1$, the scaling rules are chosen. This is the case in the IHP 130nm G2 PDK. The geometrical parameters are defined in Figure 2.1.

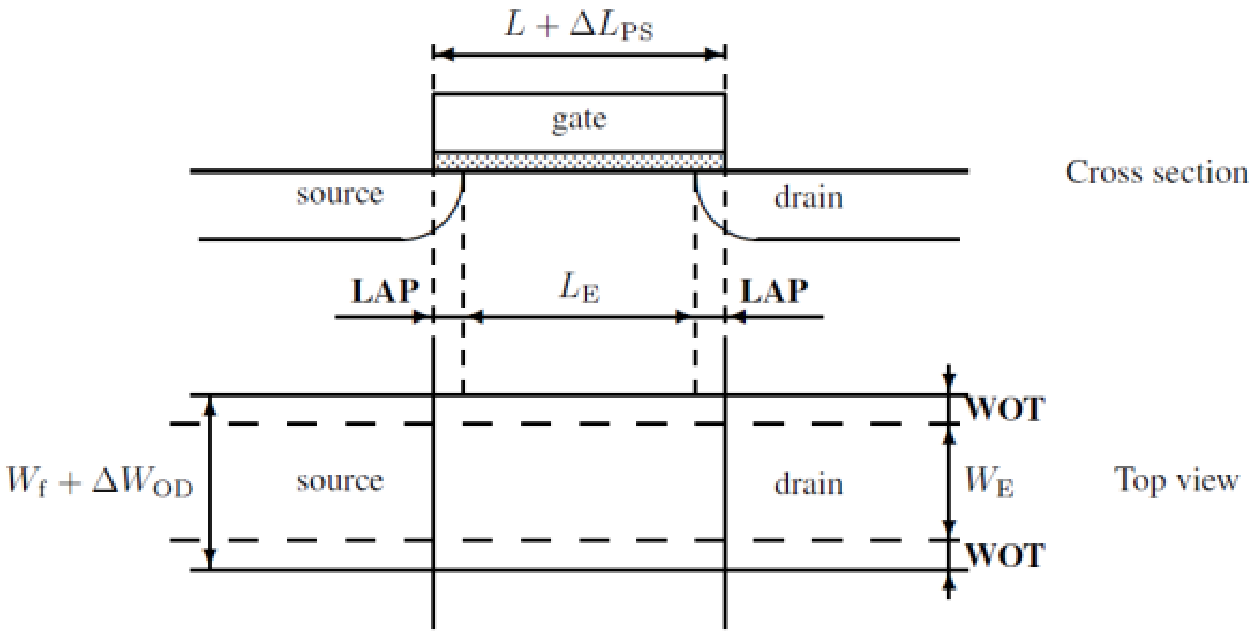


Figure 2.1: Definition of transistor geometrical parameters.

The effective length and width are defined as

$$L_{eff} = L - \Delta L, \tag{2.1}$$
$$W_{eff} = W_f - \Delta W, \tag{2.2}$$

where W_f is the width of one finger defined as

$$W_f = \frac{W}{NF}. \tag{2.3}$$

In our case we will assume that the number of fingers $NF = 1$ and hence that $W_f = W$.

ΔL and ΔW are given by

$$\Delta L = 2\,LAP - \Delta L_{PS}, \tag{2.4}$$
$$\Delta W = 2\,WOT - \Delta W_{OD}, \tag{2.5}$$

with

$$\Delta L_{PS} = LVARO \cdot \left(1 + LVARL \cdot \frac{L_{EN}}{L}\right) \cdot \left(1 + LVARW \cdot \frac{W_{EN}}{W_f}\right), \tag{2.6}$$
$$\Delta W_{OD} = WVARO \cdot \left(1 + WVARL \cdot \frac{L_{EN}}{L}\right) \cdot \left(1 + WVARW \cdot \frac{W_{EN}}{W_f}\right). \tag{2.7}$$

$L = 1.000\ \mu m$

$L_{eff} = 1.043\ \mu m$

$W = 1.000\ \mu m$

$W_{eff} = 0.970\ \mu m$

We can approximate the effective length and width by setting ΔL_{PS} and ΔW_{OD} to zero, like it is effectively the case for nMOS. In this case we can define and length and width corrections as

$DL = 51$ nm

$DW = 30$ nm

2.2 Effective length and width for capacitances

The effective length and width are slightly different for the calulation of the capacitances.

The effective length and width for the calculation of the intrinsic and overlap acacitances are defined as

$$L_{E,CV} = L - \Delta L_{CV}, \tag{2.8}$$
$$W_{E,CV} = W - \Delta W_{CV}, \tag{2.9}$$

where

$$\Delta L_{CV} = 2\,LAP - \Delta L_{PS} - DLQ, \tag{2.10}$$
$$\Delta W_{CV} = 2\,WOT - \Delta W_{OD} - DWQ. \tag{2.11}$$

As mentioned above, for the IHP 130nm for nMOS $\Delta L_{PS} = 0$ and $\Delta W_{OD} = 0$ so that

$$\Delta L_{CV} = 2\,LAP - DLQ, \tag{2.12}$$
$$\Delta W_{CV} = 2\,WOT - DWQ. \tag{2.13}$$

The effective length and width for the calculation of the fringing field capacitances are defined as

$$L_{G,CV} = L - \Delta L_{G,CV}, \tag{2.14}$$
$$W_{G,ov} = W - \Delta W_{G,CV}, \tag{2.15}$$

where

$$\Delta L_{G,CV} = -\Delta L_{PS} - DLQ, \tag{2.16}$$
$$\Delta W_{G,CV} = -\Delta W_{OD} - DWQ. \tag{2.17}$$

`Length and width correction for intrinsic and overlap capacitances:`

$L = 0.130\ \mu m$

$L_{CV} = 0.055\ \mu m$

$W = 1.000\ \mu m$

$W_{CV} = 0.985\ \mu m$

`Length and width correction for fringing capacitances:`

$L = 0.130\ \mu m$

$L_{CVG} = 0.105\ \mu m$

$W = 1.000\ \mu m$

$W_{CVG} = 1.015\ \mu m$

Similarly, we can approximate the effective length and width by setting ΔL_{PS} and ΔW_{OD} to zero, like it is effectively the case for nMOS. In this case we can define and length and width corrections for capacitance calculation as

`Length and width correction for intrinsic and overlap capacitances:`

ΔL_{CV} = 146 nm

ΔW_{CV} = 15 nm

`Length and width correction for fringing capacitances:`

$\Delta L_{G,CV}$ = 96 nm

$\Delta W_{G,CV}$ = -15 nm

The value of ΔL_{CV} and $\Delta L_{G,CV}$ seem to be very high!

Table 2.1: Length and width corrections.

	Length correction DL	Width correction DW	Comment
For current	5.051e-08	3.000e-08	extracted from PDK
For intrinsic and overlap capacitances	1.464e-07	1.500e-08	extracted from PDK

Table 2.1: Length and width corrections.

	Length correction DL	Width correction DW	Comment
For fringing-field capacitances	9.592e-08	-1.500e-08	extracted from PDK

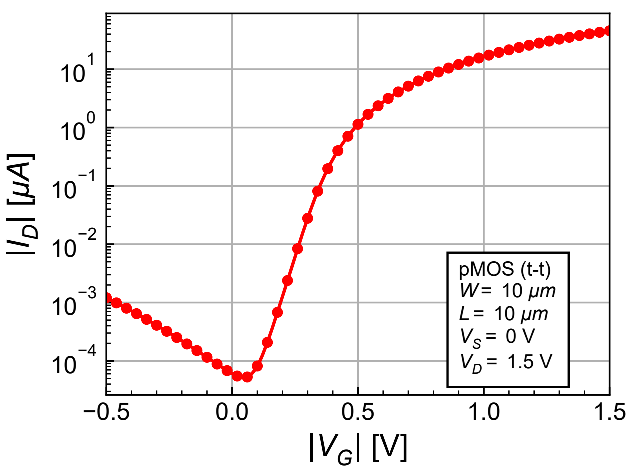
3 Long-channel parameters

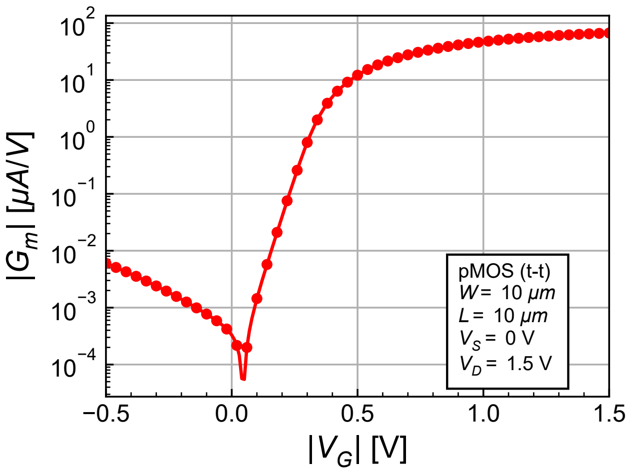
3.1 DC Transfer Characteristic Parameters

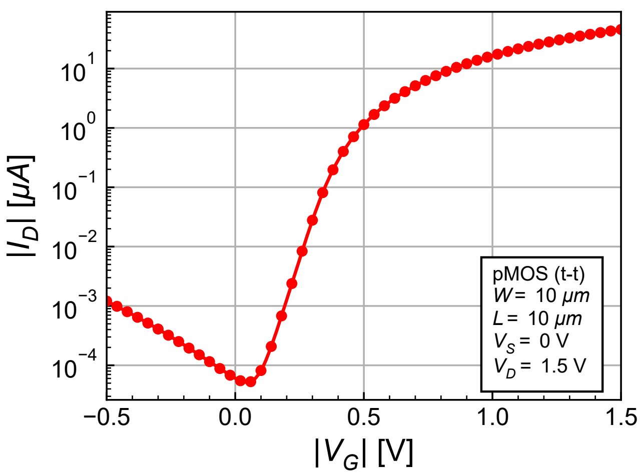
3.1.1 Generating the data

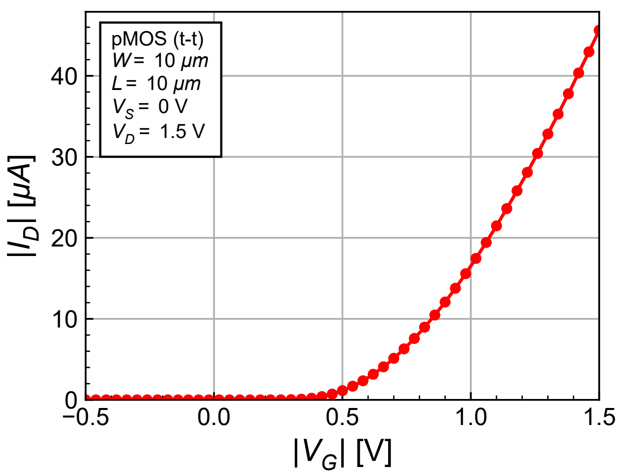
3.1.2 Importing and plotting the data

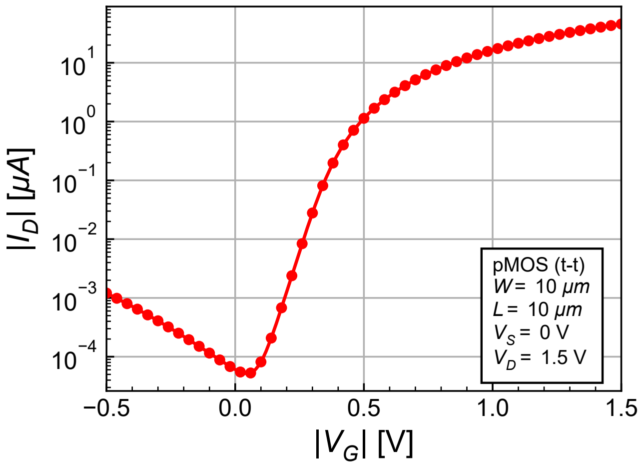
3.1.2.1 I_D and G_m versus V_G

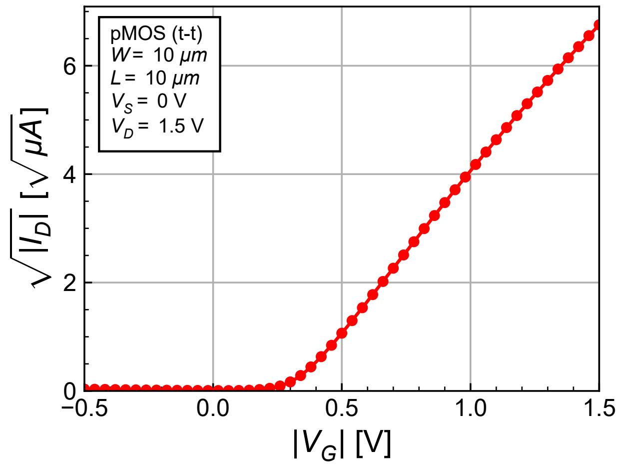




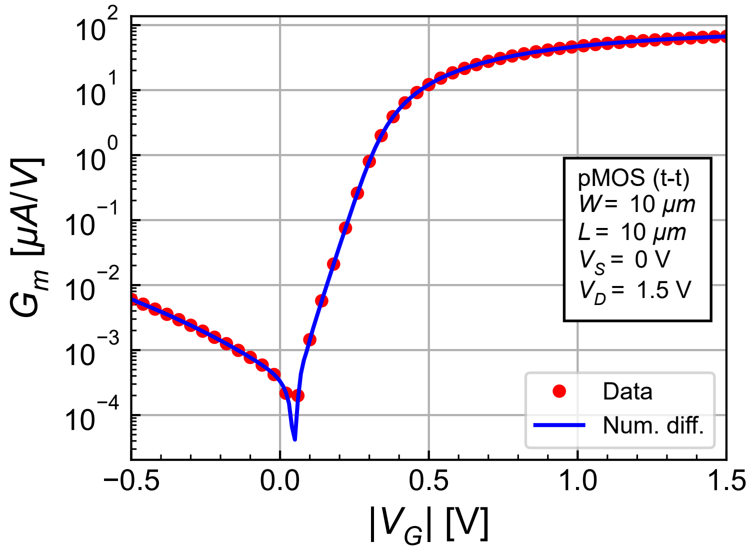






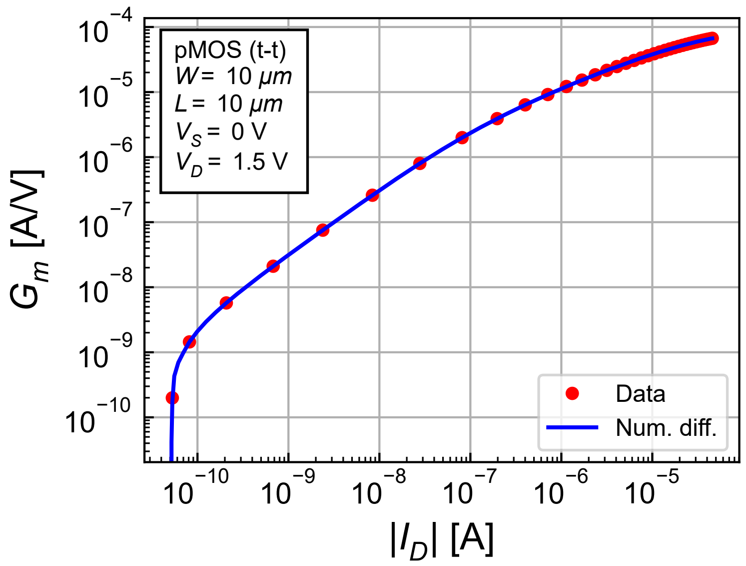


3.1.2.2 G_m-V_G

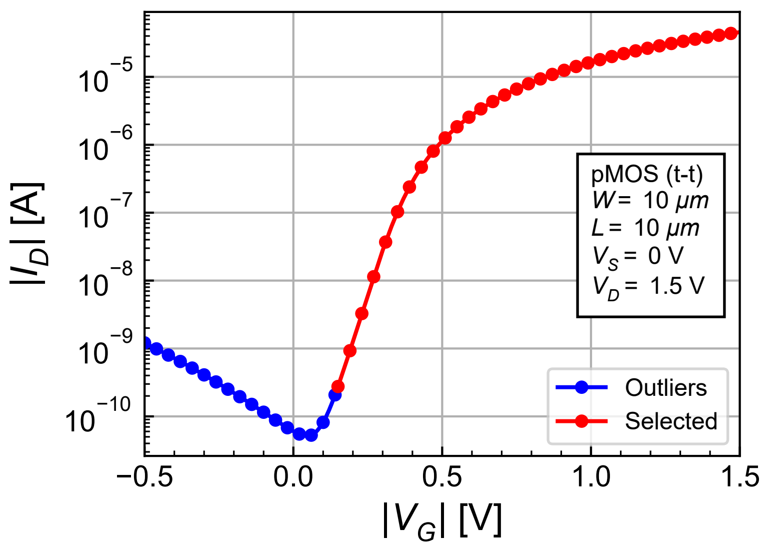


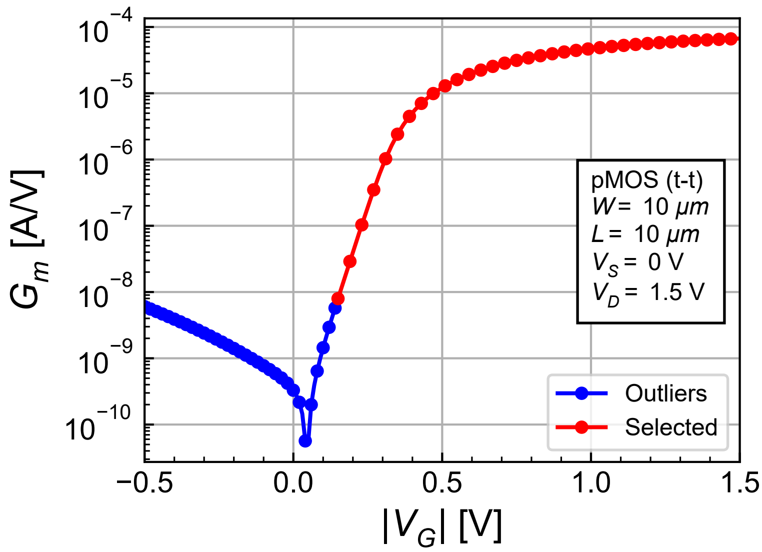
We see that the transconductance obtained by differentiating the large-signal I_D-V_G characteristic is equal to the transconductance extracted from the PSP model. We will keep the value extracted from the PSP model.

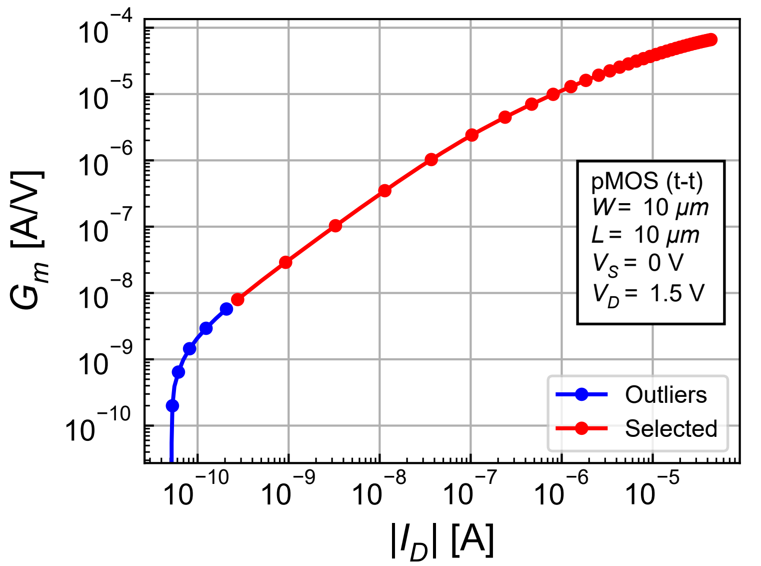
3.1.2.3 G_m-I_D



3.1.2.4 Filtering the outliers







3.1.3 Direct extraction with $\lambda_c = 0$

3.1.3.1 Slope factor n and I_{spec} extraction

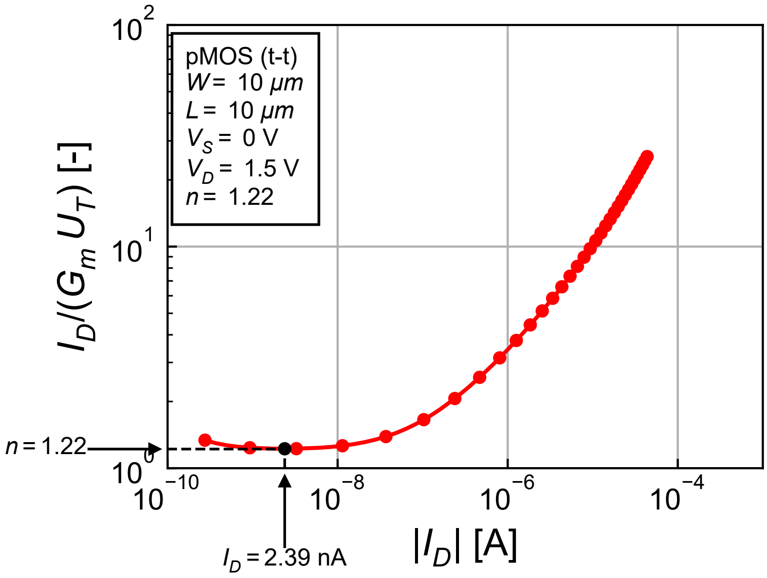
The gate transconductance in weak inversion and saturation is given by

$$G_m = \frac{I_D}{n\,U_T}. \tag{3.1}$$

So if we plot $I_D/(G_m\,U_T)$ we should see a plateau in weak inversion the value of which is equal to the slope factor n.

$n = 1.22$

$I_{D,ext} = 2.39\ nA$



On the other hand the normalized G_m/I_D function for a long-channel transistor in strong inversion and saturation is given by

$$\frac{G_m\, n\, U_T}{I_D} = \frac{1}{\sqrt{IC}} = \sqrt{\frac{I_{spec}}{I_D}}. \tag{3.2}$$

We can then plot $(G_m\, n\, U_T)^2/I_D$ which should find a maximum value equal to I_{spec}.

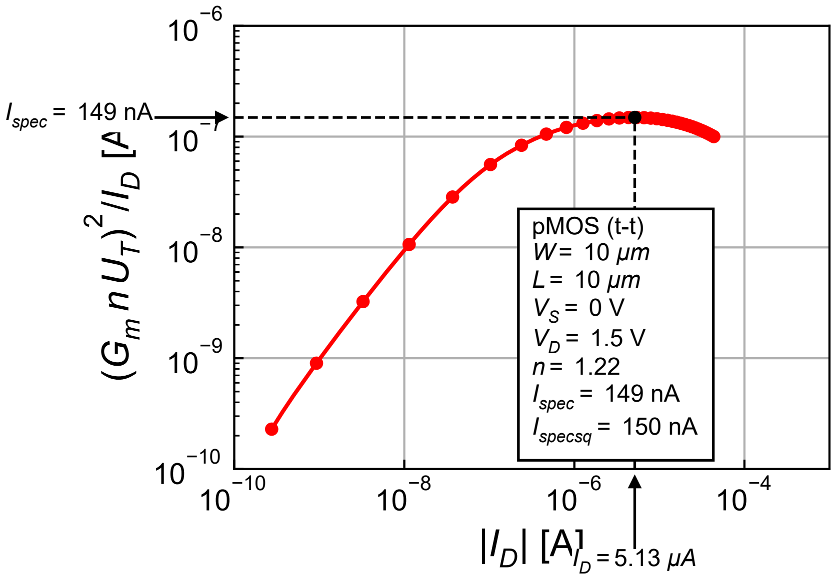
$W_{eff} = 9.970\ \mu m$

$L_{eff} = 10.046\ \mu m$

$I_{spec} = 149\ nA$

$I_{spec\square} = 150\ nA$

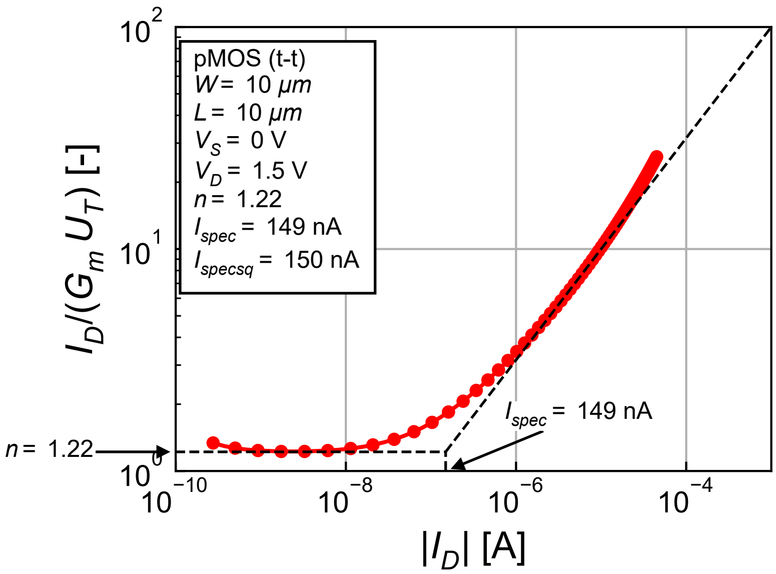
$I_{D,ext} = 5.128\ \mu A$



$n = 1.22$

$I_{spec} = 149\ nA$

$I_{spec\square} = 150\ nA$



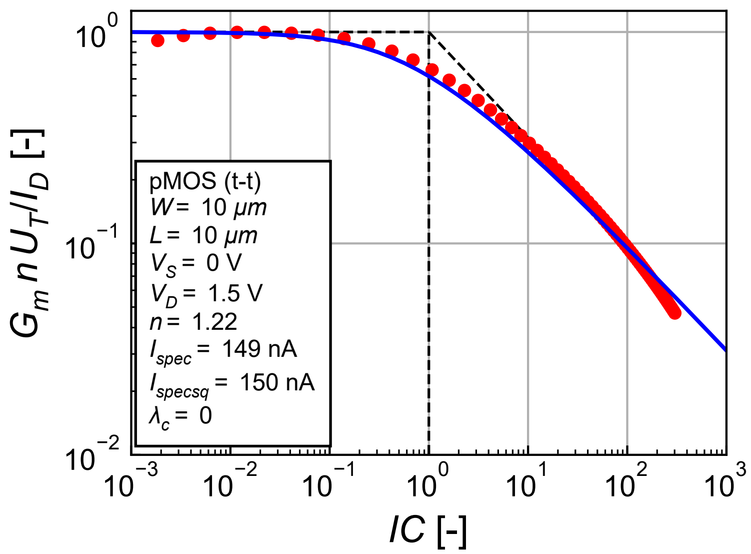
Having extracted n and I_{spec}, we can now plot the normalized G_m/I_D function.

$n = 1.22$

$I_{spec} = 149\ nA$

$I_{spec\square} = 150\ nA$

$\lambda_c = 0$



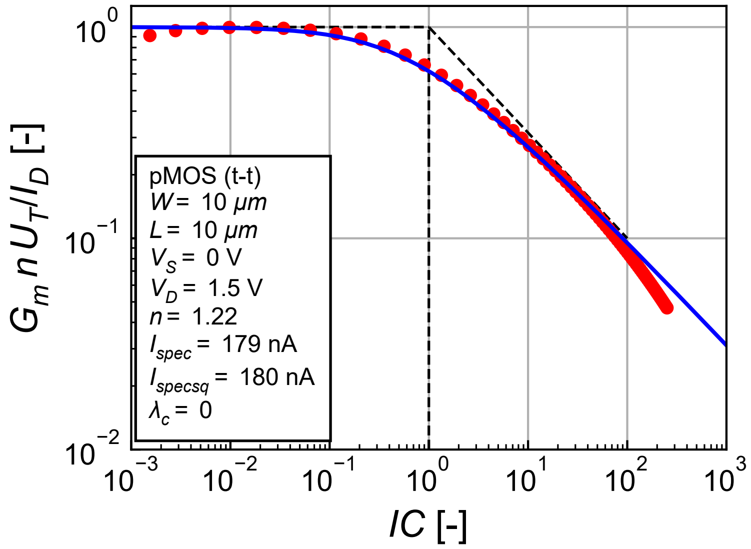
The fit is reasonable over the entire IC span. There is some discrepancy in the moderate inversion region which is due to the mobility reduction due to the vertical field appearing for $IC > 10^2$. The latter can be accounted for by using the λ_c parameter which is normally used for modeling the effect of velocity saturation in short-channel transistor but can also be used to correct the effect of mobility reduction due to the vertical field appearing in long-channel transistors. We will not do this here since we want to extract the long-channel parameters keeping $\lambda_c = 0$, but since we are mostly interested in the moderate inversion region, we can slightly increase I_{spec} to improve the fit in moderate inversion at the cost of a degradation in strong inversion.

$n = 1.22$

$I_{spec} = 179\ nA$

$I_{spec\square} = 180\ nA$

$\lambda_c = 0$



The fit is now much better in moderate inversion but less in strong inversion. This is due to mobility reduction due to the vertical field an effect that is not accounted for in the model. However, we will keep the new values.

3.1.3.2 Threshold voltage extraction

We can extract the threshold voltage in weak inversion (assuming $V_S = 0$) from the normalized current (inversion coefficient) given by

$$IC = e^{\frac{V_G - V_{T0}}{nU_T}}. \tag{3.3}$$

We can now plot

$$V_{T0} = V_G - nU_T \ln(IC) \tag{3.4}$$

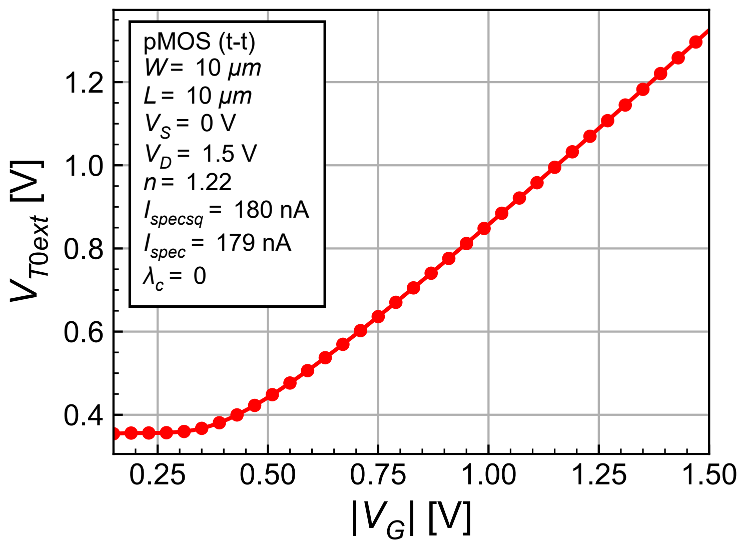
to extract the threshold voltage.

$n = 1.22$

$I_{spec} = 179\ nA$

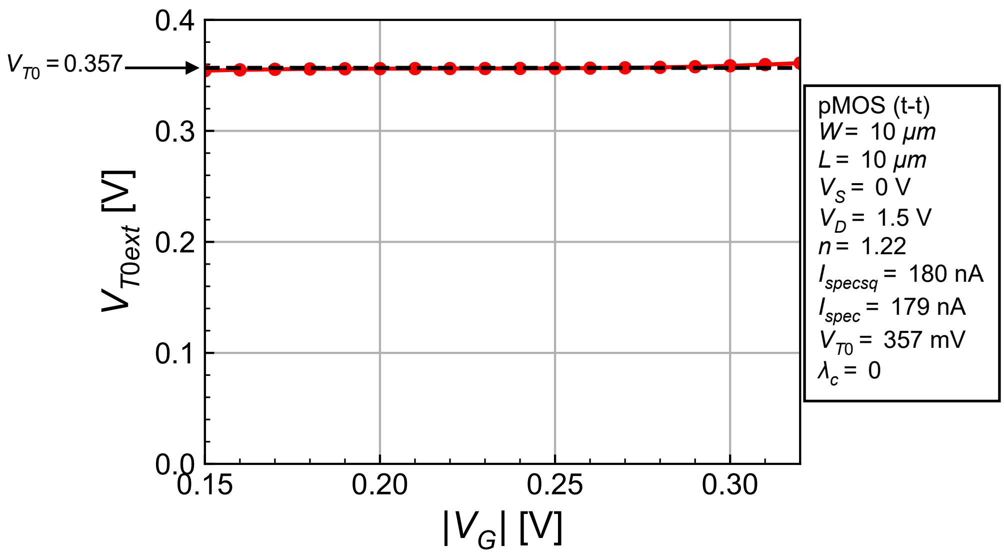
$I_{spec\square} = 180\ nA$

$\lambda_c = 0$



We see a plateau in weak inversion where we can average its value to get the threshold voltage in weak inversion.

$V_{T0,wi} = 357$ mV



The threshold voltage for this wide and long device is consistent with the documentation giving a typical-typical $V_{TH} \cong 350\,mV$ for $W = 10\,\mu m$ and $L = 10\,\mu m$.

We can now plot the I_D-V_G for this threshold voltage.

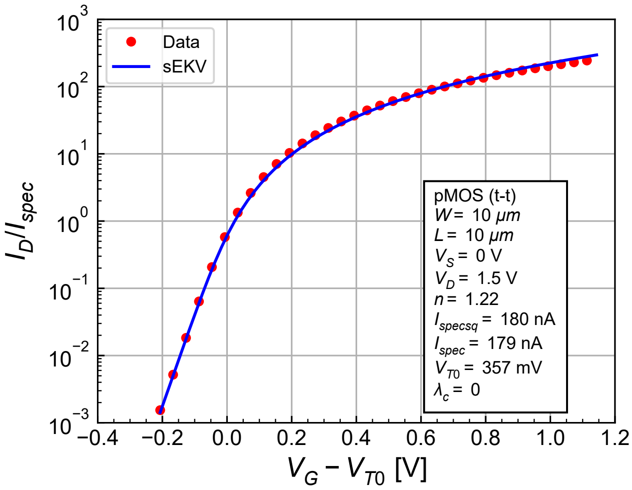
$n = 1.22$

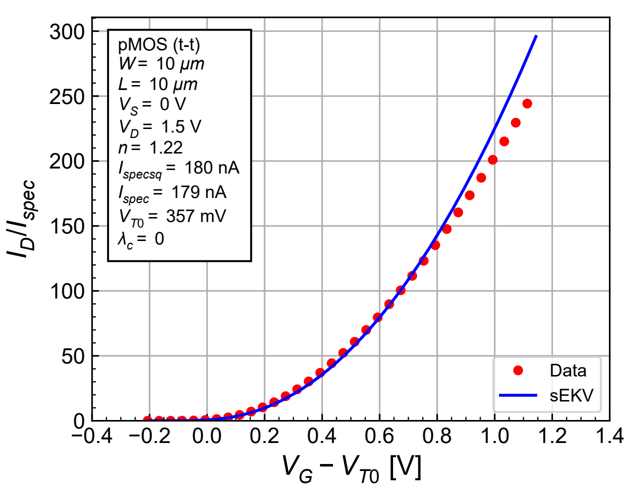
$I_{spec} = 179\ nA$

$I_{spec\square} = 180\ nA$

$\lambda_c = 0$

$V_{T0,wi} = 357$ mV





We get a reasonable fit with some deviations in strong inversion.

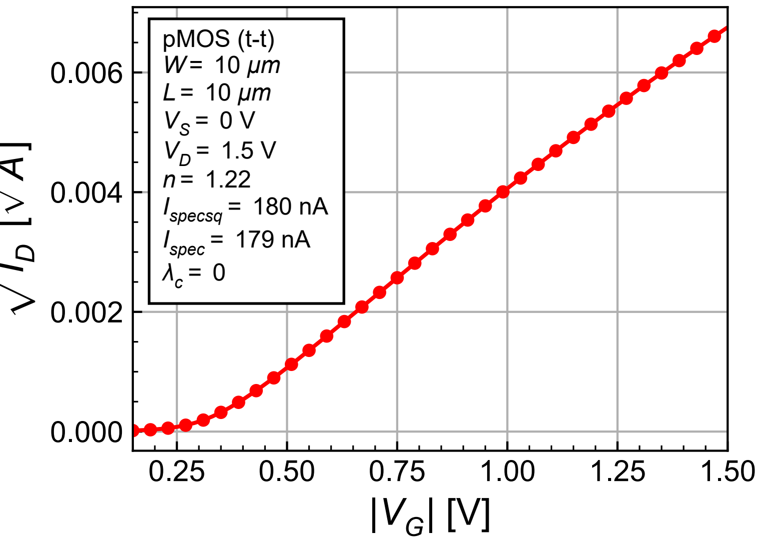
We can also extract the threshold voltage in strong inversion.

$n = 1.22$

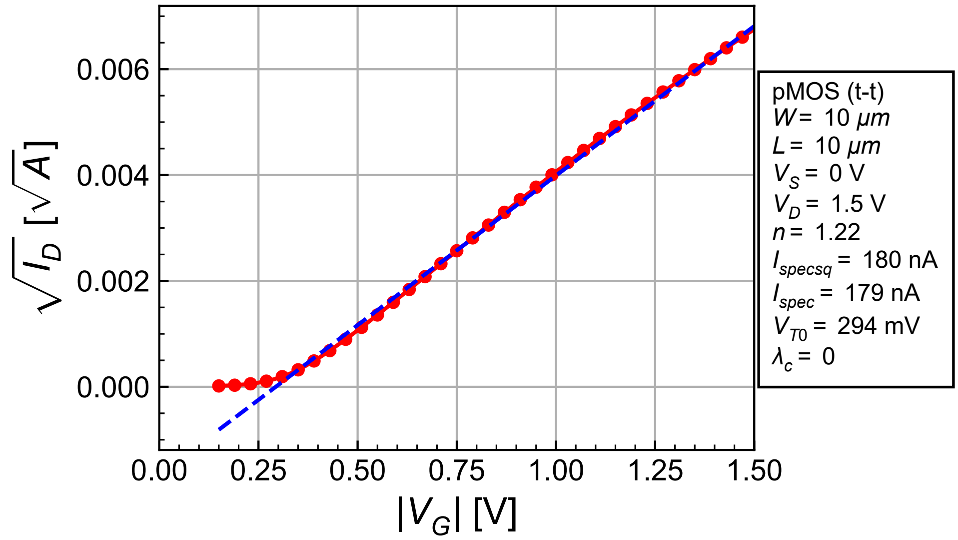
$I_{spec} = 179\ nA$

$I_{spec\square} = 180\ nA$

$\lambda_c = 0$



$V_{T0,si} = 294$ mV



We get a smaller value of the threshold voltage than the value extracted in weak inversion. We can check the fit in all regions.

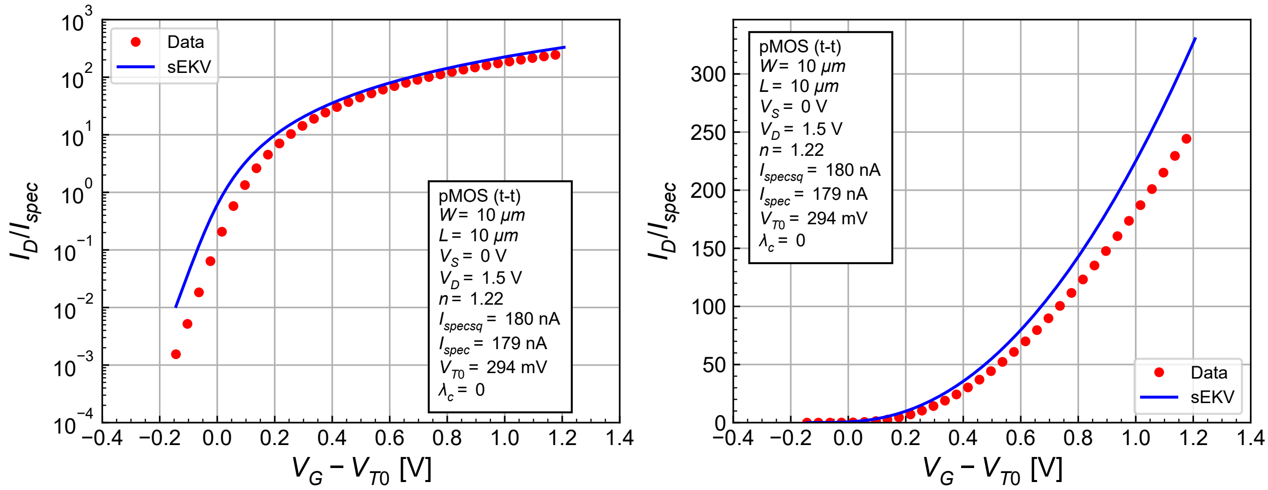
$n = 1.22$

$I_{spec} = 179\ nA$

$I_{spec\square} = 180\ nA$

$\lambda_c = 0$

$V_{T0,si} = 294$ mV



As expected, we get a less good fit in weak inversion. We therefore keep the value of the threshold voltage extracted in weak inversion.

3.1.3.3 Summary

$n = 1.22$

$I_{spec} = 179\ nA$

$I_{spec\square} = 180\ nA$

$V_{T0,wi} = 357$ mV

$\lambda_c = 0$

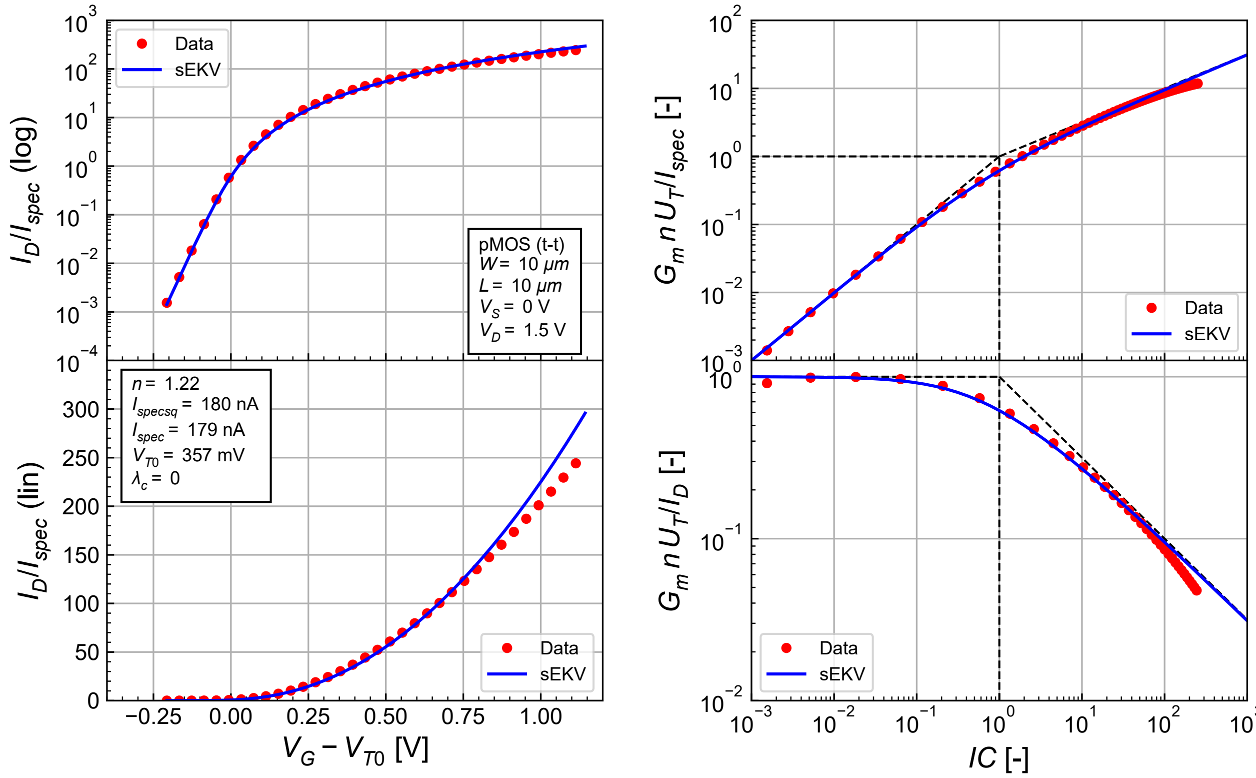


Table 3.1: Direct extraction of the sEKV parameters for the long-channel transistor with $\lambda_c = 0$

	W	Weff	L	Leff	n	Ispecsq	VT0	lambdac	Lsat	Comm
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.800e-07	3.568e-01	0	0	direc

3.1.4 Extraction using optimization with $\lambda_c = 0$

3.1.4.1 Slope factor n and I_{spec} extraction

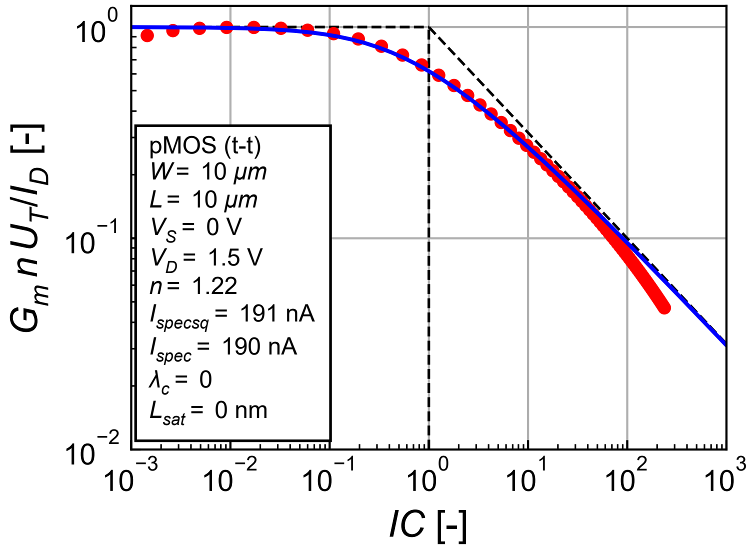
We can try to extract n and I_{spec} for a long-channel directly from the normalized G_m/I_d function.

$n = 1.22$

$I_{spec} = 190\ nA$

$I_{spec\square} = 191\ nA$

$\lambda_c = 0$



We get a reasonable fit a value of $I_{spec\square}$ larger than what we got with the direct extraction.

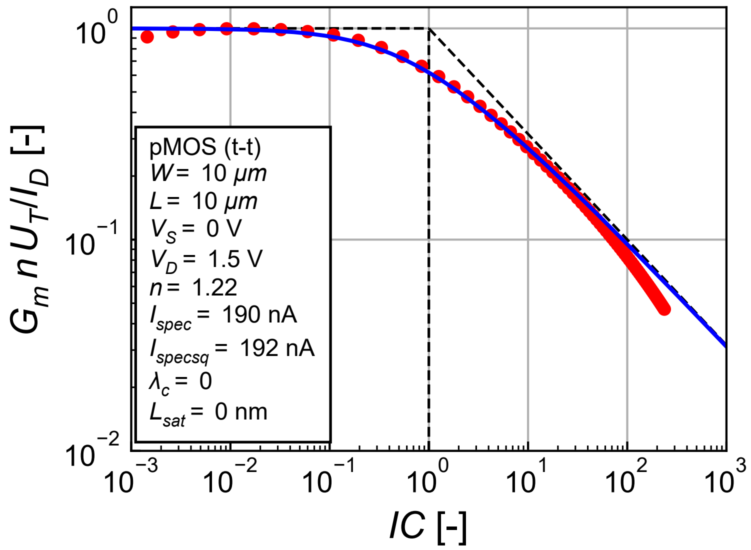
We can also try to keep the value of n extracted from the direct extraction above and optimize for I_{spec} only.

$n = 1.22$

$I_{spec} = 190\ nA$

$I_{spec\square} = 192\ nA$

$\lambda_c = 0$



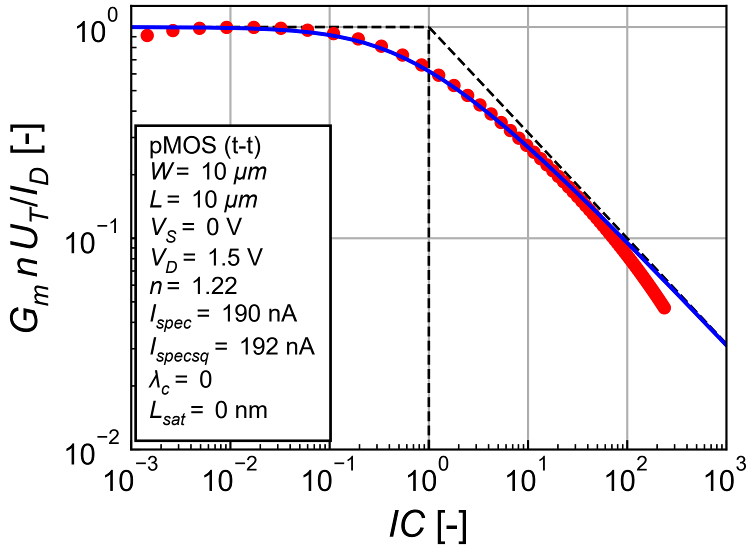
The fit is good in weak and moderate inversion, but we still have some discrepancies in strong inversion which is due to mobility reduction due to the vertical field. We will keep the last extracted values for I_{specsq}.

$n = 1.22$

$I_{spec} = 190\ nA$

$I_{spec\square} = 192\ nA$

$\lambda_c = 0$



3.1.4.2 Threshold voltage extraction

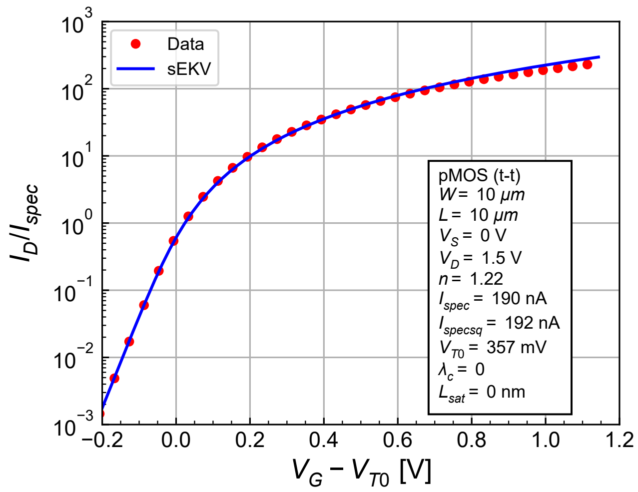
$n = 1.22$

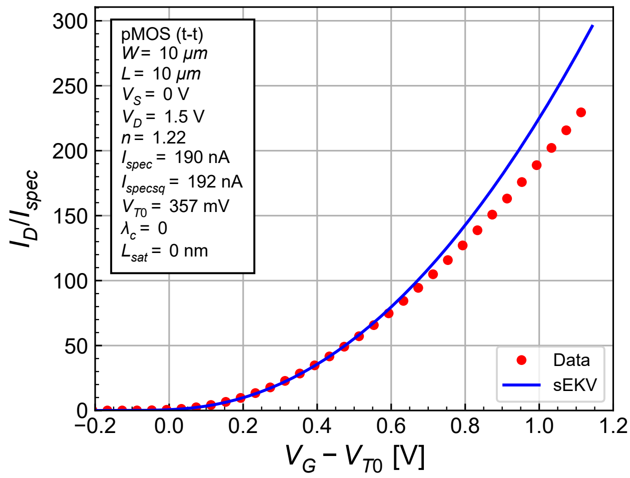
$I_{spec} = 190\ nA$

$I_{spec\square} = 192\ nA$

$V_{T0} = 357$ mV

$\lambda_c = 0$





We see a reasonable fit except in strong inversion. This is expected since we optimized the moderate inversion region.

3.1.4.3 Summary

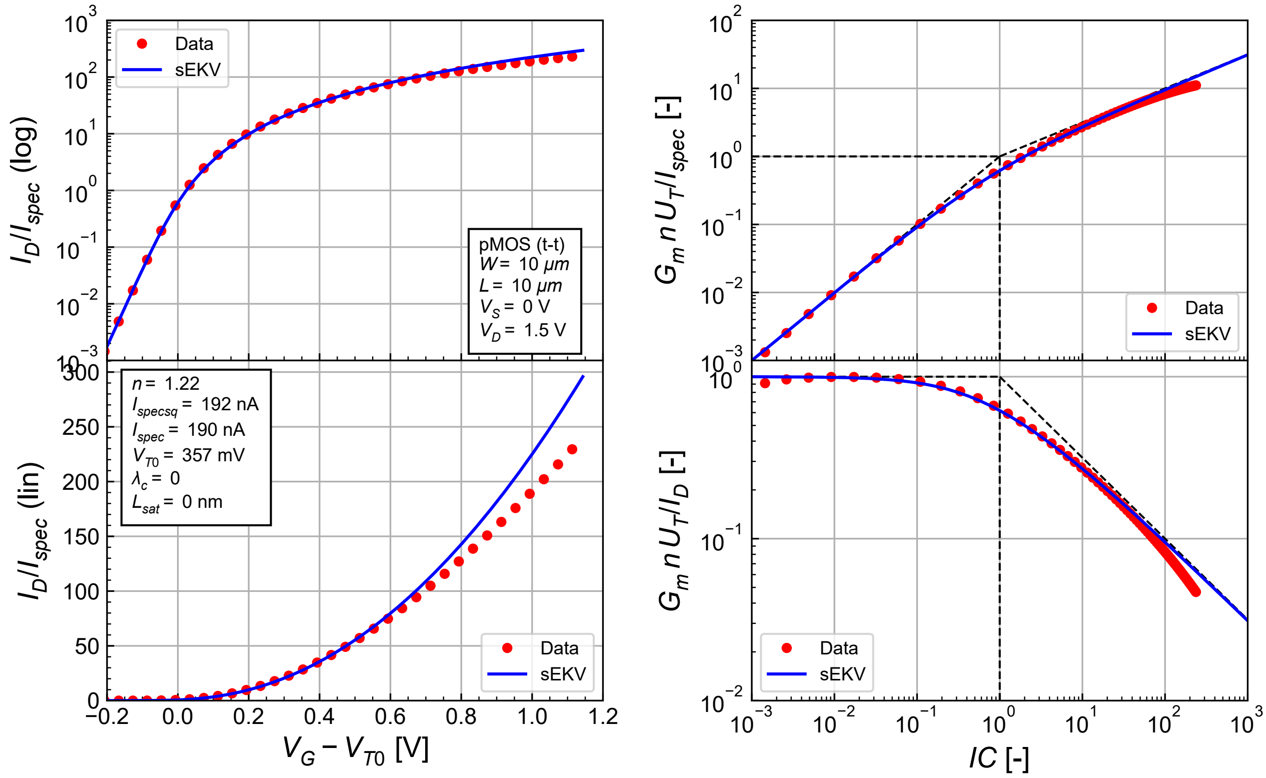
$n = 1.22$

$I_{spec} = 190\ nA$

$I_{spec\square} = 192\ nA$

$V_{T0} = 357$ mV

$\lambda_c = 0$



The extraction using curve-fitting gives a better fit in moderate inversion but less in strong inversion.

Table 3.2: Extraction of the sEKV parameters by optimization for the long-channel transisto
$\lambda_c = 0$.

	W	Weff	L	Leff	n	Ispecsq	VT0	lambdac	Lsat	Com
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.800e-07	3.568e-01	0	0	direc
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.915e-07	3.569e-01	0	0	optin

3.1.5 Extraction using optimization with $\lambda_c > 0$

We start extracting n, I_{spec} and λ_c using curve fitting on G_m/I_D.

$n = 1.23$

$I_{spec} = 212\ nA$

$I_{spec\square} = 212\ nA$

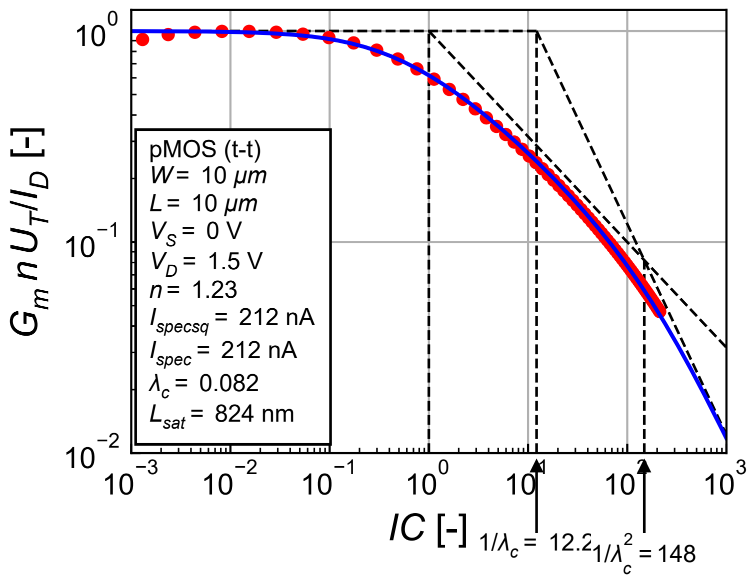
$V_{T0} = 357$ mV

$\lambda_c = 0.082$

$L_{sat} = 824.416$ nm

$1/\lambda_c = 12$

$1/\lambda_c^2 = 148$



We now have a good fit in strong inversion that we can still improve by slightly reducing the value of I_{specsq}, which seems too high and λ_c.

$n = 1.23$

$I_{spec} = 198\ nA$

$I_{spec\square} = 200\ nA$

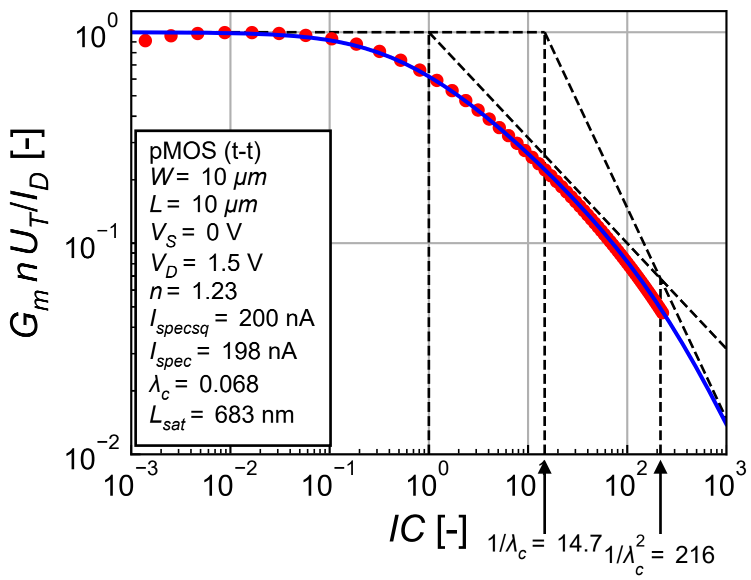
$V_{T0} = 357$ mV

$\lambda_c = 0.068$

$L_{sat} = 683$ nm

$1/\lambda_c = 15$

$1/\lambda_c^2 = 216$



We now have an almost perfect fit.

3.1.5.1 Summary

We can now check the large and small-signal characteristics.

$n = 1.23$

$I_{spec} = 198\ nA$

$I_{spec\square} = 200\ nA$

$V_{T0} = 357$ mV

$\lambda_c = 0.068$

$L_{sat} = 683$ nm

$1/\lambda_c = 15$

$1/\lambda_c^2 = 216$

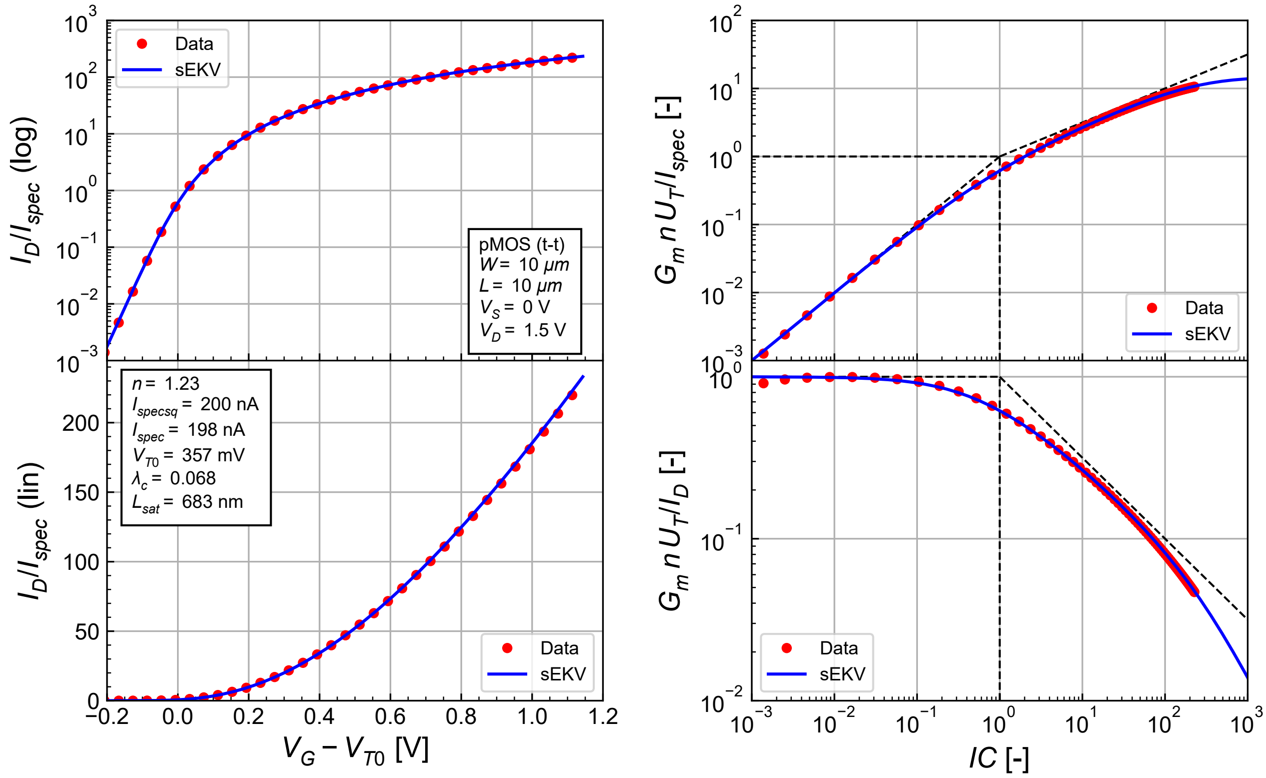


Table 3.3: Extraction of the sEKV parameters by optimization for the long-channel trans
$\lambda_c > 0$.

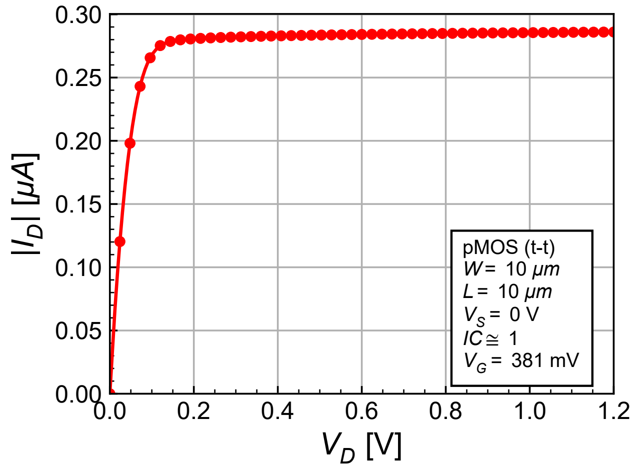
	W	Weff	L	Leff	n	Ispecsq	VT0	lambdac	Lsat
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.800e-07	3.568e-01	0.000e+00	0.000e+00
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.915e-07	3.569e-01	0.000e+00	0.000e+00
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.227e+00	2.000e-07	3.569e-01	6.800e-02	6.831e-07

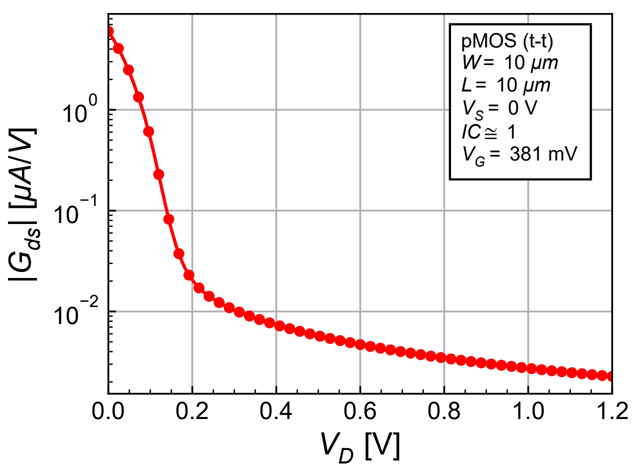
3.2 Output characteristic

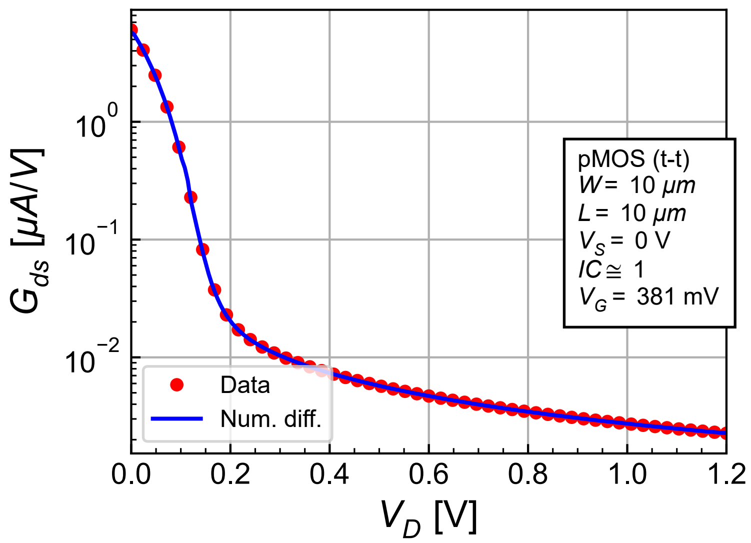
3.2.1 Generating the data

3.2.2 Importing and plotting the data

3.2.2.1 I_D and G_{ds} versus V_D

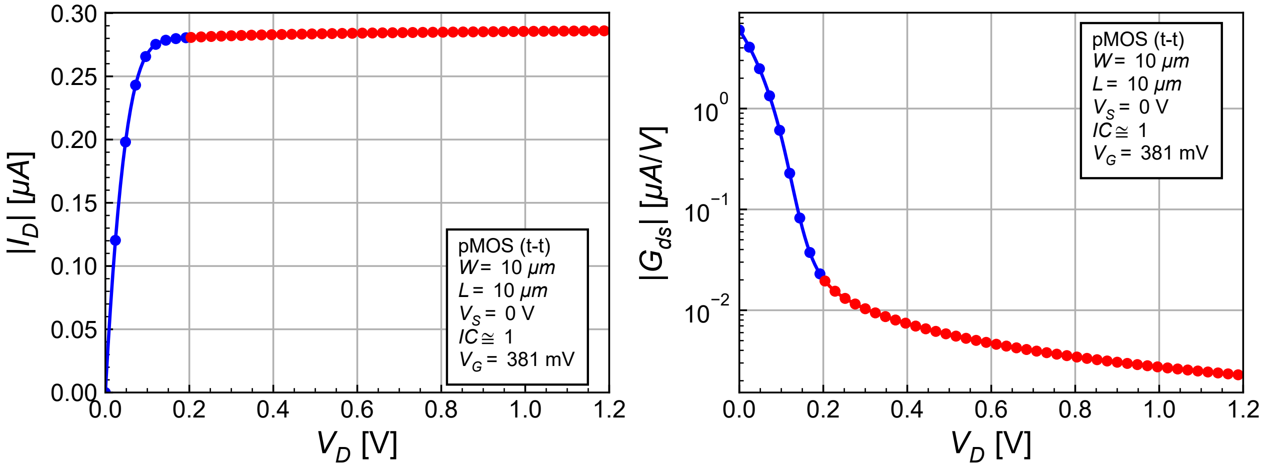






The output conductance calculated by differentiating the large-signal I_D-V_D matches the value extracted from the PSP model. We will keep the value from PSP.

3.2.2.2 Filtering the outliers



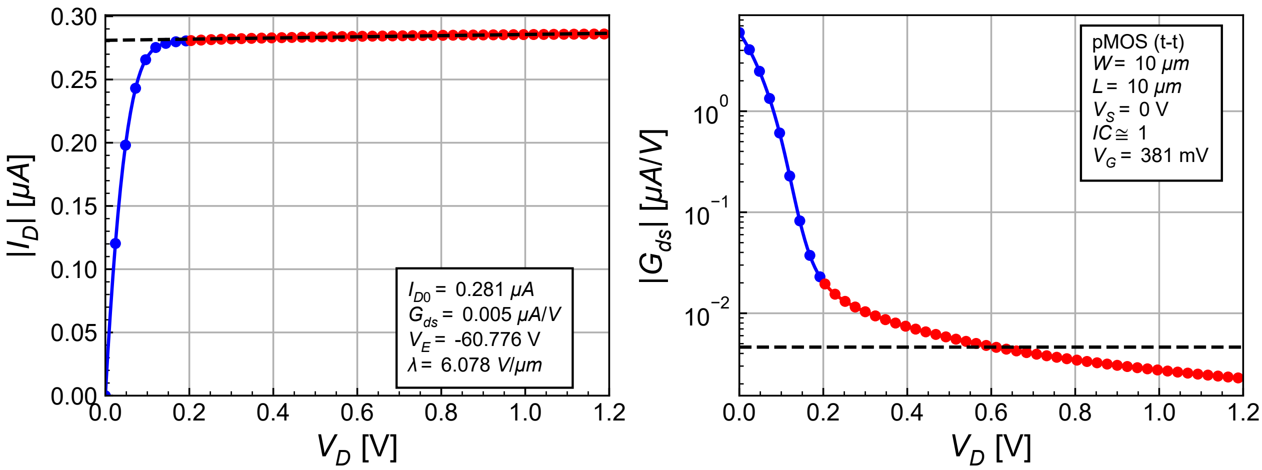
3.2.3 Extracting the CLM parameter

G_{ds} = 0.005 $\mu A/V$

I_{D0} = 0.281 μA

V_E = -60.776 V

λ = 6.078 $V/\mu m$



We get a much smaller output conductance than for the nMOS and hence a higher value of the λ parameter.

Table 3.4: CLM parameters extracted for the long-channel transistor in moderate inversion.

	W	Weff	L	Leff	IC	Gds	ID0	VE	lambda	Com
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1	4.623e-09	2.810e-07	-6.078e+01	6.078e+06	mod

3.3 Noise

In this section we will extract the flicker noise parameters to be used with sEKV and check the white noise power spectral desnity (PSD). We reuse the flicker noise model from EKV 2.6, where the input (gate) referred PSD is given by

$$S_{nin,fl}(f) = \frac{KF}{W_{eff}\, L_{eff}\, C_{ox}\; f^{AF}} \tag{3.5}$$

In this model the flicker noise is assumed to scale as $1/C_{ox}$, which is correct if the noise follows the the Hooge model (i.e. originates from mobility fluctuations). In the case of the Mc Worther model (i.e. flicker noise originating from traps in Si-SiO$_2$ interface and in the oxyde), the PSD scales as C_{ox}^2. Despiet the flicker noise is usually domanted by the trapping mechanism, we will keep the above model with a $1/C_{ox}$ scaling.

In EKV , we like to rewrite the flicker noise PSD like the thermal noise in terms of a input-referred noise resistance

$$S_{nin,fl}(f) = 4kT\, R_{nin,fl}(f) \tag{3.6}$$

where

$$R_{nin,fl}(f) = \frac{\rho}{W_{eff}\, L_{eff}\; f^{AF}} \tag{3.7}$$

with

$$\rho = \frac{KF}{4kT\, C_{ox}} \tag{3.8}$$

Note that the flicker noise parameter have some weird units. Indeed, KF is in $A \cdot V \cdot s^{2-AF}$ and ρ is in $V \cdot m^2/(A \cdot s^{AF})$. If $AF = 1$, like it is often the case, then KF is in $A \cdot V \cdot s$ and ρ is in $V \cdot m^2/(A \cdot s)$.

To extract the noise parameters, we use a common-source stage loaded by a noiseless resistor. We first will set the bias condition in terms of IC and calculate the input-referred white noise to compare it to the result obtained from the PSP simulations.

3.3.1 Setting bias conditions

Having extracted n, $I_{spec\square}$ and V_{T0}, we can impose the inversion coefficient and calculate the corresponding gate voltage V_G. We nee to make sure the transistor remains in saturation.

$W = 10\ \mu m$

$L = 10\ \mu m$

$IC = 1$

$I_D = 0.190\ \mu A$

$V_G = 0.381\ V$

$V_S = 0.000\ V$

$G_m = 3.723\ \mu A/V$

$\gamma_n = 0.688$

$R_{n,th} = 184.714\ k\Omega$

$S_{n,th} = 3.062\text{e-}15\ V^2/Hz$

$V_{n,th} = 55.334\ nV/\sqrt{Hz}$

$A_v = 10$

$R_L = 2686.093\ k\Omega$

$V_{DD} = 1.200\ V$

$V_{RL} = 0.511\ V$

$V_{DS} = 0.689\ V$

$V_{DSsat} = 0.116\ V$

```
The transistor is biased in the saturation region
```

3.3.2 Extract operating point information

We can extract the values of the PSP noise parameters from the operating point informations.

$V_{n,th} = 74.370\ nV/\sqrt{Hz}$ (PSP)

$f_k = 1.022\ kHz$ (PSP)

$KF = 8.726\text{e-}24\ VAs$ (PSP)

$\rho = 0.034\ Vm^2/(As)$ (PSP)

$AF = 1.000$ (PSP)

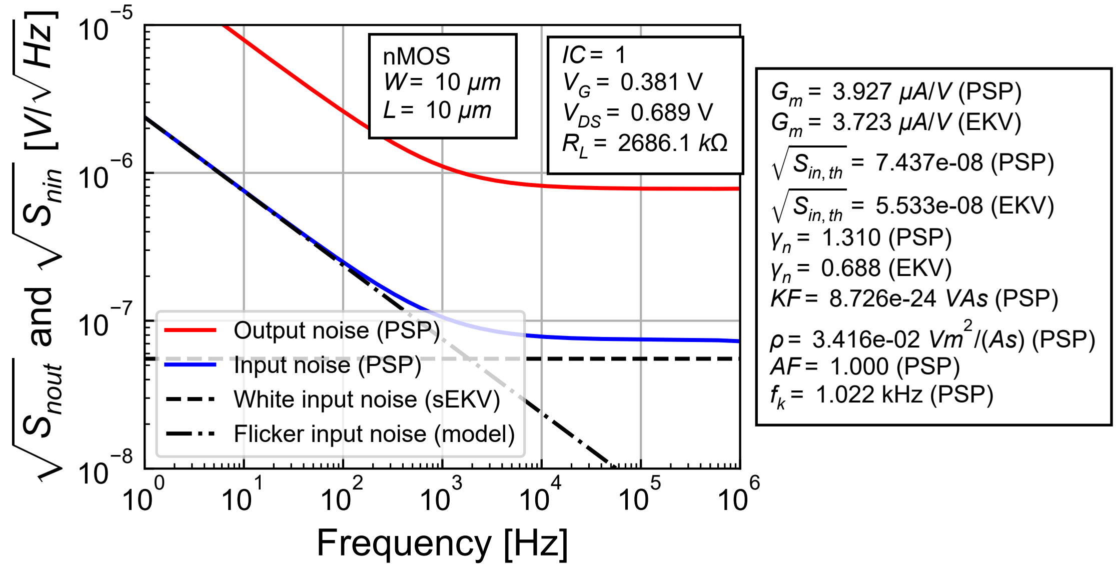
$R_{n,th} = 333.665\ k\Omega$ (PSP)

$\gamma_n = 1.310$ (PSP)

	Weff	Leff	IDS	Gm	Gds	Snidth	Vninth	Snidfl @ 1Hz	Vninfl @
Mp	9.970e-06	1.005e-05	1.994e-07	3.927e-06	2.840e-09	8.531e-26	7.437e-08	8.718e-23	7.518e-08

3.3.3 Simulating noise PSD

We can now simulate the PSD and check against the EKV model.



The flicker noise parameters are given by

Table 3.6: Extraction of the noise parameters for the long-channel transistor.

	W	Weff	L	Leff	IC	KF	AF	rho	Comment
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1	8.726e-24	1.000e+00	3.416e-02	moderate

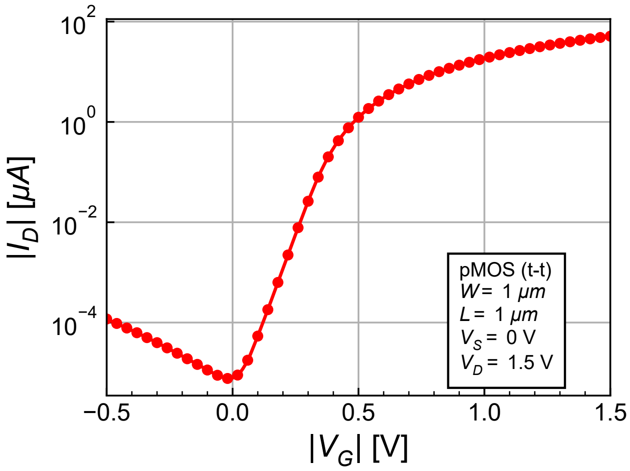
4 Medium-channel parameters

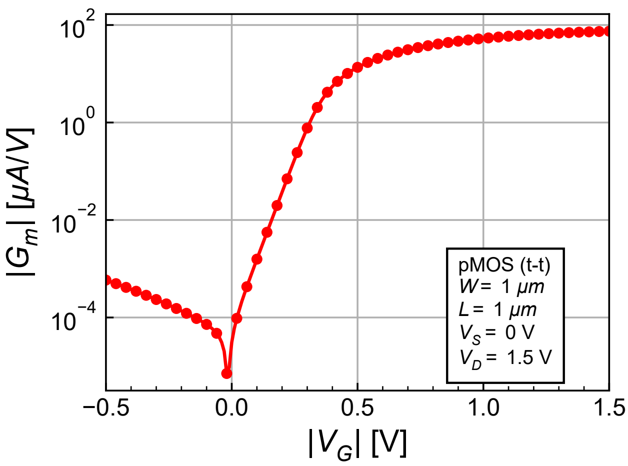
4.1 DC Transfer Characteristic Parameters

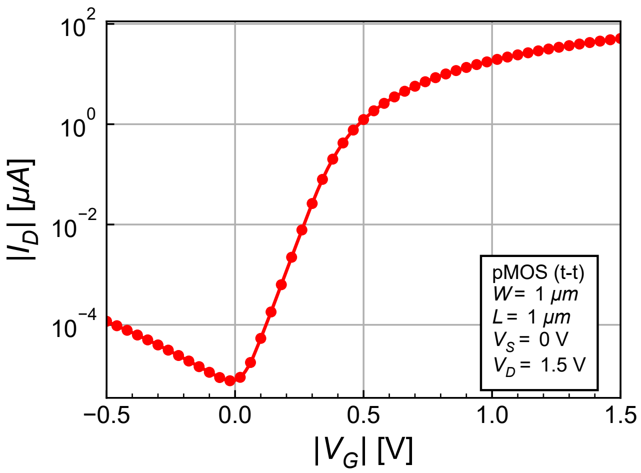
4.1.1 Generating the data

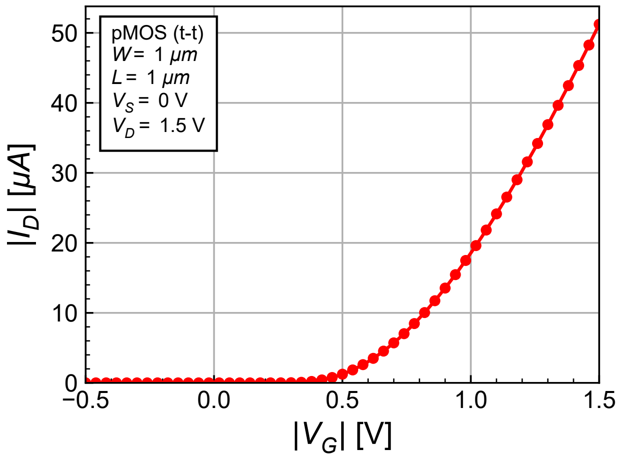
4.1.2 Importing and plotting the data

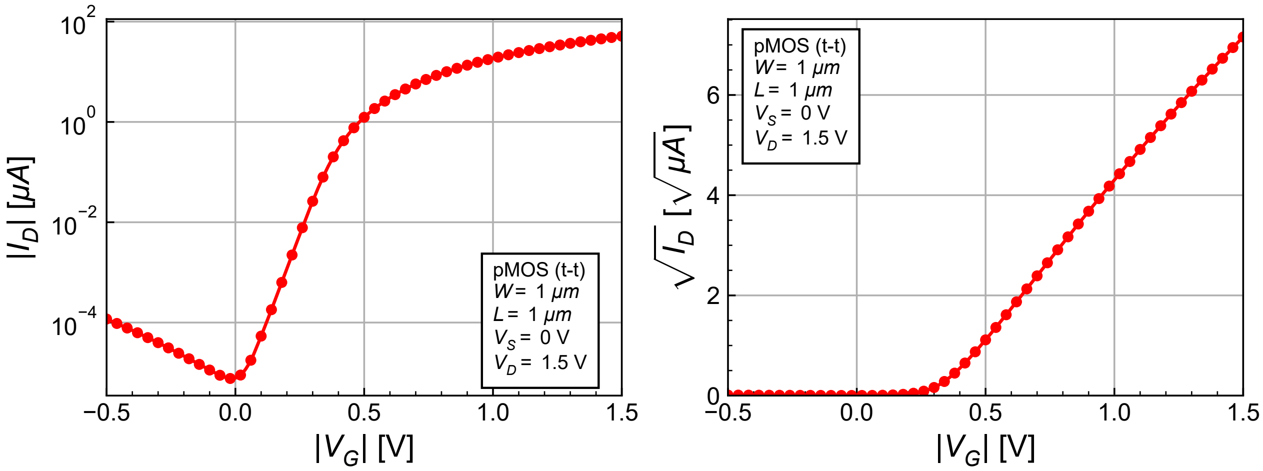
4.1.2.1 I_D and G_m versus V_G



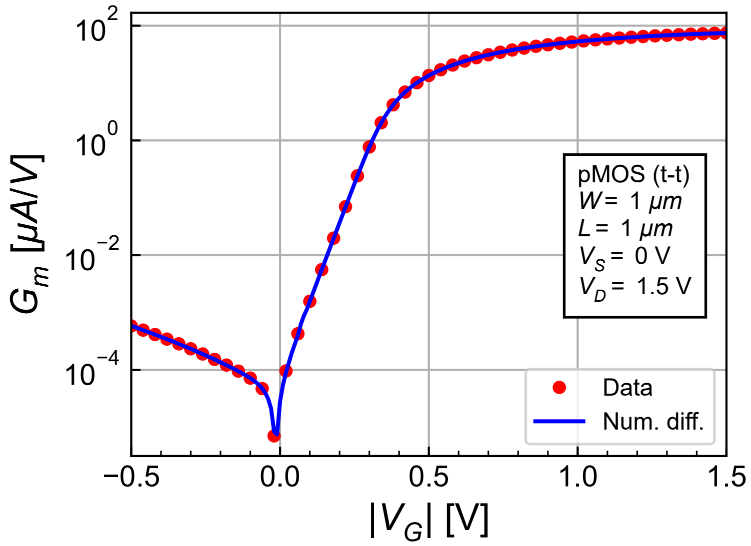






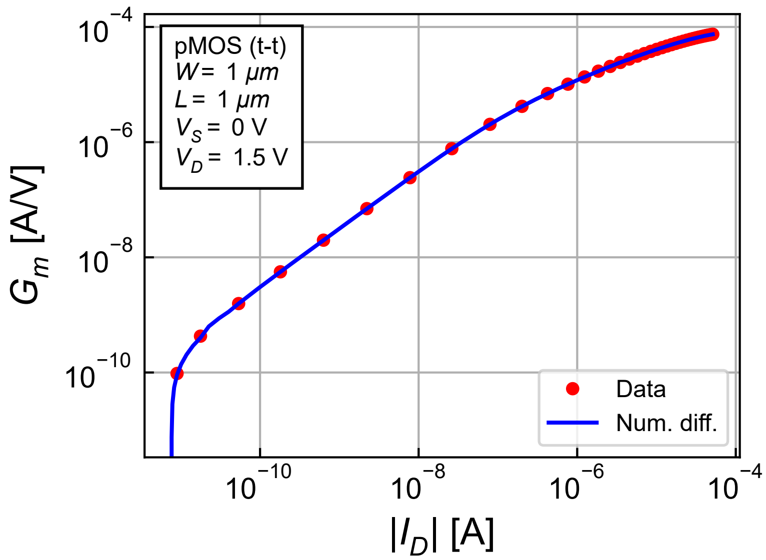


4.1.2.2 G_m-V_G

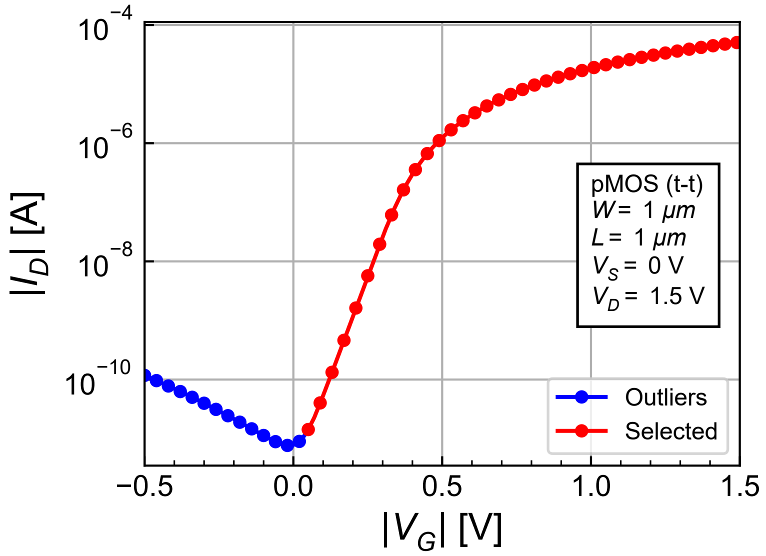


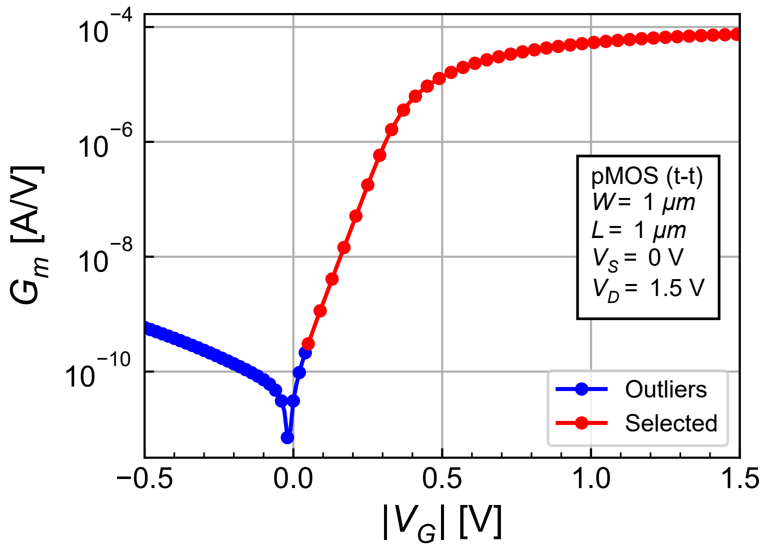
We see that the transconductance obtained by differentiating the large-signal I_D-V_G characteristic is equal to the transconductance extracted from the PSP model. We will keep the value extracted from the PSP model.

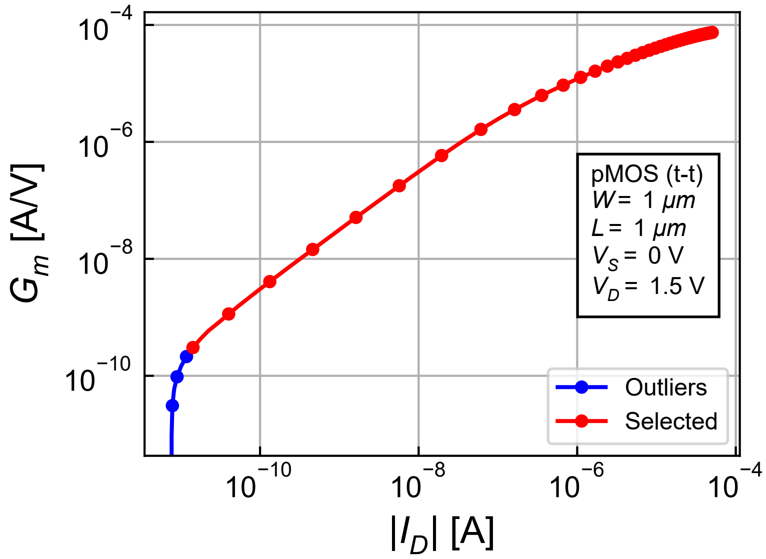
4.1.2.3 G_m-I_D



4.1.2.4 Filtering the outliers







4.1.3 Direct extraction with $\lambda_c = 0$

4.1.3.1 Slope factor n and I_{spec} extraction

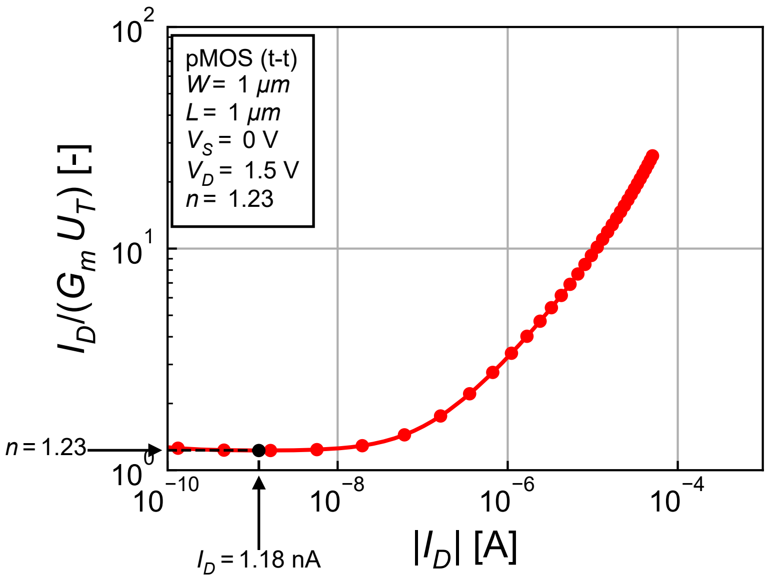
The gate transconductance in weak inversion and saturation is given by

$$G_m = \frac{I_D}{n\,U_T}. \tag{4.1}$$

So if we plot $I_D/(G_m\,U_T)$ we should see a plateau in weak inversion the value of which is equal to the slope factor n.

$n = 1.23$

$I_{D,ext} = 1.18\ nA$



On the other hand the normalized G_m/I_D function for a long-channel transistor in strong inversion and saturation is given by

$$\frac{G_m\,n\,U_T}{I_D} = \frac{1}{\sqrt{IC}} = \sqrt{\frac{I_{spec}}{I_D}}. \tag{4.2}$$

We can then plot $(G_m\,n\,U_T)^2/I_D$ which should find a maximum value equal to I_{spec}.

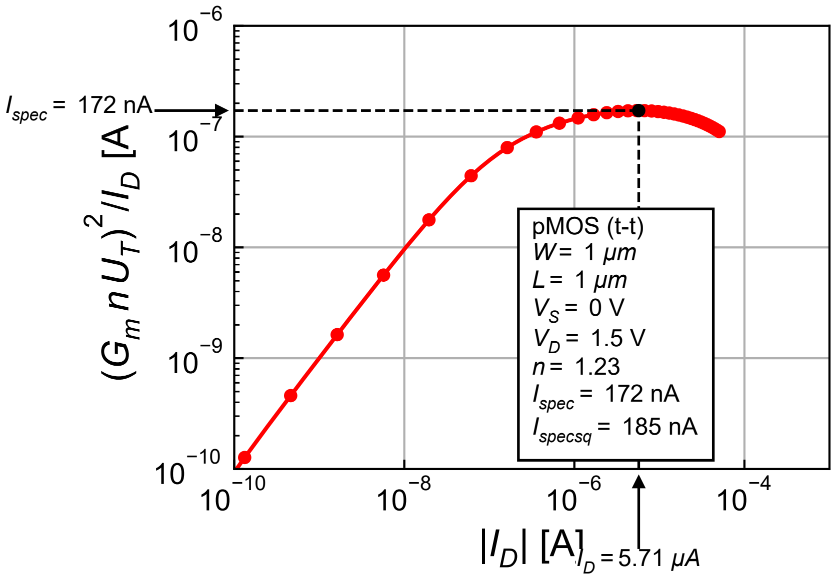
$W_{eff} = 0.970\ \mu m$

$L_{eff} = 1.043\ \mu m$

$I_{spec} = 172\ nA$

$I_{spec\square} = 185\ nA$

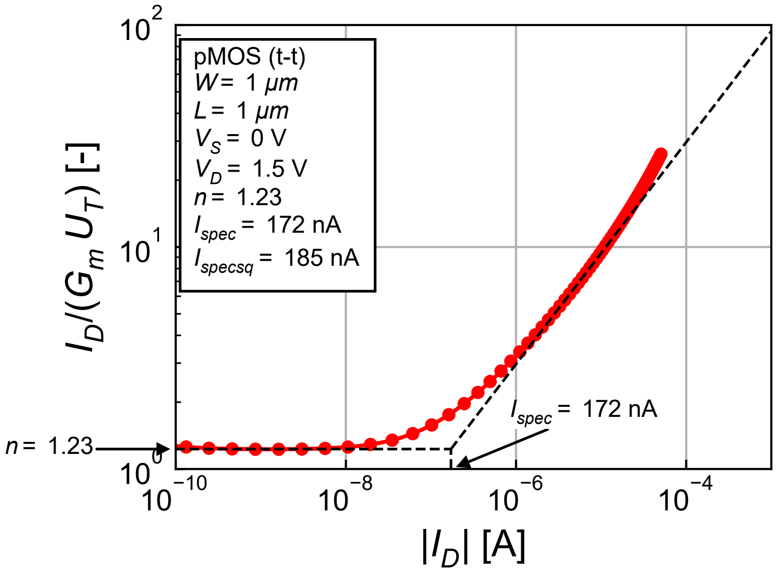
$I_{D,ext} = 5.714\ \mu A$



$n = 1.23$

$I_{spec} = 172\ nA$

$I_{spec\square} = 185\ nA$



Having extracted n and I_{spec}, we can now plot the normalized G_m/I_D function.

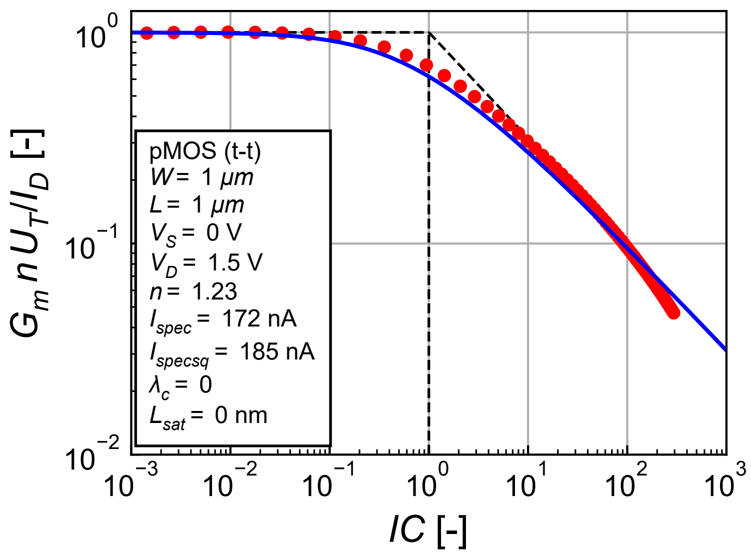
$n = 1.23$

$I_{spec} = 172\ nA$

$I_{spec\square} = 185\ nA$

$\lambda_c = 0$

$L_{sat} = 0$



The fit is reasonable over the entire IC span. There is some discrepancy in the moderate inversion region which is due to the mobility reduction due to the vertical field appearing for $IC > 10^2$. The latter can be accounted for by using the λ_c parameter which is normally used for modeling the effect of velocity saturation in short-channel transistor but can also be used to correct the effect of mobility reduction due to the vertical field appearing in long-channel transistors. We will not do this here since we want to extract the long-channel parameters keeping $\lambda_c = 0$, but since we are mostly interested in the moderate inversion region, we can slightly increase I_{spec} to improve the fit in moderate inversion at the cost of a degradation in strong inversion.

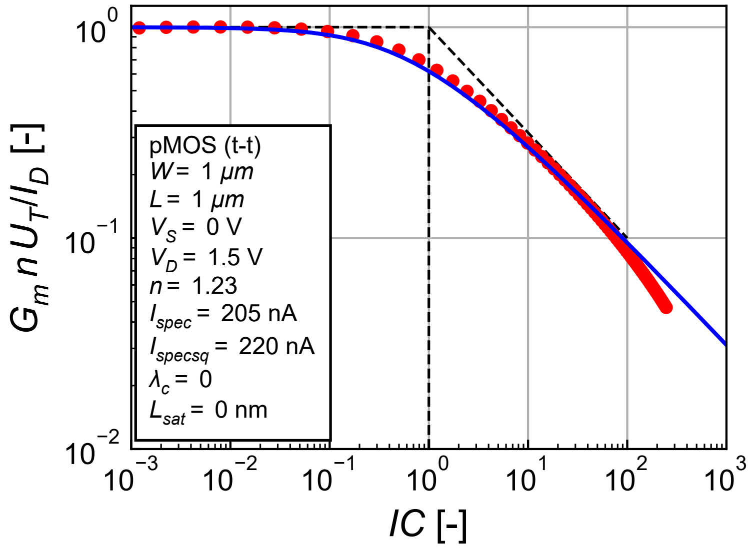
$n = 1.23$

$I_{spec\square} = 220\ nA$

$I_{spec} = 205\ nA$

$\lambda_c = 0$

$L_{sat} = 0$



The fit is now much better in moderate inversion but less in strong inversion. This is due to mobility reduction due to the vertical field an effect that is not accounted for in the model. However, we will keep the new values.

4.1.3.2 Threshold voltage extraction

We can extract the threshold voltage in weak inversion (assuming $V_S = 0$) from the normalized current (inversion coefficient) given by

$$IC = e^{\frac{V_G - V_{T0}}{nU_T}}. \tag{4.3}$$

We can now plot

$$V_{T0} = V_G - nU_T \ln(IC) \tag{4.4}$$

to extract the threshold voltage.

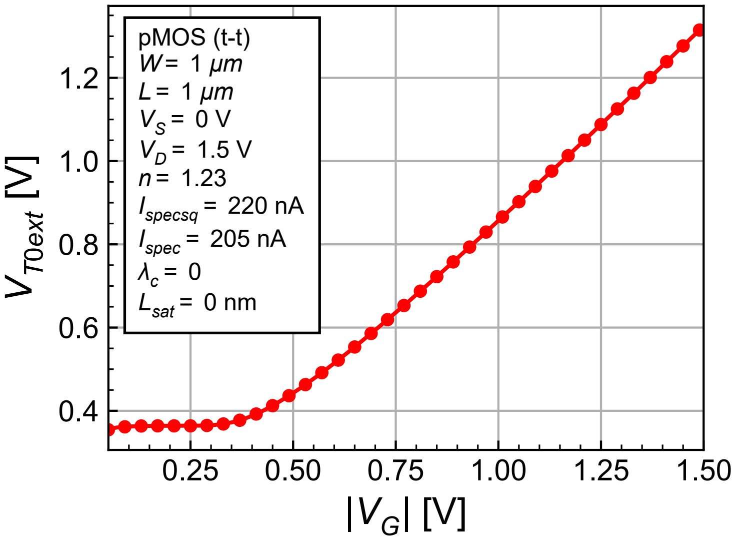
$n = 1.23$

$I_{spec} = 205\ nA$

$I_{spec\square} = 220\ nA$

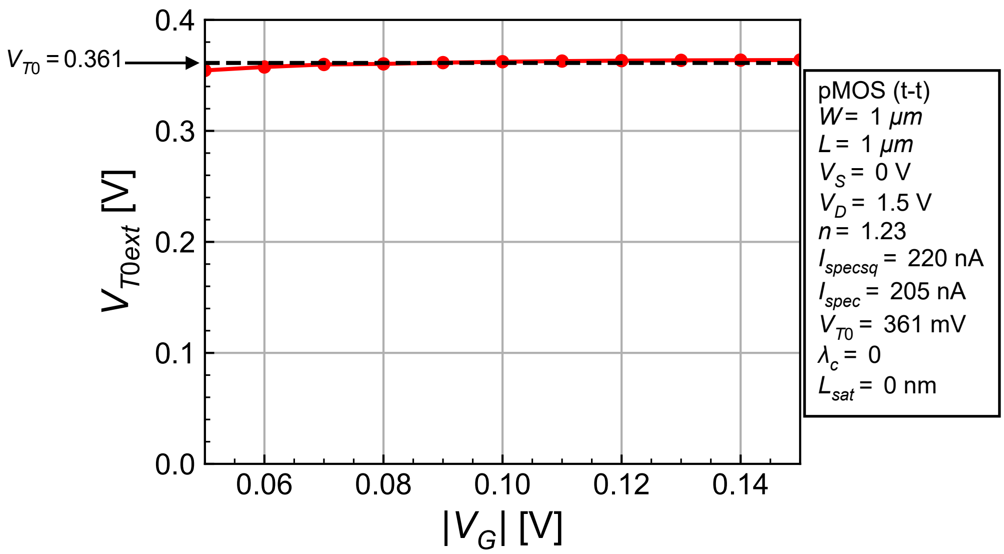
$\lambda_c = 0$

$L_{sat} = 0$



We see a plateau in weak inversion where we can average its value to get the threshold voltage in weak inversion.

$V_{T0,wi} = 361$ mV



The threshold voltage for this medium device is consistent with the documentation giving a typical-typical $V_{TH} \cong 350\,mV$ for $W = 10\,\mu m$ and $L = 10\,\mu m$.

We can now plot the I_D-V_G for this threshold voltage.

$n = 1.23$

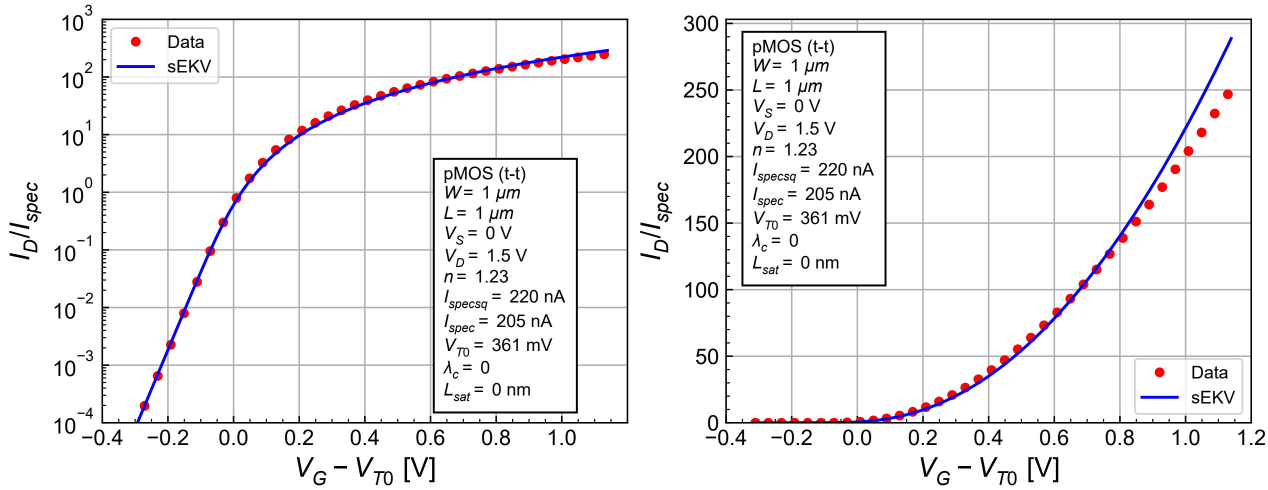
$I_{spec} = 205\ nA$

$I_{spec\square} = 220\ nA$

$\lambda_c = 0$

$L_{sat} = 0$

$V_{T0,wi} = 361$ mV



We get a reasonable fit with some deviations in strong inversion.

4.1.3.3 Summary

$n = 1.23$

$I_{spec} = 205\ nA$

$I_{spec\square} = 220\ nA$

$V_{T0,wi} = 361$ mV

$\lambda_c = 0$

$L_{sat} = 0$

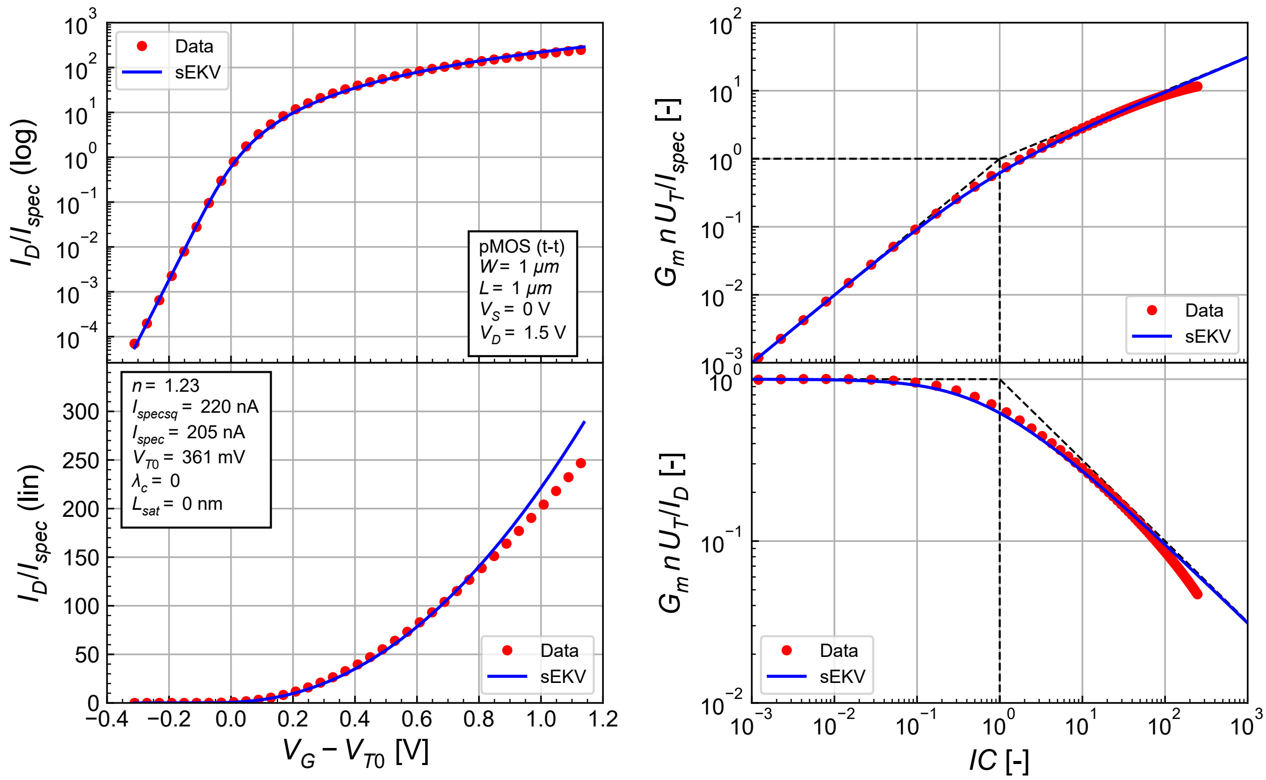


Table 4.1: Direct extraction of the sEKV parameters for the medium-channel transistor v

	W	Weff	L	Leff	n	Ispecsq	VT0	lambdac	Lsat
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.800e-07	3.568e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.915e-07	3.569e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.227e+00	2.000e-07	3.569e-01	6.800e-02	6.831e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.230e+00	2.200e-07	3.612e-01	0.000e+00	0.000e

4.1.4 Extraction using optimization with $\lambda_c = 0$

4.1.4.1 Slope factor n and I_{spec} extraction

We can try to extract n and I_{spec} for a long-channel directly from the normalized G_m/I_d function.

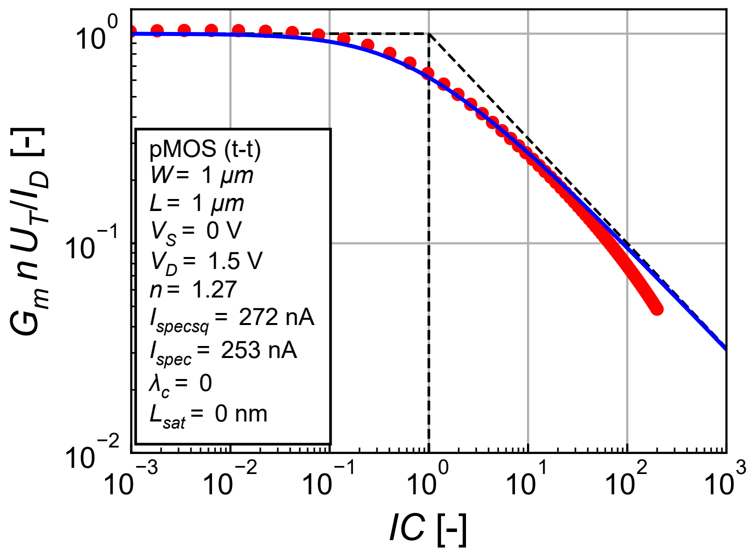
$n = 1.27$

$I_{spec} = 253\ nA$

$I_{spec\square} = 272\ nA$

$\lambda_c = 0$

$L_{sat} = 0$



We get a reasonable fit a value of $I_{spec\square}$ that is slightly higher than the direct extraction.

We can also try to keep the value of n extracted from the direct extraction above and optimize for I_{spec} only.

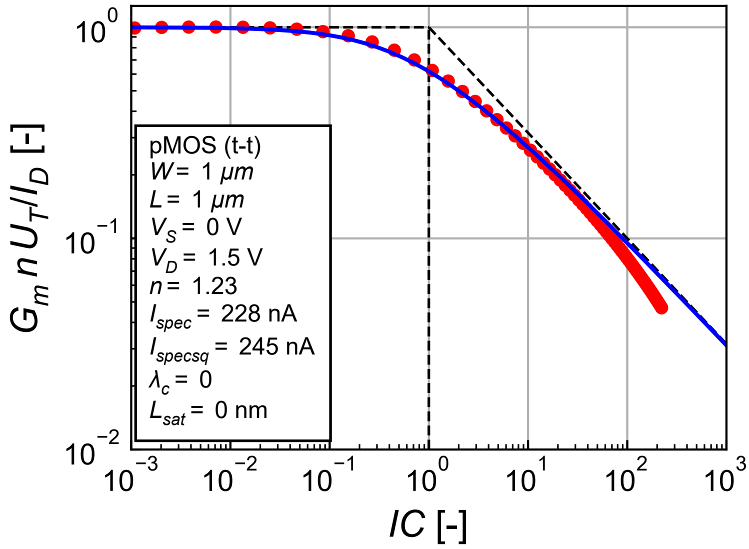
$n = 1.23$

$I_{spec} = 228\ nA$

$I_{spec\square} = 245\ nA$

$\lambda_c = 0$

$L_{sat} = 0$



The fit is good in weak and moderate inversion, but we still have some discrepancies in strong inversion which is due to mobility reduction due to the vertical field. We will keep the last extracted values for I_{specsq}.

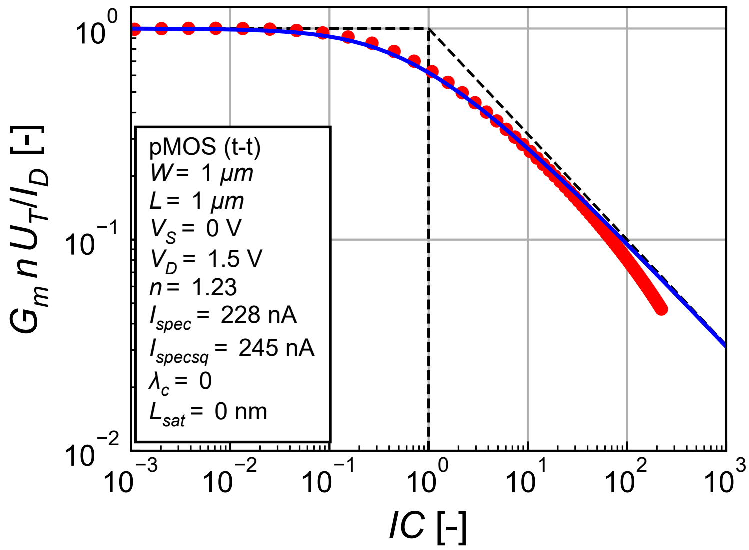
$n = 1.23$

$I_{spec} = 228\ nA$

$I_{spec\square} = 245\ nA$

$\lambda_c = 0$

$L_{sat} = 0$



4.1.4.2 Threshold voltage extraction

$n = 1.23$

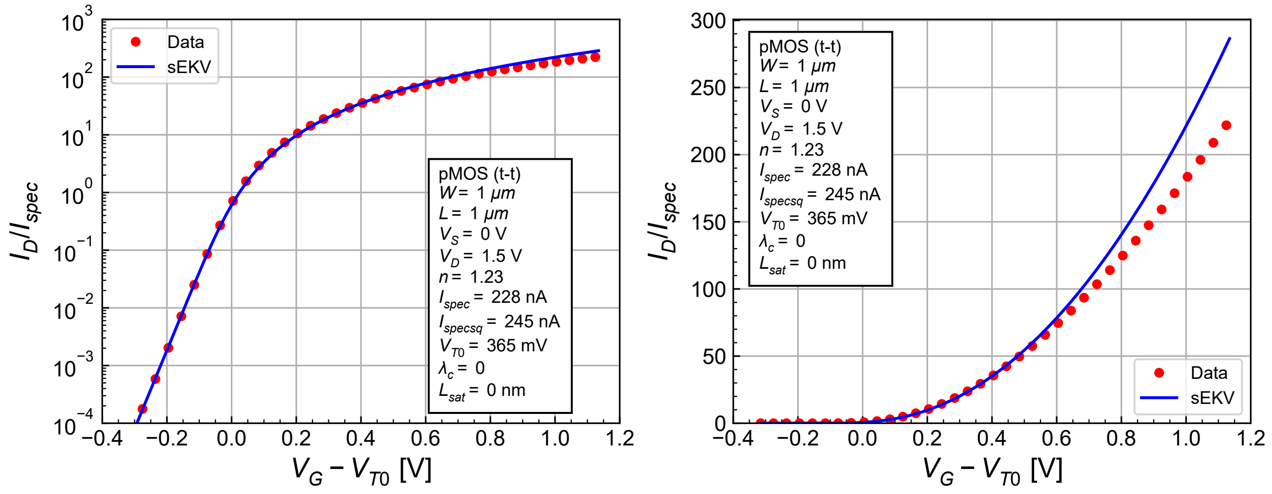
$I_{spec} = 228\ nA$

$I_{spec\square} = 245\ nA$

$V_{T0} = 365$ mV

$\lambda_c = 0$

$L_{sat} = 0$



We see a reasonable fit except in strong inversion. This is expected since we optimized the moderate inversion region.

4.1.4.3 Summary

$n = 1.23$

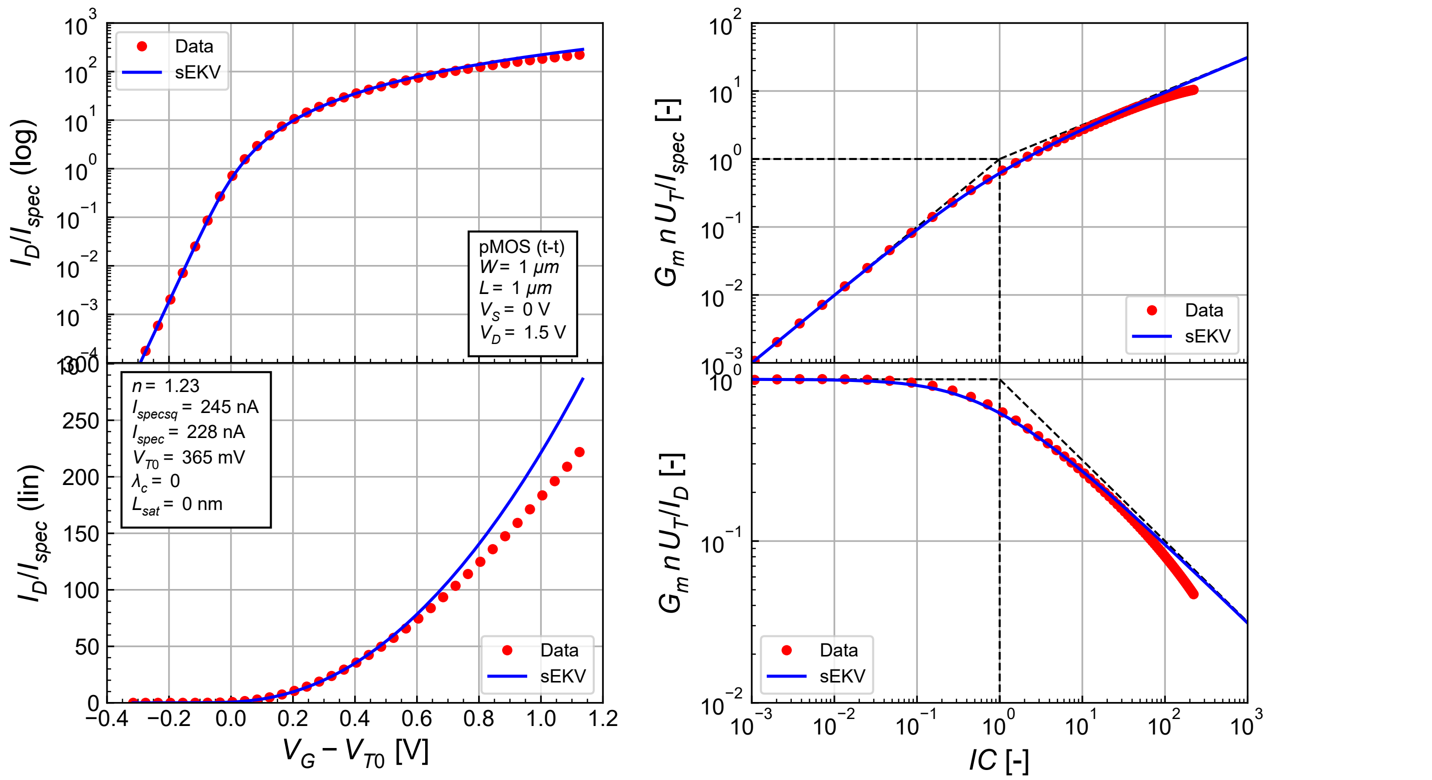
$I_{spec} = 228\ nA$

$I_{spec\square} = 245\ nA$

$V_{T0} = 365$ mV

$\lambda_c = 0$

$L_{sat} = 0$



The extraction using curve-fitting gives a better fit in moderate inversion but less in strong inversion.

Table 4.2: Extraction of the sEKV parameters by optimization for the medium-channel tra
$\lambda_c = 0$.

	W	Weff	L	Leff	n	Ispecsq	VT0	lambdac	Lsat
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.800e-07	3.568e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.915e-07	3.569e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.227e+00	2.000e-07	3.569e-01	6.800e-02	6.831e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.230e+00	2.200e-07	3.612e-01	0.000e+00	0.000e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.230e+00	2.446e-07	3.655e-01	0.000e+00	0.000e

4.1.5 Extraction using optimization with $\lambda_c > 0$

We start extracting n, I_{spec} and λ_c using curve fitting on G_m/I_D.

$n = 1.28$

$I_{spec} = 293\ nA$

$I_{spec\square} = 293\ nA$

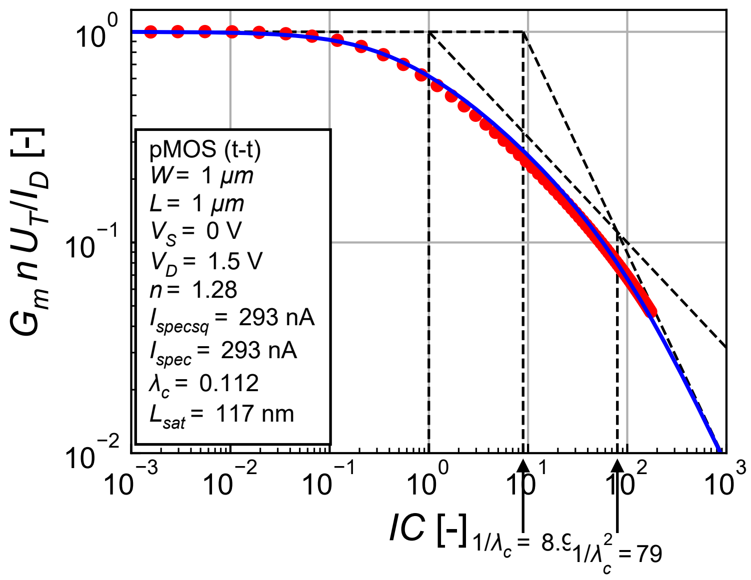
$V_{T0} = 365$ mV

$\lambda_c = 0$

$L_{sat} = 117$

$1/\lambda_c = 9$

$1/\lambda_c^2 = 79$



We now have a good fit in strong inversion that we can still improve by slightly reducing the value of I_{specsq}, which seems too high and λ_c.

$n = 1.28$

$I_{spec} = 242\ nA$

$I_{spec\square} = 260\ nA$

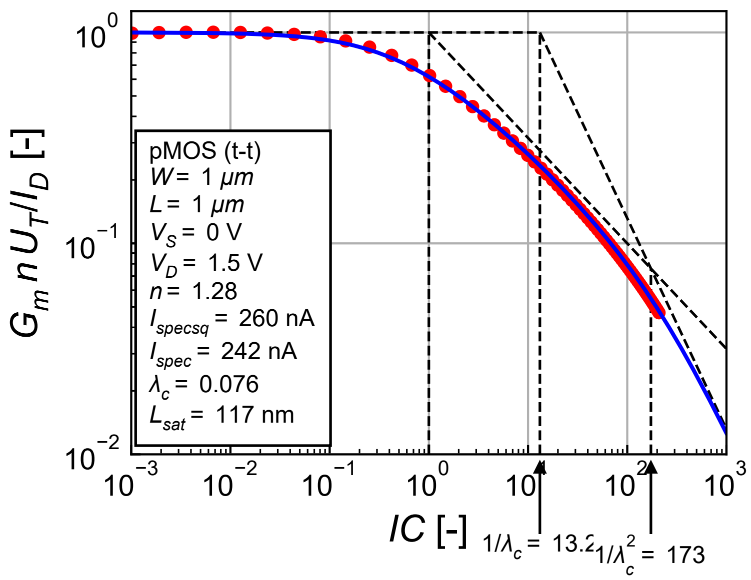
$V_{T0} = 365$ mV

$\lambda_c = 0.076$

$L_{sat} = 117$

$1/\lambda_c = 13$

$1/\lambda_c^2 = 173$



We now have an almost perfect fit.

4.1.5.1 Summary

We can now check the large and small-signal characteristics.

$n = 1.28$

$I_{spec} = 242\ nA$

$I_{spec\square} = 260\ nA$

$V_{T0} = 365$ mV

$\lambda_c = 0.076$

$L_{sat} = 117$

$1/\lambda_c = 13$

$1/\lambda_c^2 = 173$

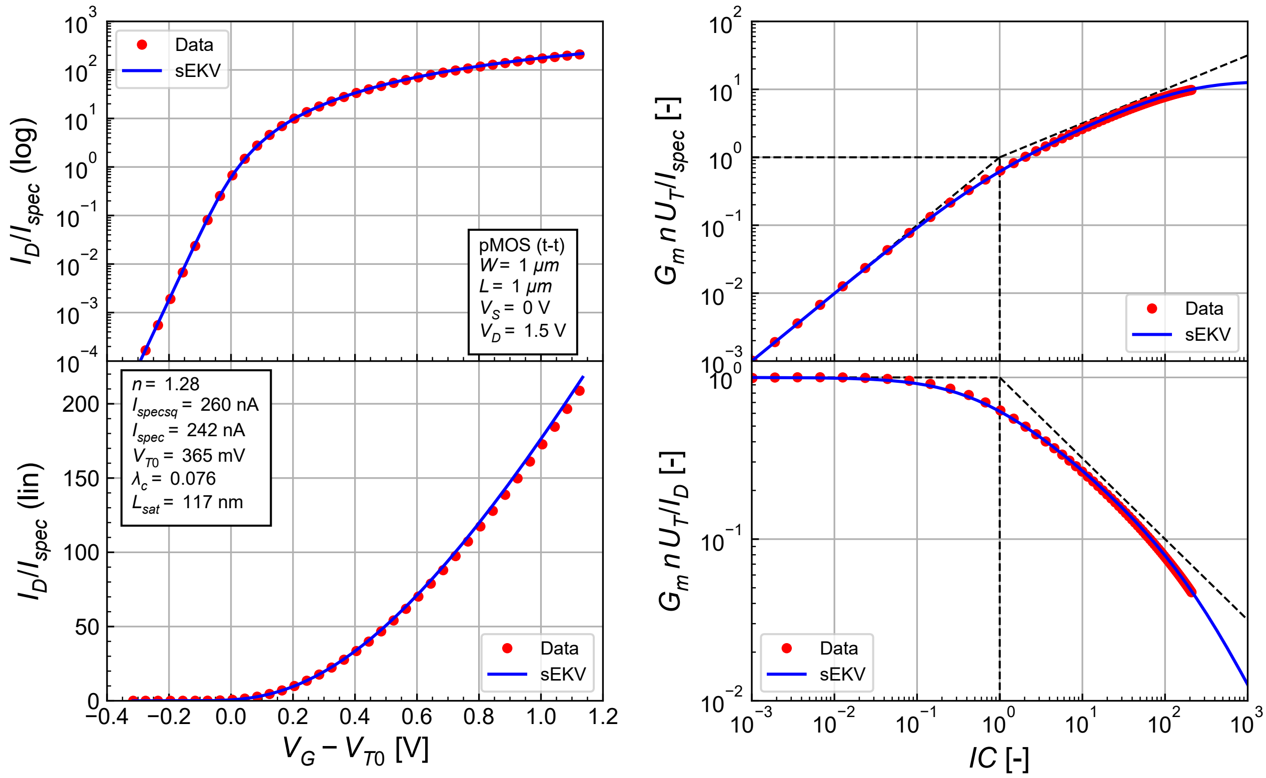


Table 4.3: Extraction of the sEKV parameters by optimization for the medium-channel tra
$\lambda_c > 0$.

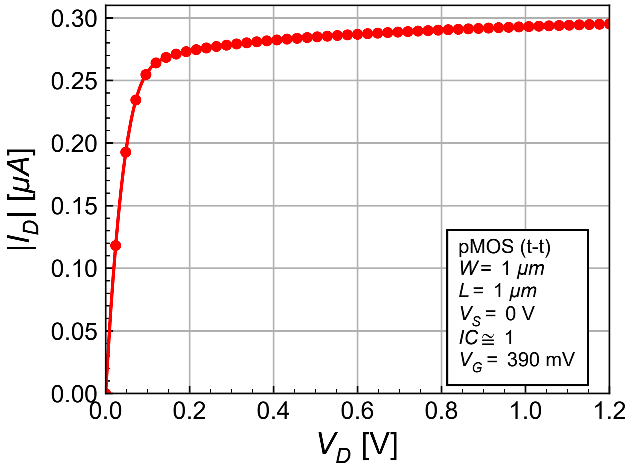
	W	Weff	L	Leff	n	Ispecsq	VT0	lambdac	Lsat
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.800e-07	3.568e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.915e-07	3.569e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.227e+00	2.000e-07	3.569e-01	6.800e-02	6.831e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.230e+00	2.200e-07	3.612e-01	0.000e+00	0.000e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.230e+00	2.446e-07	3.655e-01	0.000e+00	0.000e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.277e+00	2.600e-07	3.655e-01	7.600e-02	1.170e

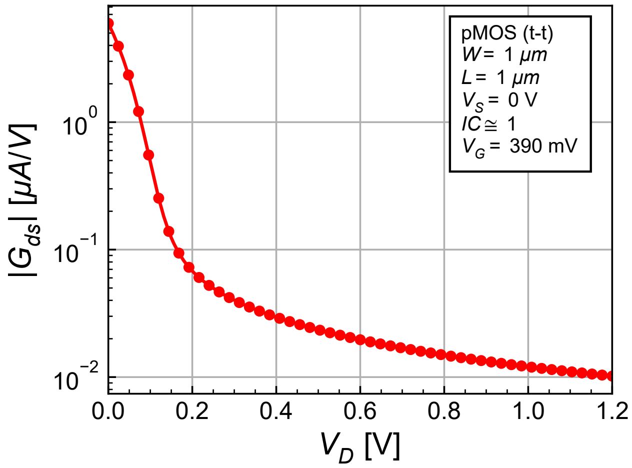
4.2 Output characteristic

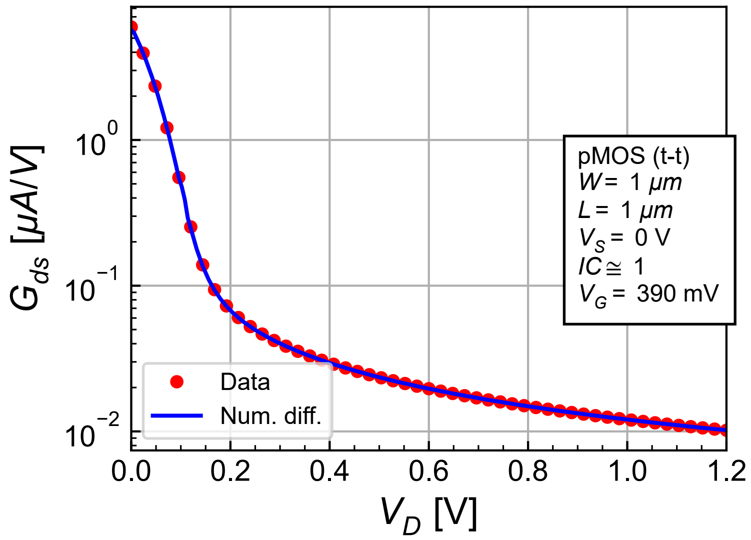
4.2.1 Generating the data

4.2.2 Importing and plotting the data

4.2.2.1 I_D and G_{ds} versus V_D

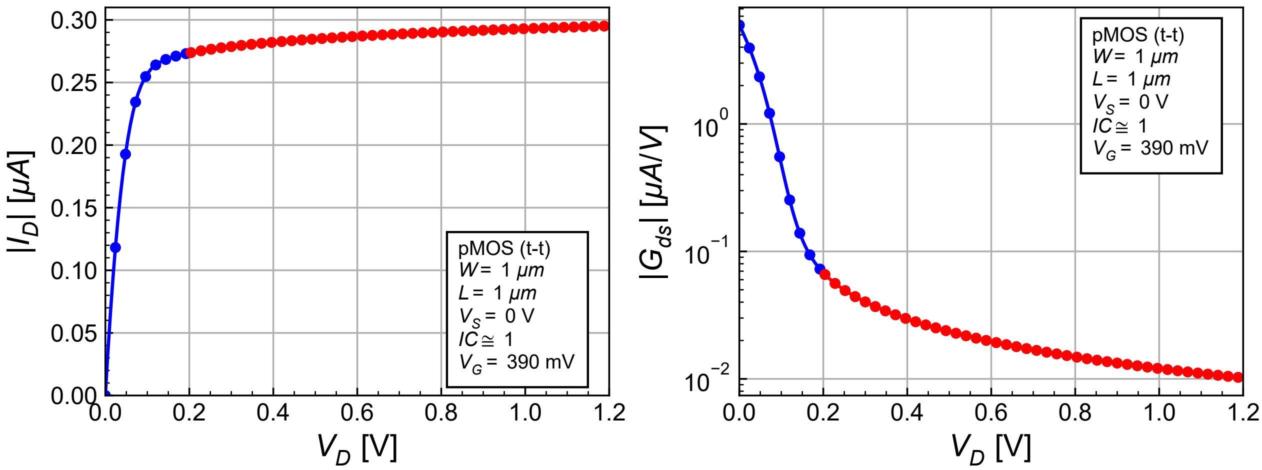






The output conductance calculated by differentiating the large-signal I_D-V_D matches the value extracted from the PSP model. We will keep the value from PSP.

4.2.2.2 Filtering the outliers



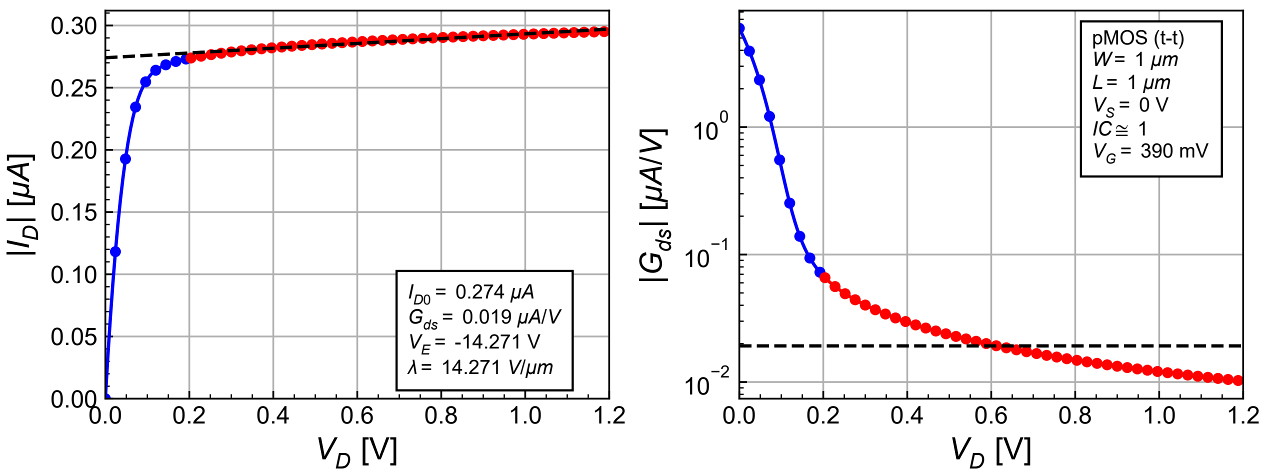
4.2.3 Extracting the CLM parameter

G_{ds} = 0.019 $\mu A/V$

I_{D0} = 0.274 μA

V_E = -14.271 V

λ = 14.271 $V/\mu m$



We get a smaller output conductance than what we got for the nMOS transistor.

Table 4.4: CLM parameters extracted for the medium-channel transistor in moderate inversion.

	W	Weff	L	Leff	IC	Gds	ID0	VE	lambda
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1	4.623e-09	2.810e-07	-6.078e+01	6.078e+06
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1	1.920e-08	2.741e-07	-1.427e+01	1.427e+07

4.3 Noise

In this section we will extract the flicker noise parameters to be used with sEKV and check the white noise power spectral desnity (PSD). We reuse the flicker noise model from EKV 2.6, where the input (gate) referred PSD is given by

$$S_{nin,fl}(f) = \frac{KF}{W_{eff}\, L_{eff}\, C_{ox}\; f^{AF}} \tag{4.5}$$

In this model the flicker noise is assumed to scale as $1/C_{ox}$, which is correct if the noise follows the the Hooge model (i.e. originates from mobility fluctuations). In the case of the Mc Worther model (i.e. flicker noise originating from traps in Si-SiO$_2$ interface and in the oxyde), the PSD scales as C_{ox}^2. Despiet the flicker noise is usually domanted by the trapping mechanism, we will keep the above model with a $1/C_{ox}$ scaling.

In EKV , we like to rewrite the flicker noise PSD like the thermal noise in terms of a input-referred noise resistance

$$S_{nin,fl}(f) = 4kT\, R_{nin,fl}(f) \tag{4.6}$$

where

$$R_{nin,fl}(f) = \frac{\rho}{W_{eff}\, L_{eff}\, f^{AF}} \tag{4.7}$$

with

$$\rho = \frac{KF}{4kT\, C_{ox}} \tag{4.8}$$

Note that the flicker noise parameter have some weird units. Indeed, KF is in $A \cdot V \cdot s^{2-AF}$ and ρ is in $V \cdot m^2/(A \cdot s^{AF})$. If $AF = 1$, like it is often the case, then KF is in $A \cdot V \cdot s$ and ρ is in $V \cdot m^2/(A \cdot s)$.

To extract the noise parameters, we use a common-source stage loaded by a noiseless resistor. We first will set the bias condition in terms of IC and calculate the input-referred white noise to compare it to the result obtained from the PSP simulations.

4.3.1 Setting bias conditions

Having extracted n, $I_{spec\square}$ and V_{T0}, we can impose the inversion coefficient and calculate the corresponding gate voltage V_G. We nee to make sure the transistor remains in saturation.

$W = 1\ \mu m$

$L = 1\ \mu m$

$IC = 1$

$I_D = 0.228\ \mu A$

$V_G = 0.390\ V$

$V_S = 0.000\ V$

$G_m = 4.420\ \mu A/V$

$\gamma_n = 0.693$

$R_{n,th} = 156.871\ k\Omega$

$S_{n,th} = 2.600\text{e-}15\ V^2/Hz$

$V_{n,th} = 50.993\ nV/\sqrt{Hz}$

$A_v = 10$

$R_L = 2262.662\ k\Omega$

$V_{DD} = 1.500\ V$

$V_{RL} = 0.515\ V$

$V_{DS} = 0.985\ V$

$V_{DSsat} = 0.116\ V$

```
The transistor is biased in the saturation region
```

4.3.2 Extract operating point information

We can extract the values of the PSP noise parameters from the operating point informations.

$V_{n,th} = 67.321\ nV/\sqrt{Hz}$ (PSP)

$f_k = 118.436\ kHz$ (PSP)

$KF = 8.371\text{e-}24\ VAs$ (PSP)

$\rho = 0.033\ Vm^2/(As)$ (PSP)

$AF = 1.000$ (PSP)

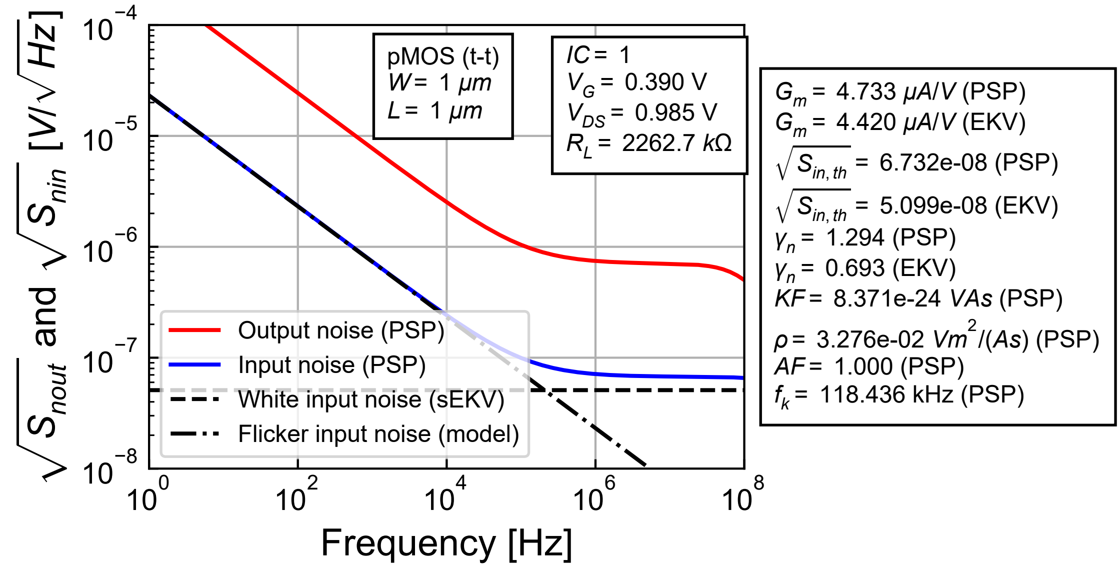
$R_{n,th} = 273.415\ k\Omega$ (PSP)

$\gamma_n = 1.294$ (PSP)

	Weff	Leff	IDS	Gm	Gds	Snidth	Vninth	Snidfl @ 1Hz	Vninfl @
Mp	9.700e-07	1.043e-06	2.417e-07	4.733e-06	1.020e-08	1.015e-25	6.732e-08	1.203e-20	7.326e-07

4.3.3 Simulating noise PSD

We can now simulate the PSD and check against the EKV model.



The flicker noise parameters are given by

Table 4.6: Extraction of the noise parameters for the medium-channel transistor.

	W	Weff	L	Leff	IC	KF	AF	rho	Comment
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1	8.726e-24	1.000e+00	3.416e-02	moderate
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1	8.371e-24	1.000e+00	3.276e-02	moderate

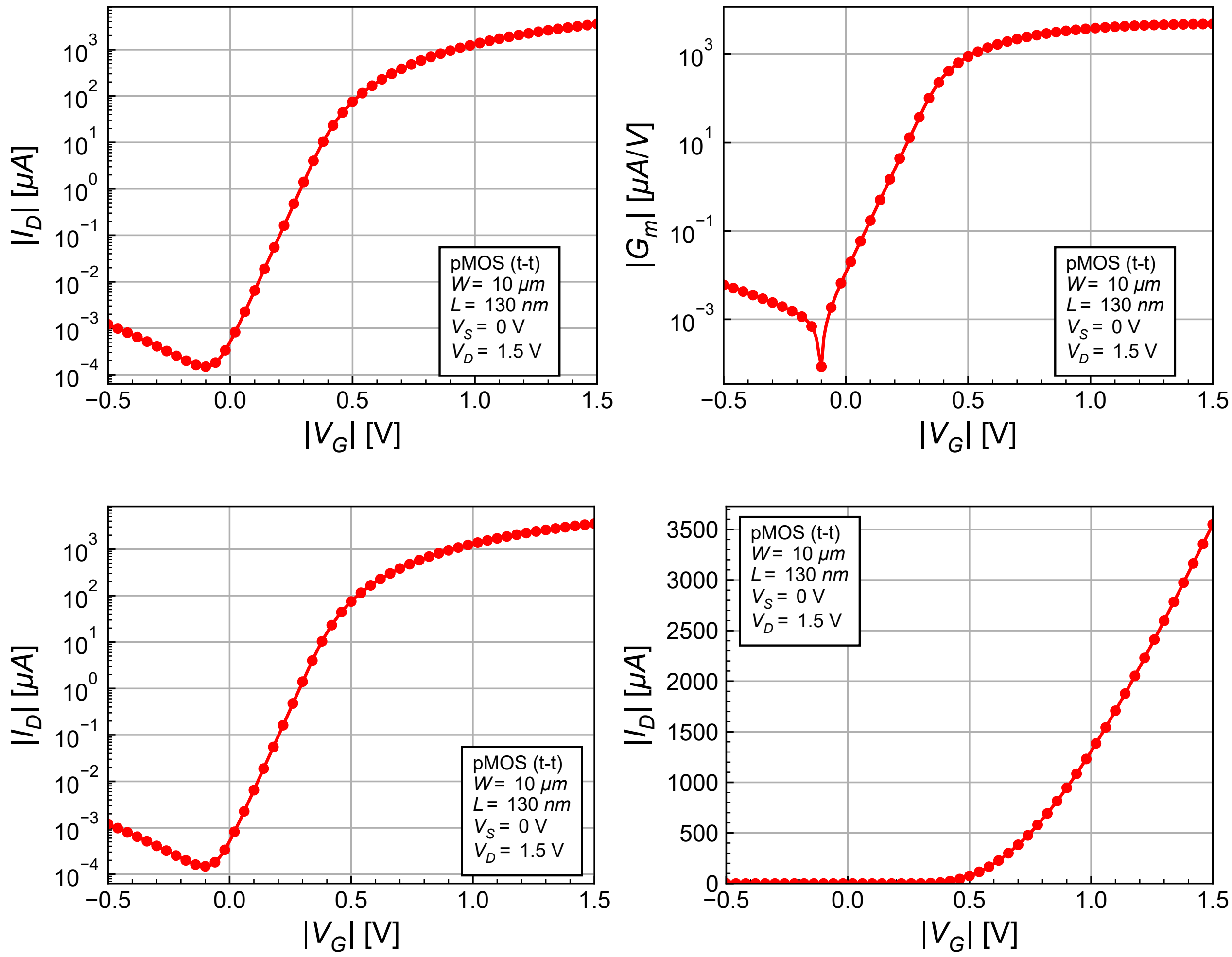
5 Short-channel parameters

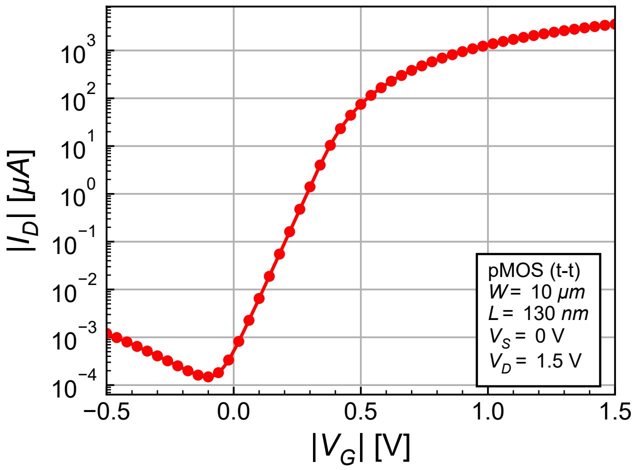
5.1 DC Transfer Characteristic Parameters

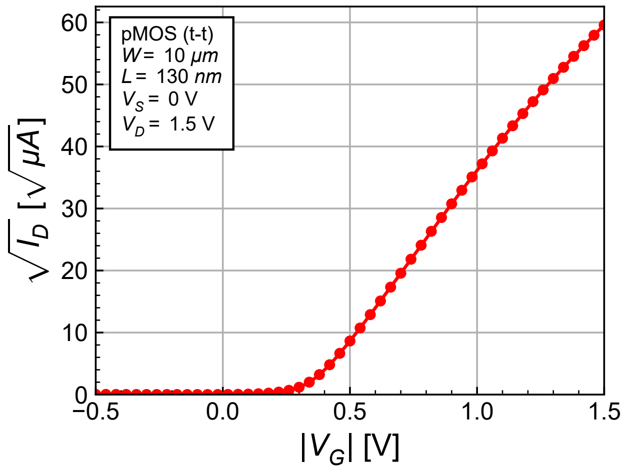
5.1.1 Generating the data

5.1.2 Importing and plotting the data

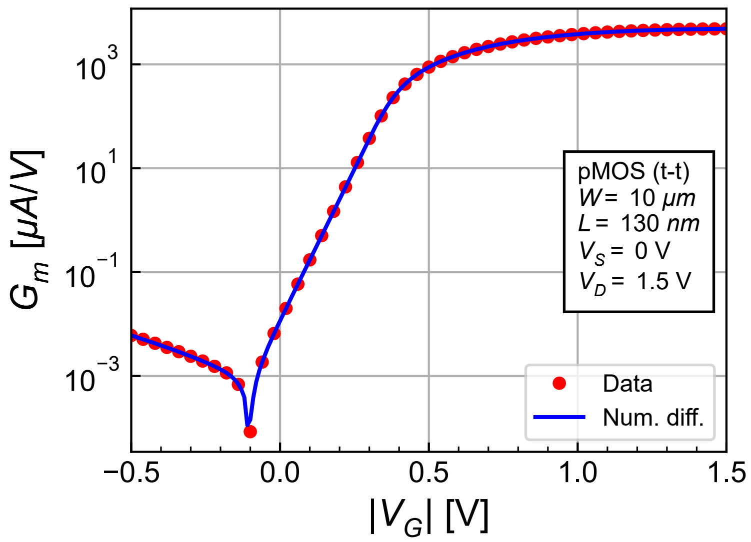
5.1.2.1 I_D and G_m versus V_G





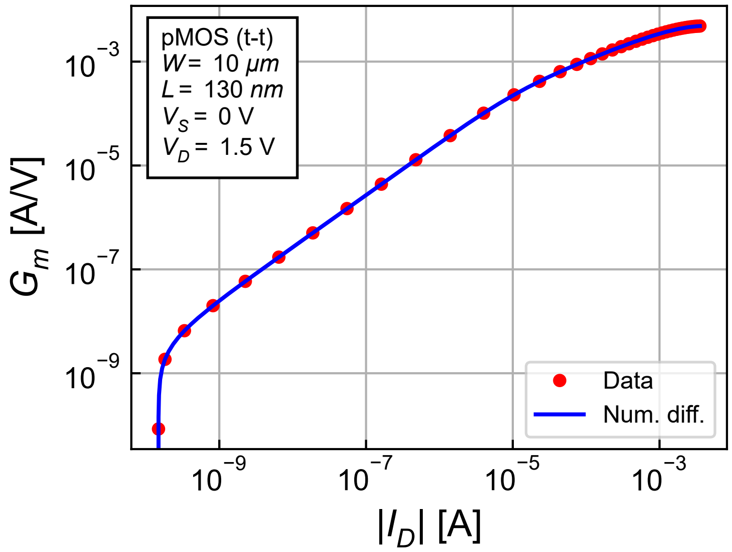


5.1.2.2 G_m-V_G

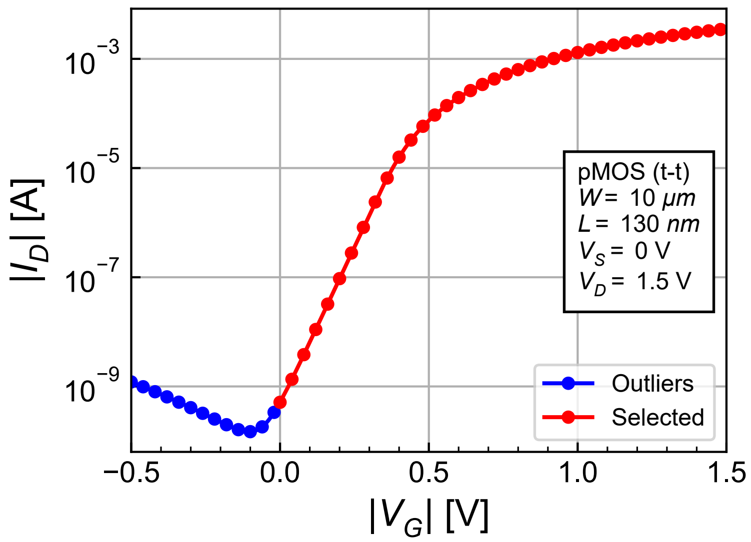


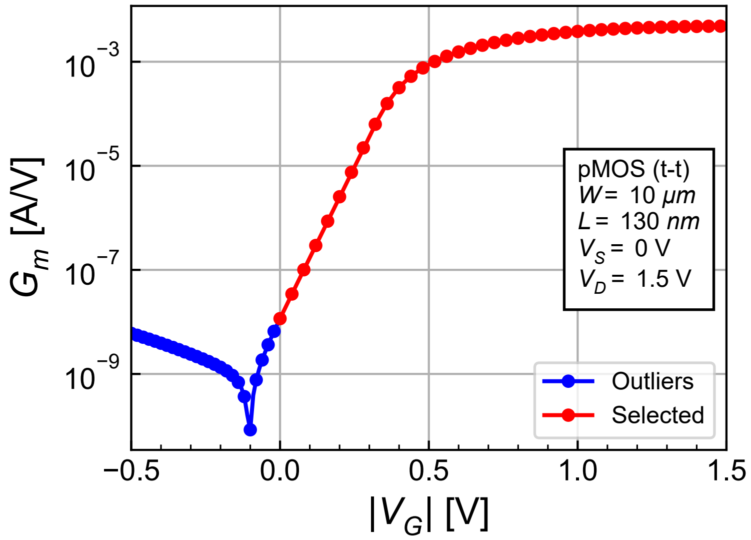
We see that the transconductance obtained by differentiating the large-signal I_D-V_G characteristic is equal to the transconductance extracted from the PSP model. We will keep the value extracted from the PSP model.

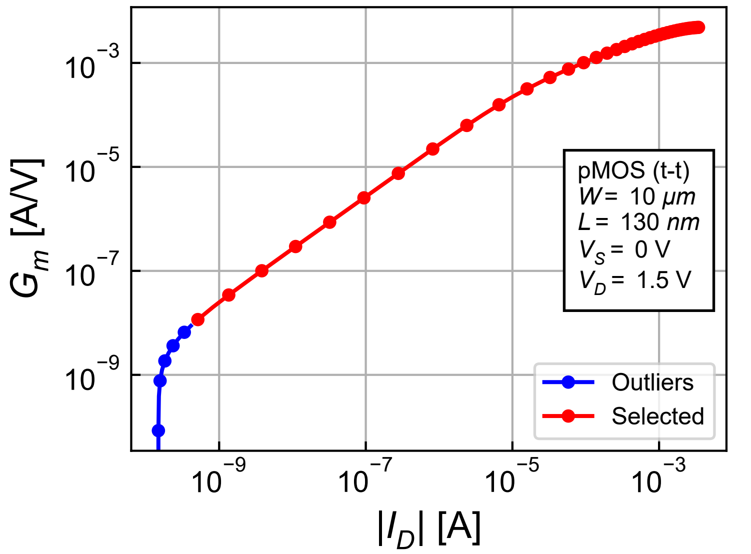
5.1.2.3 G_m-I_D



5.1.2.4 Filtering the outliers







5.2 Direct extraction with $\lambda_c = 0$

5.2.1 Slope factor n and I_{spec} extraction

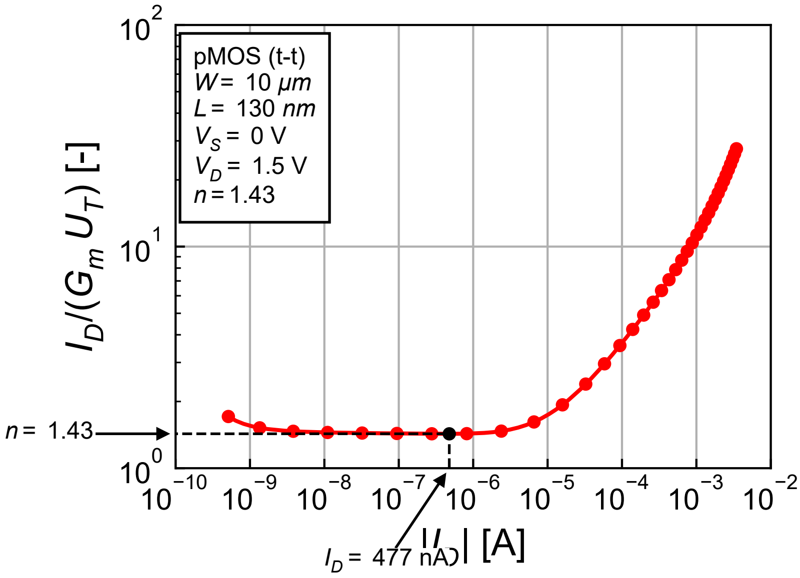
The gate transconductance in weak inversion and saturation is given by

$$G_m = \frac{I_D}{n\,U_T}. \tag{5.1}$$

So if we plot $I_D/(G_m\,U_T)$ we should see a plateau in weak inversion the value of which is equal to the slope factor n.

$n = 1.43$

$I_{D,ext} = 477.12\ nA$



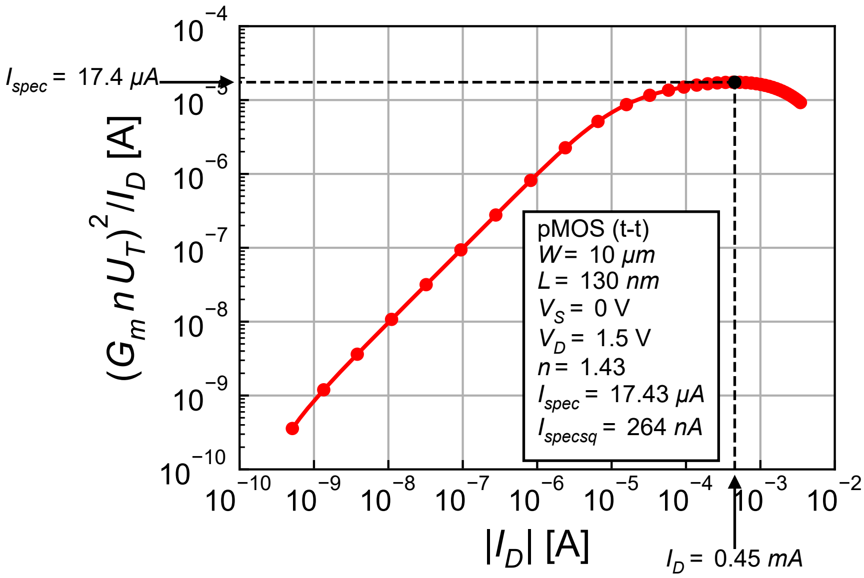
$W_{eff} = 9.970\ \mu m$

$L_{eff} = 150.802\ nm$

$I_{spec} = 17.428\ \mu A$

$I_{spec\square} = 264\ nA$

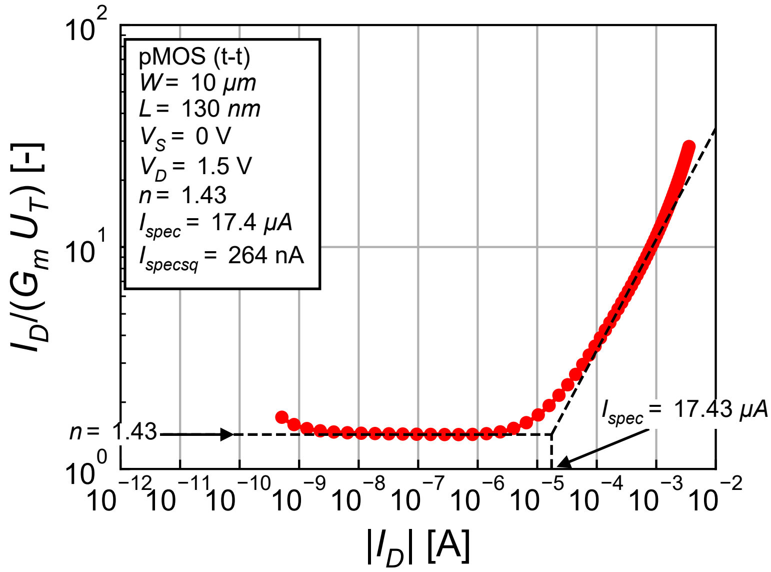
$I_{D,ext} = 0.452\ mA$



$n = 1.43$

$I_{spec} = 17.428\ \mu A$

$I_{spec\square} = 264\ nA$



Having extracted n and I_{spec}, we can now plot the normalized G_m/I_D function.

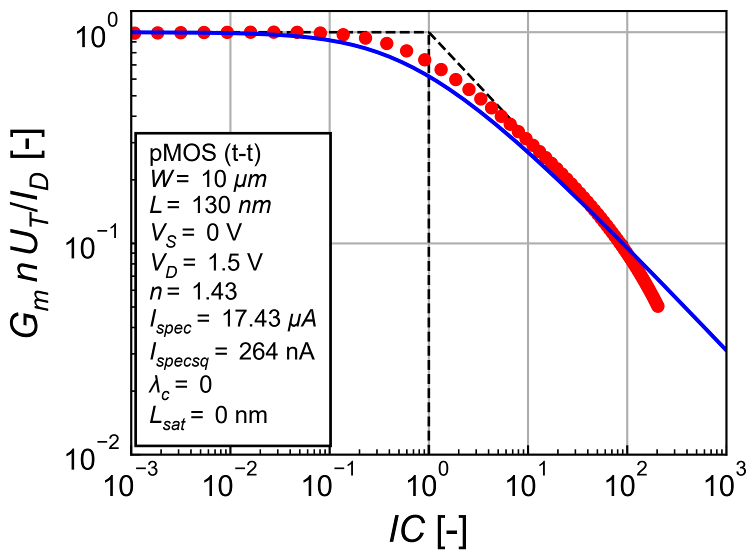
$n = 1.43$

$I_{spec} = 17\ \mu A$

$I_{spec\square} = 264\ nA$

$\lambda_c = 0$

$L_{sat} = 0$



The fit is reasonable over the entire IC span. There is a strange bump in the moderate inversion which comes from the simulation data. There is some discrepancy in the moderate inversion region which is due to the mobility reduction due to the vertical field appearing for $IC > 10^2$. The latter can be accounted for by using the λ_c parameter which is normally used for modeling the effect of velocity saturation in short-channel transistor but can also be used to correct the effect of mobility reduction due to the vertical field appearing in long-channel transistors. We will not do this here since we want to extract the long-channel parameters keeping $\lambda_c = 0$, but since we are mostly interested in the moderate inversion region, we can slightly increase I_{spec} to improve the fit in moderate inversion at the cost of a degradation in strong inversion.

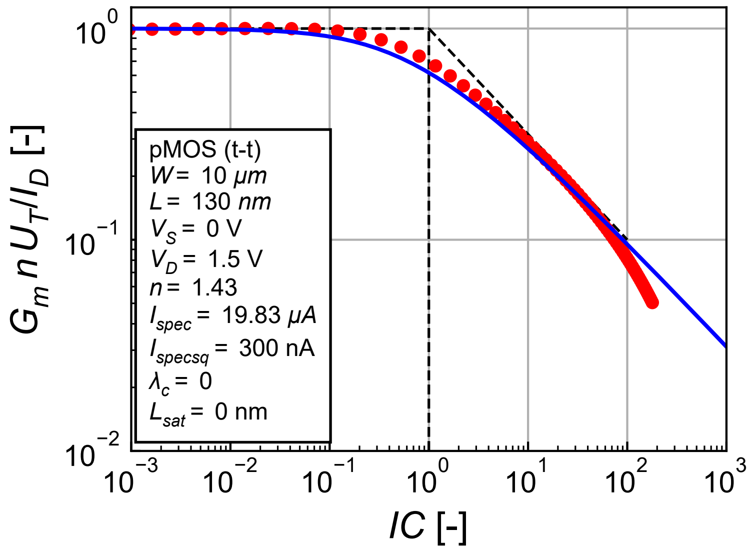
$n = 1.43$

$I_{spec} = 20\ \mu A$

$I_{spec\square} = 300\ nA$

$\lambda_c = 0$

$L_{sat} = 0$



The fit is now better in moderate inversion but less in strong inversion. This is due to mobility reduction due to the vertical field an effect that is not accounted for in the model. However, we will keep the new values since it is a good trade-off between moderate and strong inversion.

5.2.2 Threshold voltage extraction

We can extract the threshold voltage in weak inversion (assuming $V_S = 0$) from the normalized current (inversion coefficient) given by

$$IC = e^{\frac{V_G - V_{T0}}{nU_T}}. \tag{5.2}$$

We can now plot

$$V_{T0} = V_G - nU_T \ln(IC) \tag{5.3}$$

to extract the threshold voltage.

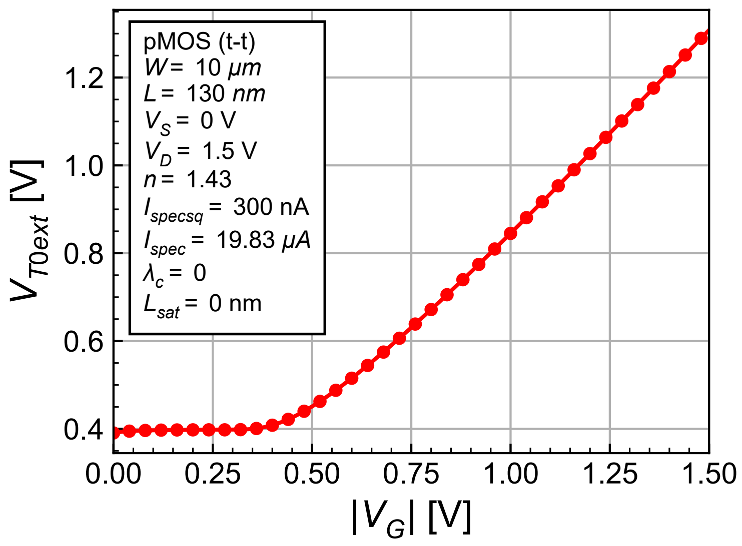
$n = 1.43$

$I_{spec} = 20\ \mu A$

$I_{spec\square} = 300\ nA$

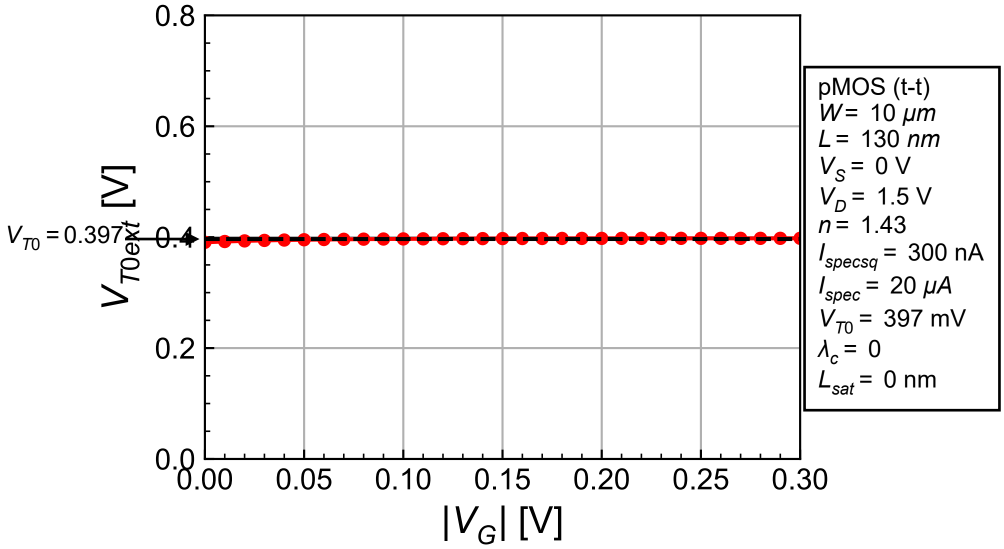
$\lambda_c = 0$

$L_{sat} = 0$



We see a plateau in weak inversion where we can average its value to get the threshold voltage in weak inversion.

$V_{T0,wi} = 397$ mV



The threshold voltage for this wide and short device is smaller than what is given in the documentation giving a typical-typical $V_{TH} \cong 500\,mV$ for $W = 10\,\mu m$ and $L = 130\,nm$.

We can now plot the I_D-V_G for this threshold voltage.

$n = 1.43$

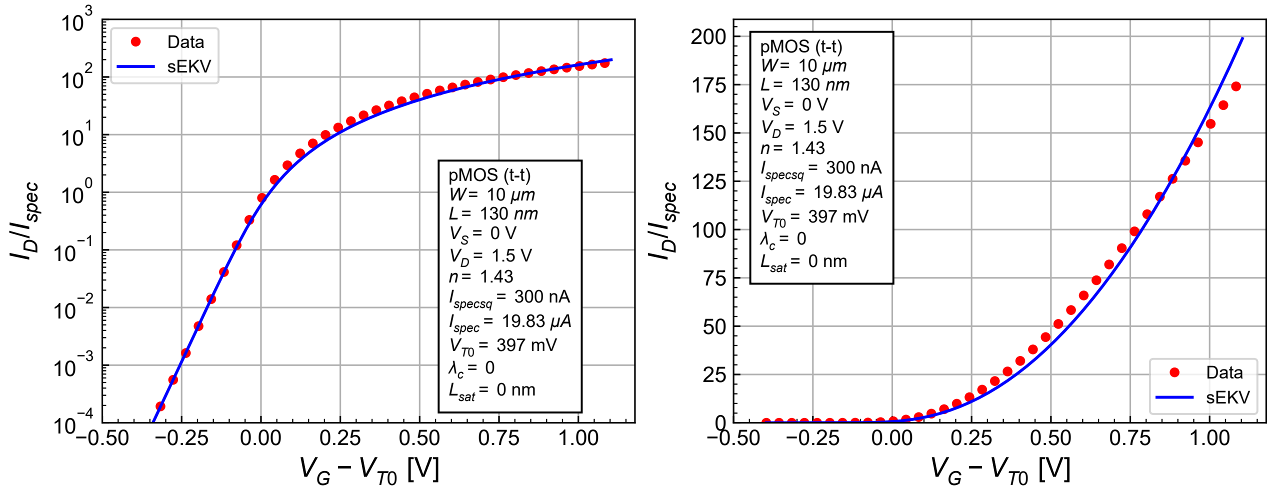
$I_{spec} = 19834\ nA$

$I_{spec\square} = 300\ nA$

$\lambda_c = 0$

$L_{sat} = 0$

$V_{T0} = 397$ mV



We get a reasonable fit across all regions.

5.2.3 Summary

$n = 1.43$

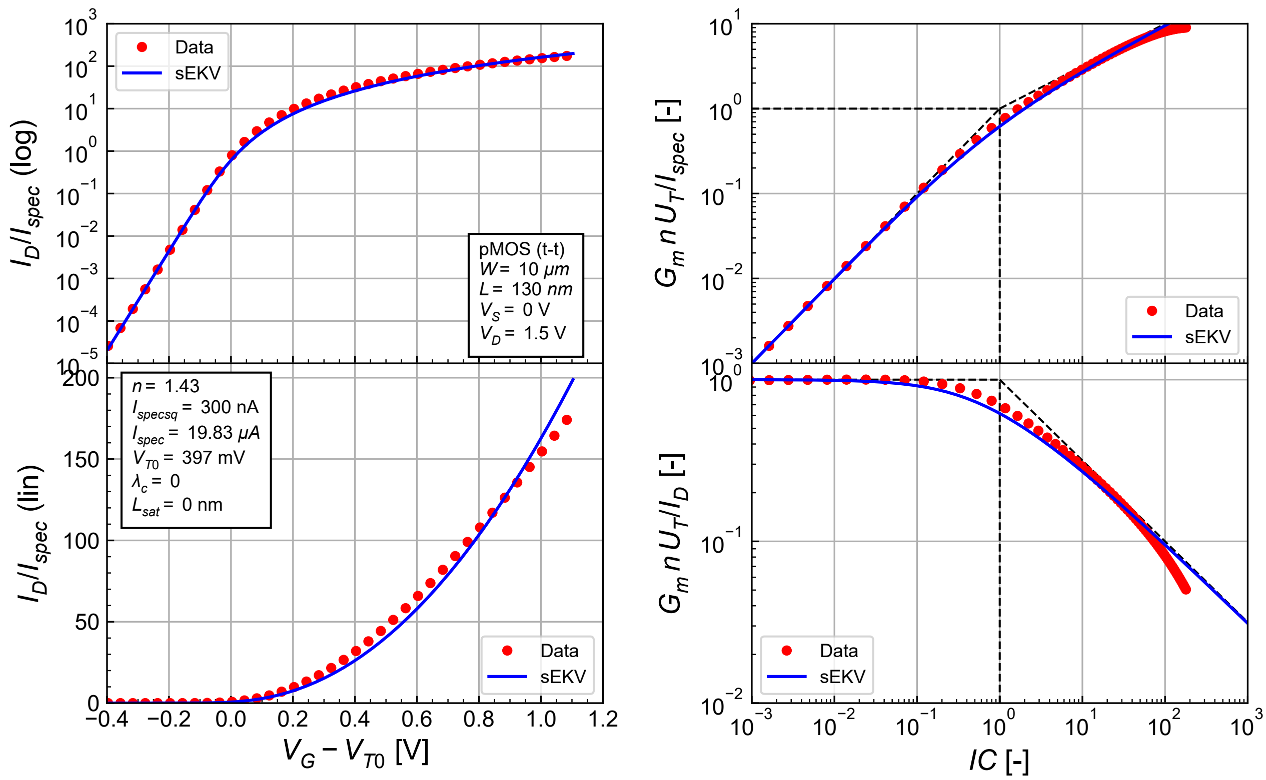
$I_{spec} = 19834\ nA$

$I_{spec\square} = 300\ nA$

$V_{T0} = 397$ mV

$\lambda_c = 0$

$L_{sat} = 0$



The fit is reasonable for the short-channel transistor accounting for the fact that $\lambda_c = 0$.

5.2.4 Direct extraction with $\lambda_c > 0$

5.2.4.1 Slope factor n extraction

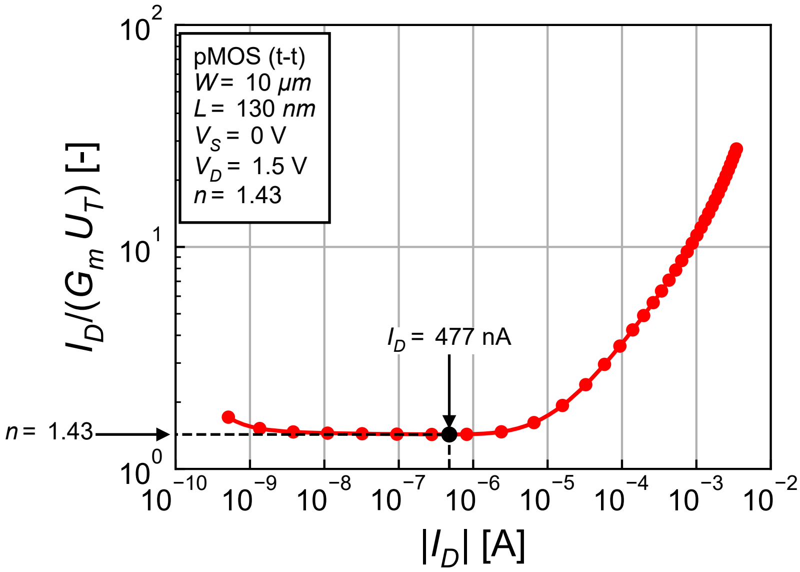
The gate transconductance in weak inversion and saturation is given by

$$G_m = \frac{I_D}{n\,U_T}. \tag{5.4}$$

So if we plot $I_D/(G_m)\,U_T$ we should see a plateau in weak inversion the value of which is equal to the slope factor n.

$n = 1.43$

$I_{D,ext} = 477.12\ nA$



5.2.4.2 Specific current I_{spec} extraction

On the other hand the normalized G_m/I_D function for a long-channel transistor in strong inversion and saturation is given by

$$\frac{G_m\,n\,U_T}{I_D} = \frac{1}{\sqrt{IC}} = \sqrt{\frac{I_{spec}}{I_D}}. \tag{5.5}$$

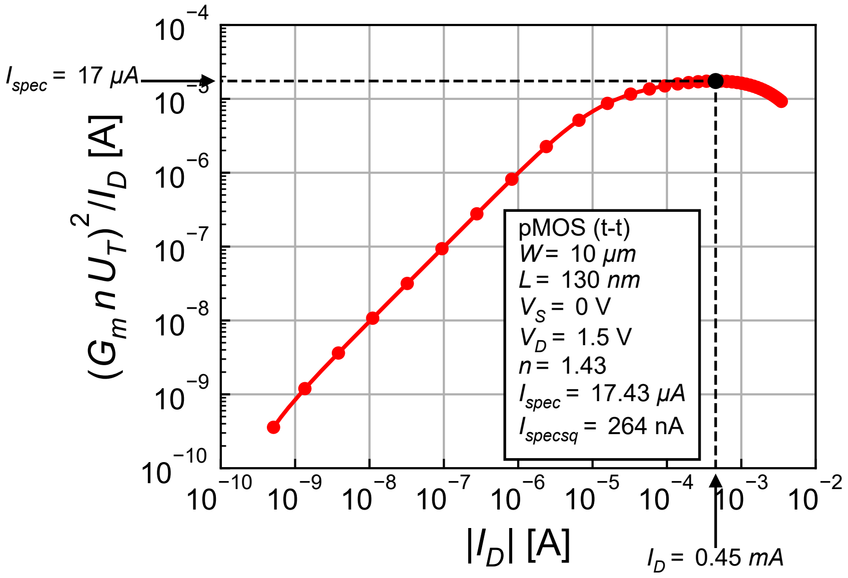
We can then plot $(G_m\,n\,U_T)^2/I_D$ which should find a maximum value equal to I_{spec}.

$n = 1.43$

$I_{spec} = 17.428\ \mu A$

$I_{spec\square} = 264\ nA$

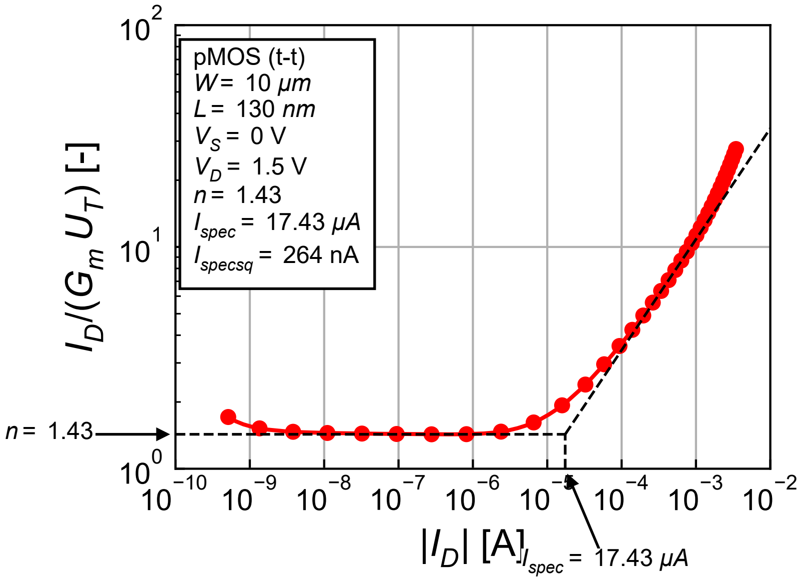
$I_{D,ext} = 0.452\ mA$



$n = 1.43$

$I_{spec} = 17\ \mu A$

$I_{spec\square} = 264\ nA$



5.2.4.3 Velocity saturation parameter λ_c extraction

We can extract λ_c by looking at the asymptote in very strong inversion. For a short-channel transistor in strong inversion and saturation, the normalized G_m/I_D is given by

$$\frac{G_m\, n\, U_T}{I_D} = \frac{1}{\lambda_c\, IC} = \frac{I_{spec}}{\lambda_c\, I_D}. \tag{5.6}$$

So if we plot $I_{spec}/(G_m\, n\, U_T)$ it will have a minimum at λ_c.

$n = 1.43$

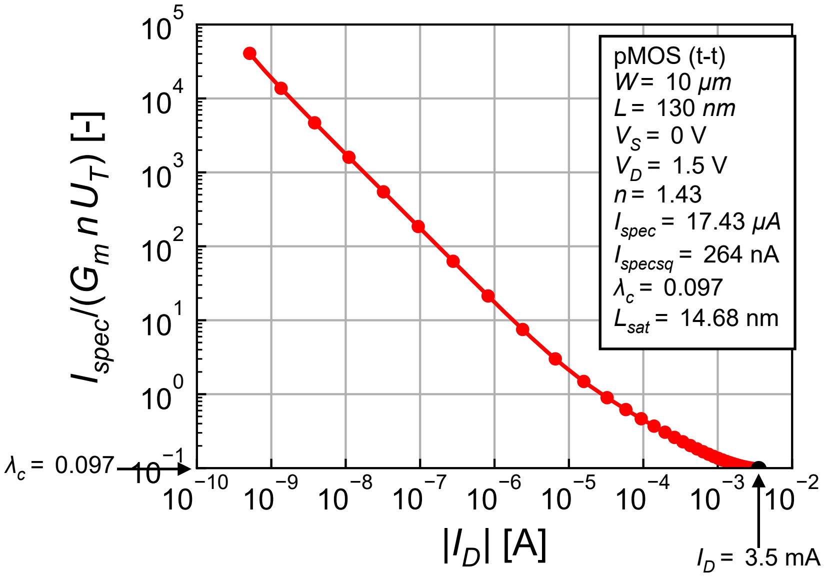
$I_{spec} = 17.428\ \mu A$

$I_{spec\square} = 264\ nA$

$\lambda_c = 0.097$

$L_{sat} = 14.681\ nm$

$I_{D,ext} = 3.550\ mA$



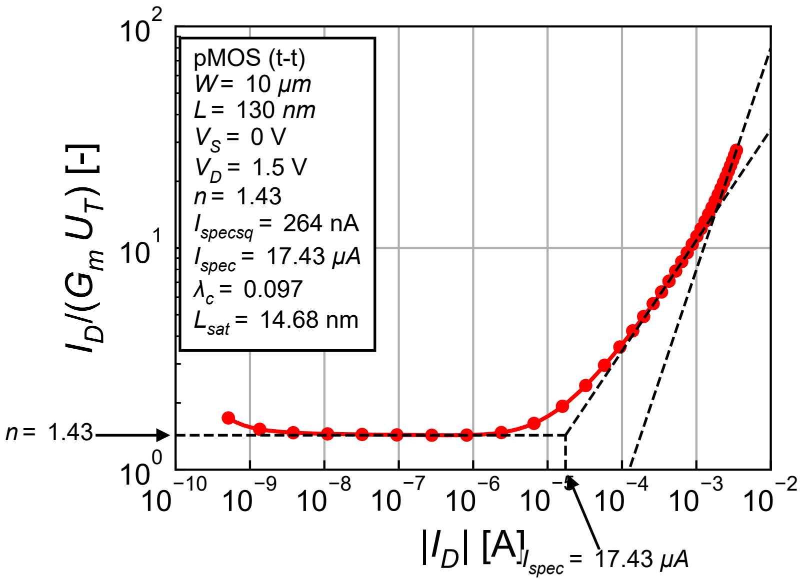
$n = 1.43$

$I_{spec} = 17.428\ \mu A$

$I_{spec\square} = 264\ nA$

$\lambda_c = 0.097$

$L_{sat} = 14.681\ nm$



We can now check the normalized G_m/I_D characteristic.

$n = 1.43$

$I_{spec} = 17428\ nA$

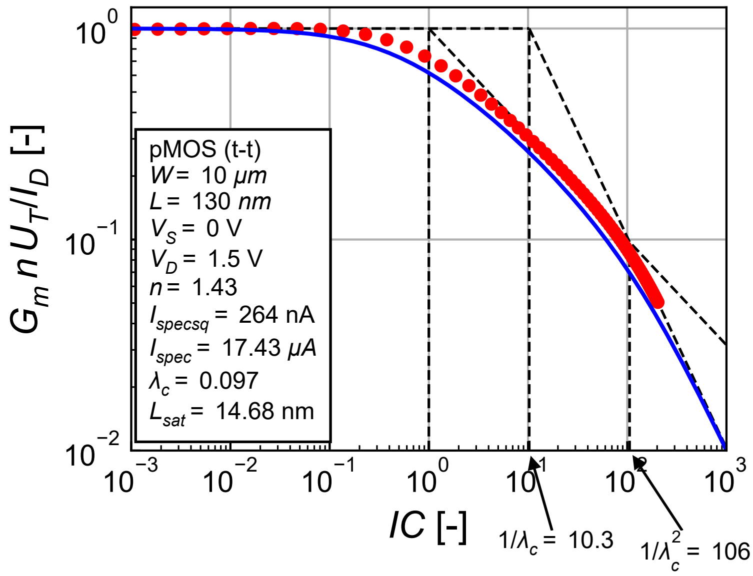
$I_{spec\square} = 264\ nA$

$\lambda_c = 0.097$

$1/\lambda_c = 10.27$

$1/\lambda_c^2 = 106$

$L_{sat} = 14.681\ nm$



The fit is not good. There is an offset with IC. We can increase the value of $I_{spec\square}$ to shift the curve to the right.

$n = 1.43$

$I_{spec} = 26\ \mu A$

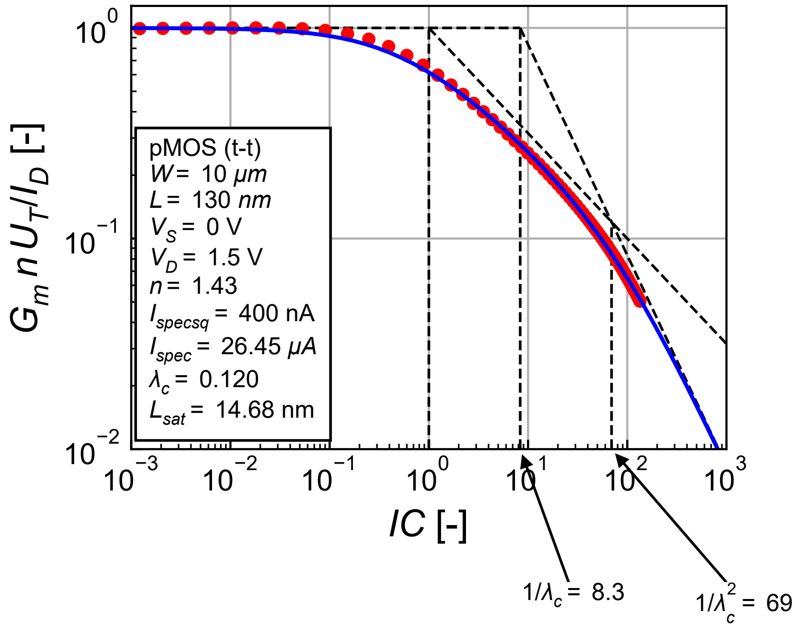
$I_{spec\square} = 400\ nA$

$\lambda_c = 0$

$1/\lambda_c = 8.33$

$1/\lambda_c^2 = 69$

$L_{sat} = 14.681\ nm$



The fit is now much better, offering a good trade-off between moderate and strong inversion.

5.2.4.4 Threshold voltage extraction

$n = 1.43$

$I_{spec} = 26.445\ \mu A$

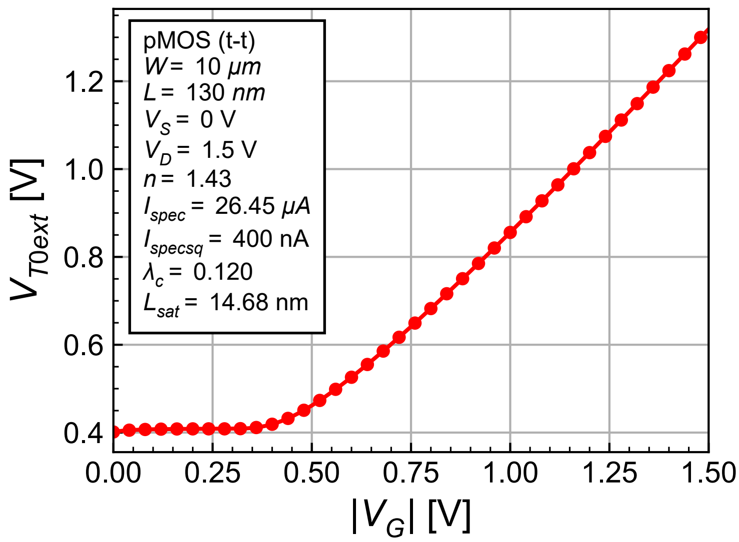
$I_{spec\square} = 400\ nA$

$\lambda_c = 0.120$

$1/\lambda_c = 8.333$

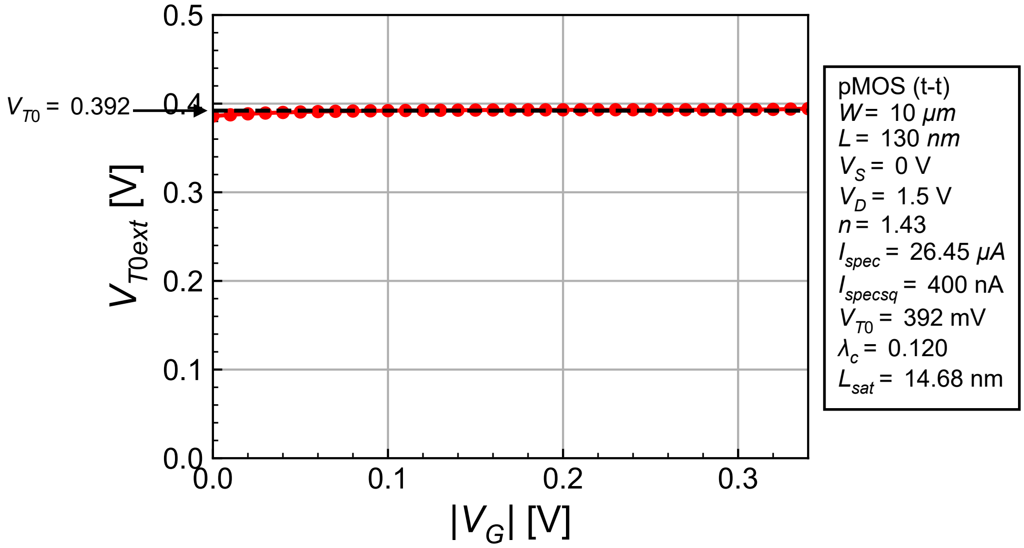
$1/\lambda_c^2 = 69.444$

$L_{sat} = 14.681\ nm$



We see a plateau in weak inversion where we can average its value to get the threshold voltage in weak inversion.

$V_{T0,wi} = 392$ mV



We can now check the I_D-V_G curves.

$n = 1.43$

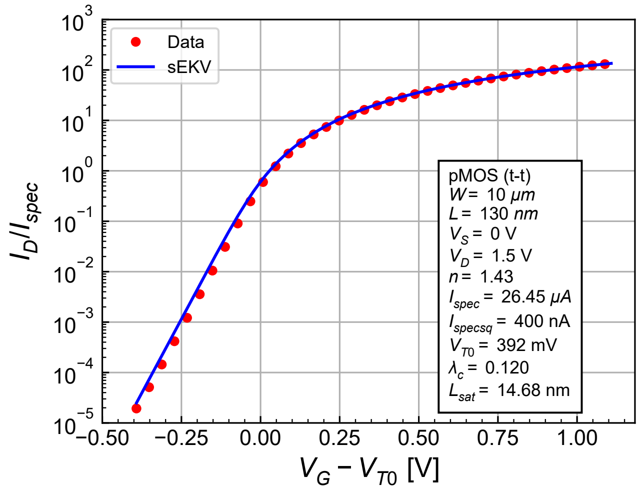
$I_{spec} = 26.445\ \mu A$

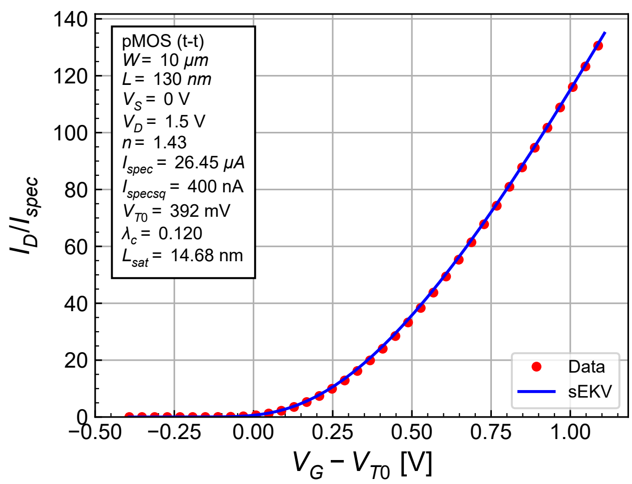
$I_{spec\square} = 400\ nA$

$V_{T0} = 392$ mV

$\lambda_c = 0.120$

$L_{sat} = 14.681\ nm$





We see that the threshold voltage is not correct. We can fine tune it manually.

$n = 1.43$

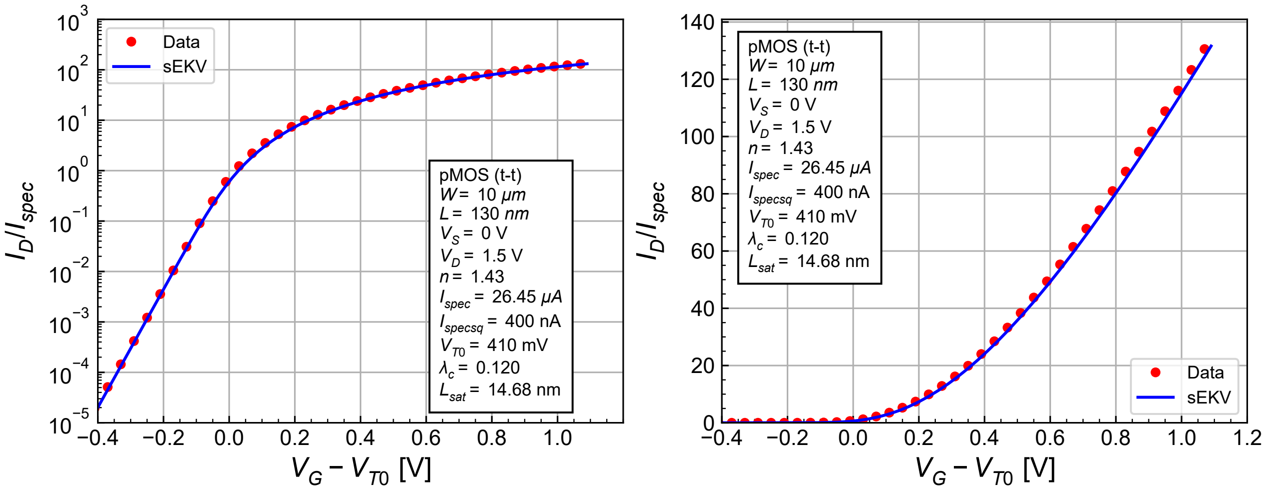
$I_{spec} = 26.445\ \mu A$

$I_{spec\square} = 400\ nA$

$V_{T0} = 410$ mV

$\lambda_c = 0.120$

$L_{sat} = 14.681\ nm$



We now have a very good fit of the I_D-V_G characteristic.

5.2.4.5 Summary

$n = 1.43$

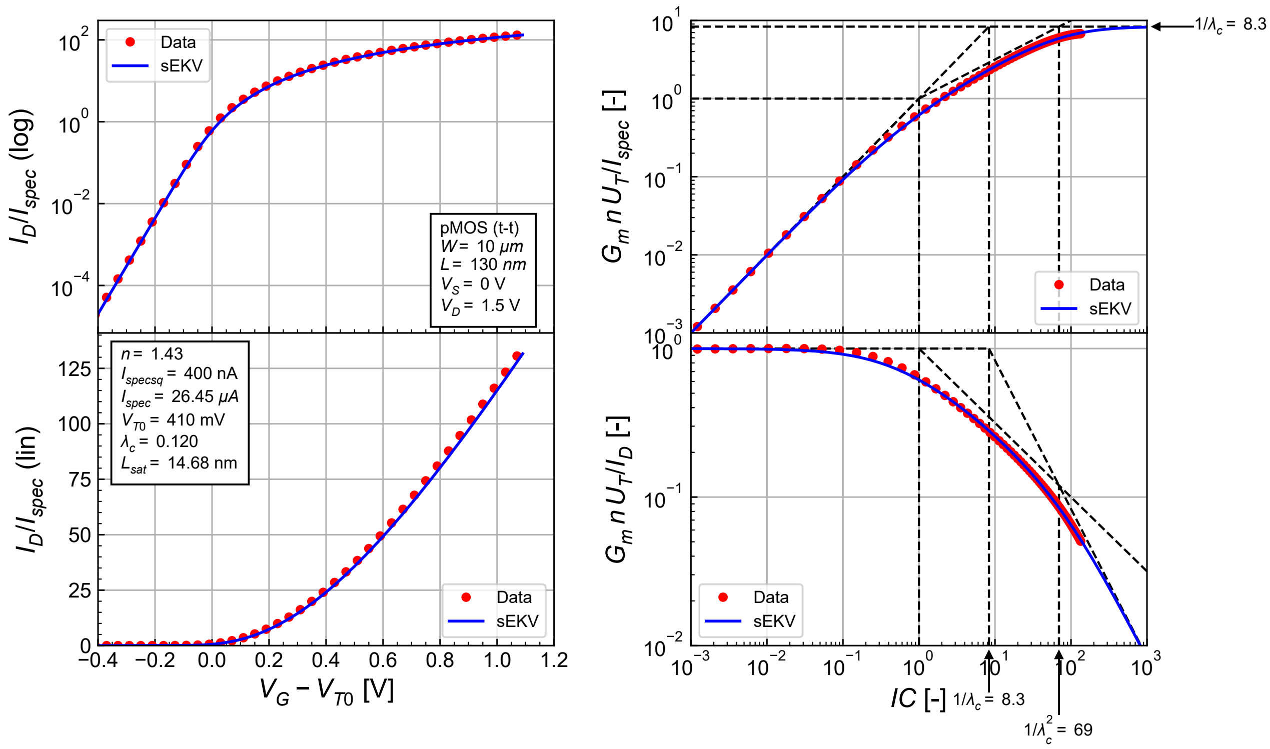
$I_{spec} = 26.445\ \mu A$

$I_{spec\square} = 400\ nA$

$V_{T0} = 410$ mV

$\lambda_c = 0.120$

$L_{sat} = 14.681\ nm$



We finally get a reasonable fit of all characteristics.

Table 5.1: Direct extraction of the sEKV parameters for the short-channel transistor wi

	W	Weff	L	Leff	n	Ispecsq	VT0	lambdac	Lsat
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.800e-07	3.568e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.915e-07	3.569e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.227e+00	2.000e-07	3.569e-01	6.800e-02	6.831e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.230e+00	2.200e-07	3.612e-01	0.000e+00	0.000e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.230e+00	2.446e-07	3.655e-01	0.000e+00	0.000e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.277e+00	2.600e-07	3.655e-01	7.600e-02	1.170e
short	1.000e-05	9.970e-06	1.300e-07	1.508e-07	1.430e+00	4.000e-07	4.100e-01	1.200e-01	1.468e

5.2.5 Extraction using optimization

5.2.5.1 Specific current I_{spec} and λ_c extraction

We can extract the slope factor n, the specific current I_{spec} and the velocity saturation parameter λ_c using curve-fitting.

$n = 1.45$

$I_{spec} = 31.718\ \mu A$

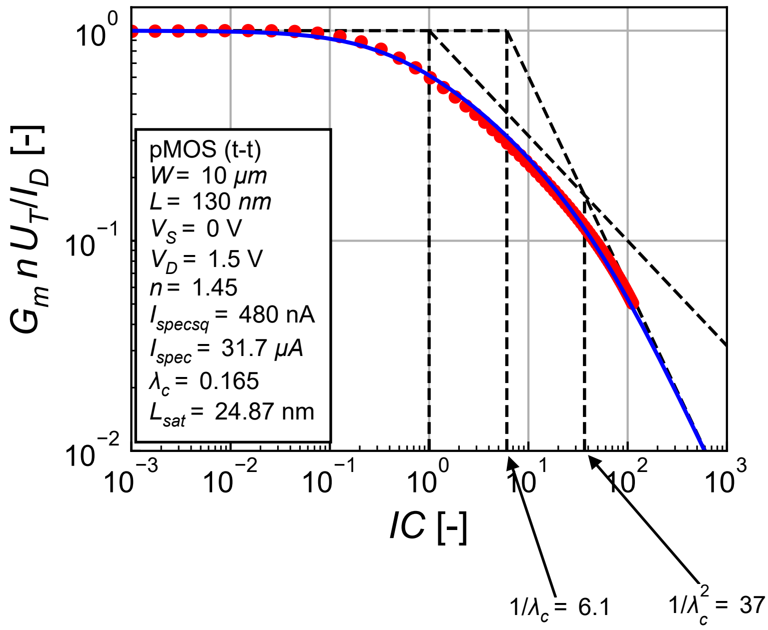
$I_{spec\square} = 480\ nA$

$\lambda_c = 0.165$

$1/\lambda_c = 6.06$

$1/\lambda_c^2 = 37$

$L_{sat} = 24.869\ nm$



We get a good fit across all regions.

5.2.5.2 Threshold voltage extraction

$n = 1.45$

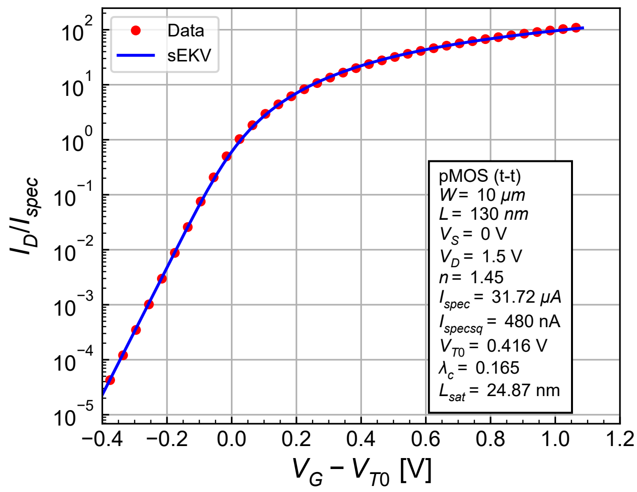
$I_{spec} = 31.718\ \mu A$

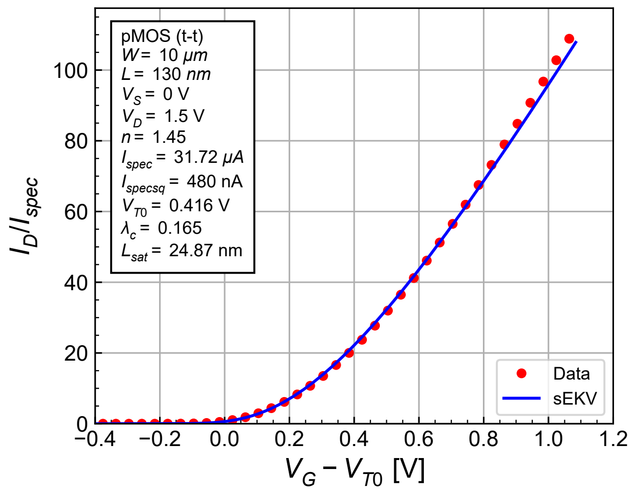
$I_{spec\square} = 480\ nA$

$V_{T0} = 416$ mV

$\lambda_c = 0.165$

$L_{sat} = 24.869\ nm$





We finally get a very good fit!

5.2.5.3 Summary

$n = 1.45$

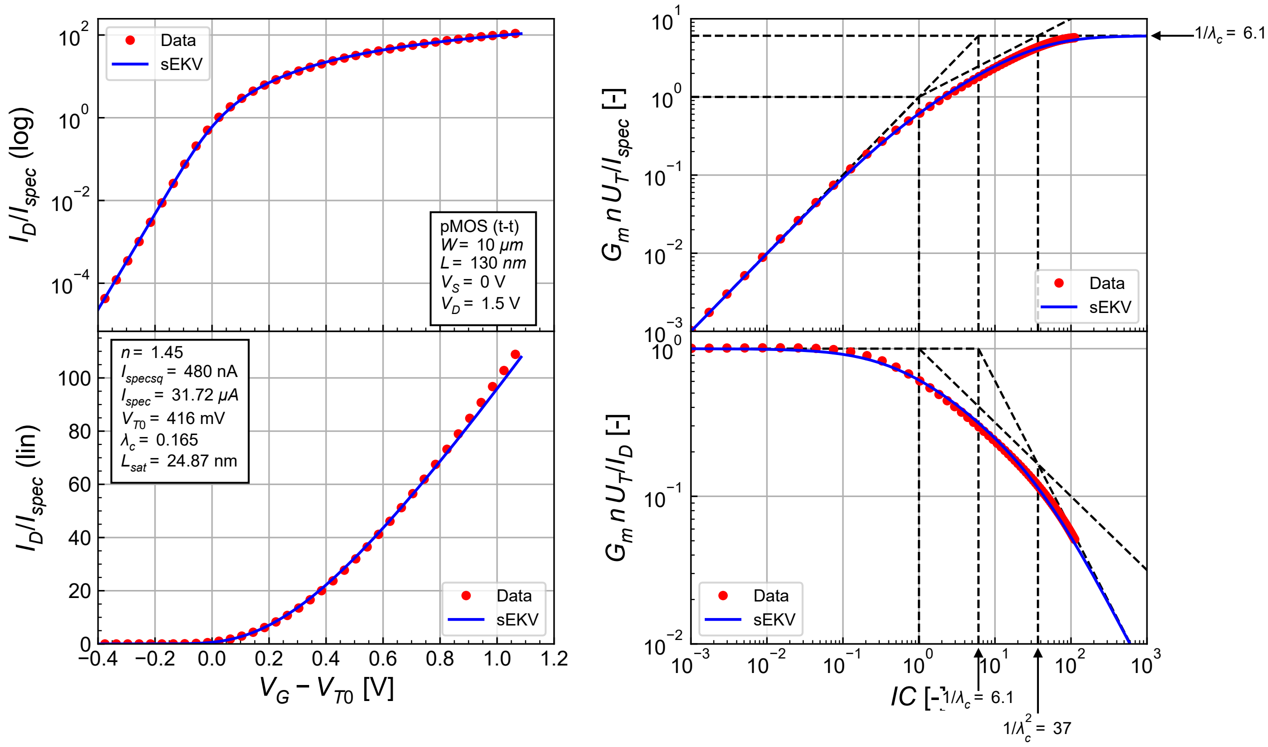
$I_{spec} = 31.718\ \mu A$

$I_{spec\square} = 480\ nA$

$V_{T0} = 416$ mV

$\lambda_c = 0.165$

$L_{sat} = 24.869\ nm$



We have an overall very good fit.

Table 5.2: Extraction of the sEKV parameters by optimization for the short-channel tra
$\lambda_c > 0$.

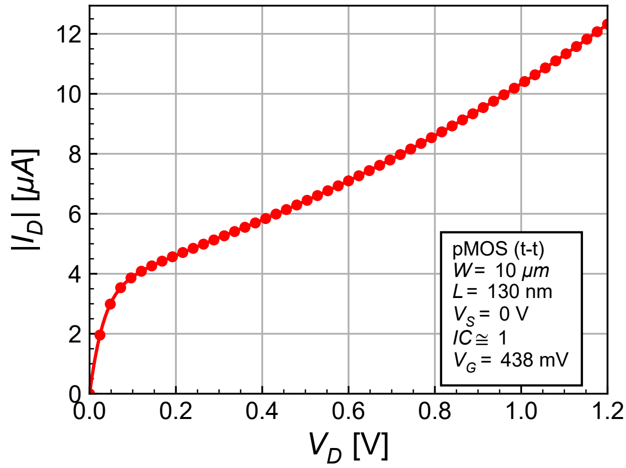
	W	Weff	L	Leff	n	Ispecsq	VT0	lambdac	Lsat
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.800e-07	3.568e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.220e+00	1.915e-07	3.569e-01	0.000e+00	0.000e
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1.227e+00	2.000e-07	3.569e-01	6.800e-02	6.831e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.230e+00	2.200e-07	3.612e-01	0.000e+00	0.000e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.230e+00	2.446e-07	3.655e-01	0.000e+00	0.000e
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1.277e+00	2.600e-07	3.655e-01	7.600e-02	1.170e
short	1.000e-05	9.970e-06	1.300e-07	1.508e-07	1.430e+00	4.000e-07	4.100e-01	1.200e-01	1.468e
short	1.000e-05	9.970e-06	1.300e-07	1.508e-07	1.449e+00	4.798e-07	4.158e-01	1.649e-01	2.487e

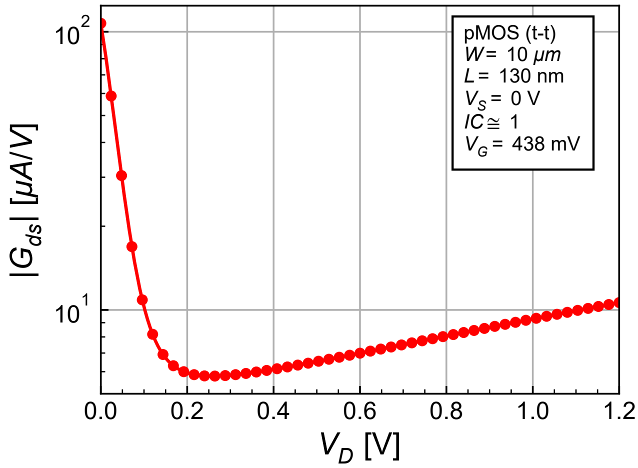
5.3 Output characteristic

5.3.1 Generating the data

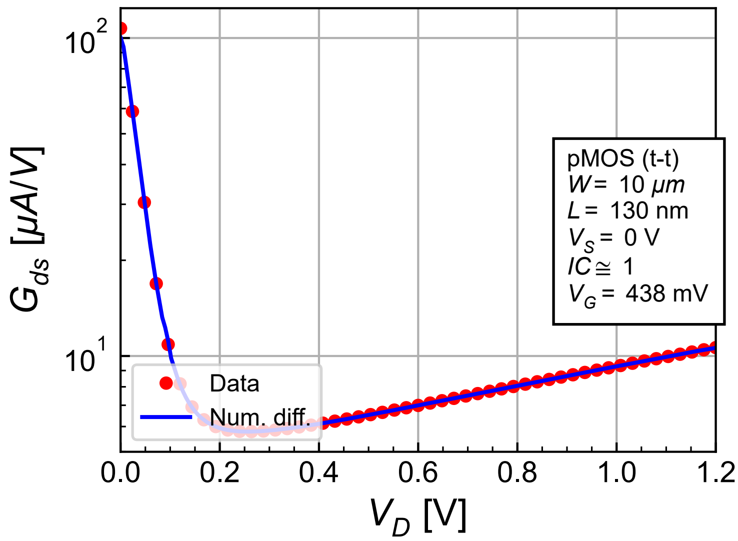
5.3.2 Importing and plotting the data

5.3.2.1 I_D and G_{ds} versus V_D

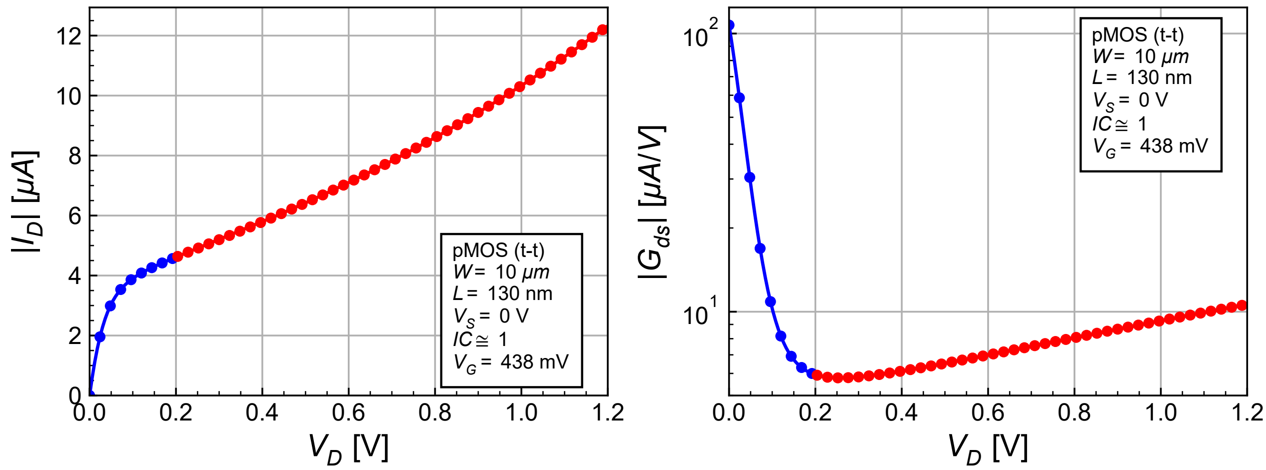




We see the effect of DIBL that will be difficult to fit with the CLM model only.



5.3.2.2 Filtering the outliers



5.3.2.3 Extracting the CLM parameter

G_{ds} = 7.630 $\mu A/V$

I_{D0} = 2.703 μA

V_E = -0.354 V

λ = 2.725 $V/\mu m$

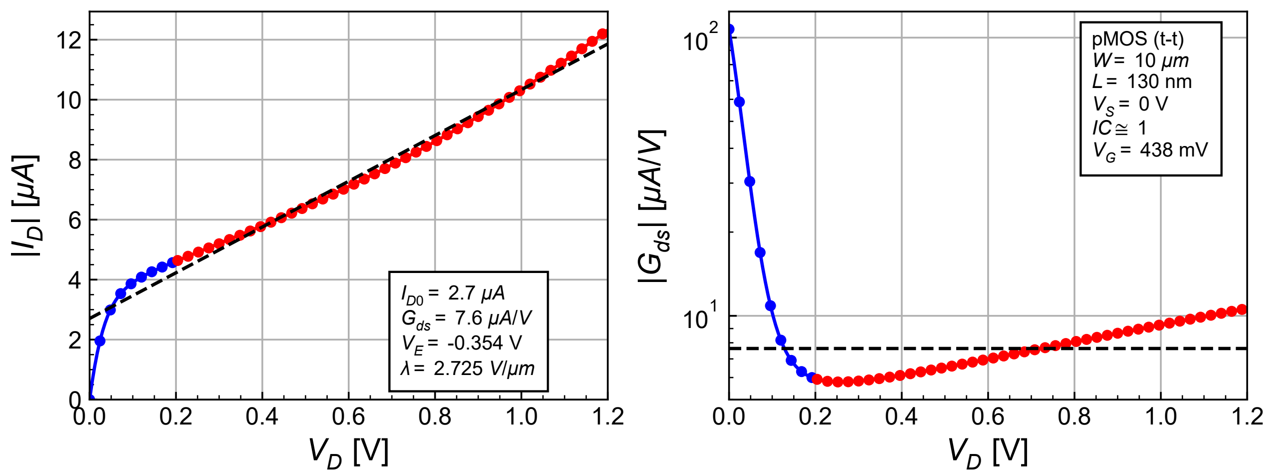


Table 5.3: CLM parameters extracted for the short-channel transistor in moderate inversion.

	W	Weff	L	Leff	IC	Gds	ID0	VE	lambda	C
long	1.000e-05	9.970e-06	1.000e-05	1.005e-05	1	4.623e-09	2.810e-07	-6.078e+01	6.078e+06	m
medium	1.000e-06	9.700e-07	1.000e-06	1.043e-06	1	1.920e-08	2.741e-07	-1.427e+01	1.427e+07	m
short	1.000e-05	9.970e-06	1.300e-07	1.508e-07	1	7.630e-06	2.703e-06	-3.543e-01	2.725e+06	m

5.4 Noise

In this section we will extract the flicker noise parameters to be used with sEKV and check the white noise power spectral density (PSD) for the short channel transistor. We first will set the bias condition in terms of IC and calculate the input-referred white noise to compare it to the result obtained from the PSP simulations.

5.4.1 Setting bias conditions

$W = 10\ \mu m$

$L = 130\ nm$

$IC = 1.0$

$I_D = 26.445\ \mu A$

$V_G = 0.438\ V$

$V_S = 0.000\ V$

$G_m = 441.888\ \mu A/V$

$\gamma_n = 0.806$

$R_{n,th} = 1.824\ k\Omega$

$S_{n,th} = 3.024\text{e-}17\ V^2/Hz$

$V_{n,th} = 5.499\ nV/\sqrt{Hz}$

$A_v = 10$

$R_L = 22.630\ k\Omega$

$V_{DD} = 1.800\ V$

$V_{RL} = 0.598\ V$

$V_{DS} = 1.202\ V$

$V_{DSsat} = 0.116\ V$

```
The transistor is biased in the saturation region
```

5.4.2 Extract operating point information

We can extract the values of the PSP noise parameters from the operating point informations.

$V_{n,th} = 6.781\ nV/\sqrt{Hz}$ (PSP)

$f_k = 8259.325\ kHz$ (PSP)

$KF = 8.801\text{e-}24\ VAs$ (PSP)

$\rho = 3.445\text{e-}02\ Vm^2/(As)$ (PSP)

$AF = 1.000$ (PSP)

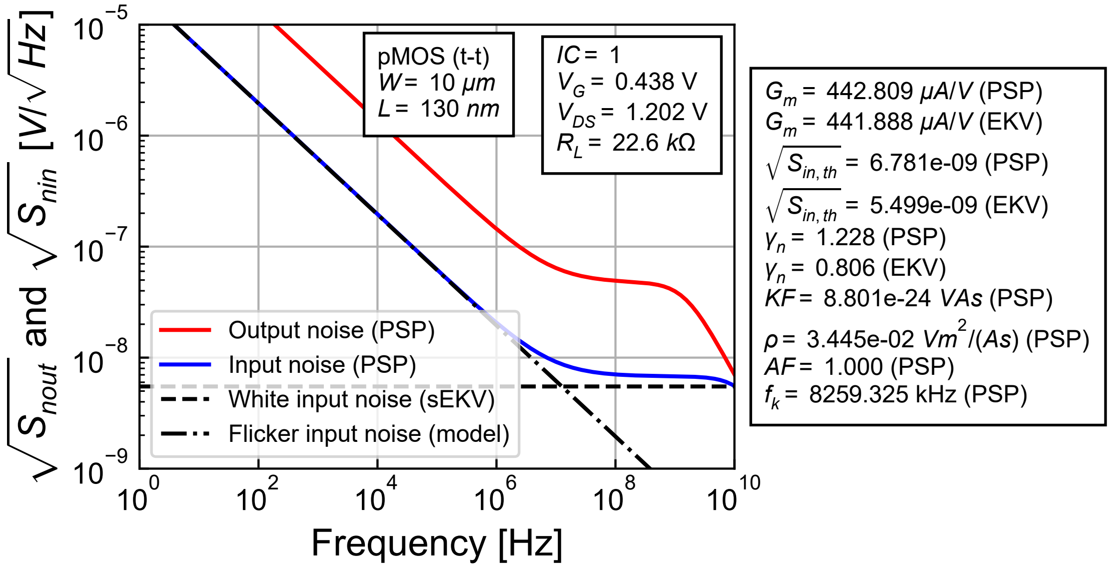
$R_{n,th} = 2.774\ k\Omega$ (PSP)

$\gamma_n = 1.228$ (PSP)

	Weff	Leff	IDS	Gm	Gds	Snidth	Vninth	Snidfl @ 1Hz	Vninfl @ 1kH
Mn	9.97E-06	1.51E-07	2.58E-05	4.43E-04	1.90E-05	9.02E-24	6.78E-09	7.45E-17	6.16E-07

5.4.3 Simulating noise PSD

We can now simulate the PSD and check against the EKV model.



The transconductance value from sEKV is very close to that of PSP. However, the thermal noise excess factor γ_n in PSP seems to be very large compared to the EKV value. This leads to a higher white noise for PSP compared to EKV.

The flicker noise parameter for the short-channel transistor is slightly larger than the values extracted for the long and medium transistors.

Table 5.5: Extraction of the noise parameters for the short-channel transistor.

	W	Weff	L	Leff	IC	KF	AF	rho	Comment
long	1.00E-05	9.97E-06	1.00E-05	1.00E-05	1	8.73E-24	1.00E+00	3.42E-02	moderate
medium	1.00E-06	9.70E-07	1.00E-06	1.04E-06	1	8.37E-24	1.00E+00	3.28E-02	moderate
short	1.00E-05	9.97E-06	1.30E-07	1.51E-07	1	8.80E-24	1.00E+00	3.44E-02	moderate

6 Extrinsic capacitances

6.1 Junction capacitances

The calculation of the junction capacitances depends on the value used for the **SWJUNCAP** parameter. In this PDK **SWJUNCAP** is equal to 3 for which the junction area AB, junction length of side-wall capacitance along the STI edge LS and junction length of the side-wall capacitance along the gate edge LG are calculated according to

$$AB = AS, \tag{6.1}$$
$$LS = PS - W_E, \tag{6.2}$$
$$LG = W_E, \tag{6.3}$$
$$\tag{6.4}$$

where AS is the source junction area and PS the total source junction perimeter and

$$AB = AD, \tag{6.5}$$
$$LS = PD - W_E, \tag{6.6}$$
$$LG = W_E, \tag{6.7}$$
$$\tag{6.8}$$

where AD is the drain junction area and PD the total drain junction perimeter.

The total junction capacitance on the source CJS and drain side CJD are then given by

$$CJS = AS \cdot CJORBOT + (PS - W_E) \cdot CJORSTI + W_E \cdot CJORGAT, \tag{6.9}$$
$$CJD = AD \cdot CJORBOT + (PD - W_E) \cdot CJORSTI + W_E \cdot CJORGAT, \tag{6.10}$$

where:

- **CJORBOT** is the zero-bias bottom capacitance per unit-area,
- **CJORSTI** is the zero-bias capacitance per unit-of-length along the STI-edge,
- **CJORGAT** is the zero-bias capacitance per unit-of-length along the gate-edge.

The above junction capacitance parameters are extracted directly from the PDK. We will use the the zero-bias bias value of th various junctions capacitances.

If AS, PD, AD and PD are not specified, they are calculated automatically in the sg13g2_moslv_mod.lib file.

In the circuit examples, we will calculate AS, PD, AD and PD for avoiding the automatic cal.culation

$CJp =$ 8.631e-04 $\frac{F}{m^2}$

$CJSWSTIp = 3.192\text{e-}11\ \frac{F}{m}$

$CJSWGATp = 2.747\text{e-}11\ \frac{F}{m}$

$CJp = 0.863\ \frac{fF}{\mu m^2}$

$CJSWSTIp = 0.032\ \frac{fF}{\mu m}$

$CJSWGATp = 0.027\ \frac{fF}{\mu m}$

Table 6.1: Extraction of the junction capacitance parameters.

	Zero-bias junction capacitance	Comment
Bottom cap per area	8.63E-04	extracted from PDK
Side-wall cap per unit length (along STI)	3.19E-11	extracted from PDK
Side-wall cap per unit length (along gate)	2.75E-11	extracted from PDK

6.2 Overlap capacitances

In PSP, the gate-to-source and gate-to-drain overlap capacitances are equal and given by

$$CGOV = \epsilon_{ox} \cdot \frac{W_{E,CV} \cdot LOV}{TOXOV}, \tag{6.11}$$

where $W_{E,CV}$ has already been defined above and is repeated here

The effective length and width for the calculation of the intrinsic and overlap acacitances are defined as

$$L_{E,CV} = L + \Delta L_{CV}, \tag{6.12}$$
$$W_{E,CV} = W + \Delta W_{CV}, \tag{6.13}$$

where

$$\Delta L_{CV} = 2\,LAP - \Delta L_{PS} - DLQ, \tag{6.14}$$
$$\Delta W_{CV} = 2\,WOT - \Delta W_{OD} - DWQ. \tag{6.15}$$

As mentioned above, for the IHP 130nm for nMOS $\Delta L_{PS} = 0$ and $\Delta W_{OD} = 0$ so that

$$\Delta L_{CV} = 2\,LAP - DLQ, \tag{6.16}$$
$$\Delta W_{CV} = 2\,WOT - DWQ. \tag{6.17}$$

`Gate-to-source and gate-to-drain overlap capacitances per effective unit width`

$C_{GSo} = 4.426\text{e-}10\ \frac{F}{m}$

$C_{GDo} = 4.426\text{e-}10\ \frac{F}{m}$

$C_{GSo} = 0.443\ \frac{fF}{\mu m}$

$C_{GDo} = 0.443\ \frac{fF}{\mu m}$

`Gate-to-bulk overlap capacitances per effective unit length`

$C_{GBo} = 2.186\text{e-}11\ \frac{F}{m}$

$C_{GBo} = 0.022\ \frac{fF}{\mu m}$

In PSP, the fringing field capacitance is given by

$$CFR = CFRW \cdot \frac{W_{G,CV}}{W_{EN}}, \tag{6.18}$$

where

$$W_{G,CV} = W_f + \Delta W_{OD} + DWQ \tag{6.19}$$

Since $\Delta W_{OD} = 0$ it reduces to

$$W_{G,CV} = W_f + DWQ \tag{6.20}$$

`Gate-to-source and gate-to-drain fringing capacitances per effective unit width`

$C_{GSf} = 1.000\text{e-}10\ \frac{F}{m}$

$C_{GDf} = 1.000\text{e-}10\ \frac{F}{m}$

$C_{GSf} = 0.100\ \frac{fF}{\mu m}$

$C_{GDf} = 0.100\ \frac{fF}{\mu m}$

`Total gate-to-source and gate-to-drain extrinsic capacitances per effective unit width`

$C_{GSe} = 5.426\text{e-}10\ \frac{F}{m}$

$C_{GDe} = 5.426\text{e-}10\ \frac{F}{m}$

$C_{GSe} = 0.543\ \frac{fF}{\mu m}$

$C_{GDe} = 0.543\ \frac{fF}{\mu m}$

Table 6.2: Extraction of the junction capacitance parameters.

	CGS per effective unit width	CGD per effective unit width	CGB per effective unit length	Comm
Overlap	4.43E-10	4.43E-10	2.19E-11	extract
Fringing	1.00E-10	1.00E-10	-	extract
Total	5.43E-10	5.43E-10	-	extract

7 Conclusion

The sEKV parameters have been extracted for a long, medium and short pMOS transistor. The overall results are good.

For the long-channel transistor both the direct extraction and optimization with $\lambda_c = 0$ give similar results. The fit is good up to about $IC = 100$. Above that the model cannot catch the effect due to the mobility reduction due to the vertical field.

For the short-channel transistor, again the direct extraction and the optimization with $\lambda_c > 0$ give similar results. The fit is good over the whole range of IC. Notice that the bump observed in moderate inversion for the nMOS does not appear for the pMOS.

Overall, the sEKV can do a good job for the long, medium and short pMOS transistors.