PSP103.8 MOSFET MODEL: IMPROVEMENT OF THE CHARGE MODEL FOR SHORT CHANNEL TRANSISTORS

MOS-AK ESSDERC/ESSCIRC event

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OUTLINE

- Introduction to PSP
- Overview of recent PSP versions
- Parasitic charges included in PSP103.7 and before
- Inner fringe charge model
- Inversion charges of overlaps
- Conclusion

INTRODUCTION TO PSP

- **PSP is a surface potential based model for deep-submicron bulk MOSFET**
  - Its development is supported by the CMC (Compact Model Coalition) : https://si2.org/cmc/
  - In December 2005, PSP has been elected a new industrial standard model by the CMC. This initial version was based on MM11 (from NXP Semiconductors) and SP (from Pennsylvania State University and later at Arizona State University).
  - PSP contains all relevant physical effects such as mobility degradation, velocity saturation, DIBL, gate leakage currents, lateral doping gradient effects, STI stress, etc.
  - PSP meets numerical requirements for Digital, Analog-Mixed Signal, and RF circuit designs, in particular continuous derivation of currents and charges is insured.
  - Since the first standard version, the developers have provided 16 releases.

OVERVIEW OF RECENT PSP VERSIONS

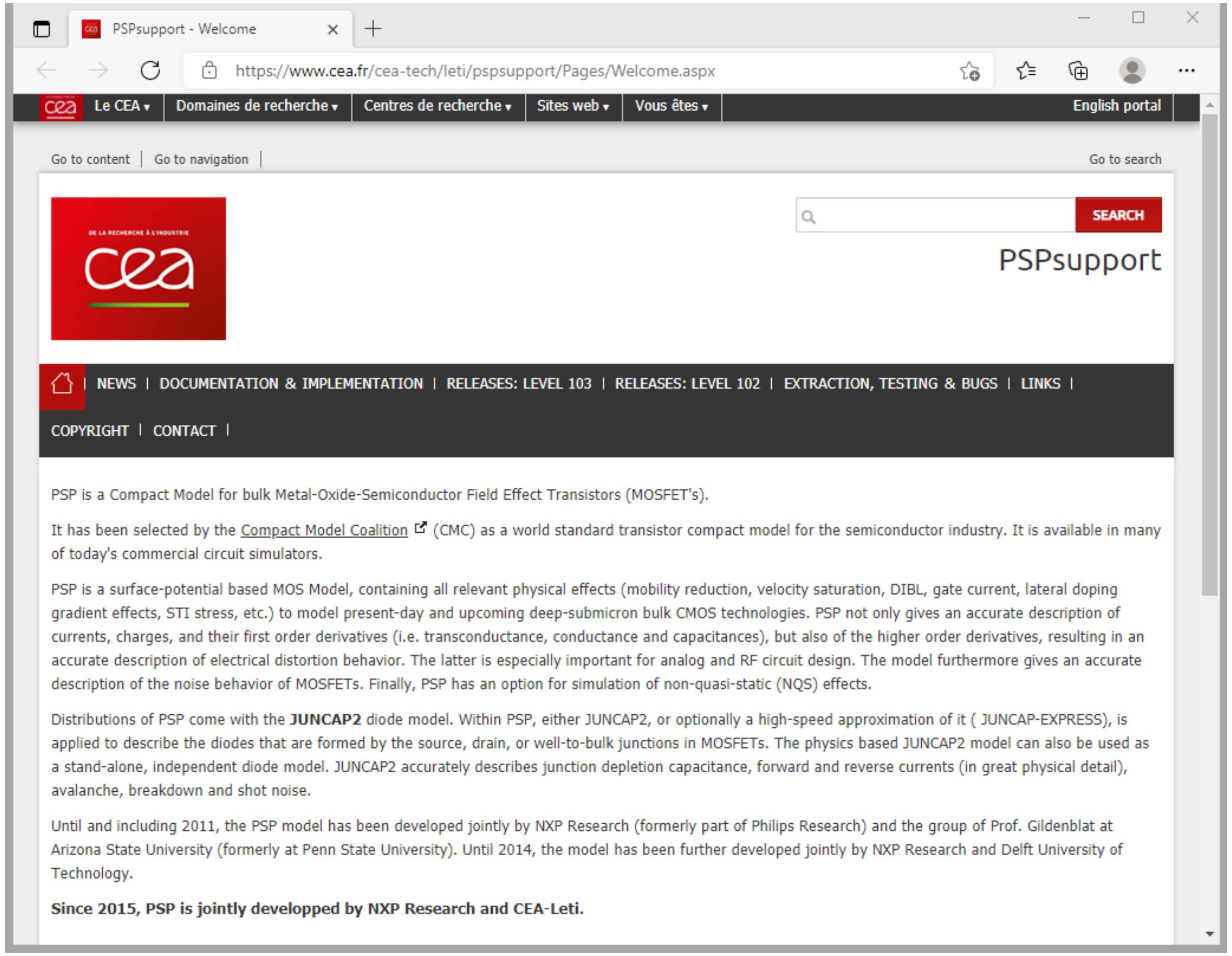
- **Since 2015, CEA-Leti is the main developer of PSP**

Website address:

https://www.cea.fr/cea-tech/leti/pspsupport

Contains:

- Release information
- Model documentation for PSP and JUNCAP2
- Downloadable Verilog-A codes



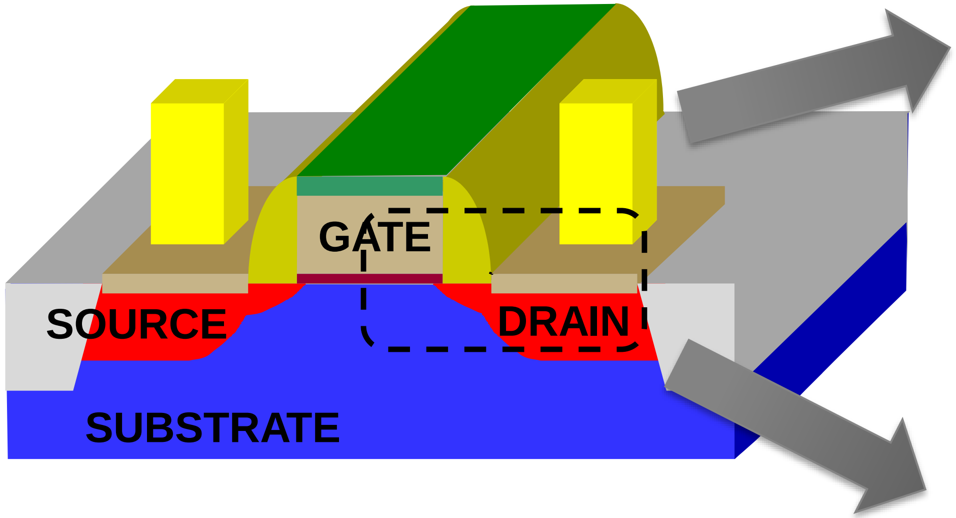
OVERVIEW OF RECENT PSP VERSIONS

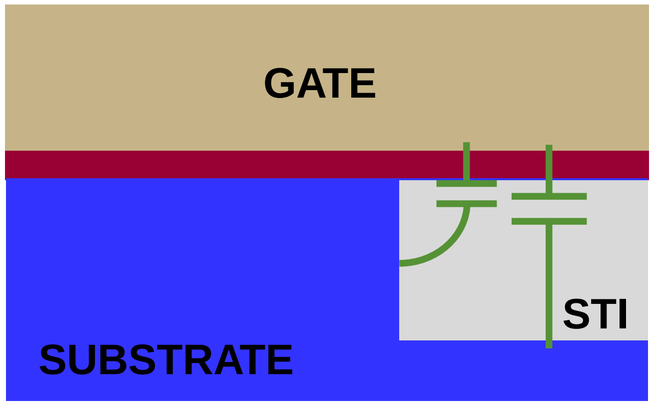
- **Since 2015, CEA-Leti is the main developer PSP: one release per year**

Date	Release	Major improvements/features
08/2016	PSP103.4	Modeling of edge MOSFET to reproduce the subthreshold hump effect Improved model of the subthreshold slope degradation induced by the short channel effects
04/2017	PSP103.5	New parameters for Coulomb scattering effect in mobility Improvement of temperature dependence of the flatband voltage
12/2017	PSP103.6	New model of interface states for better accuracy of g_m/I_d
02/2019	PSP103.7	Improvement of gate leakage currents model Possibility of charge model decoupling from IV for accurate CV of short channel transistors in saturation
07/2020	PSP103.8	Model of Inner fringe charges Inversion charge of overlaps

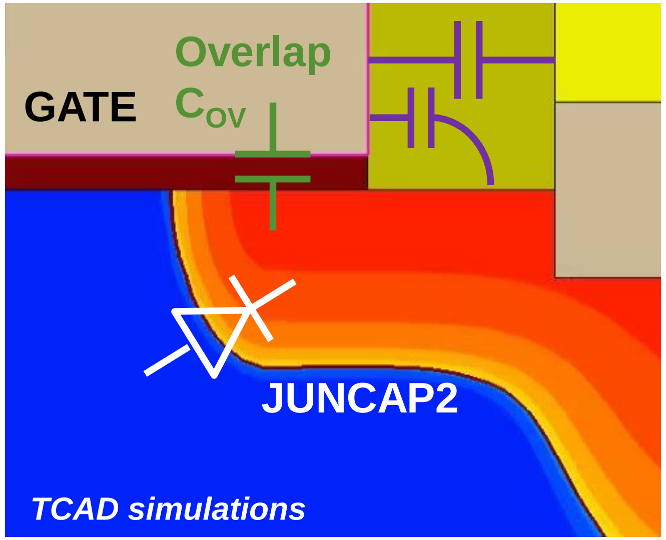
PARASITIC CHARGES INCLUDED IN PSP103.7 AND BEFORE

- Parasitic capacitances: COV, CFR, CGBOV, junction capacitances





Bias independent gate to substrate overlap charge $Q_{gb,ov}$



Bias independent outer fringe charges: $Q_{of,s}$,and $Q_{of,d}$

Bias dependent gate to drain/source overlap charges $Q_{s,ov}$ and $Q_{d,ov}$

These charges model don't include the inversion regime

$$Q_g = Q_{g,i} + Q_{s,ov} + Q_{d,ov} + Q_{of,s} + Q_{of,d} + Q_{gb,ov}$$

$$Q_s = Q_{s,i} - Q_{s,ov} - Q_{of,s}$$

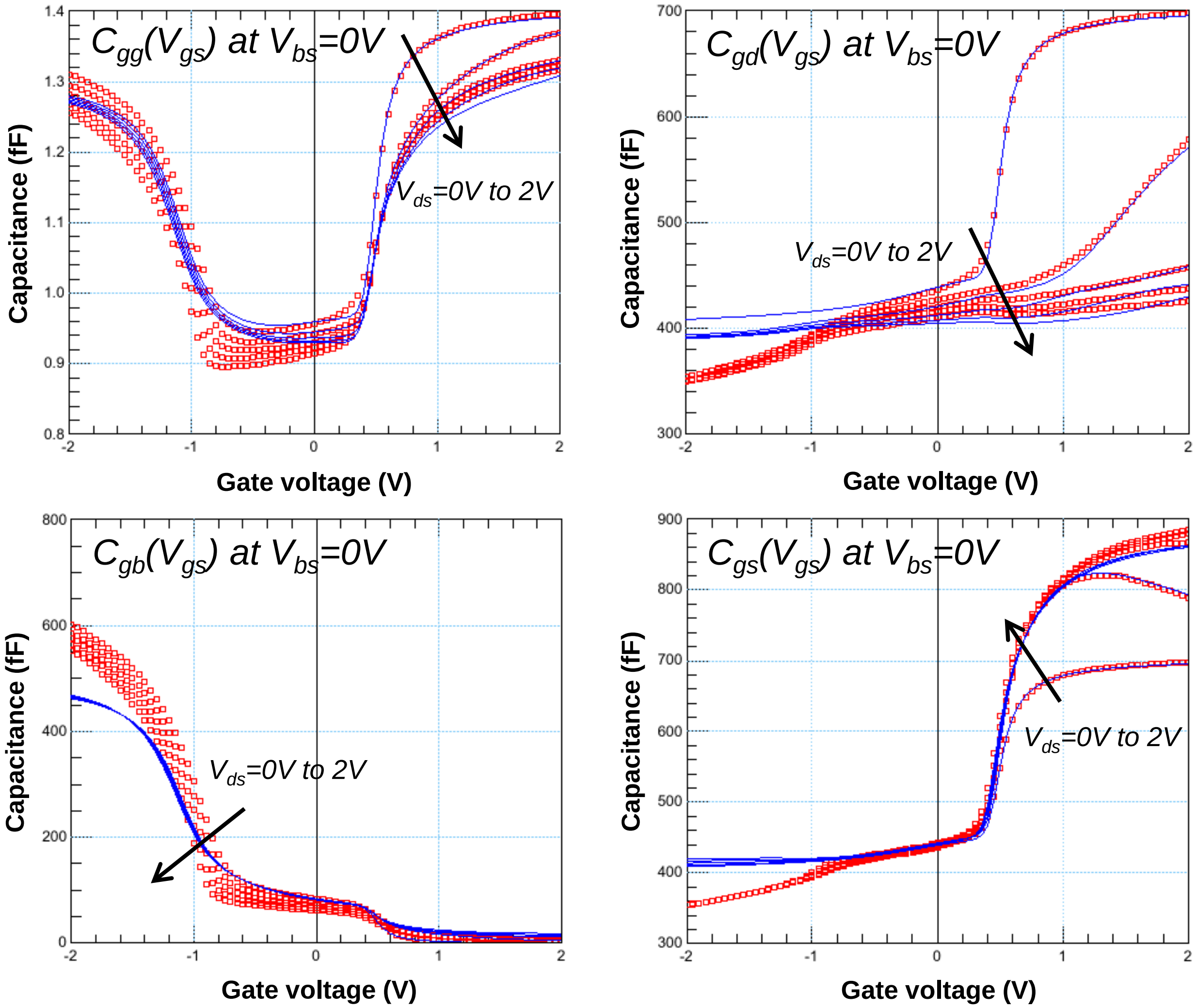
$$Q_d = Q_{d,i} - Q_{d,ov} - Q_{of,d}$$

$$Q_b = -Q_g - Q_s - Q_d$$

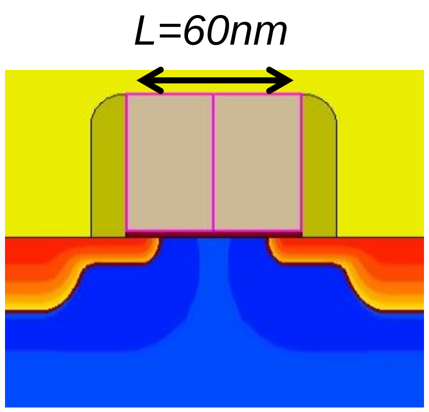
In red, intrinsic charges

PARASITIC CHARGES INCLUDED IN PSP103.7 AND BEFORE

- Analysis of PSP103.7 versus TCAD simulations: CV for short channel MOSFET



Red dots: TCAD
Blue lines: PSP103.7

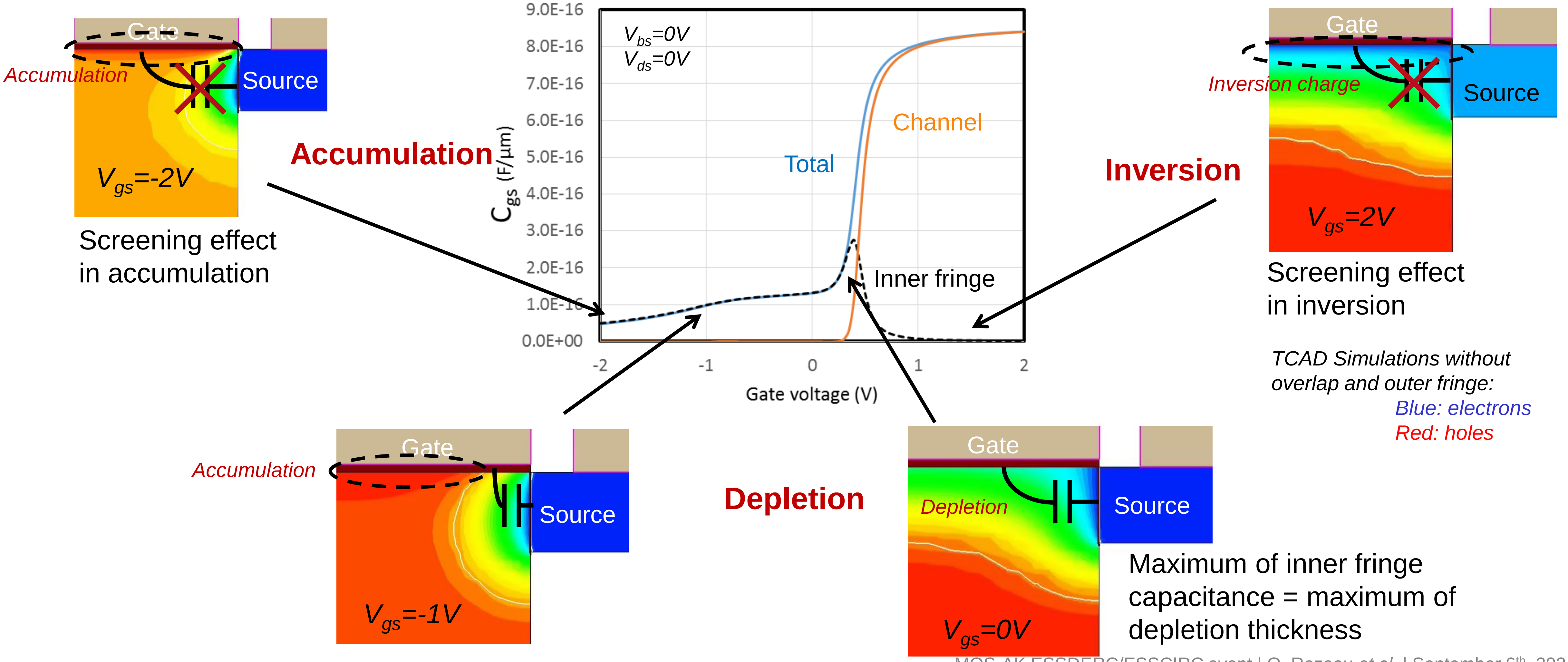


Requires improvements in accumulation regime for short channel MOSFET:

- Inner fringe capacitances are not modeled
- Inversion of overlaps is not modeled

INNER FRINGE CHARGE MODEL

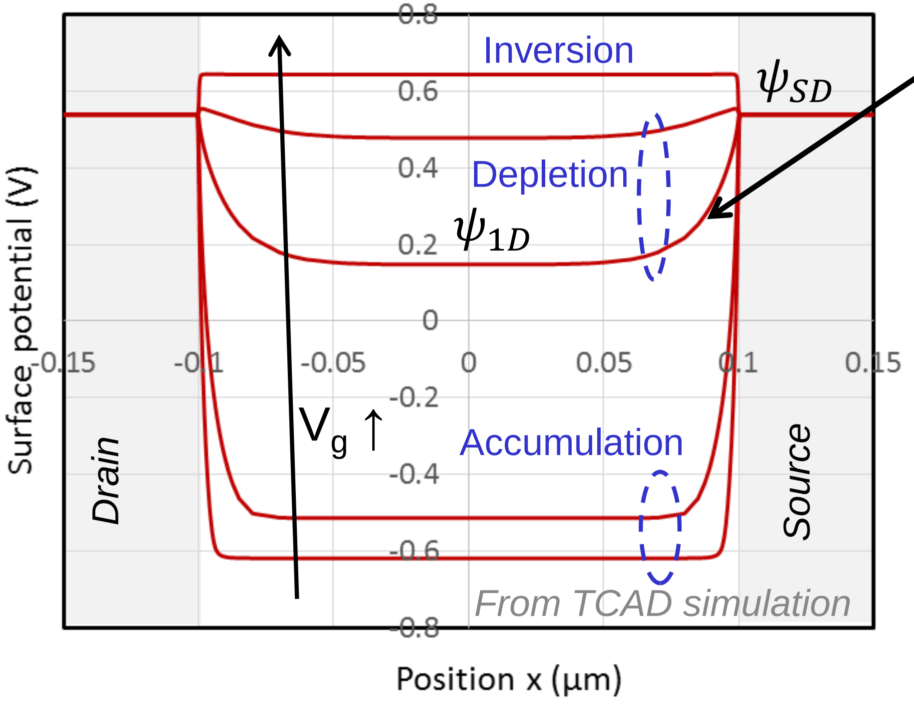
- Intrinsic MOSFET: inner fringe charges versus channel charge



TCAD Simulations without overlap and outer fringe:
Blue: electrons
Red: holes

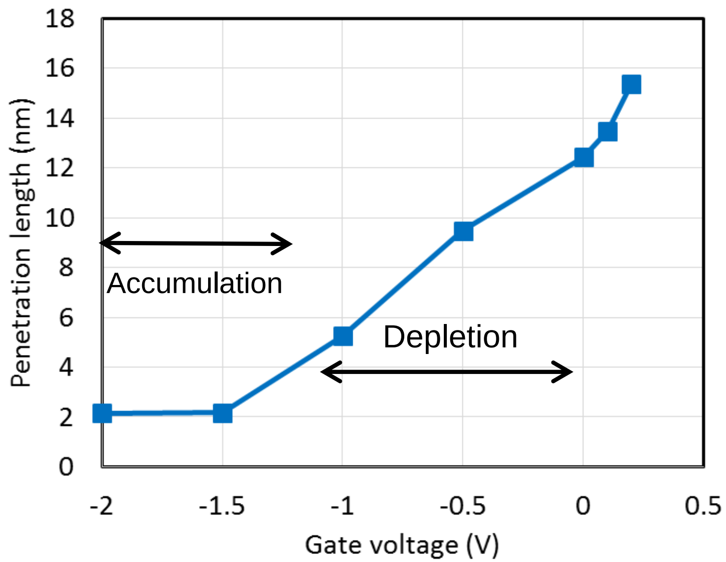
INNER FRINGE CHARGE MODEL

- **Surface potential profile near to the drain and the source**



$$\psi_{2D} \approx \psi_{1D} + (\psi_{SD} - \psi_{1D}) \cdot exp\left(-\frac{L/2 - x}{\lambda}\right) + (\psi_{SD} - \psi_{1D}) \cdot exp\left(-\frac{L/2 + x}{\lambda}\right)$$

λ is the length of the electrostatic field penetration



Calculation of charges:

$$\begin{cases} Q_{g,inr} = -W \cdot C'_{ox} \cdot \lambda \cdot (\psi_{SD} - \psi_{1D}) \\ Q_{b,inr} = W \cdot C'_{ox} \cdot \lambda \cdot q_{b,1D} \end{cases}$$

Inner fringe capacitances

INNER FRINGE CHARGE MODEL

- **Modeling method of inner fringe charge**

Rigorous calculation of λ is very complex and depends on doping profiles, thicknesses, etc.

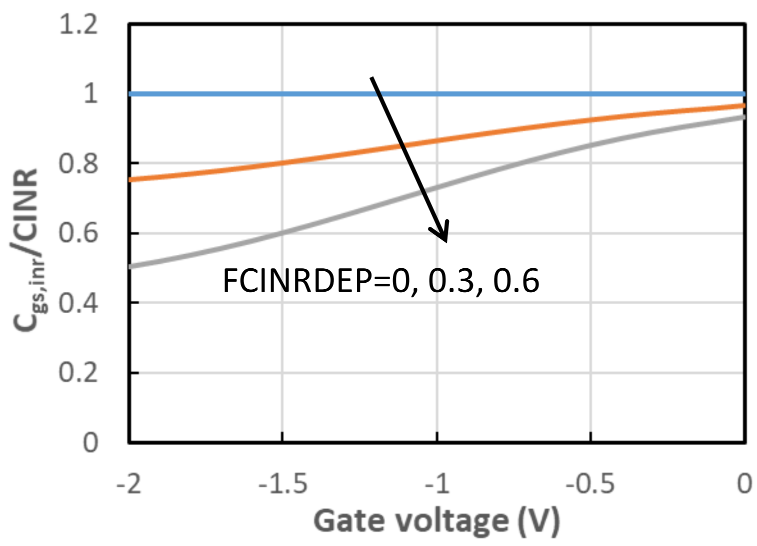
In depletion, we can write the inner fringe capacitance as:

Model parameter for dependence with the channel depletion thickness

$$C_{gs,inr} = C_{sg,inr} = \mathbf{CINR} \cdot \left(\mathbf{FCINRDEP} \cdot \left(f_{inr,dep} - 1\right) + 1\right)$$

$$C_{gd,inr} = C_{dg,inr} = \mathbf{CINRD} \cdot \left(\mathbf{FCINRDEP} \cdot \left(f_{inr,dep} - 1\right) + 1\right)$$

With,
$$\begin{cases} f_{inr,dep} = \dfrac{\mathbf{1}}{1 + exp\left(-\dfrac{V_{GB}^{*} - \mathbf{DVFBINR}}{\phi_T^{*} \cdot \Delta_{inr,dep}}\right)} \\ \Delta_{inr,dep} = \dfrac{1}{2} \cdot \left(\dfrac{\phi_B}{2 \cdot \phi_T^{*}} + \dfrac{G}{\sqrt{2}} + 1\right) \end{cases}$$



INNER FRINGE CHARGE MODEL

- **Modeling method of inner fringe charge**

In accumulation, the decrease of inner fringe charges due to screening effect is done by:

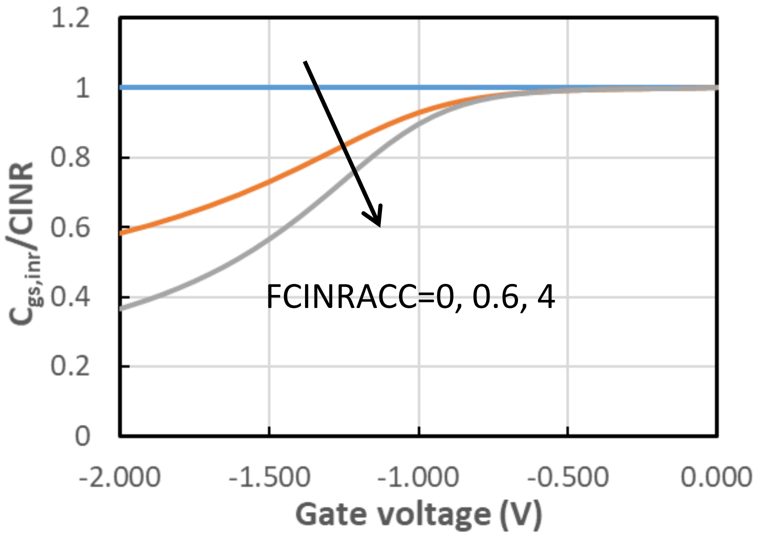
$$C_{gs,inr} = C_{sg,inr} = \mathbf{CINR} \cdot f_{inr,acc}$$

$$C_{gd,inr} = C_{dg,inr} = \mathbf{CINRD} \cdot f_{inr,acc}$$

$f_{inr,acc}$ is a mathematical function to reproduce the behavior

$$\begin{cases} V_{\mathrm{g,inr}} = V^{*}_{\mathrm{GB,ac}} - \mathbf{DVFBINR} + \boldsymbol{V}_{\mathbf{inr,max}} \\ V_{\mathrm{x1,inr}} = MAXA\left(V_{\mathrm{g,inr}}, \boldsymbol{V}_{\mathbf{inr,max}}, \boldsymbol{a}_{\mathbf{inr}}\right) \\ V_{\mathrm{x2,inr}} = V_{\mathrm{x1,inr}} \cdot \left(2 \cdot V_{\mathrm{x1,inr}} - \boldsymbol{V}_{\mathbf{inr,max}} - V_{\mathrm{g,inr}}\right) \\ V_{\mathrm{g,inr,eff}} = \dfrac{V_{\mathrm{g,inr}} \cdot \boldsymbol{V}_{\mathbf{inr,max}}}{V_{\mathrm{x1,inr}}} \\ f_{\mathrm{q,inr}} = \sqrt{1 - \mathbf{FCINRACC} \cdot V_{\mathrm{g,inr,eff}}} \\ f_{\mathrm{inr,acc}} = \left(\dfrac{1}{2 \cdot f_{\mathrm{q,inr}}} - 1\right) \cdot \dfrac{V_{\mathrm{x2,inr}} + V_{\mathrm{g,inr}} \cdot \left(\boldsymbol{V}_{\mathbf{inr,max}} - V_{\mathrm{x1,inr}}\right)}{V_{\mathrm{x2,inr}}} \cdot \dfrac{\boldsymbol{V}_{\mathbf{inr,max}}}{V_{\mathrm{x1,inr}}} + 1 \end{cases}$$

Parameter for screening effect in accumulation



INNER FRINGE CHARGE MODEL

- **Modeling method of inner fringe charge**

In general case, by combining both effects:

$$\begin{cases} C_{gs,inr} = C_{sg,inr} = \mathbf{CINR} \cdot f_{inr} \\ C_{gd,inr} = C_{dg,inr} = \mathbf{CINRD} \cdot f_{inr} \end{cases}$$

“Channel” depletion

Screening effect in accumulation

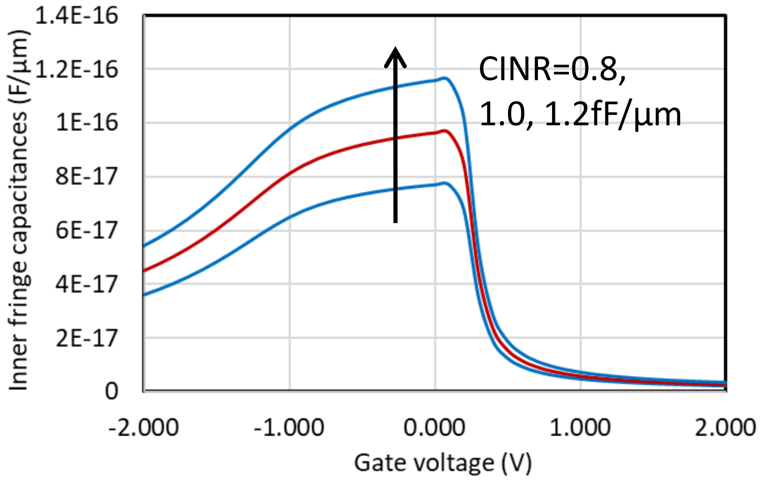
$$f_{inr} = \boxed{\mathbf{FCINRDEP} \cdot f_{inr,dep}} + \boxed{(1 - \mathbf{FCINRDEP}) \cdot f_{inr,acc}}$$

In PSP, the calculations of the inner fringe <u>charges</u> are based on these equations

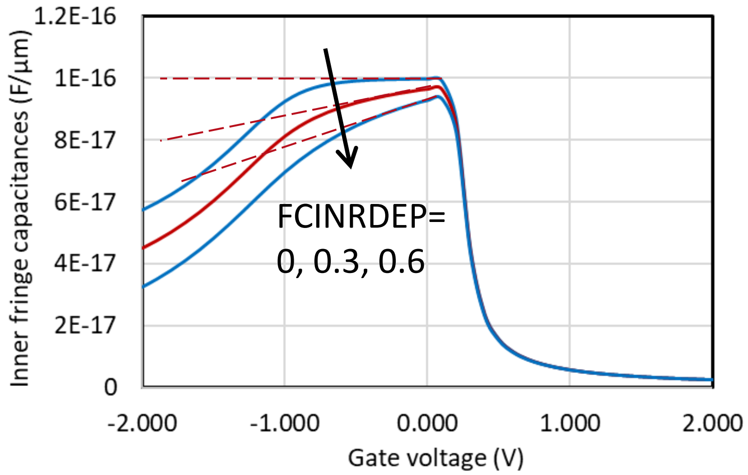
INNER FRINGE CHARGE MODEL

- Parameter description of inner fringe charge model

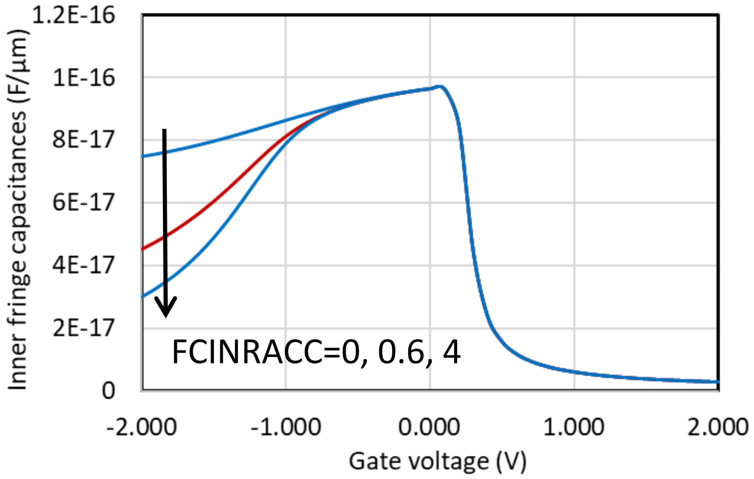
Charge quantities



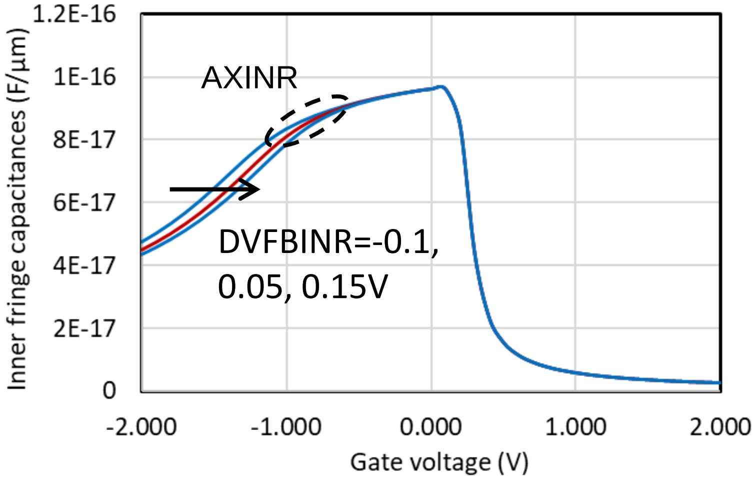
Modulation in depletion



Screening effect in accumulation

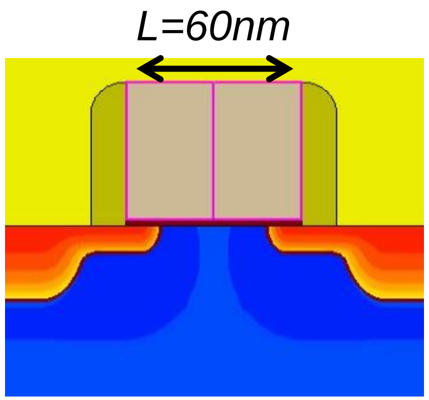


Accumulation to depletion transition

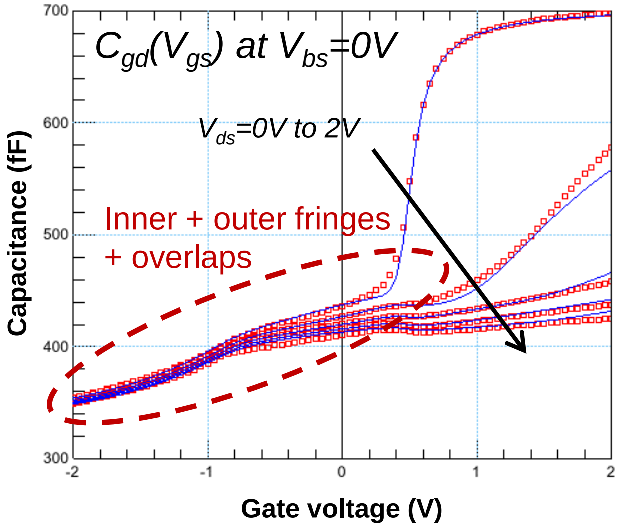


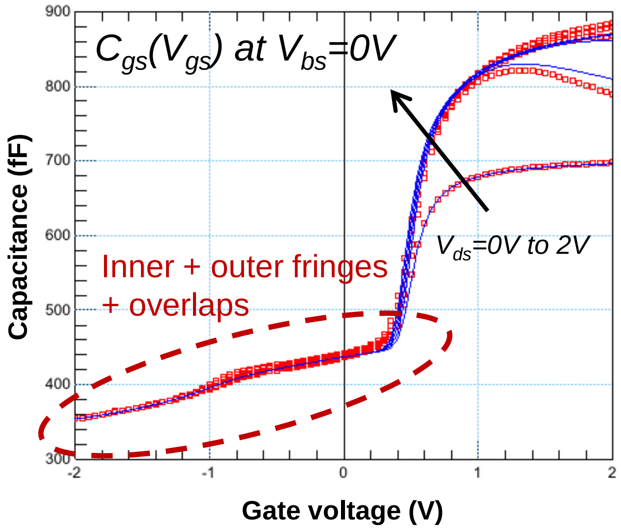
INNER FRINGE CHARGE MODEL

- **Introduction and validation of inner fringe charge model**



Red dots: TCAD
Blue lines: PSP103.8





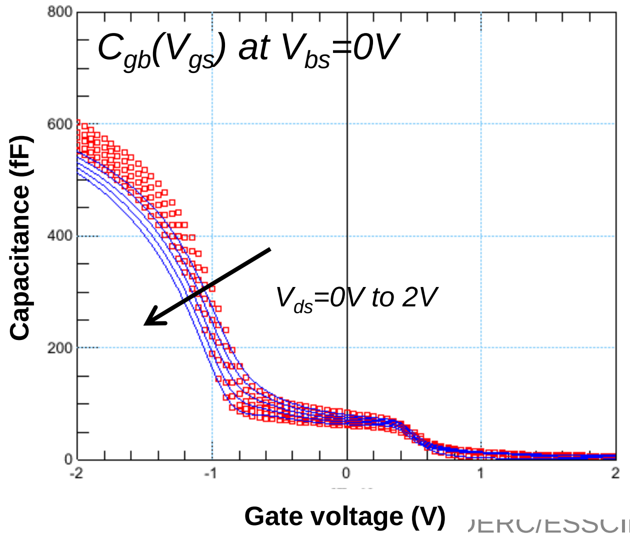
Charges induced by the inner fringes are introduced as:

$$Q_g = Q_{g,i} + Q_{g,inr} + Q_{s,ov} + Q_{d,ov} + Q_{of,s} + Q_{of,d} + Q_{gb,ov}$$

$$Q_s = Q_{s,i} + Q_{s,inr} - Q_{s,ov} - Q_{of,s}$$

$$Q_d = Q_{d,i} + Q_{d,inr} - Q_{d,ov} - Q_{of,d}$$

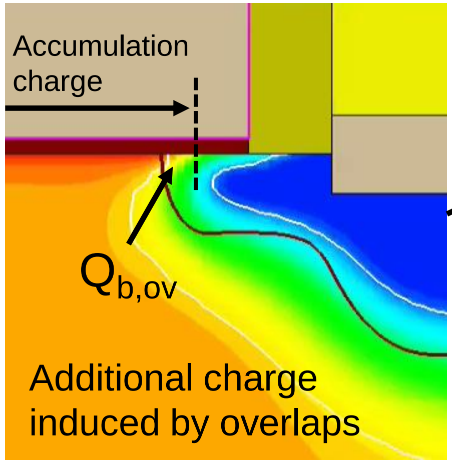
$$Q_b = -Q_g - Q_s - Q_d$$

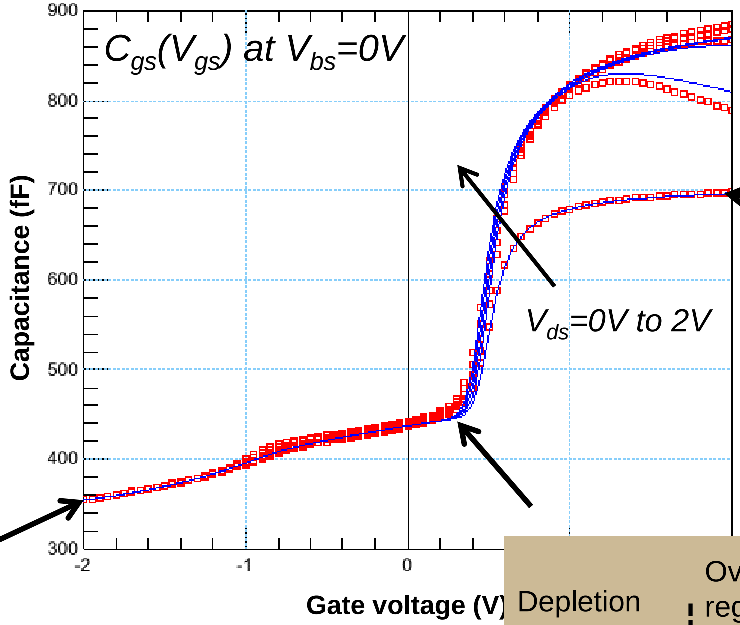


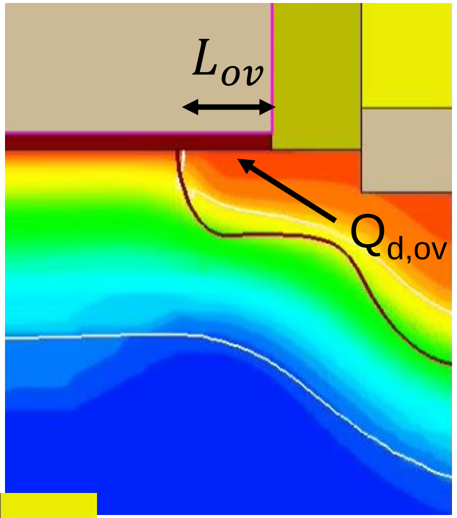
- Improvement on C_{gs} and C_{gd}
- Issue: C_{gb} is too low due to the lack of inversion charges in overlap regions

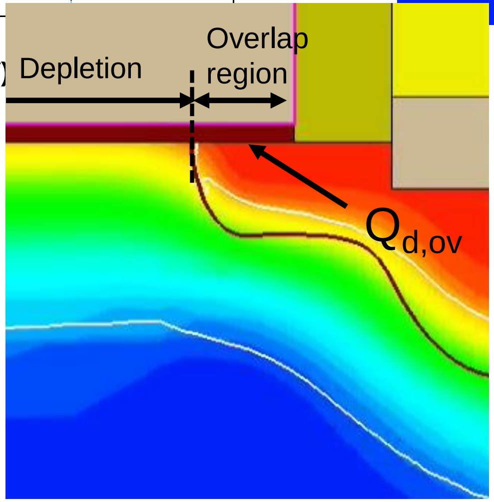
INVERSION CHARGES OF OVERLAPS

- **Analysis from TCAD simulations: partial inversion of overlaps**









New parameter to define the accumulated area of overlaps: $A_{ov} = \mathbf{FCGOVACC} \cdot W \cdot L_{ov}$ (used only for bulk charge calculation of overlaps)

INVERSION CHARGES OF OVERLAPS

- **Introduction of overlap charges in inversion (channel in accumulation)**

Charges induced by the inversion of overlaps are added at the gate and the bulk

$$Q_g = Q_{g,i} + Q_{g,inr} + Q_{s,ov} + Q_{d,ov} + Q_{of,s} + Q_{of,d} + Q_{gb,ov} + Q_{g,ov} + Q_{g,dov}$$

$$Q_s = Q_{s,i} + Q_{s,inr} - Q_{s,ov} - Q_{of,s}$$

$$Q_d = Q_{d,i} + Q_{d,inr} - Q_{d,ov} - Q_{of,d}$$

$$Q_b = -Q_g - Q_s - Q_d$$

The calculation of these charges is based on the use of Lambert W-function:

$$x_{\mathrm{gb,eff,ov}} = \ln\left(1 + \exp\left(\mathrm{CGOVACCG} \cdot \left(\frac{V_{\mathrm{GB}} - \boldsymbol{V}_{\mathbf{FB}}}{2 \cdot \phi_{\mathrm{T}}} + \boldsymbol{\Delta x}_{\mathbf{gb,ov}}\right)\right)\right)$$

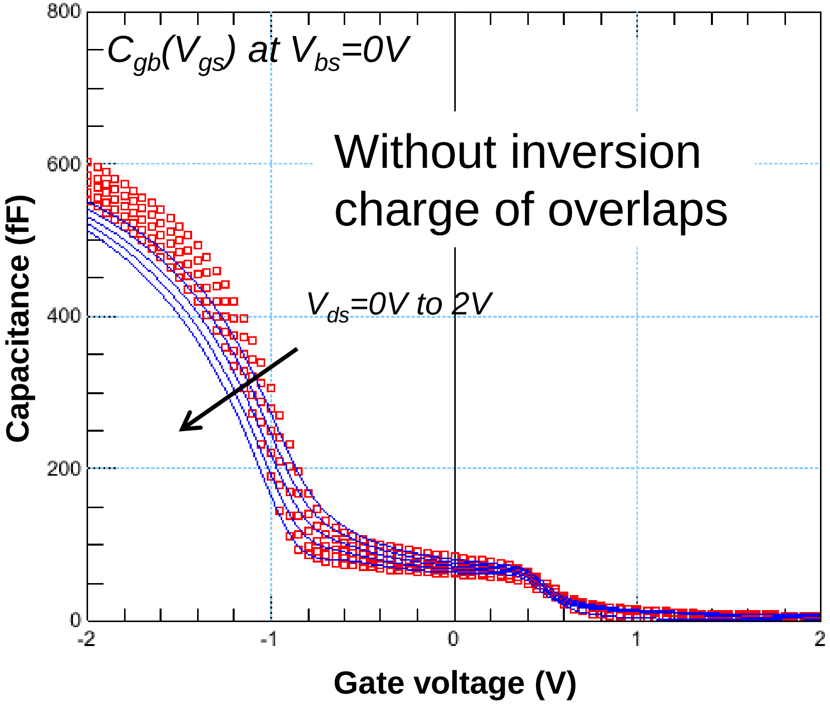
$$Q_{\mathrm{g,ov}} = -2 \cdot \phi_{\mathrm{T}} \cdot \mathrm{FCGOVACC} \cdot \mathrm{CGOV} \cdot \frac{x_{\mathrm{gb,eff,ov}}}{\mathrm{CGOVACCG}} \cdot \left(1 - \frac{\ln\left(1 + x_{\mathrm{gb,eff,ov}}\right)}{2 + x_{\mathrm{gb,eff,ov}}}\right)$$

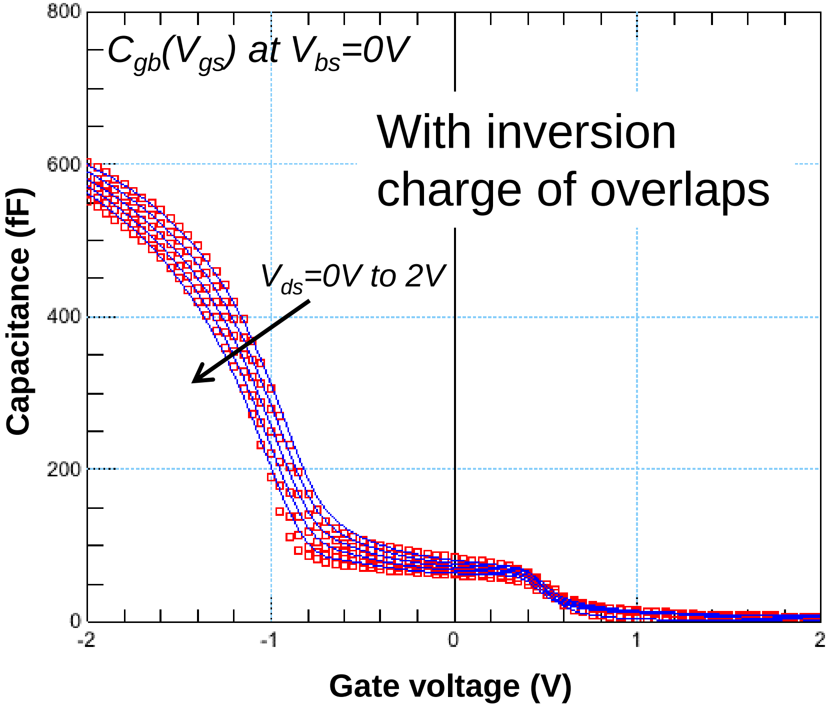
$$x_{\mathrm{gb,eff,dov}} = \ln\left(1 + \exp\left(\mathrm{CGOVACCG} \cdot \left(\frac{V_{\mathrm{GB}} - \boldsymbol{V}_{\mathbf{FB}}}{2 \cdot \phi_{\mathrm{T}}} + \boldsymbol{\Delta x}_{\mathbf{gb,dov}}\right)\right)\right)$$

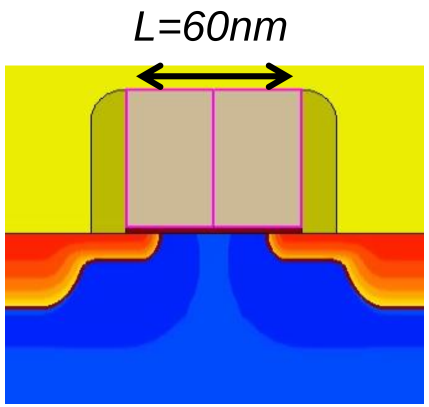
$$Q_{\mathrm{g,dov}} = -2 \cdot \phi_{\mathrm{T}} \cdot \mathrm{FCGOVACC} \cdot \mathrm{CGOVD} \cdot \frac{x_{\mathrm{gb,eff,dov}}}{\mathrm{CGOVACCG}} \cdot \left(1 - \frac{\ln\left(1 + x_{\mathrm{gb,eff,dov}}\right)}{2 + x_{\mathrm{gb,eff,dov}}}\right)$$

INVERSION CHARGES OF OVERLAPS

- **Improvement of gate-bulk capacitance for short channel transistors**



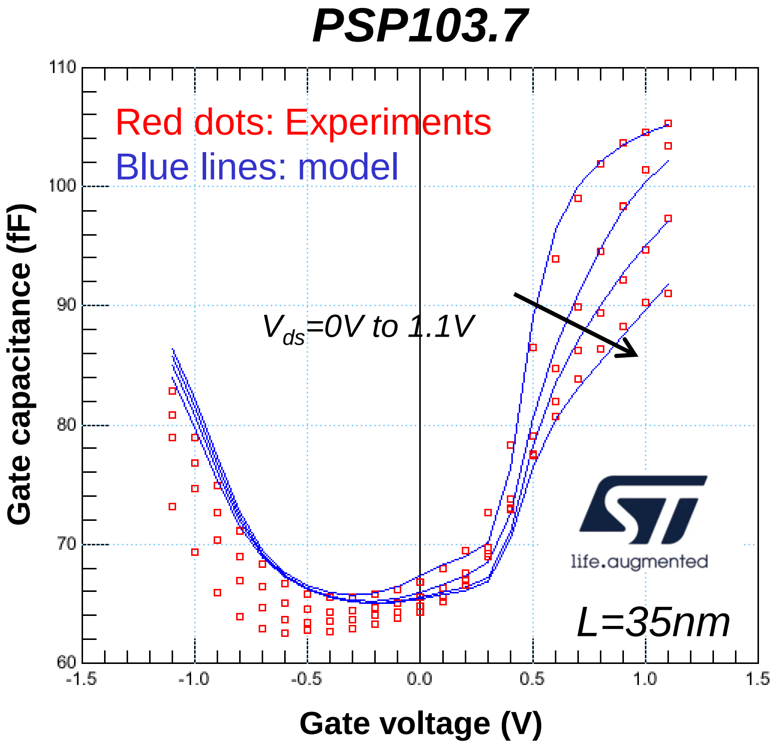


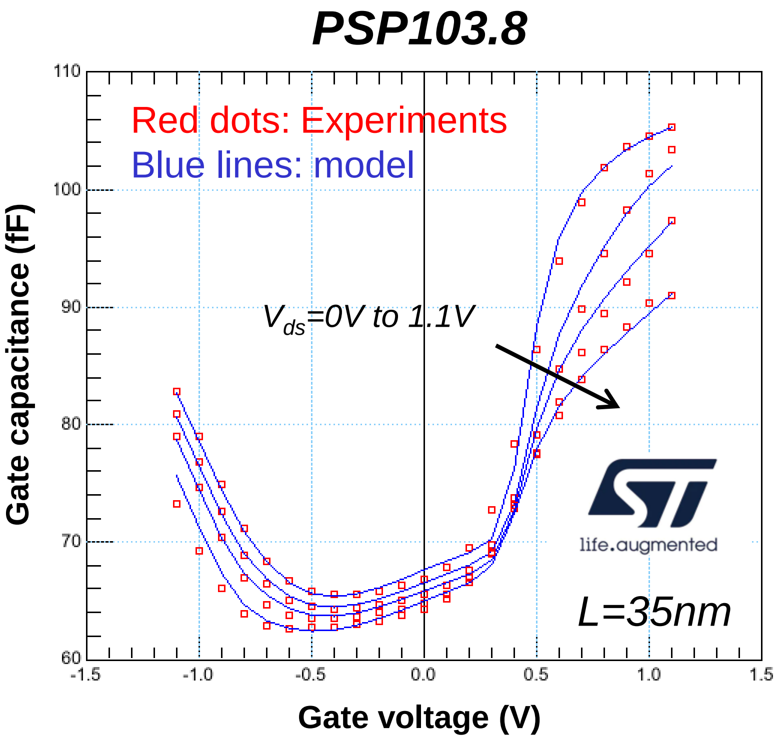


Red dots: TCAD
Blue lines: PSP103.8

CONCLUSION

- **Model validation using experimental data**





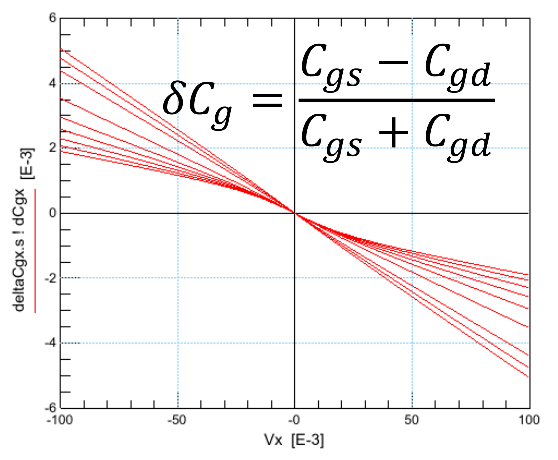
Better description of CV characteristics in accumulation and depletion regimes for short channel MOSFET (here L=35nm)

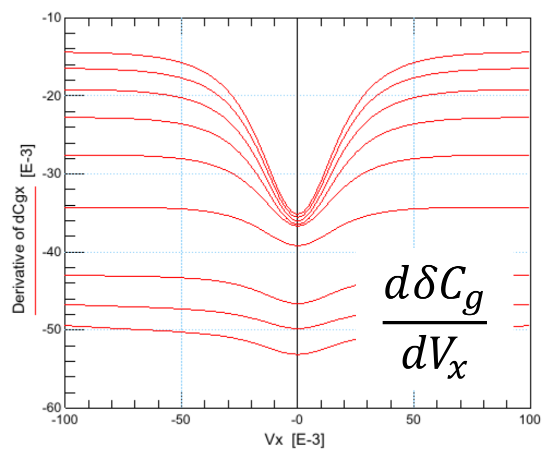
CONCLUSION

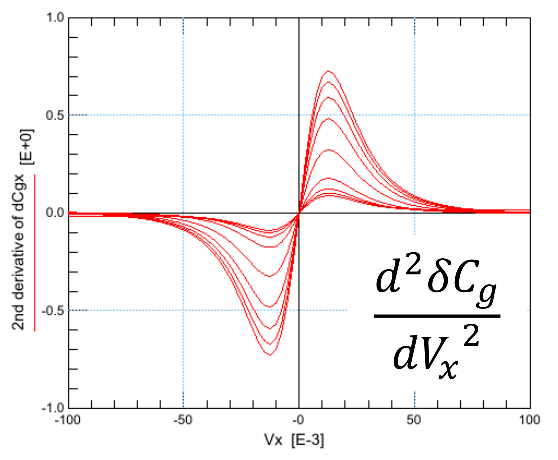
- **Validations of Source-Drain symmetry and capacitance reciprocities**

❑ No issue during the symmetry test on capacitances using definition from C. McAndrew (TED 2006)

V_{gs}=-2V to 0V

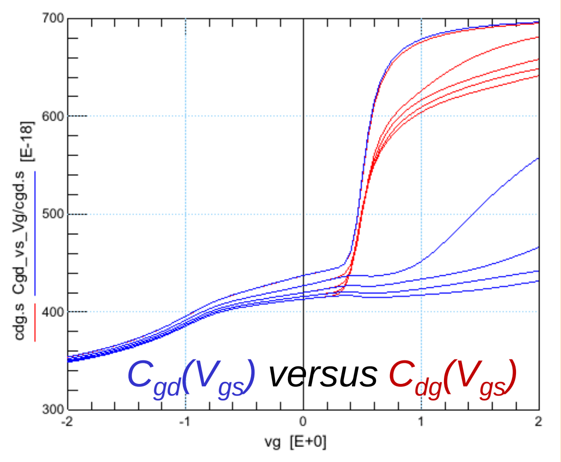


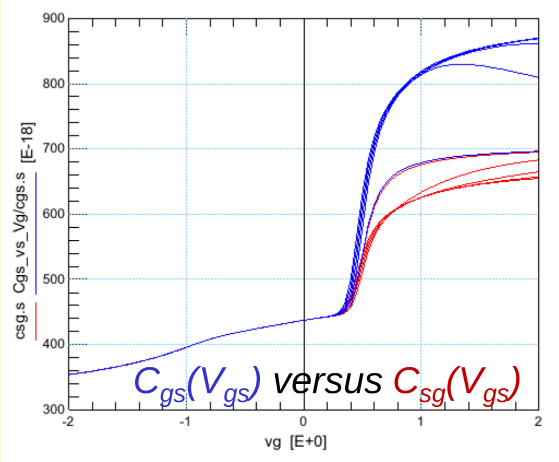


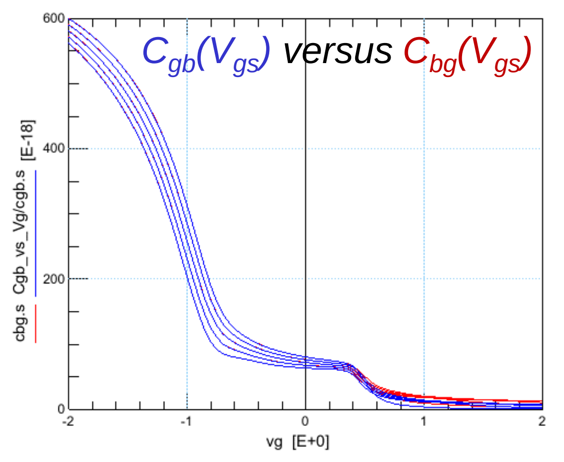


❑ Reciprocities of parasitic capacitances whatever the supplied voltages

L=60nm
V_{ds}=0V to 2V
V_{bs}=0V







CONCLUSION

- **PSP103.8 is a significant release for the modeling of short channel CV in accumulation regime**

- **Where to find PSP releases**

  - Verilog-A versions of PSP are free downloadable at https://www.cea.fr/cea-tech/leti/pspsupport

  - PSP can be used in most of commercial circuit simulators

  - PSP103.8.0 has been released in July 2020

  - PSP103.8.1, containing minor bug fixes and new parameters for temperature control, has been released in Avril 2021

Thank You

CEA-Leti, technology research institute
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