Cascode Gain Stage

For IHP 130nm Process (Version 1)

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1 Introduction

This notebook presents the design of a cascode gain stage using the sEKV model and the inversion coefficient approach [1], [2], [3].

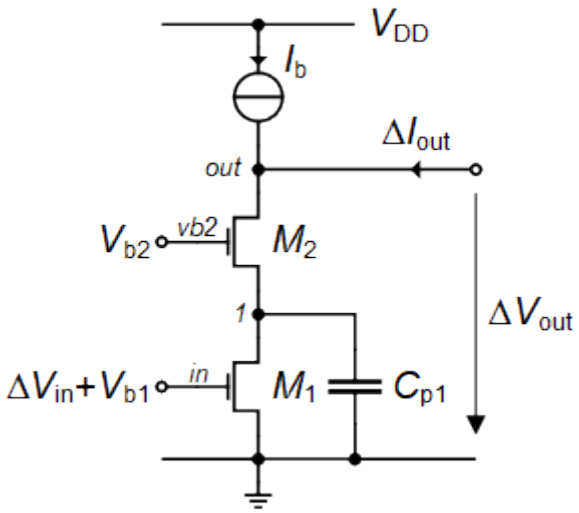

Figure 1.1: Schematic of the cascode gain stage.

The schematic of the cascode gain stage is shown in Figure 1.1. Let's start with the small-signal analysis.

2 Analysis

2.1 Small-signal analysis

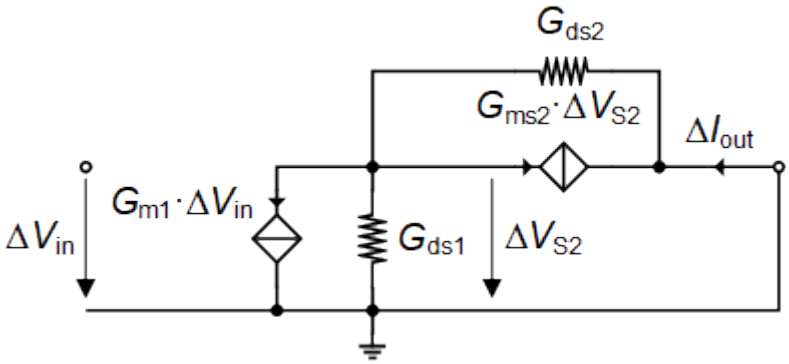

Figure 2.1: Small-signal schematic of the cascode stage for the calculation of the equivalent transconductance.

> **Note**
>
> In the following analysis, the current source will be considered as ideal, i.e. zero output conductance. Of course, this current source is implemented by one or several transistors. In order not to degrade the overall output conductance and the DC gain, the current source should have an output conductance smaller than the cascode gain stage. This means that the current source should also be cascoded.

The small-signal schematic corresponding to Figure 1.1 for the derivation of the equivalent transconductance is given in Figure 2.1. Note that the output is short-circuited for calculating the short-circuit output current and the corresponding transconductance. The equivalent transconductance is given by

$$G_{meq} \triangleq \left.\frac{\Delta I_{out}}{\Delta V_{in}}\right|_{\Delta V_{out}=0} = \frac{G_{m1}(G_{ms2}+G_{ds2})}{G_{ms2}+G_{ds1}+G_{ds2}} \cong G_{m1}, \tag{2.1}$$

which shows that assuming $G_{ms2} \gg G_{ds1}, G_{ds2}$, the equivalent transconductance of the cascode stage is equal to the transconductance of the driver transistor M_1. This result is expected since the cascode transistor is a common gate stage which has a unity current gain so that the current coming from the driver transistor M_1 is directly directed to the output.

The small-signal schematic for the calculation of the output conductance is shown in Figure 5.3. The output conductance is given by

$$G_{out} \triangleq \frac{\Delta I_{out}}{\Delta V_{out}} = \frac{G_{ds1}G_{ds2}}{G_{ms2}+G_{ds1}+G_{ds2}} \cong \frac{G_{ds1}}{G_{ms2}/G_{ds2}}, \tag{2.2}$$

which is equal to the output conductance of M_1, G_{ds1}, divided by the voltage gain of the cascode G_{ms2}/G_{ds2}. This means that, at low-frequency, the output conductance of a single transistor can be reduced by adding a cascode stage at the cost of some voltage headroom to maintain M_2 in saturation.

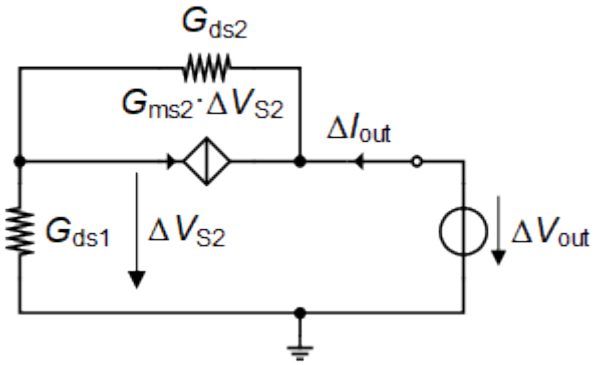

Figure 2.2: Small-signal schematic of the cascode stage for the calculation of the output conductance.

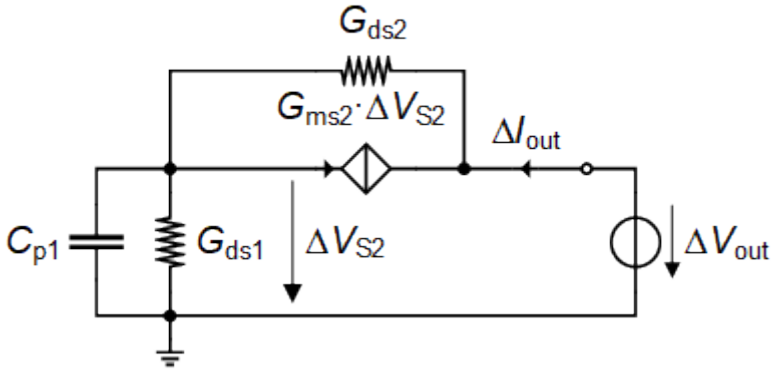

Figure 2.3: Small-signal schematic of the cascode stage for the calculation of the output conductance including the parasitic capacitance C_{p1}.

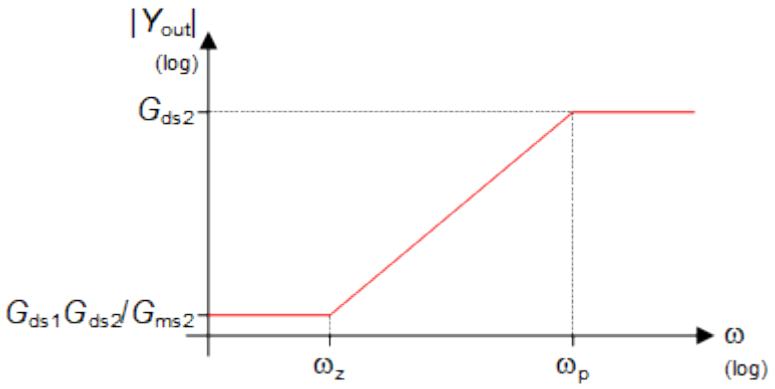

Figure 2.4: Effect of the parasitic capacitance C_{p1} on the output admittance Y_{out}.

The impact of the parasitic capacitance at node 1 on the output conductance can be investigated by adding the capacitance as shown in Figure 2.3. The output admittance then becomes

$$Y_{out} = G_{out} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_p}, \tag{2.3}$$

where

$$G_{out} = \frac{G_{ds1}G_{ds2}}{G_{ms2} + G_{ds1} + G_{ds2}} \cong \frac{G_{ds1}G_{ds2}}{G_{ms2}}, \tag{2.4}$$

$$\omega_z = \frac{G_{ds1}}{C_{p1}}, \tag{2.5}$$

$$\omega_p = \frac{G_{ms2} + G_{ds1} + G_{ds2}}{C_{p1}} \cong \frac{G_{ms2}}{C_{p1}}. \tag{2.6}$$

The magnitude of Y_{out} versus frequency is sketched in Figure 2.4. For $\omega \ll \omega_z \ll \omega_p$, $Y_{out} \cong G_{out}$. However for $\omega_z \ll \omega_p \ll \omega$, the output admittance becomes $Y_{out} \cong G_{ds2}$. We see that the cascode effect is lost. This can easily be understood since for $\omega_p \ll \omega$, the cascode node 1 is shortened to the ac ground and the voltage controlling the source of M_2 is zero leaving the output conductance of M_2 only.

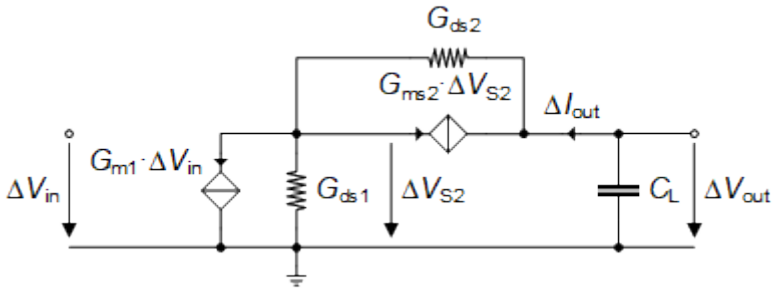

Figure 2.5: Small-signal schematic for voltage gain calculation.

The transfer function can be calculated using the schematic shown in Figure 2.5 resulting in

$$A_v(s) = \frac{A_{dc}}{1 + s/\omega_c}, \tag{2.7}$$

with

$$A_{dc} = -\frac{G_{m1}\,(G_{ms2} + G_{ds2})}{G_{ds1}\,G_{ds2}} \cong -\frac{G_{m1}\,G_{ms2}}{G_{ds1}\,G_{ds2}}, \tag{2.8}$$

$$\omega_c = \frac{G_{ds1}\,G_{ds2}}{(G_{ms2} + G_{ds1} + G_{ds2})\,C_L} \cong \frac{G_{ds1}\,G_{ds2}}{G_{ms2}\,C_L}. \tag{2.9}$$

.

The gain-bandwidth product is then given by

$$\omega_u = \frac{G_{m1}\,(G_{ms2} + G_{ds2})}{(G_{ms2} + G_{ds1} + G_{ds2})\,C_L} \cong \frac{G_{m1}}{C_L}, \tag{2.10}$$

which, as expected, is equal to the ratio of the cascode equivalent transconductance G_{m1} to the load capacitance C_L.

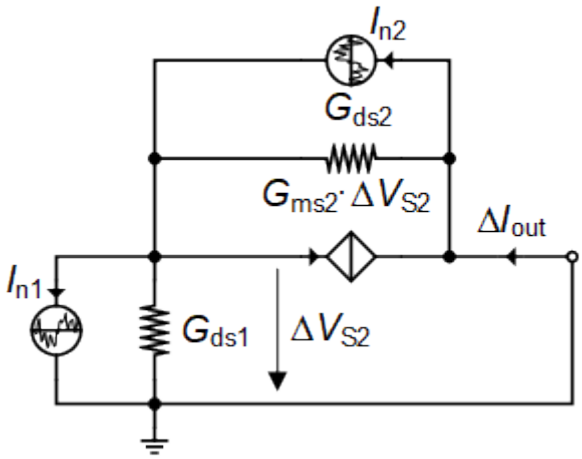

Figure 2.6: Small-signal schematic of the cascode stage for the noise calculation.

2.2 Noise analysis

To calculate the output noise power spectral density (PSD) we can use the schematic shown in Figure 2.6. The output noise current is then given by

$$I_{nout} = \frac{G_{ms2} + G_{ds2}}{G_{ms2} + G_{ds1} + G_{ds2}} \cdot I_{n1} + \frac{G_{ds1}}{G_{ms2} + G_{ds1} + G_{ds2}} \cdot I_{n2} \cong I_{n1} + \frac{I_{n2}}{G_{ms2}/G_{ds1}}, \tag{2.11}$$

for $G_{ms2} \gg G_{ds1}, G_{ds2}$. We see that the contribution to the output noise current of the cascode stage is actually divided by G_{ms2}/G_{ds1}. Provided that this gain can be made sufficiently large and that both transistor have the same noise, the noise of the cascode stage can be made negligible compared to the noise due to M_1. Ultimately if $G_{ds1} = 0$, the noise current I_{n2} circulates in the cascode transistor M_2 (G_{ms2} in the small-signal schematic) and hence does not reach the output.

The output noise conductance is then given by

$$G_{nout}(f) \cong G_{n1}(f) + \left(\frac{G_{ds1}}{G_{ms2}}\right)^2 G_{n2}(f) \tag{2.12}$$

where the noise conductances are given by

$$G_{ni}(f) = \gamma_{ni} \cdot G_{mi} + \frac{\rho_n}{f\, W_i\, L_i} \cdot G_{mi}^2 \quad \text{for } i = 1, 2. \tag{2.13}$$

The input-referred noise is obtained by dividing G_{nout} by G_{meq}^2, resulting in

$$R_{nin} = \frac{G_{nout}(f)}{G_{meq}}. \tag{2.14}$$

It can be decomposed into the thermal and flicker noise components according to

$$R_{nin} = R_{nt} + R_{nf}(f) \tag{2.15}$$

where R_{nt} is the total input-referred thermal noise

$$R_{nt} \cong \frac{\gamma_{n1}}{G_{m1}} + \left(\frac{G_{ds1}}{G_{m1}}\right)^2 \frac{\delta_{n2}}{G_{ms2}} = \frac{\gamma_{n1}}{G_{m1}}(1 + \eta_{th}), \tag{2.16}$$

where

$$\eta_{th} = \frac{G_{ds1}^2}{G_{m1} G_{ms2}} \frac{\delta_{n2}}{\gamma_{n1}} \ll 1 \tag{2.17}$$

represents the contribution to the input-referred thermal noise of the cascode transistor M_2 relative to that of the driver transistor M_1. Since for long-channel transistors γ_{n1} and δ_{n2} are of the same order of magnitude and since $G_{m1}G_{ms2} \gg G_{ds1}^2$ then $\eta_{th} \ll 1$. This means that the contribution of the cascode transistor to the input-referred thermal noise is negligible.

$R_{nf}(f)$ is the input-referred 1/f noise

$$R_{nf}(f) \cong \frac{\rho_n}{f\,W_1L_1} + \left(\frac{G_{ds1}}{G_{m1}}\right)^2 \frac{\rho_n}{n_2^2 f\,W_2L_2} = \frac{\rho_n}{f\,W_1L_1} \cdot (1+\eta_{fl}), \tag{2.18}$$

where

$$\eta_{fl} = \left(\frac{G_{ds1}}{n_2\,G_{m1}}\right)^2 \frac{W_1L_1}{W_2L_2} \tag{2.19}$$

represents the contribution to the input-referred flicker noise of the cascode transistor M_2 relative to the driver transistor M_1. If M_1 and M_2 have about the same area, then $\eta_{fl} \ll 1$, meaning that the contribution of the cascode transistor to the input-referred flicker noise is negligible.

The γ_n noise factor of the cascode stage is given by

$$\gamma_{cas} \triangleq G_{meq} \cdot R_{nt} = G_{m1} \cdot R_{nt} = \gamma_{n1} \cdot (1+\eta_{th}) \cong \gamma_{n1}, \tag{2.20}$$

since $G_{m1}G_{ms2} \gg G_{ds1}^2$. The contribution of the cascode transistor to the overall noise excess factor is therefore negligible. The same remark holds for the 1/f noise. Indeed, assuming M_1 and M_2 have the same area and $G_{m1}/G_{ds1} \gg 1$, (2.18) simplifies to

$$R_{nf}(f) \cong \frac{\rho_n}{f\,W_1L_1}, \tag{2.21}$$

which corresponds to the contribution of M_1 only.

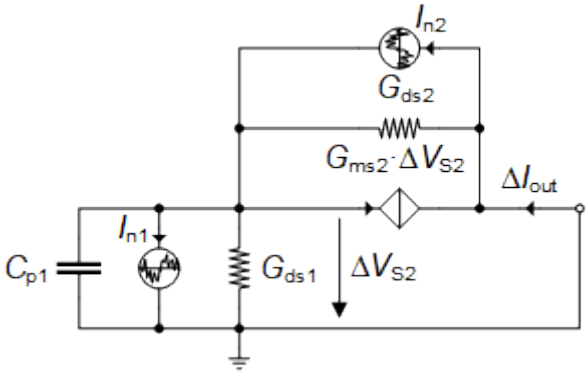

Figure 2.7: Small-signal schematic of the cascode stage for the calculation of the output noise including the effect of the parasitic capacitance C_{p1}

Similarly, the impact of the parasitic capacitance on the noise can be calculated from Figure 2.7. The output noise conductance is then given by

$$G_{nout} = |H_{n1}(\omega)|^2 \cdot G_{n1} + |H_{n2}(\omega)|^2 \cdot G_{n2}, \tag{2.22}$$

where

$$H_{n1}(s) = \frac{G_{ms2}+G_{ds2}}{G_{ms2}+G_{ds1}+G_{ds2}} \cdot \frac{1}{1+s/\omega_p} \cong \frac{1}{1+s/\omega_p} \tag{2.23}$$

$$H_{n2}(s) = \frac{G_{ds1}}{G_{ms2}+G_{ds1}+G_{ds2}} \cdot \frac{1+s/\omega_z}{1+s/\omega_p} \cong \frac{G_{ds1}}{G_{ms2}} \cdot \frac{1+s/\omega_z}{1+s/\omega_p}. \tag{2.24}$$

The magnitude of H_{n1} and H_{n2} versus frequency are sketched in Figure 2.8. For $\omega \ll \omega_z \ll \omega_p$, $H_{n1} \cong 1$ and $H_{n2} \cong G_{ds1}/G_{ms2}$ which is the result obtained above. However, for $\omega_z \ll \omega_p \ll \omega$, $H_{n1} \cong \omega_p/s$

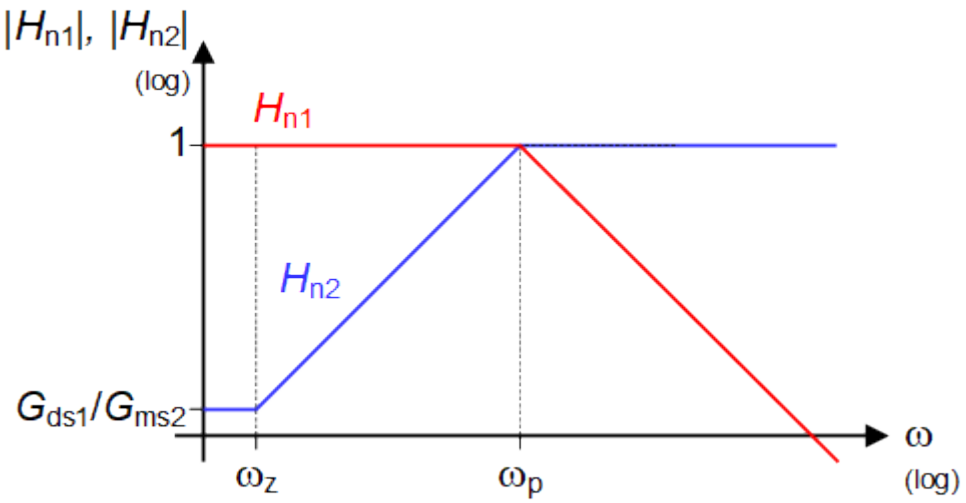

Figure 2.8: Noise transfer functions H_{n1} and H_{n2} versus frequency.

and $H_{n2} \cong 1$. We see that the cascode effect is lost since the noise of M_2 is no more divided by the cascode gain G_{ms2}/G_{ds1} but is entirely transferred to the output.

As a conclusion, adding a cascode stage reduces the output conductance without penalty on the noise, but at the cost of a slight voltage overhead for maintaining M_2 in saturation. This is only true for $\omega < \omega_z = G_{ds1}/C_{p1}$. For frequencies $\omega \gg \omega_p = G_{ms2}/C_{p1}$ the cascode effect is lost. Note that in order to maximize G_{ms2} at a given current and minimize its saturation voltage, M_2 should be biased in weak inversion.

We now will use the above equations to design the cascode gain stage.

3 Design

3.1 Circuit

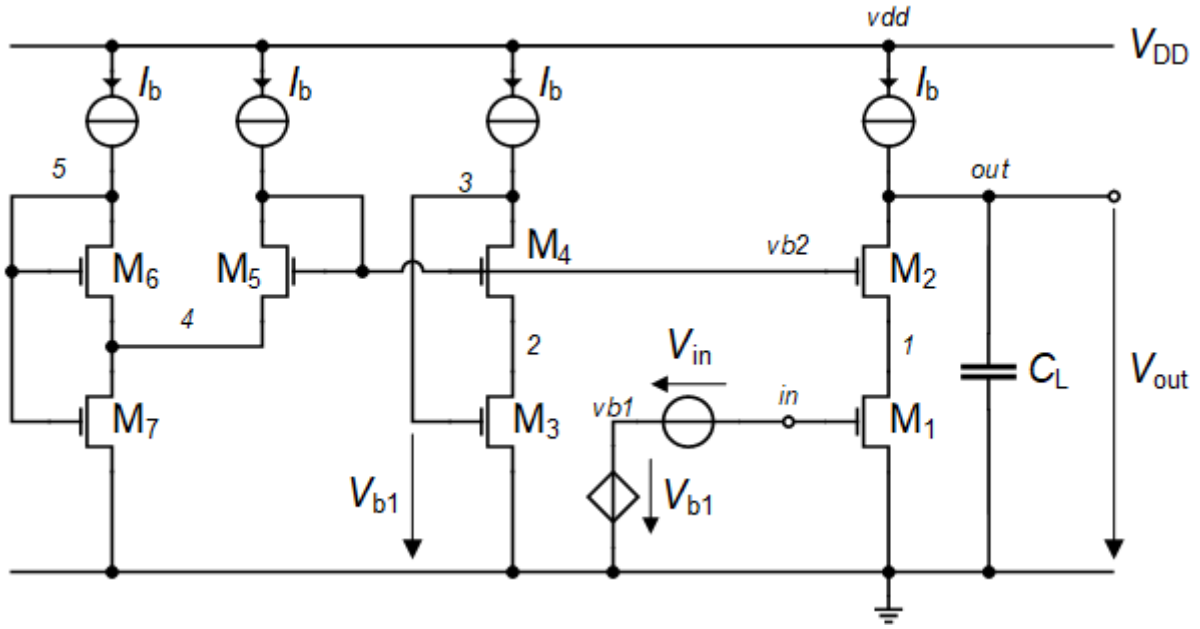

Figure 3.1: Cascode gain stage including the bias circuit.

The schematic of the cascode gain stage is shown in Figure 3.1. We have included the bias circuit made of transistors M_3 to M_7. Transistors M_3 and M_4 are added to correctly set the gate bias voltage of M_1 for the the bias current I_b for the simulation. M_3 and M_4 are made identical to M_1 and M_2, respectively. They are sharing the same cascode bias voltage V_{b2} generated by transistors M_5, M_6 and M_7. Assuming that transistors M_5, M_6 and M_7 are all biased in weak inversion, it can be shown that the drain voltage V_{D1} (voltage at node 1), is given by

$$V_{D1} = U_T \cdot \ln\left[\frac{\beta_2}{\beta_5}\left(1 + 2\,\frac{\beta_6}{\beta_7}\right)\right], \tag{3.1}$$

where

$$\beta = \frac{I_{spec}}{2nU_T^2} = \mu\, C_{ox}\,\frac{W}{L}. \tag{3.2}$$

The bias voltage V_{D1} should be at least $4\,U_T$. If we make M_5 identical to M_2 and M_4, then $\beta_2/\beta_5 = 1$. To get $V_{D1} = 4\,U_T$ would require $\beta_6/\beta_7 \cong 54$ which is prohibitive. We therefore need to take advantage of the additional degree of freedom choosing $\beta_2 > \beta_5$. For example if we take $\beta_2/\beta_5 = \beta_6/\beta_7 = 5$ we get $V_{D1} \cong 4\,U_T$.

3.2 Specifications

We will design the cascode gain stage for the specifications given in Table 3.1, namely a given gain-bandwidth product GBW and DC gain A_{dc}. Note that, contrary to the common-source optimization,

in this design, increasing the width of M_1 does not increase the load capacitance but increases the parasitic capacitance C_{p1} at the cascode node.

Table 3.1: Specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	100	-
Minimum DC gain	A_{dc}	40	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF

3.3 Process

We will design the cascode gain stage for the open source IHP 13G2 BiCMOS process [4]. The physical parameters are given in Table 3.2, the global process parameters in Table 3.3 and finally the MOSFET parameters in Table 3.4.

> **Warning**
>
> The matching parameters for IHP 130nm are unknown. We will use those from a generic 180nm technology.

Table 3.2: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.865	mV

Table 3.3: Process parameters.

Parameter	Value	Unit	Comment
t_{ox}	2.24	nm	SiO_2 oxyde thickness
C_{ox}	15.413	$\frac{fF}{\mu m^2}$	Oxyde capacitance per unit area
V_{DD}	1.2	V	Nominal supply voltage
L_{min}	130	nm	Minimum drawn gate length
W_{min}	150	nm	Minimum drawn gate width
z_1	340	nm	Minimum outer diffusion width
z_2	389	nm	Minimum diffusion width between two fingers

Table 3.4: Transistors parameters.

Parameter	nMOS	pMOS	Unit
Length and width correction parameters for current			
DL	59	51	nm
DW	-20	30	nm
Length and width correction for intrinsic and overlap capacitances			
$DLCV$	93	146	nm
$DWCV$	-10	15	nm

Table 3.4: Transistors parameters.

Parameter	nMOS	pMOS	Unit
Length and width correction parameter for fringing capacitances			
$DLGCV$	34	96	nm
$DWGCV$	10	-15	nm
Long-channel sEKV parameters parameters			
n	1.22	1.23	-
$I_{spec\square}$	708	245	nA
V_{T0}	246	365	mV
Short-channel sEKV parameters parameters			
L_{sat}	7.1	24.9	nm
λ	1.375	6.078	$\frac{V}{\mu m}$
Junction capacitances parameters			
C_J	0.976	0.863	$\frac{fF}{\mu m^2}$
C_{JSWSTI}	0.025	0.032	$\frac{fF}{\mu m}$
C_{JSWGAT}	0.03	0.027	$\frac{fF}{\mu m}$
Overlap capacitances parameters			
C_{GSo}	0.453	0.443	$\frac{fF}{\mu m}$
C_{GDo}	0.453	0.443	$\frac{fF}{\mu m}$
C_{GBo}	0	0.022	$\frac{fF}{\mu m}$
Fringing capacitances parameters			
C_{GSf}	0.2	0.1	$\frac{fF}{\mu m}$
C_{GDf}	0.2	0.1	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	2.208e-24	1.2e-23	VAs
AF	1	1	-
ρ	0.008642	0.04697	$\frac{Vm^2}{As}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$

As shown in Figure 3.2, it is worth notting that the threshold voltage in saturation is strongly dependent on the gate length [5]. From Figure 3.2, we see that the threshold voltage for a long-channel transistor with $V_{SB} = 0$ is as low as $V_{T0} \cong 50\,mV$. It then increases to about $V_{T0} \cong 250\,mV$ for a short-channel transistor. This threshold voltage change (about 200 mV) can have an important impact on the bias voltages, such as the voltages generated by the bias circuit shown in Figure 3.1.

3.4 Design procedure

3.4.1 Sizing of M_1

M_1 is biased in weak inversion in order to maximize the current efficiency and is sized according to the specification on the GBW and the load capacitance according to

$$GBW = \frac{G_{m1}}{2\pi C_L}. \tag{3.3}$$

The gate transconductance of M_1 G_{m1} in deep weak inversion is given by

$$G_{m1} = \frac{I_b}{nU_T}. \tag{3.4}$$

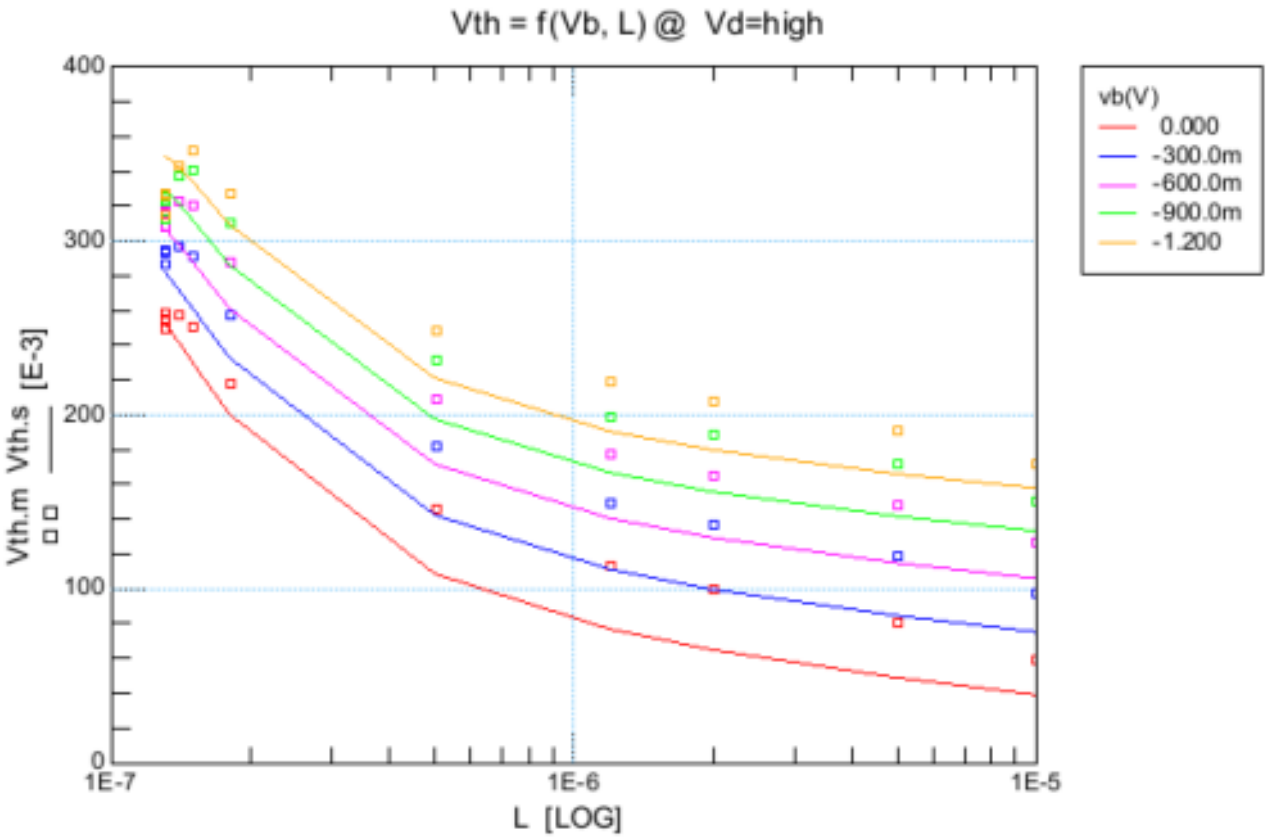

Figure 3.2: Threshold voltage of nMOS transistor in saturation versus gate length L.

The bias current I_b must satisfy the following inequality

$$I_b \geq 2\pi n_{0n} U_T C_L GBW_{min}, \tag{3.5}$$

which for the given specifications gives $I_{b,min} = 198\ nA$.

To have some margin to account for the additional parasitic capacitance at the output that add to the load capacitance C_L, we set $I_b = 250\ nA$ and the inversion coefficient of M_1 to $IC_1 = 0.1$. The transconductance can be calculated from the G_m/I_D function as

$G_{m1} = \frac{I_b}{n_{0n}\, U_T} \cdot gmsid(IC_1) = 7.258\ \frac{\mu A}{V}$.

This leads to a gain-bandwidth product

$GBW = \frac{G_{m1}}{2\pi\, C_L} = 1.2\ MHz$,

which is slightly higher than the target specification offering some margin.

Knowing the drain current I_{D1} and the inversion coefficient, we can calculate the W/L aspect ratio for M_1 as

$\frac{W_1}{L_1} = \frac{I_b}{I_{spec\square n}\, IC_1} = 3.5.$

To choose the length of M_1, we can split the gain equally between the driver transistor $A_{v1} = G_{m1}/G_{ds1}$ and the cascode transistor $A_{v2} = G_{ms2}/G_{ds2}$. This leads to $A_{v1} = A_{v2} = 10$ giving the desired overall gain of $A_{dc} = 40$ dB. We can then deduce the transistor length and width as

$L_1 = 250\ nm$ and

$W_1 = 880\ nm$.

Before sizing M_2 we need to size M_5.

3.4.2 Sizing the bias circuit

Since we need to bias M_2, M_4 and M_5 in weak inversion we need to make sure that that M_2 and M_4 remain in weak inversion despite they are much wider than M_5 and biased with the same current I_b. For this reason we start sizing M_5 first. Since we know the drain current of M_5, if we choose its inversion coefficient we get the W/L. Let's choose $IC_5 = 0.1$ for which we get $W/L = 3.530$. As mentioned above, we need to be careful choosing the length of M_5 because of the strong dependence of the threshold voltage to the transistor length. Since the bias circuit is based on the assumption that all the transistors have the same threshold voltage, it is safer to choose the same length for all transistors. We can choose L_1 since we already have chosen it. Therefore $L_7 = L_6 = L_5 = L_4 = L_3 = L_2 = L_1 = 250\ nm$. This leads to $W_5 = 880\ nm$ and $L_5 = 250\ nm$.

Note that choosing $L_2 = L_1$ leads to $G_{ds2} \cong G_{ds1}$ since M_1 and M_2 carry the same current. The DC gain of the cascode transistor G_{ms2}/G_{ds2} should be slightly larger than the DC gain of the driver transistor $G_{m1}/G_{ds1} = 10$, because $G_{ms2} > G_{m1}$. The DC gain should therefore be achieved.

Since M_7 carries twice the current of M_1, if we want M_7 to have the same inversion coefficient than M_1, we need to choose $W_7 = 2\,W_1 = 1.76\ \mu m$. The width of M_6 needs to be 5 times larger than W_7 leading to $W_6 = 5\ W_7 = 8.80\ \mu m$.

Finally M_3 is taken identical to M_1 resulting in $W_3 = W_1 = 0.88\ \mu m$ and $L_3 = 250\ nm$.

3.4.3 Sizing of M_2

We can now finalize the design by sizing M_2. In order to save voltage headroom we need to bias M_2 in weak inversion. This is done by choosing W_2 to be 5 times W_5, leading to $W_2 = 4.40\ \mu m$ with $L_2 = 250\ nm$. With these dimensions, the inversion coefficient of M_2 is 5 times smaller than that of M_5, $IC_2 = 0.020$, which is making sure that M_2 is biased in weak inversion. We can now check the DC gain. The source transconductance and output conductance of M_2 are equal to $G_{ms2} = 9.479\ \mu A/V$ and $G_{ds2} = 727.273\ nA/V$. This leads to a cascode voltage gain of $A_{v2} = 13.03$ and an overall gain $A_{dc} = 42.30\ dB$ which, as expected, is slightly higher than the specs.

The sizing procedure is now finished and is summarized in the next section.

3.5 Summary

3.5.1 Specifications

The specifications are recalled in Table 3.5.

Table 3.5: Specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	40	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF

3.5.2 Bias

The bias information are summarized in Table 3.6.

Table 3.6: Bias information.

Bias voltage or current	Symbol	Value	Unit
Supply voltage	V_{DD}	1.2	V
Bias current	I_b	250	nA

3.5.3 Transistor information

The transistor sizes and bias information are summarized in Table 3.7 and Table 3.8, respectivily. Table 3.9 gives the small-signal and thermal noise parameters. An Excel table is generated with more information (e.g. all the parasitic capacitances).

Table 3.7: Transistor size information.

Transistor	W $[\mu m]$	L $[\mu m]$	W_{eff} $[\mu m]$	L_{eff} $[\mu m]$	W/L	AD $[\mu m^2]$	PD $[\mu m]$
M1	0.88	0.25	0.900	0.191	4.708	0.299	2.440
M2	4.40	0.25	4.420	0.191	23.123	1.496	9.480
M3	0.88	0.25	0.900	0.191	4.708	0.299	2.440
M4	4.40	0.25	4.420	0.191	23.123	1.496	9.480
M5	0.88	0.25	0.900	0.191	4.708	0.299	2.440
M6	8.80	0.25	8.820	0.191	46.141	2.992	18.280
M7	1.76	0.25	1.780	0.191	9.312	0.598	4.200

Table 3.8: Transistor bias information.

Transistor	I_D $[nA]$	I_{spec} $[nA]$	IC	$V_P - V_S$ $[mV]$	$V_G - V_{T0}$ $[mV]$	V_{DSsat} $[mV]$
M1	250	3335	0.075	-65	-53	104
M2	250	16378	0.015	-108	-88	104
M3	250	3335	0.075	-65	-53	104
M4	250	16378	0.015	-108	-88	104
M5	250	3335	0.075	-65	-53	104
M6	250	32682	0.008	-126	-103	104
M7	500	6596	0.076	-65	-53	104

Table 3.9: Transistor small-signal and thermal noise parameters.

Transistor	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M1	128.933	9.033	7.404	727.273	0.623
M2	633.206	9.522	7.805	727.273	0.613
M3	128.933	9.033	7.404	727.273	0.623
M4	633.206	9.522	7.805	727.273	0.613
M5	128.933	9.033	7.404	727.273	0.623
M6	1263.547	9.593	7.863	727.273	0.612
M7	255.002	18.053	14.798	1454.545	0.623

4 Theoretical estimations

We can now check the transfer function and the input-referred noise PSD.

4.1 Transfer function

The parameters that are required to evaluate the transfer function are calculated in Table 4.1.

Table 4.1: Small-signal parameters required to calculate the transfer function.

Symbol	Theoretical Value	Unit
A_{dc}	43	dB
G_{m1}	7.404	$\mu A/V$
G_{ms2}	9.522	$\mu A/V$
f_c	7.669	kHz
GBW	1.1	MHz

Using the values given in Table 4.1, we can now plot the transfer function which is plotted in Figure 4.1.

4.2 Input-referred noise

We can now compute all the parameters needed for the calculation of the OTA thermal noise excess factor and its input-referred thermal noise resistance. They are given in Table 4.2.

> **Warning**
>
> In order to check the effect of the cascode on the noise, we will ignore the noise contribution of the bias circuit. Of course in reality the bias circuit will also contribute to the output noise.

Table 4.2: Thermal noise parameters.

Symbol	Theoretical Value	Unit
G_{m1}	7.404	$\mu A/V$
G_{ms2}	9.522	$\mu A/V$
G_{ds1}	0.727	$\mu A/V$
$G_{m1}\,G_{ms2}/G_{ds1}^2$	133.295	-
γ_{n1}	0.623	-
δ_{n2}	0.502	-
η_{th}	0.006048	-
R_{nt}	84.696	$k\Omega$
γ_{cas}	0.627	-
$\sqrt{S_{ninth}}$	37.469	$nV/\sqrt{Hz}$

Table 4.2: Thermal noise parameters.

Symbol	Theoretical Value	Unit
$10 \cdot \log(S_{ninth})$	-148.527	$dBv/\sqrt{Hz}$

Table 4.3: Flicker noise parameters.

Symbol	Theoretical Value	Unit
$(n_2\, G_{m1}/G_{ds1})^2$	154.3	-
$\frac{W_1 \cdot L_1}{W_2 \cdot L_2}$	0.2	-
η_{fl}	0.001	-
$\sqrt{S_{ninfl}(1\,Hz)}$	28.9	$\mu V/\sqrt{Hz}$
$10 \cdot \log(S_{ninfl}(1\,Hz))$	-90.8	$dBv/\sqrt{Hz}$
f_k	929	kHz

We can plot the input-referred noise PSD which is shown in Figure 4.2.

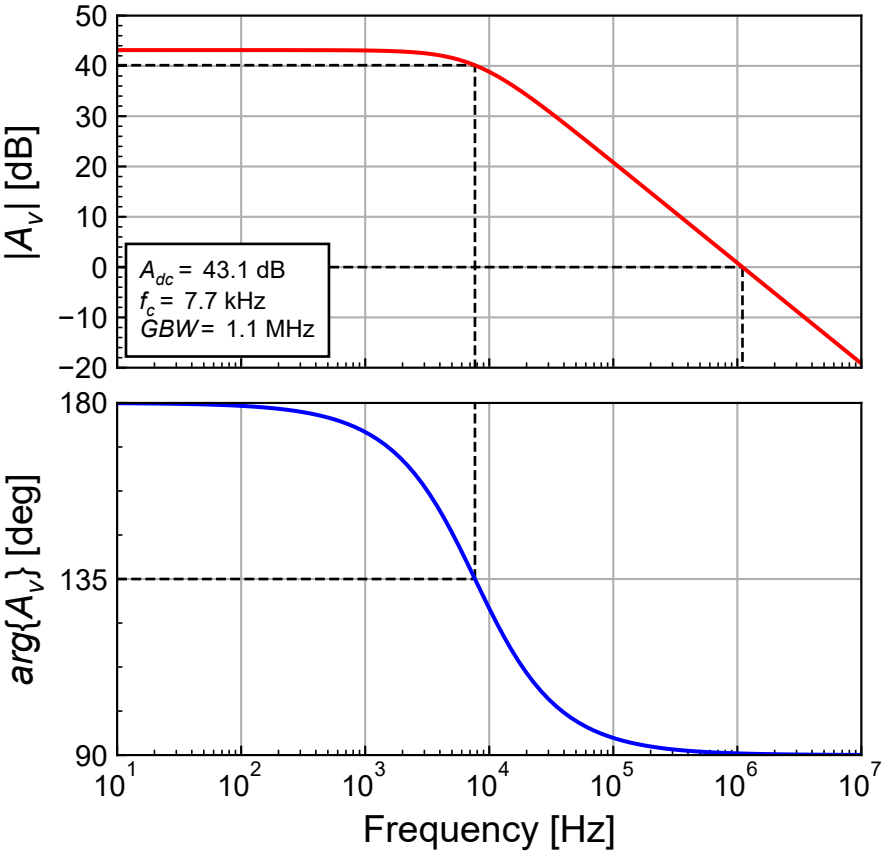

Figure 4.1: Theoretical transfer function.

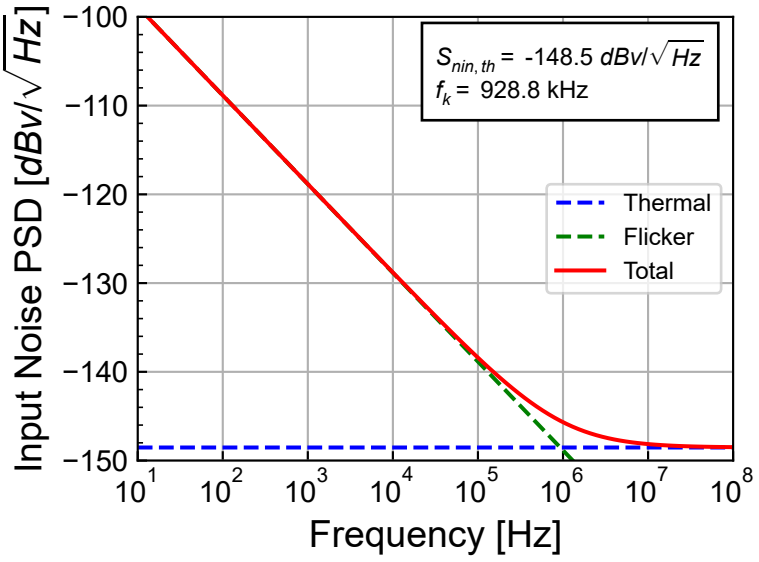

Figure 4.2: Theoretical input-referred noise PSD.

5 Validation by simulation

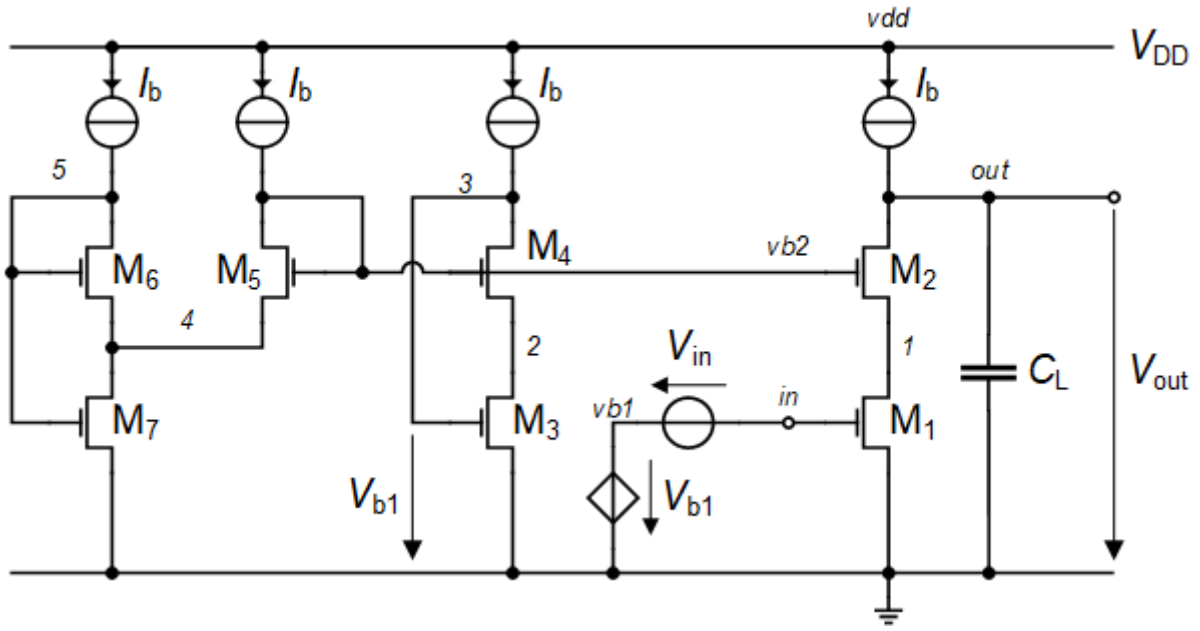

Figure 5.1: Schematic of the cascode gain stage used for simulation.

The above design can be verified using ngspice simulations. We will use the circuit shown in Figure 5.1 to run the simulations. Note that the bias voltage V_{b1} is generated by the additonal current branch with M_3 and M_4. In this way we ensure that the DC gate voltage of M_1 actually corresponds to its drain current. The bias voltage V_{b2} is generated by transistors M_5, M_6 and M_7.

> **Note**
>
> The simulations are performed with the PSP 103.6 compact model [6]. For ngspice, we use the Verilog-A implementation given in the IHP package [4] and compiled the OSDI file with OpneVAF [7] to run with ngspice [8]. In addition to the PSP user manual [6] a documentation of PSP and other MOSFET compact models and their parameter extraction can be found in [9].

We start checking the transistors operating point in the next section.

5.1 Operating point

Before running the AC and NOISE simulations, we first need to check the quiescent voltages and currents and the operating points of all transistors by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 5.1. The transistor drain current and voltages are presented in Table 5.2. The small-signal parameters are given in Table 5.3 and the noise PSD are given in Table 5.4.

Table 5.1: Cascode gain stage node voltages.

Node	Voltage
vdd	1.2
in	0.302368
out	0.302368
vb1	0.302368
vb2	0.409582
1	0.159909
2	0.159909
3	0.302368
4	0.103188
5	0.302163

Table 5.2: PSP operating point information extracted from ngspice .op file for each transistor.

Transistor	$I_D\ [nA]$	$V_{GS}\ [mV]$	$V_{DS}\ [mV]$	$V_{SB}\ [mV]$	$V_{GS}-V_T\ [mV]$	$V_{Dsat}\ [mV]$
M1	250	302	160	0	-49	116
M2	250	250	142	160	-104	115
M3	250	302	160	0	-49	116
M4	250	250	142	160	-104	115
M5	250	306	306	103	-58	116
M6	250	199	199	103	-131	114
M7	500	302	103	0	-47	117

Table 5.3: PSP small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	$G_m\ [\mu A/V]$	$G_{mb}\ [\mu A/V]$	$G_{ds}\ [nA/V]$
M1	6.729	0.971	520.208
M2	7.408	0.954	638.083
M3	6.729	0.971	520.208
M4	7.408	0.954	638.083
M5	6.823	0.899	429.712
M6	7.501	0.959	536.693
M7	13.424	1.933	1418.369

Table 5.4: PSP noise operating point information extracted from ngspice .op file for each transistor.

Transistor	$S_{ID,th}\ [A^2/Hz]$	$S_{ID,fl}$ at 1Hz $[A^2/Hz]$
M1	7.304e-26	2.778e-20
M2	7.676e-26	6.483e-21
M3	7.304e-26	2.778e-20
M4	7.676e-26	6.483e-21
M5	7.179e-26	2.233e-20
M6	7.523e-26	2.993e-21
M7	1.549e-25	6.015e-20

Table 5.5: sEKV parameters calculated from the values extracted from the simulation.

Transistor	W_{eff} $[\mu m]$	L_{eff} $[\mu m]$	W_{eff}/L_{eff}	I_{spec} $[\mu A]$	IC
M1	0.900	0.191	4.708	3.335	0.075
M2	4.420	0.191	23.123	16.378	0.015
M3	0.900	0.191	4.708	3.335	0.075
M4	4.420	0.191	23.123	16.378	0.015
M5	0.900	0.191	4.708	3.335	0.075
M6	8.820	0.191	46.141	32.682	0.008
M7	1.780	0.191	9.312	6.596	0.076

Table 5.6: sEKV small-signal parameters calculated from the values extracted from the simulation.

Transistor	G_{spec} $[\mu A/V]$	n	G_m $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_{ds} $[nA/V]$
M1	128.933	1.144	6.729	7.700	520.208
M2	633.206	1.129	7.408	8.362	638.083
M3	128.933	1.144	6.729	7.700	520.208
M4	633.206	1.129	7.408	8.362	638.083
M5	128.933	1.132	6.823	7.721	429.712
M6	1263.547	1.128	7.501	8.460	536.693
M7	255.002	1.144	13.424	15.357	1418.369

Table 5.7: sEKV noise parameters calculated from the values extracted from the simulation.

Transistor	$\sqrt{S_{nin,th}}$ $[nV/\sqrt{Hz}]$	$R_{nin,th}$ $[k\Omega]$	γ_n $[-]$	$\sqrt{S_{nin,fl}}$ $[nV/\sqrt{Hz}]$
M1	40.166	97.329	0.655	24768.869
M2	37.398	84.377	0.625	10868.814
M3	40.166	97.329	0.655	24768.870
M4	37.398	84.377	0.625	10868.820
M5	39.272	93.045	0.635	21900.429
M6	36.567	80.665	0.605	7294.033
M7	29.319	51.860	0.696	18270.585

Table 5.8: Bias voltages and operating regions of each transistor.

Trans.	Type	V_G $[V]$	V_S $[V]$	V_D $[V]$	V_{DS} $[mV]$	V_{DSsat} $[mV]$	Reg.	Sat.
M1	n	0.302	0.000	0.160	160	116	WI	sat
M2	n	0.410	0.160	0.302	142	115	WI	sat
M3	n	0.302	0.000	0.160	160	116	WI	sat
M4	n	0.410	0.160	0.302	142	115	WI	sat
M5	n	0.410	0.103	0.410	306	116	WI	sat
M6	n	0.302	0.103	0.302	199	114	WI	sat
M7	n	0.302	0.000	0.103	103	117	WI	lin

From Table 5.1, we observe that the drain voltage of M_1 (voltage at node 1) is $V_{D1} = V(1) = 160\ mV$ which is sligtly larger than $4\,U_T = 104\ mV$. This comes from the fact that transistor M_5 is not biased deep in weak inversion but with an inversion coefficient $IC_5 = 0.075$ which makes its V_{GS} voltage larger moving the voltage at node 1 a bit higher.

The V_{DS} voltages of Table 5.2 are all larger than the V_{Dsat} voltages, confirming that all the transistors are biased in saturation. This is also confirmed in Table 5.8.

Comparing to the theoretical values of Table 3.9, we see that the simulated transconductance values are slightly smaller than the theoretical values, while the simulated output conductances are smaller than the theoretical values.

5.2 Small-signal transfer function

After having checked the operating point and making sure that all transistors are biased in saturation, we can now perform the AC simulation. The simulation results are compared to the theoretical estimations in Figure 5.2. The simulated GBW is slightly smaller than the theoretical value but remains on target. The simulated DC gain is larger than the theoretical estimation.

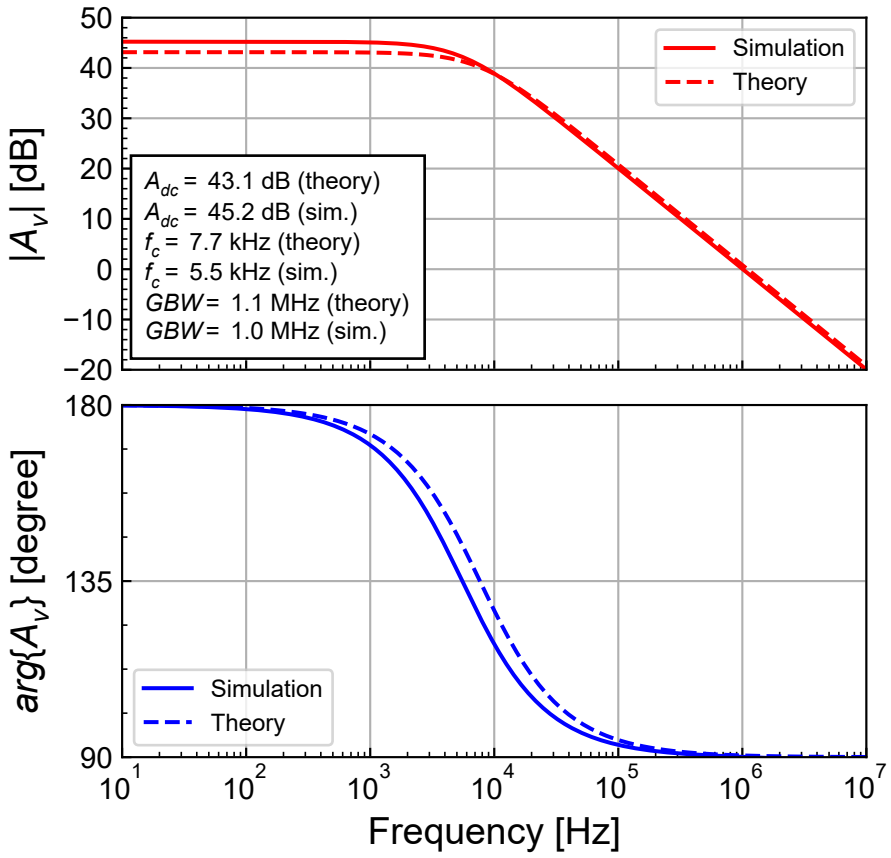

Figure 5.2: Simulated gain response compared to theoretical estimation.

5.3 Output resistance

We can check that the cascode significantly reduces the output conductance (increases the output resistance). In order to do this we add an AC current source at the output with zero DC value as shown in Figure 5.3. This AC current source will not change the oquiscent output voltage but will inject a small-signal current at the ouput. Measuring the output voltage we can then deduce the output admittance or impedance.

The result of the simulation is presented in Figure 5.4 where the simulated small-signal output impedance is plotted versus frequency and compared to $R_{ds1} = 1/G_{ds1}$, $R_{ds2} = 1/G_{ds2}$ and the

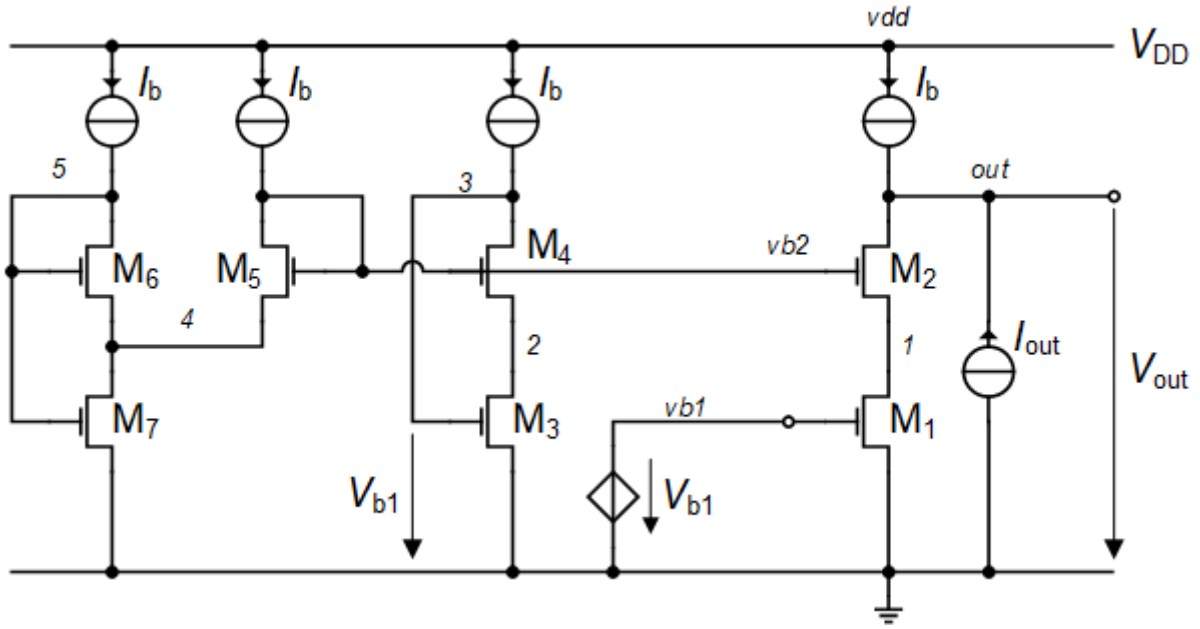

Figure 5.3: Schematic for simulating the output impedance.

theoretical expression

$$R_{out} = \frac{G_{ms2} + G_{ds1} + G_{ds2}}{G_{ds1}G_{ds2}} \cong \frac{G_{ms2}}{G_{ds1}G_{ds2}}. \tag{5.1}$$

The values of G_{ms2}, G_{ds1} and G_{ds2} are extracted from PSP. We see a perfect match between the simulation and theoretical value of R_{out}.

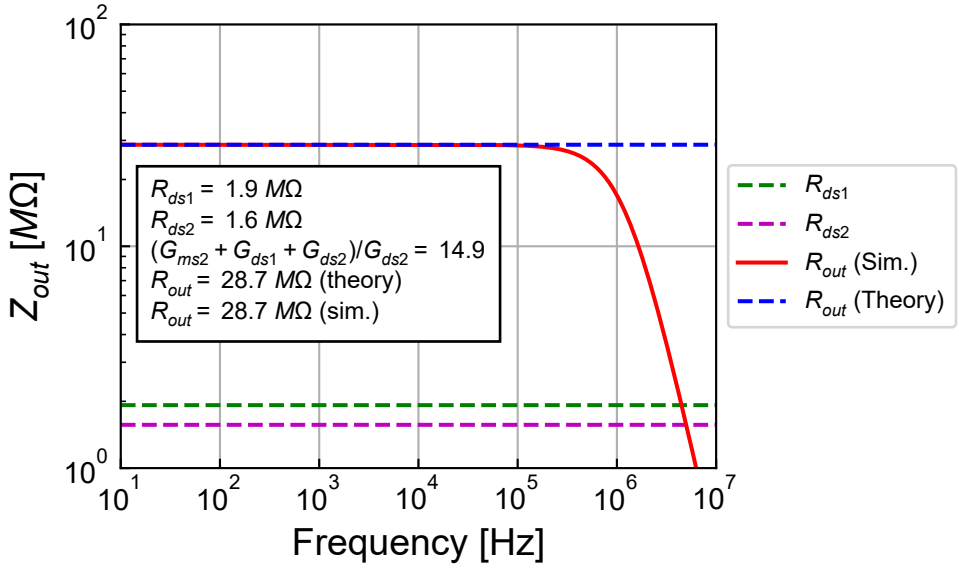

Figure 5.4: Simulated output resistance compared to theoretical value.

The output resistance is increased by a factor

$$R_{out} \cdot G_{ds1} = \frac{G_{ms2} + G_{ds1} + G_{ds2}}{G_{ds2}} \cong \frac{G_{ms2}}{G_{ds2}} \tag{5.2}$$

which is about $(G_{ms2} + G_{ds1} + G_{ds2})/G_{ds2} = 14.9$.

This demonstrates that adding a cascode transistor significantly improves the output resistance at the cost of slightly less voltage headroom. It is particularly usefull for this technology where the nMOS transistor have a very low output resistance.

5.4 Input-referred noise

We can now simulate the input-referred noise PSD and check whether the noise of the cascode transistor M_2 is indeed much lower than the noise of the driver transistor M_1. To avoid the noise contribution of the biasing circuit, we set the bias voltages V_{b1} and V_{b2} with two voltage sources having the appropriate values extracted from the OP simulation, namely $V_{b1} = 302\ mV$ and $V_{b2} = 410\ mV$. The input-referred noise PSD is plotted in Figure 5.5 and compared to the theoretical estimation. We see that the simulated white noise is reasonably close to the theoretical estimation, however the simulated flicker noise is smaller than the theoretical estimation. This comes from the fact that in PSP the gate-referred flicker noise is bias dependent which is not the case in the sEKV model.

The contributions of M_1 and M_2 to the input-referred white noise are shown in Figure 5.6. As expected, we can observe that the contribution of the cascode transistor M_2 is more than 20 dB lower than that of M_1.

Figure 5.7 shows that the contribution of M_2 to the input-referred flicker noise PSD. We can observe that the contribution of M_2 is also about 20 dB lower than that of M_1.

The breakdown of the contributions of M_1 and M_2 to the total input-referred noise is summarized in Figure 5.8 which shows again that the noise contribution of M_2 is more than 20 dB lower than that of M_1.

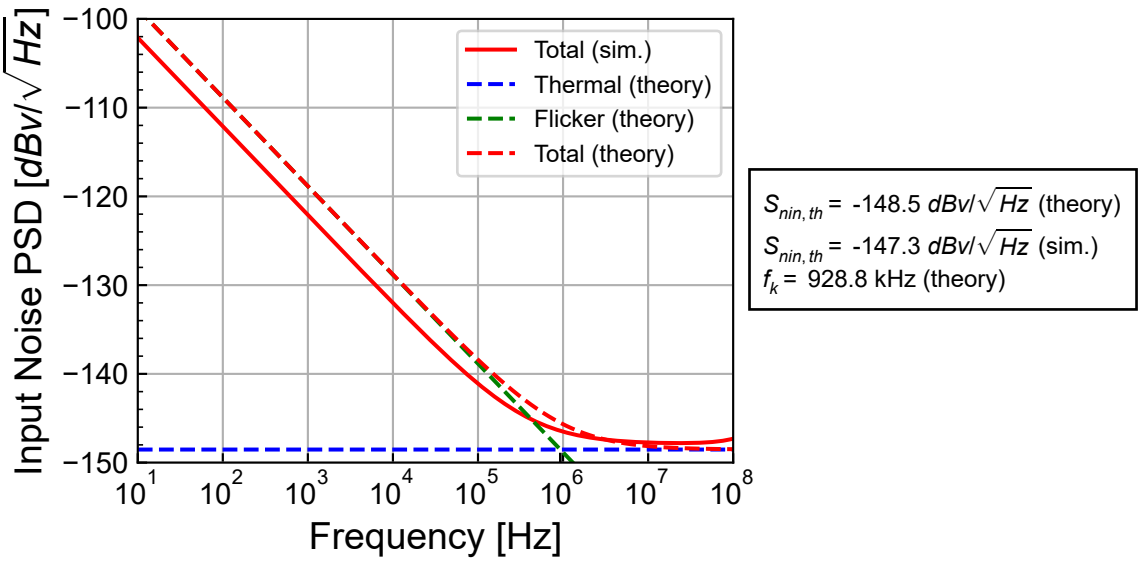

Figure 5.5: Simulated input-referred noise PSD compared to theoretical estimation.

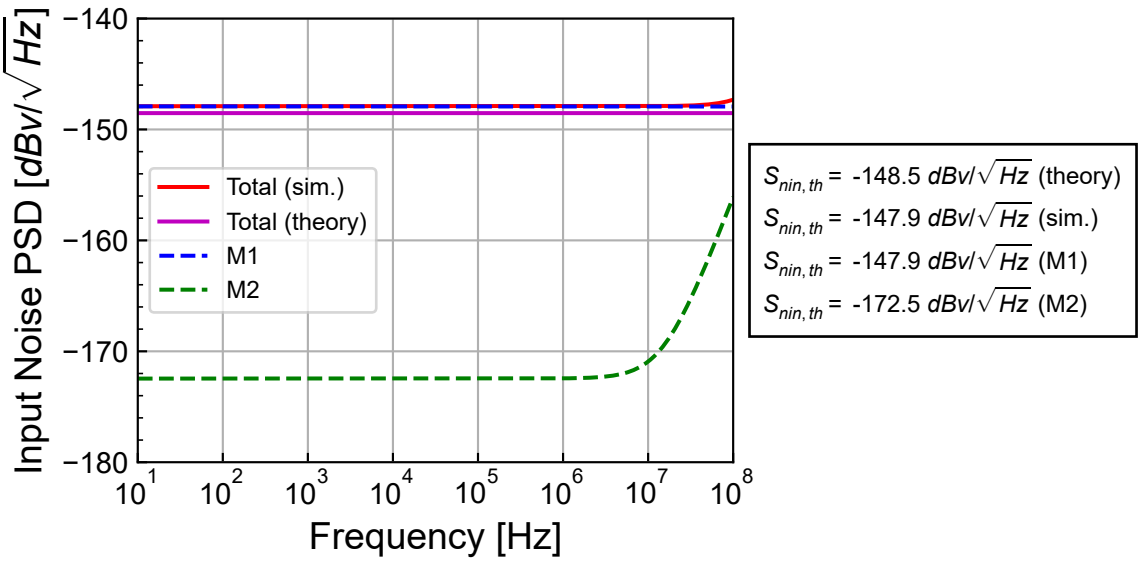

Figure 5.6: Breakdown of the contributions to the simulated input-referred white noise PSD.

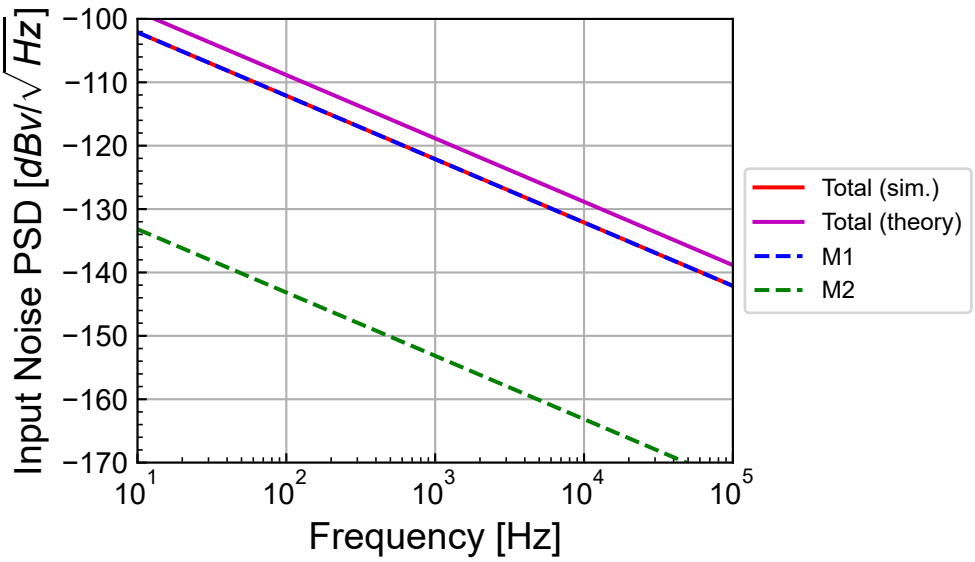

Figure 5.7: Breakdown of the contributions to the simulated input-referred flicker noise PSD.

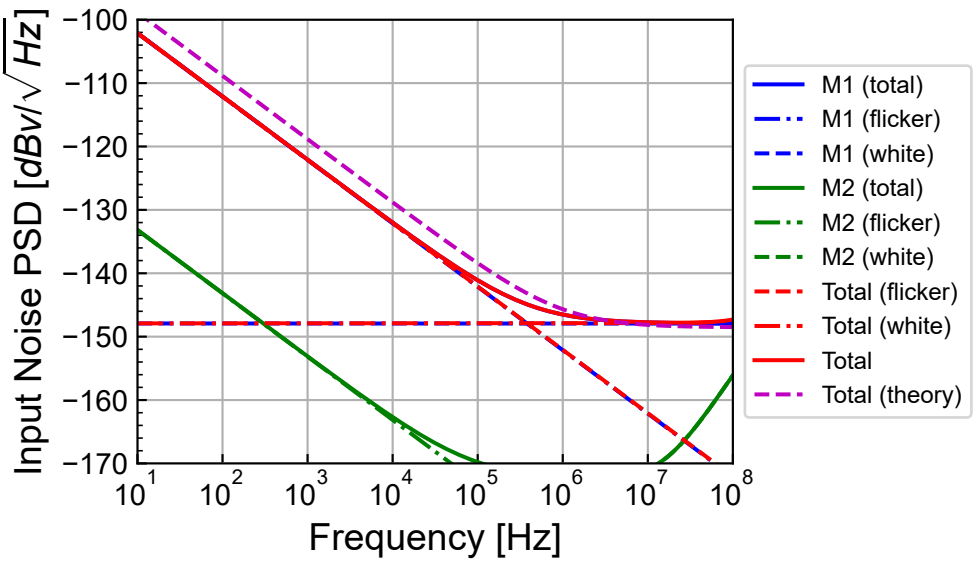

Figure 5.8: Breakdown of the contributions to the simulated input-referred noise PSD.

6 Conclusion

In this notebook, we have first analyzed the cascode gain stage showing that the DC voltage gain is equivalent to a two-stage amplifier. We also have shown that the output resistance is increased by the voltage gain of the cascode transistor. In addition, the noise of the cascode transistor is much lower than that of the driver transistor and can usually be neglected. We then have designed the cascode gain stage for achieving a certain DC gain and gain-bandwidth product for a given load capacitance for the IHP SG13G2 130nm BiCMOS technology. A particular attention was brought to the design of the bias circuit to make sure that both transistors M_1 and M_2 are biased in weak inversion and in saturation. The circuit was then simulated with ngspice for the chosen IHP 130nm CMOS process taking advantage of the open source PDK. The simulation results are usually quite close to the values predicted by the theory. The simulations have also confirmed the main features of the cascode gain stage, namely a high voltage gain, high output resistance and low-noise. These features are achieved without increase of the current consumption (except the bias circuit which is needed anyway) thanks to the current reuse feature of the cascode stage.

References

[1] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design*, 1st ed. John Wiley, 2006.

[2] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 1: The Simplified EKV Model for the Design of Low-Power Analog Circuits," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 3, pp. 26–35, 2017.

[3] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 2: Using the Inversion Coefficient as the Primary Design Parameter," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 4, pp. 73–81, 2017.

[4] IHP, "IHP SG13G2 Open Source PDK." https://github.com/IHP-GmbH/IHP-Open-PDK, 2025.

[5] IHP, "IHP SG13G2 DC CV NMOS LV Documentation (Rev. 1.2)." ihp-sg13g2/libs.doc/meas/MOS/doc/report_nmos_lv.pdf, 2023.

[6] G.D.J. Smit, A.J. Scholten, D.B.M. Klaassen, O. Rozeau, S. Martinie, T. Poiroux and J.C. Barbé, "PSP 103.6 - The PSP model is a joint development of CEA-Leti and NXP Semiconductors." https://www.cea.fr/cea-tech/leti/pspsupport/Documents/psp103p6_summary.pdf, 2017.

[7] SemiMod GmbH, "Open VAF." https://openvaf.semimod.de/docs/getting-started/introduction/, 2025.

[8] Dietmar Warning, "Verilog-A Models for Circuit Simulation." https://github.com/dwarning/VA-Models, 2024.

[9] Agilent Technologies, "IC-CAP 2008, Nonlinear Device Models - Volume 1." https://people.ece.ubc.ca/robertor/Links_files/Files/ICCAP-2008-doc/pdf/icmdl.pdf, 2008.