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The New CMC Standard Compact MOS Model PSP: Advantages for RF Applications

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***Abstract*—The surface-potential-based compact MOS model PSP is reviewed with special emphasis to features of interest to analog and RF designers. Various aspects of the model are discussed, such as Gummel symmetry, capacitance reciprocity at $V_{\rm DS} = 0$ V, parasitic resistances, junction modeling, distortion modeling, and noise modeling. Examples from circuit design are used to illustrate the benefits of the PSP model.**

***Index Terms*—Compact MOS models, distortion, noise, PSP model.**

I. Introduction

AT PRESENT, a consensus has been reached by both users and developers of compact MOSFET models that the surface-potential-based approach offers unique advantages for advanced circuit simulations. This is reflected by the adoption of the surface-potential-based PSP model as the next-generation standard MOSFET model by the Compact Model Council (CMC) [1], which operates within the framework of the Government Electronics and Information Technology Association (GEIA). Until 2005, the threshold-voltage-based BSIM model [2] from the University of Berkeley, California, had been the only standard MOSFET model of the CMC since its inception in 1995.

The PSP model is being jointly developed by Arizona State University [3] and the NXP-TSMC Research Center [4] and is part of a larger family of models which also contains the CMC-standard varactor model [5] and the PSP-SOI model [6]. The main difference between the BSIM models and the PSP model is that, while the BSIM models are threshold-voltage-based, the PSP model is surface-potential-based [7]. In threshold-voltage-based models, such as BSIM3, BSIM4, and MOS Model 9 [8], separate, non-intersecting expressions for *i)* the diffusion current in the subthreshold region (exponential in gate-source voltage) and *ii)* the drift current in the strong inversion region (a power of the gate-source voltage) are mathematically "glued" together. In surface-potential-based models, the diffusion and drift currents are expressed in terms of the surface potential. These equations are valid for all levels of inversion (sub-threshold, moderate, and strong inversion). The total drain current is the sum of drift and diffusion currents. This results in a more accurate, physics-based modeling of the transition region (see Fig. 1) and offers a sound basis for statistical modeling.

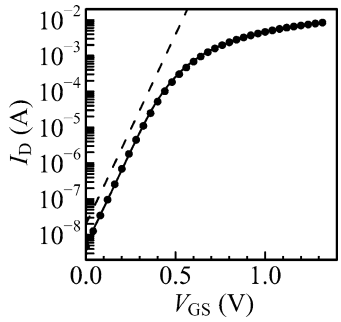

Fig. 1. Drain current $I_{\rm D}$ of an n-channel transistor with a gate width of 10 μm and a gate length of 0.04 μm as a function of $V_{\rm GS}$ at $V_{\rm DS} = 1.2$ V. Symbols represent measurements and the solid line represents the PSP model. The dashed line represents a simple exponential dependence on $V_{\rm GS}$.

This paper is an extended version of a conference paper [9] and is organized as follows. In Section 2 the various physical effects relevant for DC modeling will be discussed. It will be shown that PSP is able to model the MOSFET DC currents very accurately while retaining the desired Gummel symmetry properties (i.e., symmetric response around $V_{\rm DS} = 0$ V with continuous derivatives to at least 3rd order). The PSP capacitance model is the subject of Section 3. It will be demonstrated that at the—seemingly trivial—bias condition $V_{\rm DS} = 0$, PSP gives the result expected from physics, whereas other models fail to do so. In Section 4, various parasitic effects such as gate resistance and junction leakage will be discussed. It will also be demonstrated that the "JUNCAP Express" option alleviates the computational burden of the junction model to such an extent that PSP/BSIM4 simulation time ratios around 1 are achieved. In Section 5, PSP will be shown to give excellent results when used for distortion analysis. Finally, in Section 6, PSP's ability to accurately predict MOSFET noise behavior is demonstrated with the help of examples from RF circuit design.

II. DC Characteristics and Gummel Symmetry

The PSP model [10] was developed by selecting, combining, and enhancing the best features of the SP model (developed

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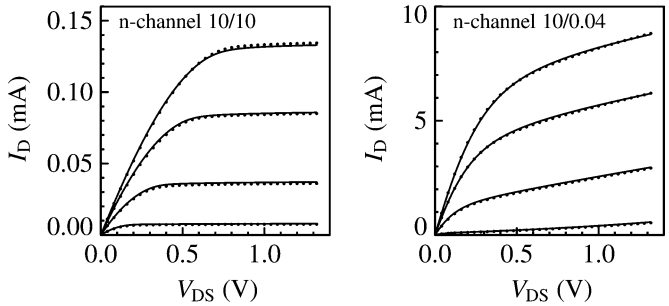

Fig. 2. Drain current I_D of n-channel transistors with a gate width of 10 μm and gate lengths of 10 μm (left) and 0.04 μm (right), as a function of V_{DS}. Symbols represent measurements and lines represent the PSP model. The gate-source voltages used in the measurements were $V_{GS} = 0.550, 0.825, 1.100,$ and 1.320 V.

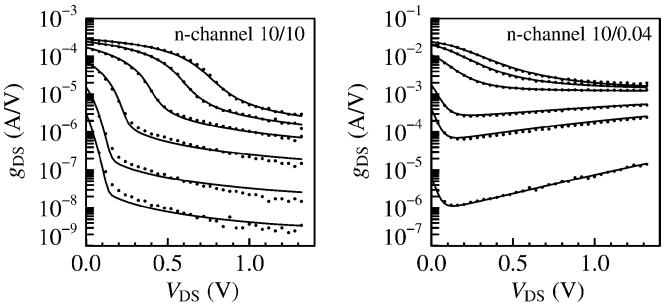

Fig. 3. Output conductance g_{DS} of n-channel transistors with a gate width of 10 μm and gate lengths of 10 μm (left) and 0.04 μm (right), as a function of drain-source voltage V_{DS}. Symbols represent measurements and lines represent the PSP model. The gate-source voltages used in the measurements were 0.275, 0.360, 0.550, 0.825, 1.100, and 1.320 V for the gate length of 10 μm (left), and 0.275, 0.457, 0.550, 0.825, 1.100, and 1.320 V for the gate length of 0.04 μm (right).

at The Pennsylvania State University) [11] and those of MOS Model 11 (developed at Philips Research) [12], [13]. The PSP model contains a sophisticated mobility model including velocity saturation and Coulomb scattering. All short-channel and narrow-width effects and features necessary to describe advanced CMOS technologies are incorporated in the PSP model (e.g., drain-induced barrier-lowering, reverse short-channel effect, channel-length modulation, etc.) [10]–[13]. The PSP model accurately describes the effects of poly-depletion and non-uniform lateral and vertical doping. Thin gate oxides cause both quantum-mechanical confinement effects in the inversion layer and tunneling currents through the thin gate oxide [14]. Due to the high doping gradients in the source and drain junctions of advanced MOSFETs, additional leakage currents occur, such as gate-induced drain and source leakage (GIDL, GISL) and tunneling currents (TAT, BBT) in the junctions themselves [15]. All of these leakage currents are accurately modeled with the PSP model. Technology-related effects caused by STI stress and proximity of deep wells (WPE) are also included in the PSP model. The model for the overlap capacitances is also surface-potential-based. Features of the PSP model that are of special importance for RF applications include the extensive noise modeling, the description of non-quasi-static (or transit time) effects [16], and the option for external gate and bulk resistances. The noise modeling in the PSP model comprises flicker (or $1/f$) noise, thermal noise, induced gate noise, and shot noise. An overview of all modeled effects and a full list of all model parameters can be found in the model documentation [3], [4]. Figs. 2 and 3 show that both long-channel and short-channel devices of an advanced 45 nm CMOS technology are accurately described by the PSP model, using a single set of parameters (i.e., the "global model" approach). Note that, besides this global model approach, PSP also has a binning option.

Normal MOSFETs are symmetrical devices with respect to source-drain interchange. In compact modeling, only expressions for positive drain-source voltage are being derived [e.g., $I^{+}_{DS}(V_D, V_G, V_S, V_B)$]. At negative drain-source voltages, the source-drain interchange mechanism is applied, i.e., $I^{-}_{DS}(V_D, V_G, V_S, V_B) = -I^{+}_{DS}(V_S, V_G, V_D, V_B)$. Special care should be taken to ensure that the expressions are at least C^3-continuous at zero drain-source bias (i.e., third-order

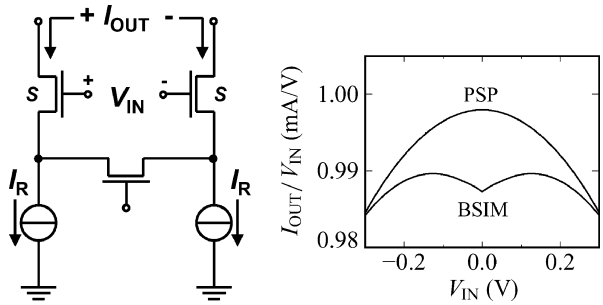

Fig. 4. Variable transconductance (or V-I converter) circuit (left) and its transfer characteristic (right) simulated with BSIM and PSP. Only a Gummel-symmetric model (e.g., PSP) gives realistic, smooth, output characteristics.

derivatives exist and are continuous). Although in principle this can be achieved with threshold-voltage-based models, the surface potential formalism gives a much more solid base upon which to achieve this C^3-continuity and build a truly symmetrical model [17]. Fig. 4 shows the example of a variable-transconductance circuit [18]. In this circuit, the magnitude of the transfer is determined by the gate voltage of the middle transistor, which is at zero DC drain-source bias and determines the shape of the transfer characteristic. For a Gummel-symmetrical model like PSP, the transfer curve is smooth at $V_{IN} = 0$ V, while for an asymmetrical model like BSIM, even the first-order derivative of the transfer curve is not defined at $V_{IN} = 0$ V.

III. Capacitances

The MOSFET (trans-)capacitances C_{ij} (with $i, j = D, G, S,$ or B) are given by

$$C_{ij} = (2 \cdot \delta_{ij} - 1) \cdot \frac{\partial Q_i}{\partial V_j} \tag{1}$$

where Q_i and V_j are the terminal charges and voltages, respectively, and δ_{ij} is the Kronecker delta. Gummel symmetry requirements, similar to those discussed in the previous section, can also be derived for these MOSFET capacitances [19]. PSP fulfills these Gummel symmetry requirements for capacitances, as shown in [19]. Here, we focus on another implication of the symmetry of a MOSFET, i.e., that at zero drain-source bias the

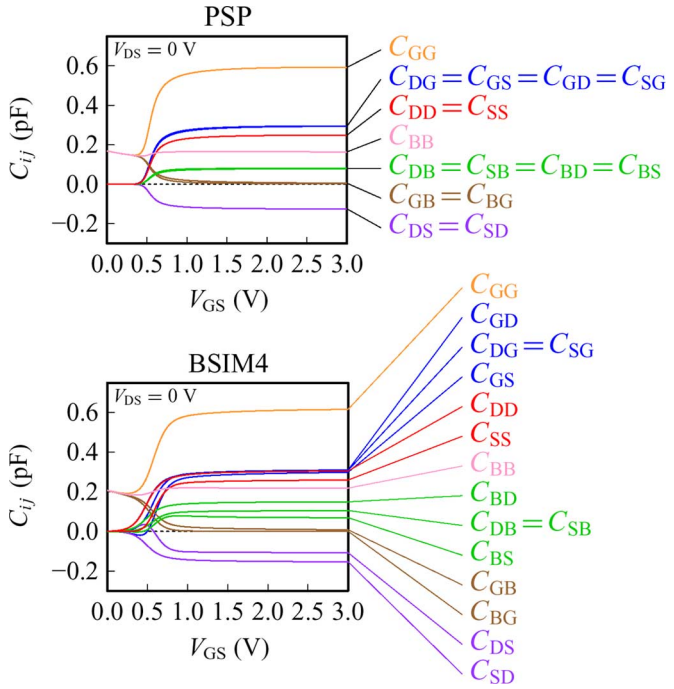

Fig. 5. The sixteen MOSFET capacitances C_{ij} calculated with the PSP model (top) and the BSIM4 model (bottom) as a function of V_{GS} for a long-channel thick-oxide device at $V_{DS} = 0$ V.

capacitances C_{ij} should be symmetrical w.r.t. source-drain interchange. This symmetry requirement means that the capacitances C_{ij} remain unchanged when, simultaneously, all indices 'S' are replaced by 'D' and all indices 'D' are replaced by 'S'. In other words:

$$C_{DG} = C_{SG}, \tag{2}$$
$$C_{DB} = C_{SB}, \tag{3}$$
$$C_{GD} = C_{GS}, \tag{4}$$
$$C_{BD} = C_{BS}, \tag{5}$$
$$C_{DD} = C_{SS}, \tag{6}$$
$$C_{DS} = C_{SD}. \tag{7}$$

Yet another requirement that the MOSFET capacitances have to fulfill at $V_{DS} = 0$ V, is reciprocity, i.e.,

$$C_{ij} = C_{ji}. \tag{8}$$

Note that for non-zero V_{DS}, the MOSFET capacitances are generally non-reciprocal (i.e., $C_{ij} \neq C_{ji}$). Combining the symmetry requirement [(2)–(7)] with the reciprocity requirement [(8)], it follows that at $V_{DS} = 0$ V there are only 7 different capacitance values. This fact is perfectly captured by the PSP model (see Fig. 5). With a threshold-voltage-based model it is almost impossible to fulfill these symmetry and reciprocity requirements for the capacitances, and, indeed, this is not the case in BSIM4 (see Fig. 5). Fig. 5 also reveals some other imperfections of the BSIM4 capacitances: both C_{GS} and C_{DS} show some unexpected zero-crossings near the threshold voltage. It should be noted that, for BSIM4, we use *XPART* $= 0$, corresponding to physical Ward–Dutton charge partitioning. For other settings of *XPART* the results become significantly worse.

To bear this out further, we inspect the capacitances $C_m \equiv C_{DG} - C_{GD}$, $C_{mb} \equiv C_{DB} - C_{BD}$, and $C_{mx} \equiv C_{BG} - C_{GB}$, as defined in [20]. In Fig. 6, these capacitances are plotted as a function of drain-source voltage for three models, namely PSP, BSIM4, and for reference also the Tsividis model in its simplest form [20]. The reciprocity requirement tells us that all these three capacitances should be zero for $V_{DS} = 0$ V. This is, indeed, exactly the case for the Tsividis model. For BSIM4, both C_{mb} and C_{mx} violate the reciprocity requirement, and the trends of C_{mb} and C_{mx} as a function of V_{DS} are not correct in the linear regime. For the PSP model, on the other hand, the reciprocity requirement is fulfilled quite well (only C_{mx} at $V_{DS} = 0$ V is slightly off) and the trends of C_m, C_{mb} and C_{mx} as a function of V_{DS} are all correct.

IV. Series Resistances and Source and Drain Junctions

The PSP model contains an option to use external gate and bulk resistances (see [3]). In particular, the gate resistance is of special importance for the modeling of the RF behavior of CMOS devices. In the PSP model, not only the distributed resistance of the silicide layer, but also the silicide-to-polysilicon contact resistance [21] as well as the vertical polysilicon resistance is accounted for:

$$R_{gate} = \frac{1}{N_f} \cdot \left(\frac{\rho_{\square,sil}}{3 \cdot N^2_{gate\ con}} \cdot \frac{W_f}{L} + \frac{\rho_{con} + \rho_{poly}}{W_f \cdot L} \right) \tag{9}$$

where $\rho_{\square,sil}$ is the silicide sheet resistance, ρ_{con} is the contact resistance between silicide and polysilicon, ρ_{poly} is the vertical resistance of the polysilicon, W_f is the finger width, L is the gate (or channel) length, N_f is the number of fingers, and $N_{gate\ con}$ indicates the number of gate contacts, i.e., it equals one for a single-sided contacted gate and it equals two for a double-sided contacted gate. The expression for the effective gate resistance given by (9); can be rewritten as follows

$$R_{gate} = \frac{\rho_{\square,sil}}{3 \cdot N^2_{gate\ con} \cdot N^2_f} \cdot \frac{W}{L} + \frac{\rho_{con} + \rho_{poly}}{W \cdot L} \tag{10}$$

where W is the total gate width, $W = N_f \cdot W_f$. From the second term in (10) it can be seen that the effect of the contact resistance between silicide and polysilicon cannot be reduced by varying the layout (i.e., N_f) of the device. The importance of the gate resistance for the noise behavior of CMOS devices will be discussed in Section 4.

In advanced CMOS technologies the short-channel behavior is controlled by pocket implants. As a consequence, the doping gradients and thus the electric fields in the source-bulk and drain-bulk junctions are quite high. These high electric fields lead to increased junction leakage due to various tunneling effects. In the PSP model the source and drain junctions are modeled by the JUNCAP2 model [15]. This model includes Shockley-Read-Hall generation/recombination, trap-assisted tunneling, and band-to-band tunneling, leading to a relatively complicated expression for the resulting current. In the JUNCAP2 model, three components to both current and capacitance are distinguished for each junction: a bottom component, a gate-edge component, and an isolation-edge component. Each of these components is modeled independently and has its own set of model parameters. From Fig. 7 it can be seen that the

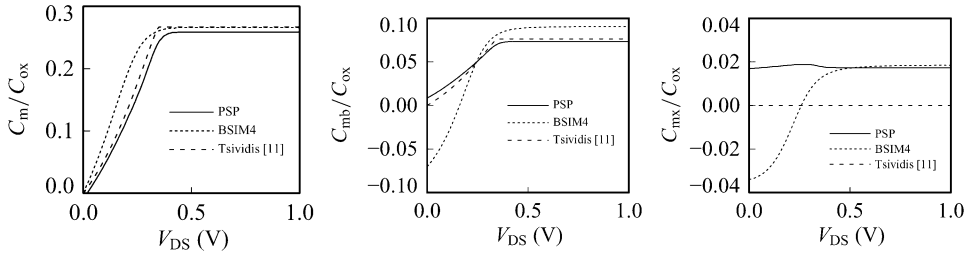

Fig. 6. The capacitances $C_{\rm m}$ (left), $C_{\rm mb}$ (middle), and $C_{\rm mx}$ (right) as a function of drain-source voltage. The comparison is between PSP, BSIM4 (with $XPART = 0$), and the Tsividis model in its simplest form \protect [20]. The gate-source voltage is $V_{\rm GS} = 1$ V.

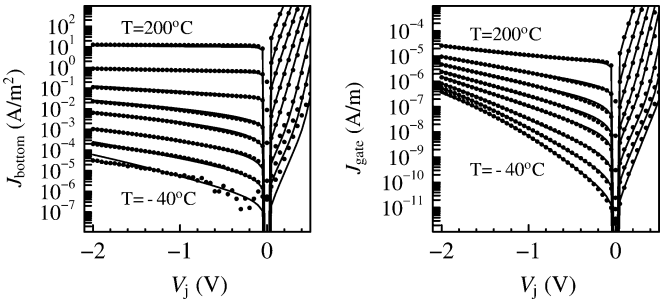

Fig. 7. Bottom component ($J_{\rm bottom}$, left) and gate-edge component ($J_{\rm gate}$, right) of the junction current as a function of the voltage $V_{\rm j}$ across the junction. Symbols represent measurements, and lines represent simulations with the JUNCAP2 model. The currents were measured on n$^+$/p-well junctions from a 0.12 μm CMOS technology for temperatures of $-40, -10, 21, 60, 90, 125, 160$, and 200°C.

JUNCAP2 model gives a very good description of the junction currents, both in forward and reverse bias, and as a function of temperature.

To calculate the current in a MOSFET at a given bias condition, the junction currents in all three components (bottom, gate-edge, and isolation edge) of both the source and drain junctions have to be calculated. So, while the expression for the channel current is evaluated once, the expression for the junction current is evaluated *six* times. To alleviate this calculational burden, the "JUNCAP2 Express" option has recently been developed; see Fig. 8. In the bias-independent part of the model (only called in the initialization phase), the full expressions for all three components are used to calculate the coefficients of a very simple expression. Now, in the bias-dependent part, which is called repeatedly by the circuit simulator in all the bias- or time-steps of the circuit simulation, only this very simple expression needs to be evaluated. Details of the JUNCAP Express calculations are given in Appendix A. In Fig. 9, the JUNCAP Express simulations are shown to be in close agreement with the original full JUNCAP2 simulations, validating the JUNCAP Express approach.

Using the JUNCAP Express option, the junction calculation overhead in PSP is reduced by a factor of 5–15 (dependent on simulator and analysis type). As a consequence, the junction calculation now only consumes $\sim$10% of the total PSP runtime, while its accuracy is hardly sacrificed at all. In Fig. 10, the PSP runtime is benchmarked against BSIM4 for transient analyses on a set of representative circuits with varying transistor count. The circuit simulator used was Eldo from Mentor Graphics [22]. In PSP, the JUNCAP Express option was switched on. As can be seen, the PSP/BSIM4 runtime ratio is on average close to 1. Moreover, as expected, there is *no* systematic increase/decrease in this number with transistor count.

V. Distortion

As mentioned in the introduction, the surface-potential-based approach is an ideal starting point for developing a symmetrical MOSFET model. As argued in Section 2, great care has been taken in PSP to maintain this symmetry under source-drain exchange (or C^3-continuity) at zero drain-source voltage, while implementing all necessary physical effects. Consequently, PSP passes all symmetry benchmark tests [19], [23]. As a consequence, PSP gives an adequate description of the distortion behavior when the drain-source voltage $V_{\rm DS}$ is alternating around zero, as shown in Fig. 11. This property is of importance for adequate distortion modeling in variable-gain circuits (cf. Fig. 4), passive mixers [24], and continuous time integrators [25], [26]. Note that the capability of the PSP model to describe data such as that presented in Fig. 11 has also been verified experimentally and independently [27].

Distortion behavior at non-zero drain-source voltage is also important. For this purpose the higher-order derivatives of the drain current with respect to the drain-source and gate-source voltages need to be accurately modeled. In Fig. 12, measurements and simulations of $g_{\rm DS3}$, the third-order derivative of the drain current with respect to the drain-source voltage are shown. It should be noted that only transconductance and output conductance and no higher-order derivatives are included in the parameter extraction procedure of the PSP model. Consequently, the good description presented in Fig. 12 is an intrinsic property of the PSP model. Additional verification of the modeling with the PSP model of higher-order derivatives of the drain current with respect to both the drain-source and gate-source voltages can be found in Fig. 13 of [10].

In the above, we have shown that PSP gives a good description of the higher-order derivatives of DC currents. Next, we consider the second-order distortion at RF frequencies, where also higher-order derivatives of charges play a role. Inspired by Volterra analysis [28] we generalize the well-known linear Y-parameters to include weakly nonlinear effects. For this purpose, we define the second-order Y-parameters as

$$Y_{klm} = \frac{i_k}{v_l \cdot v_m}, \tag{11}$$

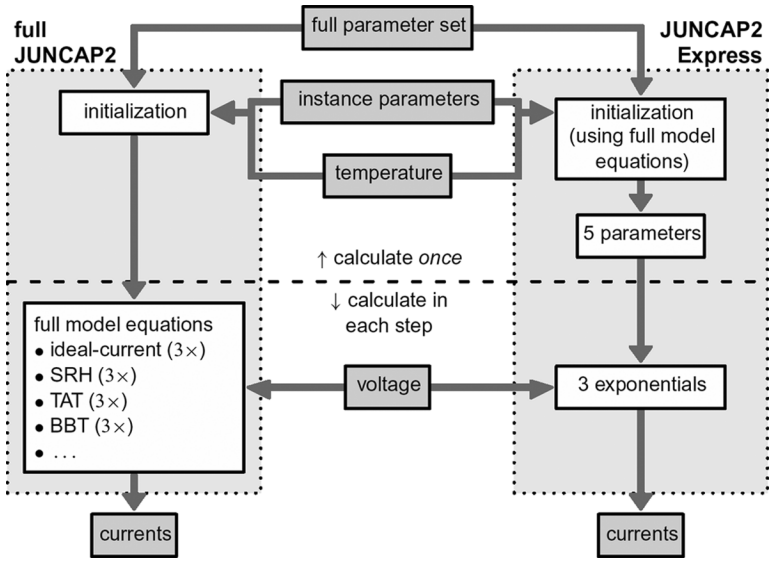

Fig. 8. Illustration of the basic idea behind JUNCAP Express: in the frequently called voltage-dependent part of the model, the computationally expensive calculations are replaced by simple ones. This set of simple equations is mapped onto the full JUNCAP model in the initialization part of the model.

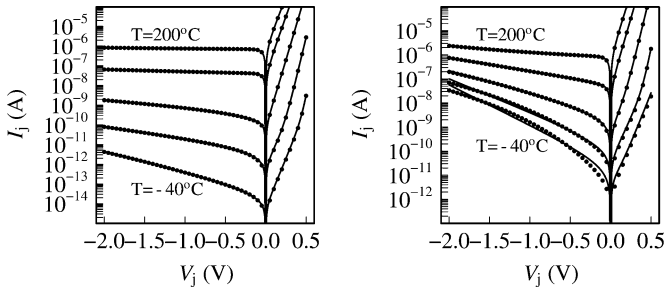

Fig. 9. Junction current I_j as a function of the voltage V_j across n^+/p-well junctions in a 0.12 μm CMOS technology for temperatures of -40, 21, 90, 160, and 200°C. Symbols represent simulations with the full JUNCAP2 model, while lines represent the corresponding JUNCAP Express results. Left picture: large square junction with a bottom area of 70000 μm^2 and an STI edge of 1100 μm. Right picture: multi-fingered junction with a bottom area of 23100 μm^2 and gate edges of 77000 μm.

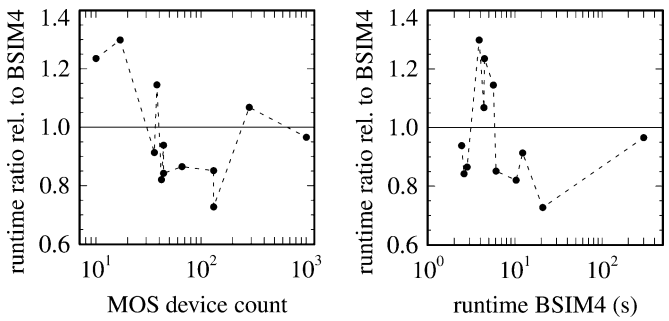

Fig. 10. Runtimes of PSP relative to BSIM4 for 12 representative digital standard cells as a function of MOS device count (left) and BSIM4 runtime (right) using the circuit simulator Eldo from Mentor Graphics [22]. Dashed lines serve to guide the eye.

where $k, l, m = 1$ or 2; i_k is the small-signal current at port k, and v_l and v_m are the small-signal excitations at ports l and m at frequencies f_l and f_m, respectively. If there is no excitation at one of the ports, this port should be AC short-circuited. The output i_k is taken at the sum $(f_l + f_m)$ or difference $(f_l - f_m)$ frequency. Experimentally, the second-order Y-parameters are derived from the second-order S-parameters which are measured using the harmonic-power measurement option available on the 50 GHz Agilent E8364B performance network analyzer. In this type of measurements one has to ensure the transistor is operated in the weakly nonlinear regime to prevent higher-order mixing terms from becoming significant. Moreover, signal-source and signal-receiver nonlinearities have to be accounted for, and measurements have to be taken at different source and load terminations to allow for proper extraction of these non-linear Y-parameters. In Fig. 13, measurements and simulations of the absolute value of the second-order Y-parameter Y_{211} are presented. In this experiment, $f_l = f_m$ and, at the output, the sum frequency is considered. It is observed that the PSP model describes both the bias dependence of this RF distortion quite well. The frequency dependence of this quantity appears to be insignificant in this frequency range. In Fig. 14, the results for $|Y_{212}|$ and $|Y_{222}|$ are depicted, which show more frequency dependence. PSP is observed to give a good prediction of both bias and frequency dependencies, proving its suitability for distortion analysis on circuits.

VI. Noise

There are two main contributions to the noise behavior of a MOSFET: $1/f$ (or flicker) noise and thermal noise. The flicker noise model in PSP is based on the correlated mobility fluctuation theory [29], [30], which is capable of describing the rather different bias dependencies of flicker noise in n- and p-channel devices. This theory also formed the basis of the BSIM4 flicker noise model. In PSP, however, it has been developed within the surface-potential framework, leading to a smooth single-piece expression valid in all regions of operation (see also PSP documentation [3] and [13]). Extensive experimental model verification has been presented elsewhere [31].

The thermal noise in MOSFETs leads to white noise in the drain current and to noise in the gate current ("induced gate

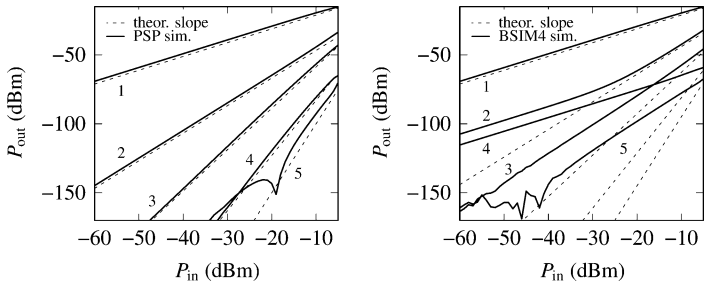

Fig. 11. First through fifth harmonic output power as a function of input power simulated with the PSP model (left) and the BSIM4 model (right) for an n-channel device from 90 nm CMOS technology with a gate width of 5 μm and a gate length of 0.3 μm. Dashed lines indicate the theoretical slopes. In this two-tone intermodulation distortion simulation ($f_1 = 1.8$ GHz, $f_2 = 1.9$ GHz), the device was operated in common-gate configuration with 50 Ω at the input and 50 Ω at the output and with $V_{\rm GS} = 1$ V and $V_{\rm DS} = V_{\rm SB} = 0$ V.

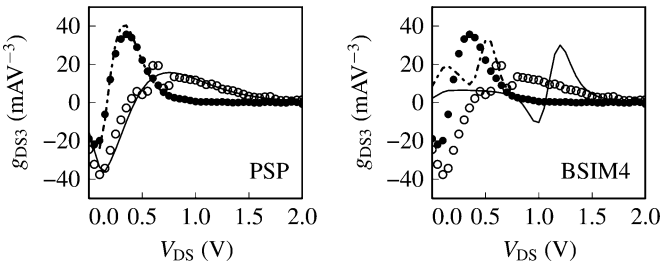

Fig. 12. Third-order derivative of the drain current with respect to the drain-source voltage ($g_{\rm DS3} = \partial^3 I_{\rm D}/\partial V_{\rm DS}^3$), as a function of the drain-source voltage $V_{\rm DS}$ for a GO2 n-channel transistor from 65 nm technology with a gate width of 10 μm and a gate length of 0.28 μm. Full and open circles represent measurements at gate-source voltages of 1.25 and 3.0 V, respectively. Lines represent simulations for the PSP model (left) and the BSIM4 model (right), at gate-source voltages of 1.25 V (dashed lines) and 3.0 V (solid lines).

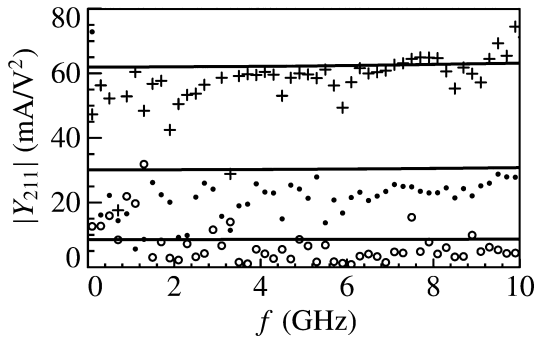

Fig. 13. Absolute value of the second-order Y-parameter, Y_{211}, (at twice the excitation frequency) as a function of the excitation frequency for an n-channel transistor from 90 nm technology with a gate width of 120 μm and a gate length of 0.1 μm. Symbols represent measurements at a drain-source voltage of 1.5 V and various gate-source voltages, $V_{\rm GS}$: crosses $V_{\rm GS} = 1.0$ V, solid dots $V_{\rm GS} = 0.7$ V, and open circles $V_{\rm GS} = 0.5$ V. Lines represent simulations with the PSP model.

noise"), which is proportional to the frequency squared. In most compact MOS models, the description of the thermal noise is based on the Klaassen-Prins equation [32]. This equation is used in many textbooks [20], [33], but does not take velocity saturation fully into account. The thermal noise model of PSP, however, is based on the so-called "improved Klaassen-Prins equation," which incorporates the effect of velocity saturation correctly [34], [35]. It has been extensively verified on various CMOS processes down to the 90 nm technology node (see also [31], [34]). In Fig. 15 measurements and simulations of the drain and gate current noise are shown for two devices from a 90 nm CMOS technology. Details on the experimental procedure can be found in [36]. A good agreement between measurements and simulations is observed. The large impact of the gate resistance on noise behavior is demonstrated in Fig. 16. The device with the double-sided contacted gates and a finger width of 4 μm has an effective gate resistance that is four times smaller than that of the device with the single-sided contacted gates and a finger width of 5 μm [see also (10)]. This smaller gate resistance results in a reduction of the minimum noise figure by a factor of about 1.6. Further analysis of the various contributions to the drain and gate current noise can be found in [31]. Obviously, it is of importance to include all these effects in the compact model to allow for versatile RF design in CMOS technology.

Next, a comparison of noise measurements and simulations on RF circuits made in a baseline 65 nm LP CMOS technology is presented. The first design is a wide-band low-noise amplifier (LNA) targeting ultra wide-band applications like WiMedia W-USB. The LNA uses a cascode configuration with dual loop feedback, of which one loop incorporates an integrated transformer (see [37] and Fig. 17). In this circuit, the drain current thermal noise of the input MOSFET has a dominant contribution to the noise figure. Fig. 18 shows the measured and simulated voltage gain and noise figure of this LNA, up to a frequency of 10 GHz. The simulated curves track the measured curves well, indicating an accurate prediction of the performance.

A second RF circuit used for the comparison is an RF oscillator. The oscillator has four identical differential gain stages connected in a ring configuration to generate the four quadrature phases [38]. Frequency tuning of the oscillator is realized by turning ON/OFF MOS capacitors. The biasing of the oscillator is realized using NMOS current mirrors coming from the overall bias-current generator unit. Initially, the RF oscillator gave more phase noise than expected. Using the PSP model, this could easily be traced back to several non-used devices in the biasing unit which had a zero drain-source voltage. The induced gate noise of these devices was injected into the gates of the NMOS current mirrors and therefore worsened the overall phase-noise performance of the oscillator. Fig. 19 shows the measured and simulated phase noise performance of the oscillator running at a frequency of 3432 MHz. Good agreement between measurements and simulations is observed. Using the ac-

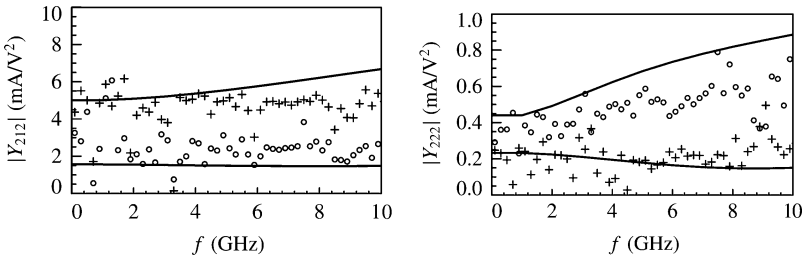

Fig. 14. Same as Fig. 13, but now for Y_{212} (left) and Y_{222} (right). For clarity, here only $V_{\rm GS} = 0.5$ V (open circles) and $V_{\rm GS} = 1.0$ V (crosses) are shown. Lines represent simulations with the PSP model.

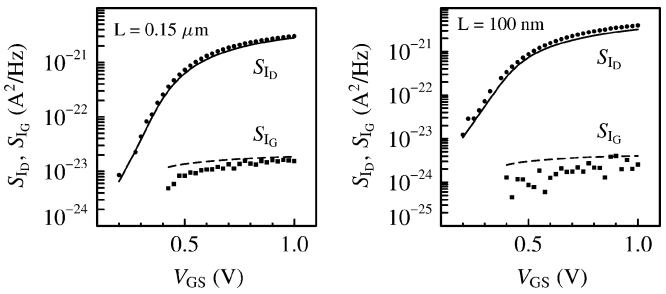

Fig. 15. Drain current noise $S_{\rm I_D}$ and gate current noise $S_{\rm I_G}$ as a function of gate-source voltage $V_{\rm GS}$ for n-channel devices. The drain bias is $V_{\rm DS} = 1$ V (devices are in saturation region) and the frequency is $f = 10$ GHz. Symbols represent measurements and lines represent simulations with the PSP model. The device at the left-hand side has a channel length of 0.15 μm and consists of 24 fingers of 5 μm width, which are contacted from one side only. The device at the right-hand side has a channel length of 100 nm and consists of 60 fingers of 2 μm width, which are contacted from both sides.

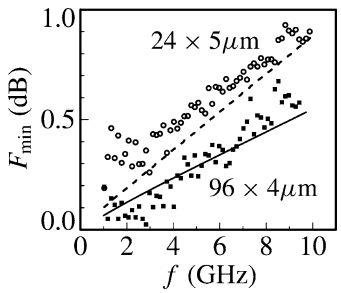

Fig. 16. Minimum noise figure as a function of the frequency for two n-channel devices with 100 nm gate lengths, but with different layouts. Symbols represent measurements and lines represent simulations with the PSP model. The open circles and the dashed line represent a device with 24 fingers, which are 5 μm wide and contacted from one side only. The solid squares and the solid line represent a device with 96 fingers, which are 4 μm wide and contacted from both sides.

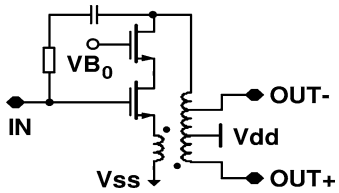

Fig. 17. Schematic view of the low-noise amplifier (biasing circuitry not shown).

quired insight, the excess noise circuit could easily be removed, leading to better phase noise performance than shown in Fig. 19.

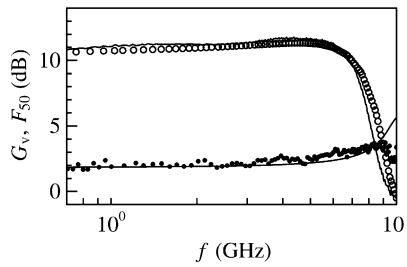

Fig. 18. Voltage gain $G_{\rm v}$ (open circles) and 50-Ω noise figure F_{50} (solid dots) of the low-noise amplifier of Fig. 17, designed in 65 nm CMOS technology, as a function of the frequency. Symbols represent measurements and lines represent simulations with the PSP model.

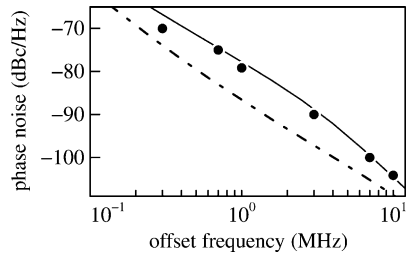

Fig. 19. Phase noise of an ultra-wide-band, digitally controlled oscillator designed in 65 nm CMOS technology as a function of the offset frequency (at a center frequency of 3.43 GHz). Symbols represent measurements; the dashed line represents simulations with the PSP model without induced gate noise; and the solid line represents simulations with the PSP model with induced gate noise.

VII. Summary

In this paper we have focused on the distinctive properties of PSP for RF circuit design. These properties are that *(i)* it is accurate enough to be used for distortion analysis, *(ii)* it is Gummel symmetric, *(iii)* it has a physically sound charge model that retains capacitance reciprocity at $V_{\rm DS} = 0$ V, and *(iv)* it contains accurate physics-based expressions for junction leakage and noise. It has been demonstrated that these advances in compact modeling have been achieved without sacrificing simulation time. Several circuit design examples have been given that benefit from PSP's unique properties.

Appendix

A. JUNCAP Express

In JUNCAP Express, the full JUNCAP2 equations are mapped onto a single, much simpler equation $I_{\rm j} = I_{\rm for1} + I_{\rm for2} + I_{\rm rev}$, where $I_{\rm for1}$, $I_{\rm for2}$, and $I_{\rm rev}$ model the ideal current, the

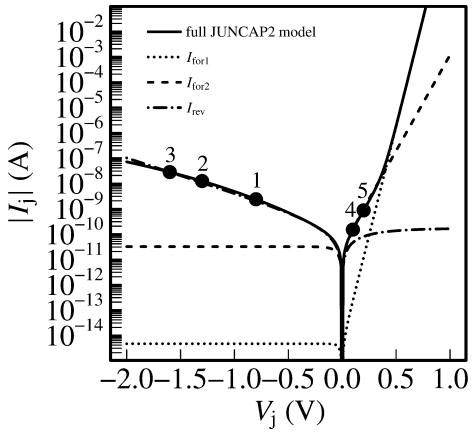

Fig. 20. Solid black line: example of an IV characteristic calculated with the full JUNCAP2 model; points 1, 2, 3, 4, and 5 on this line are used in the JUNCAP2 Express calculations. Orange dashed line: JUNCAP2 Express ideal current contribution. Blue dashed line: JUNCAP2 Express non-ideal forward current contribution, calculated using blue-colored points 4 and 5. Green dashed line: JUNCAP2 Express reverse current contribution, calculated using green-colored points 1, 2, and 3.

non-ideal forward current, and the remaining non-ideal reverse current, respectively, and are given by the equations

$$I_{\rm for1} = g(V_{\rm AK}, \mathbf{ISATFOR1}, 1), \tag{12}$$

$$I_{\rm for2} = g(V_{\rm AK}, \mathbf{ISATFOR2}, \mathbf{MFOR2}), \tag{13}$$

$$I_{\rm rev} = -g(-V_{\rm AK}, \mathbf{ISATREV}, \mathbf{MREV}), \tag{14}$$

where the function g is given by

$$g(V, I_0, m) = I_0 \cdot [\exp(V \cdot m/\phi_{\rm TD}) - 1.0]. \tag{15}$$

In the JUNCAP Express pre-processing step, we determine the coefficients $\mathbf{ISATFOR1}, \mathbf{ISATFOR2}$, $\mathbf{MFOR2}, \mathbf{ISATREV}$, and $\mathbf{MREV}$ in such a way that the original JUNCAP2 IV-curves are reproduced as accurately as possible.

Ideal Current: The coefficient $\mathbf{ISATFOR1}$ is easily found: for the three junction components (bottom, STI-edge, and gate edge), the voltage dependence of the ideal current is the same, so that the total ideal current of JUNCAP Express, (12), can be mapped directly onto that of the full JUNCAP2 model. This immediately leads to

$$\mathbf{ISATFOR1} = AB \cdot I_{\rm DSAT,bot} + {\rm LS} \cdot I_{\rm DSAT,sti} + {\rm LG} \cdot I_{\rm DSAT,gat} \tag{16}$$

where $I_{\rm DSAT,bot}, I_{\rm DSAT,sti}$, and $I_{\rm DSAT,gat}$ are the saturation current densities of the three junction components after temperature scaling.

Non-Ideal Forward Current: Determination of the coefficients $\mathbf{ISATFOR2}$ and $\mathbf{MFOR2}$ is less straightforward. Here, we first determine the full-JUNCAP2 currents I_4 and I_5, which are calculated at low forward voltages $V_4 = 0.1$ V and $V_5 = 0.2$ V, respectively (points '4' and '5' in Fig. 20). Next, the ideal contributions to these currents are subtracted to arrive at the non-ideal contributions $I_{4,\rm cor}$ and $I_{5,\rm cor}$:

$$I_{i,\rm cor} = I_i - g(V_i, \mathbf{ISATFOR1}, \mathbf{MFOR1}) \tag{17}$$

where $i = 4, 5$. Now we are ready to determine $\mathbf{ISATFOR2}$ and $\mathbf{MFOR2}$ by demanding that the $I_{\rm for2}$ curve crosses the points (V_4, I_4) and (V_5, I_5). This leads to a set of equations that cannot be solved analytically. However, using the fact that $\mathbf{MFOR1}$ will always be close to $1/2$, so that both $\mathbf{MFOR1} \cdot V_4$ and $\mathbf{MFOR1} \cdot V_5$ are well in excess of $\phi_{\rm TD}$, it is easy to find that in good approximation:

$$\mathbf{MFOR2} = \frac{\phi_{\rm TD} \cdot \ln(I_{4,\rm cor}/I_{5,\rm cor})}{V_4 - V_5}, \tag{18}$$

and

$$\mathbf{ISATFOR2} = \frac{I_{4,\rm cor}}{[\exp(V_4 \cdot \mathbf{MFOR2}/\phi_{\rm TD}) - 1]}. \tag{19}$$

Non-Ideal Reverse Current: The determination of the coefficients $\mathbf{ISATREV}$ and $\mathbf{MREV}$ is similar to that of $\mathbf{ISATFOR2}$ and $\mathbf{MFOR2}$, but is somewhat more involved. The reason is that the value of $\mathbf{MREV}$ can be much smaller than $\mathbf{MFOR2}$ so that the approximation used in the determination of $\mathbf{MFOR2}$ is no longer sufficient. First, we choose three voltages $V_1 = -0.4 \cdot \mathbf{VJUNREF}$, $V_2 = -0.65 \cdot \mathbf{VJUNREF}$, and $V_3 = -0.8 \cdot \mathbf{VJUNREF}$ in the reverse mode of operation, where $\mathbf{VJUNREF}$ is an adjustable model parameter that determines the range of validity of the JUNCAP Express approach. The corresponding full JUNCAP2 currents are I_1, I_2, and I_3, respectively (points '1', '2', and '3' in Fig. 20). The ideal and non-ideal forward contributions to these currents are subtracted:

$$I_{i,\rm cor} = I_i - g(V_i, \mathbf{ISATFOR1}, \mathbf{MFOR1}) - g(V_i, \mathbf{ISATFOR2}, \mathbf{MFOR2}) \tag{20}$$

where $i = 1, 2, 3$. Points "1" and "2" are used for the determination of $\mathbf{MREV}$. Similarly to (18), the value of $\mathbf{MREV}$ is (to a first-order approximation) given by

$$m_0 = \frac{\phi_{\rm TD} \cdot \ln(\alpha_{\rm rev})}{V_2 - V_1}, \tag{21}$$

where $\alpha_{\rm rev} = I_{1,\rm cor}/I_{2,\rm cor}$. Using a Newton-Raphson step we obtain a first-order result:

$$\mathbf{MREV} = m_0 + \phi_{\rm TD} \cdot \frac{(\alpha_{\rm rev} - 1) \cdot \left(\alpha_{\rm rev}^{\frac{V_2}{V_2 - V_1}} - 1\right)}{\alpha_{\rm rev} \cdot V_1 - V_2 + (V_2 - V_1) \cdot \alpha_{\rm rev}^{\frac{V_1}{V_1 - V_2}}}. \tag{22}$$

Having fixed $\mathbf{MREV}$, we finally determine the reverse-current prefactor $\mathbf{IDSATREV}$ by demanding JUNCAP Express to cross the point '3', which leads to

$$\mathbf{ISATREV} = \frac{-I_{3,\rm cor}}{[\exp(V_3 \cdot \mathbf{MREV}/\phi_{\rm TD}) - 1]}. \tag{23}$$

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reproduced with permission of the author. The compact modeling research at ASU is supported in part by SRC and CMC. C. McAndrew (Freescale) is acknowledged for numerous discussions of symmetry issues in compact MOSFET models.

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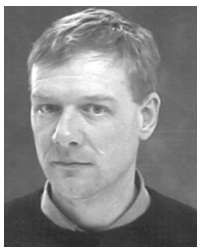

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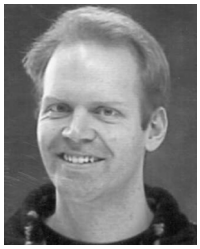
Jeroen A. Croon was born in Delft, The Netherlands, in 1975. In 1998, he received the Master's degree in applied physics from the Delft University of Technology. His thesis involved the optimization of the receiving coil and pre-amplifier of an Overhauser MRI system at 77 K and at room temperature. After this, he started working in IMEC, Belgium, and in 2004 he received the Ph.D. degree in electrical engineering from the Catholic University of Leuven, Belgium, for his study of the matching properties of deep-submicron MOSFETs.

After obtaining his Ph.D. he worked in IMEC on the characterization of MOSFETs fabricated on germanium substrates and on the study of variability in advanced CMOS processes. Since the beginning of 2005, he has been working in the compact modeling group of NXP Semiconductors Research, Eindhoven, The Netherlands, on the modeling of RF circuit blocks. He is the author of the book *Matching Properties of Deep Sub-Micron MOS Transistors*.

Dirk B. M. Klaassen (M'01) received the Ph.D. degree in experimental physics from the Catholic University of Nijmegen, Nijmegen, The Netherlands, in 1982.

He then joined Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on various subjects in the field of luminescence from the solid state and modeling for silicon device simulation, most notably the Philips Unified Mobility Model. In the early 1990s, he switched to compact modeling for circuit simulation. He is currently with NXP Corporate Research, Eindhoven, where he is an NXP Research Fellow. He has codeveloped and industrialized well-known compact models such as Mextram, MOS Model 9, and MOS Model 11. He is the holder of several patents and has authored or coauthored over 80 papers in scientific journals and conferences.

Dr. Klaassen was the Short-Course Chair of the 1999 International Electron Devices Meeting.



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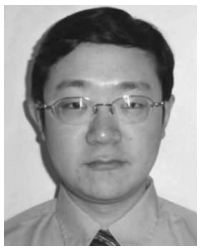
Since 1998, he has been with Philips Research Laboratories, Eindhoven, where he worked on compact MOS models for circuit simulation and is now working on RF CMOS circuit design. He is the main developer of MOS Model 11 and a codeveloper of the PSP MOSFET model.



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