Design of the Simple OTA

For IHP 130nm Process (Version 1)

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1 Introduction

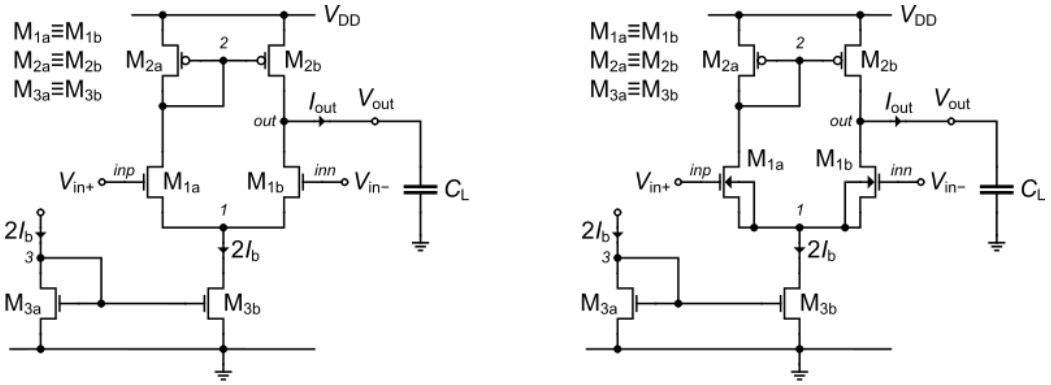

Figure 1.1: Schematic of the simple differential OTA.

This notebook presents the design of the simple differential OTA shown in Figure 1.1. We can distinguish the case where M_{1a}-M_{1b} are in the common substrate (Figure 1.1 a) and the case where M_{1a}-M_{1b} are in a separate well (Figure 1.1 b). We will see below that in fully differential mode the effects of the source transconductances on the common substrate schematic are actually canceled.

We will design the circuit with M_{1a}-M_{1b} in a separate well for the specifications given below. In this example, we don't give any specification on the slew-rate. However the sew-rate specification can determine a bias current that is way above the one derived in this example ignoring the SR. If the SR is too high, we can move to adaptive biasing OTAs.

2 Analysis

2.1 Large-signal Analysis

2.1.1 Voltage Transfer Characteristic

Since there are two input terminals, several large-signal voltage transfer characteristics can be derived. In many situations, one of the two input terminals will be maintained at a constant common mode voltage (typically $V_{DD}/2$) while the other is connected to some feedback network. If for example the negative input is set constant, at for example the middle of the supply voltage $V_{DD}/2$, the positive input can be swept from ground to V_{DD}. The output voltage will change from ground to V_{DD} as well. The amplifier will provide some gain for V_{in+} ranging close to V_{in-}. Outside this high gain region, the output voltage will saturate either to V_{DD} for V_{in+} larger than V_{in-}, or to 0 for V_{in+} smaller than V_{in-}. Under the above conditions, the maximum output voltage $V_{out,max}$ in the linear range is limited by M_{2b} going out of saturation

$$V_{out,max} = V_{DD} - V_{DSsat4}. \tag{2.1}$$

On the other hand, the minimum output voltage $V_{out,min}$ of the linear range is limited by M_{1b} going out of saturation and depends linearly on the common-mode voltage set on V_{in-} according to

$$V_{out,min} = V_{DSsat3} - V_{GS3} + V_{in-}. \tag{2.2}$$

If M_{1b} is biased in weak inversion then $V_{DSsat3} \cong 4U_T \cong 100mV$. The value of V_{GS3} depends wether M_{1a}-M_{1b} are in a separate well or are in the common substrate.

2.1.1.1 M_{1a}-M_{1b} in a separate well:

In the case M_{1a}-M_{1b} are in a separate well, then $V_{S3} = 0$ and hence $V_{GS3} \cong V_{T0n}$. The minimum output voltage in the linear range is then given by

$$V_{out,min} = 4U_T - V_{T0n} + V_{in-}. \tag{2.3}$$

As long as M_{2b} remains in saturation (i.e. for $V_{out} < V_{out,max}$), the currents flowing in M_{1a} and M_{1b} are imposed equal by the current mirror. When decreasing V_{in+} and for V_{out} below $V_{out,min}$, the current in M_{1b} is equal to $I_b/2$ as long as M_{3b} remains in saturation. The gate voltage of M_{1b} is equal to V_{in-} and the source voltage of M_{1a} and M_{1b} follows V_{in+} with a shift of $V_{GS1a} \cong V_{T0n}$. Since the current is imposed equal to $I_b/2$ by the current mirror, the increase in V_{G3} has to be compensated by a decrease of the drain voltage, which is the only remaining degree of freedom in M_{1b}. This decrease of the drain voltage of M_{1b} brings it in the linear region with a drain-to-source voltage close to zero. In such condition, the output voltage is about equal to the source voltage which decreases linearly with the positive input voltage

$$V_{out} \cong V_1 = V_{in+} - V_{GS1a} \cong V_{in+} - V_{T0n}. \tag{2.4}$$

These considerations lead to the large-signal characteristic shown in Figure 2.1 which is obtained from simulation in the case of a 0.18~μm process with $V_{DD} = 1.8\,V$.

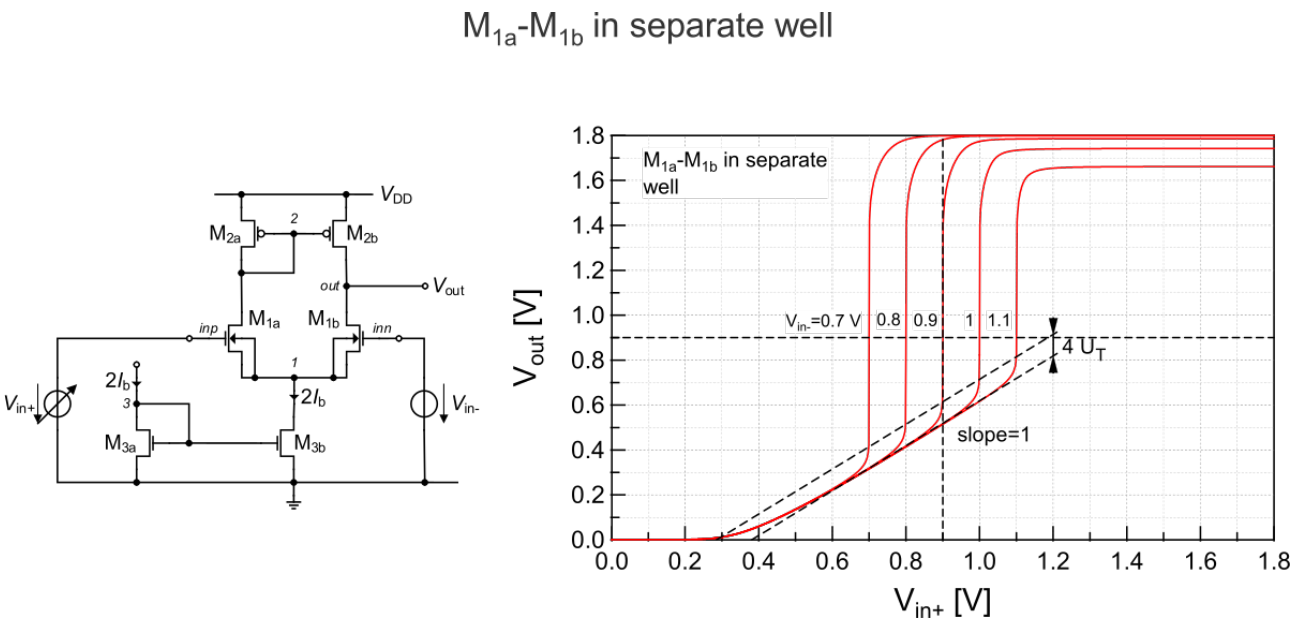

Figure 2.1: Large-signal V_{out} versus V_{in+} voltage transfer characteristic for various values of the negative input V_{in-} (M_{1a}-M_{1b} in separate well).

2.1.1.2 M_{1a}-M_{1b} in the common substrate:

In the case M_{1a}-M_{1b} are in the common substrate, the gate-to-source voltage of M_{1b} will depend on the source voltage V_S of M_{1a} and M_{1b} according to

$$V_{GS1b} = V_{G1b} - V_S = n_3 V_{P1b} + V_{T0n} - V_S = n_3(V_{P1b} - V_S) + V_{T0n} + (n_{1b} - 1)V_S, \tag{2.5}$$

where the approximation $V_{P1b} \cong (V_{G1b} - V_{T0n})/n_{1b}$ has been used. Since M_{1a}-M_{1b} are in weak inversion, $V_{P1b} - V_S \cong 0$ and therefore (2.5) simplifies to

$$V_{GS1b} \cong V_{T0n} + (n_{1b} - 1)V_S. \tag{2.6}$$

The source voltage is also given by

$$V_S = -V_{GS1b} + V_{in-} \cong -V_{T0n} - (n_{1b} - 1)V_S + V_{in-} \tag{2.7}$$

from which we can deduce V_S as

$$V_S \cong \frac{V_{in-} - V_{T0n}}{n_{1b}}. \tag{2.8}$$

The gate-to-source voltage of M_{1b} then writes

$$V_{GS1b} \cong V_{in-} - \frac{V_{in-} - V_{T0n}}{n_{1b}} \tag{2.9}$$

Finally, the minimum output voltage is given by

$$V_{out,min} \cong V_{in-} + 4U_T - V_{GS1b} = \frac{V_{in-} - V_{T0n}}{n_{1b}} + 4U_T. \tag{2.10}$$

Below $V_{out,min}$, the output voltage will decrease linearly with V_{in+} with a slope $1/n_{1a}$

$$V_{out} \cong \frac{V_{in+} - V_{T0n}}{n_{1a}}. \tag{2.11}$$

This is confirmed by the simulations results shown in Figure 2.2.

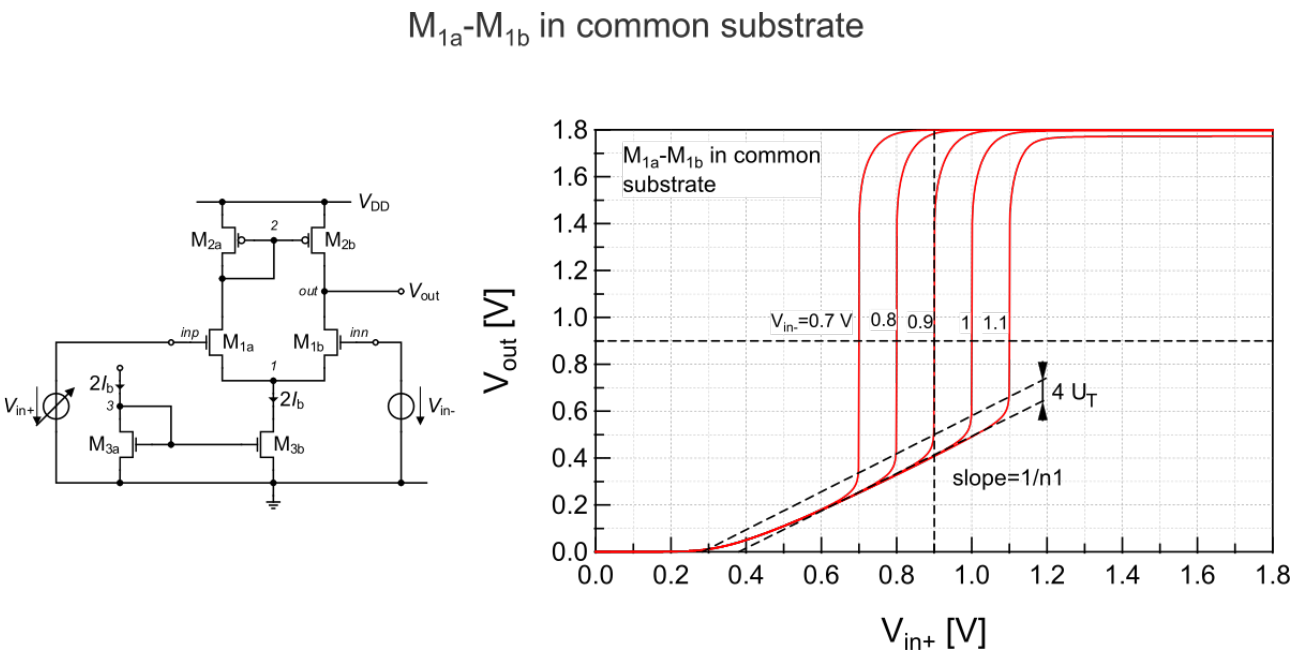

Figure 2.2: Large-signal V_{out} versus V_{in+} voltage transfer characteristic for various values of the negative input V_{in-} (M_{1a}-M_{1b} in common substrate).

2.1.2 Input Common Mode Voltage Range

The minimum common mode input voltage $V_{ic,min}$ is given by the saturation limit of M_{3b}

$$V_{ic,min} = V_{GS1} + V_{DSsat3b}. \tag{2.12}$$

The maximum common mode input voltage $V_{ic,max}$ is given by the limit of saturation of M_{1a}

$$V_{ic,max} = V_{GS1a} - V_{DSsat1a} - V_{SG2} + V_{DD} \cong V_{GS1a} - 4U_T - V_{SG2} + V_{DD}. \tag{2.13}$$

The gate-to-source voltage of M_{1a} V_{GS1} depends whether M_{1a}-M_{1b} are in a separate well or in the common substrate.

2.1.2.1 M_{1a}-M_{1b} in a separate well:

In the case M_{1a}-M_{1b} are biased in weak inversion and are in a separate well, $V_{GS1} \cong V_{T0n}$, and the common mode input voltage limits are given by

$$V_{ic,min} \cong V_{T0n} + V_{DSsat3b} \tag{2.14}$$
$$V_{ic,max} \cong V_{T0n} - 4U_T - V_{SG2} + V_{DD}. \tag{2.15}$$

The common mode input voltage range ΔV_{ic} is then given by

$$\Delta V_{ic} \triangleq V_{ic,max} - V_{ic,min} \cong V_{DD} - V_{SG2} - 4U_T - V_{DSsat3b}. \tag{2.16}$$

Equation (2.16) shows that although it is appropriate to bias M_{2a}-M_{2b} and M_{3a}-M_{3b} in strong inversion, choosing a too large saturation voltage will reduce the available common mode input range.

2.1.2.2 M_{1a}-M_{1b} in a common substrate:

In the case M_{1a}-M_{1b} are biased in weak inversion and are in a common substrate, the gate-to-source voltage of M_1 is given by

$$V_{GS1} \cong V_{T0n} + (n_1 - 1) \cdot V_S \tag{2.17}$$

For $V_{ic} = V_{ic,min}$, $V_S = V_{DSsat3b}$ and

$$V_{ic,min} = V_{GS1} + V_{DSsat3b} = V_{T0n} + (n_1 - 1)V_{DSsat3b} + V_{DSsat3b} = V_{T0n} + n_1 V_{DSsat3b}. \tag{2.18}$$

The source voltage for $V_{ic} = V_{ic,max}$ is equal to

$$V_S \cong V_{ic,max} - V_{GS1} = V_{ic,max} - V_{T0n} - (n_1 - 1)V_S \tag{2.19}$$

and hence

$$V_S \cong \frac{V_{ic,max} - V_{T0n}}{n_1}. \tag{2.20}$$

Replacing in (2.17) results in

$$V_{GS1} \cong V_{ic,max} - \frac{V_{ic,max} - V_{T0n}}{n_1} \tag{2.21}$$

and finally

$$V_{ic,max} \cong n_1(V_{DD} - V_{SG2} - 4U_T) + V_{T0n}. \tag{2.22}$$

Finally, the common mode input voltage range ΔV_{ic} is given by

$$\Delta V_{ic} \triangleq V_{ic,max} - V_{ic,min} \cong n_1(V_{DD} - V_{SG2} - 4U_T - V_{DSsat7}). \tag{2.23}$$

From (2.16) and (2.23), we see that having M_{1a}-M_{1b} in the common substrate gives a common mode input voltage range n_1 larger than having them in a separate well. Since the upper limit is identical, it comes from the fact that the slope of the output voltage versus V_{in+} is $1/n_1$ which is slightly smaller than 1.

2.1.3 Slew-Rate

Assuming that the differential pair is biased in weak inversion, when the magnitude of the differential voltage becomes larger than about $4U_T$, the magnitude of the output current saturates to I_b. The OTA then behaves like a current source of value I_b loaded by the load capacitance C_L. The rate of voltage change across the load capacitance is therefore limited to a maximum given by

$$SR \triangleq \left|\frac{dVout}{dt}\right|_{max} = \left|\frac{I_{out}}{C_L}\right|_{max} = \frac{I_b}{C_L}. \tag{2.24}$$

For a given load capacitance and a given available transient time, (2.24) often determines the minimum required bias current.

2.2 Small-signal analysis

We start with the small-signal analysis. The small-signal schematic corresponding to the schematics of Figure 1.1 are shown in Figure 2.3.

We see the source transconductances in Figure 2.3 which are controlled by the common voltage at the source ΔV_1.

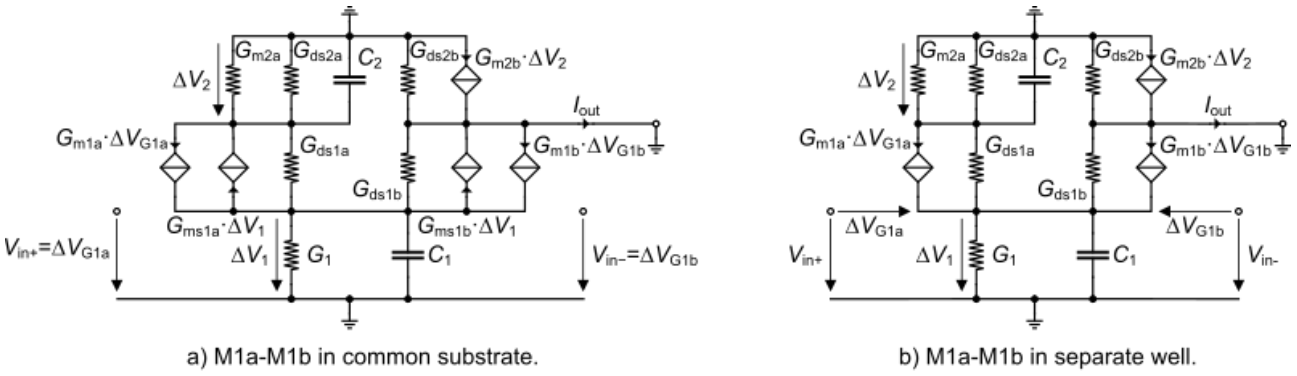

Figure 2.3: Small-signal schematic of the simple OTA.

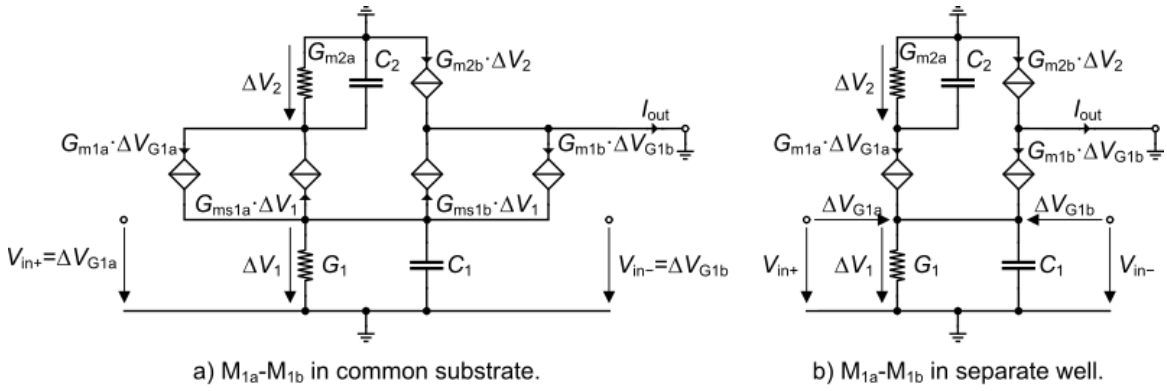

Figure 2.4: Simplified small-signal schematic.

2.2.1 Differential mode

In order to derive the differential transadmittance, we first will simplify the small-signal schematic of Figure 2.3 by considering that the output conductances are much smaller than the transconductances $G_{ds} \ll G_m < G_{ms}$ for all transistors. This leads to the simplified small-signal schematics shown in Figure 2.4.

The differential transadmittance is defined as

$$Y_{md} \triangleq \frac{I_{out}}{V_{id}}, \tag{2.25}$$

where $V_{id} \triangleq V_{in+} - V_{in-}$ is the input differential voltage and I_{out} the output current. Note that in the small-signal schematic, the output node has been connected to the ac ground. The output conductance of transistor M_{2b} G_{ds2b} is then grounded and can therefore be neglected. Also, the output conductance of transistor M_{2a} G_{ds2a} is in parallel with its transconductance G_{m2a} and since usually $G_{ds2a} \ll G_{m2a}$, it can also be neglected. Assuming a perfect matching, i.e. $G_{m1b} = G_{m1a} = G_{m1}, G_{ms1b} = G_{ms1a} = G_{ms1}, G_{m2b} = G_{m2a} = G_{ms2}$, the differential transadmittance is then given by

$$Y_{md} = G_{m1}\frac{1 + s\tau_2/2}{1 + s\tau_2} = G_{m1}\frac{1 + s/(2\omega_2)}{1 + s/\omega_2} \tag{2.26}$$

where $\tau_2 = 1/\omega_2 \triangleq C_2/G_{m2}$ is the time constant introduced by the current mirror M_{2a}-M_{2b} due to the parasitic capacitance C_2 at node 2. Note that (2.26) is valid for both M_{1a}-M_{1b} in a separate well and in a common substrate. This is due to the fact that in differential mode and assuming a perfect matching, the common source node 1 does not change and can be considered as an ac ground. This means that $\Delta V_1 = 0$ and hence the two small-signal circuits of the left and right schematic become identical.

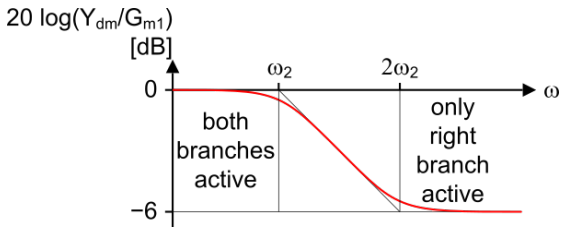

Figure 2.5: Magnitude of the transadmittance Y_{md} normalized to G_{m1} versus the frequency.

The magnitude of Y_{md} normalized to the low-frequency value G_{m1} versus the frequency is shown in Figure 2.5.

A transfer function like (2.26) is called a pole-zero doublet. This means that the zero, situated at twice the value of the pole, is canceling the effect of the pole at frequencies above the zero. For $\omega < \omega_2$, both current branches of the differential pair are active. On the other hand, for $\omega_2 < \omega$, the voltage at node 2 is low-pass filtered and ac grounded and therefore the small-signal current coming from transistor M_{1a} is not copied to the output anymore. The output current is hence only coming from transistor M_{1b}, resulting in half the low-frequency transconductance corresponding to the -6 dB shown in the the plot of Figure 2.5.

The differential mode voltage transfer function A_{vd} is simply given by

$$A_{vd} \triangleq \frac{V_{out}}{V_{id}} = Y_{md} \cdot Z_L \tag{2.27}$$

where Z_L is the output load. In the case the output load is only capacitive

$$Y_L \triangleq 1/Z_L = G_o + s\,C_L \tag{2.28}$$

where G_o is the total conductance at the output node $G_o = G_{ds1b} + G_{ds2b}$. This results in

$$A_{vd} = \frac{G_{m1}}{G_o + sC_L}\frac{1 + s/(2\omega_2)}{1 + s/\omega_2} = A_{dc}\frac{1 + s/(2\omega_2)}{(1 + s/\omega_0)(1 + s/\omega_2)} \tag{2.29}$$

where $A_{dc} \triangleq G_{m1}/G_o$ is the DC gain, $\omega_o \triangleq G_o/C_L$ the dominant pole set by the load capacitance C_L and $\omega_2 \triangleq G_{m2}/C_2$ the non-dominant due to the parasitic capacitance at the current mirror node 2. The Bode plot of the small-signal differential voltage transfer function is plotted in Figure 2.6.

Assuming that the non-dominant pole ω_2 is much higher than the unity gain frequency ω_u (or gain-bandwidth product GBW), the latter is then given by

$$\omega_u = A_{dc} \cdot \omega_0 = \frac{G_{m1}}{G_o}\frac{G_o}{C_L} = \frac{G_{m1}}{C_L}. \tag{2.30}$$

Note that the phase reaches a minimum for $\omega = \sqrt{2}\omega_2$

$$\Phi_{min} = -\frac{\pi}{2} + arctg(\sqrt{2}/2) - arctg(\sqrt{2}) \cong -109.5°. \tag{2.31}$$

2.2.2 Common mode

In common mode, the differential voltage is zero $V_{id} = 0$ and both inputs are controlled by the common mode voltage V_{ic}. The common mode transadmittance Y_{mc} is defined as

$$Y_{mc} \triangleq \frac{I_{out}}{V_{ic}} = -G_{m1}\frac{s^2\tau_1\tau_2}{(1 + s\tau_1)(1 + s\tau_2)} = -G_{m1}\frac{s^2/(\omega_1\omega_2)}{(1 + s/\omega_1)(1 + s/\omega_2)} \tag{2.32}$$

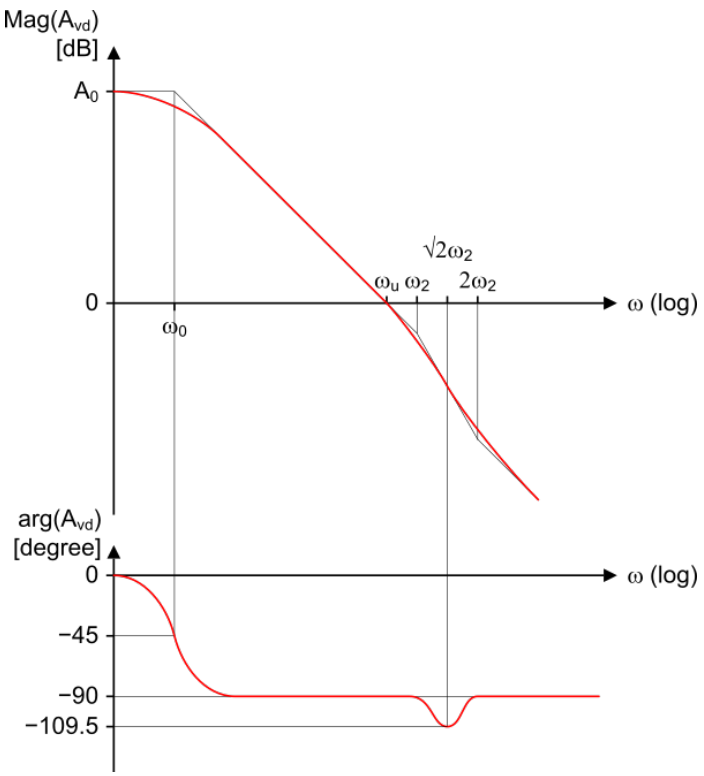

Figure 2.6: Magnitude and phase of the open-loop voltage differential gain A_{vd} normalized to G_{m1} versus the frequency.

where τ_1 corresponds to the time constant of the common source node 1 of the differential pair given by

$$\tau_1 = \frac{1}{\omega_1} = \frac{C_1}{2G_{m1}} \tag{2.33}$$

for M_{1a}-M_{1b} in a separate well and

$$\tau_1 = \frac{1}{\omega_1} = \frac{C_1}{2G_{ms1}} = \frac{C_1}{2n_1 G_{m1}} \tag{2.34}$$

for M_{1a}-M_{1b} in a common substrate. τ_2 corresponds to the time constant of the current mirror node 2 and is given by

$$\tau_2 = \frac{1}{\omega_2} \triangleq \frac{C_2}{G_{m2}}. \tag{2.35}$$

From (2.32) we see that Y_{mc} is zero at low frequency. Note that it is actually limited by the conductance at node 1 G_1 and the mismatch in the differential pair and the current mirror. At high frequency (i.e. $\omega \gg \omega_1$ and $\omega \gg \omega_2$), nodes 1 and 2 are ac grounded and the output current is directly provided by M_{1b}, so that Y_{mc} becomes equal to $-G_{m1}$.

The common-mode rejection ratio (CMMR) is then given by

$$CMRR \triangleq \frac{Y_{md}}{Y_{mc}} = -\frac{(1+s\tau_1)(1+s\tau_2/2)}{s^2\tau_1\tau_2} = -\frac{(1+s/\omega_1)(1+s/(2\omega_2)}{s^2/(\omega_1\omega_2)}, \tag{2.36}$$

which, assuming a perfect matching, is ideally infinite at low frequency and degrades for increasing frequency to reach -6dB at high frequency.

2.3 Noise Analysis

In order to calculate the noise output current I_{nout}, the input terminals are grounded. The small-signal equivalent circuit including the noise sources of all the transistors are shown in Figure 2.7.

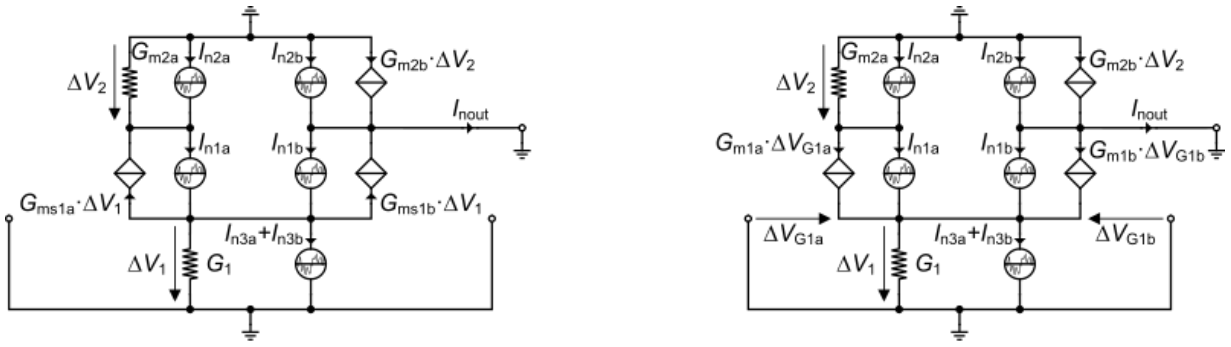

Figure 2.7: Simplified small-signal noise schematic. a) M_{1a}-M_{1b} in common substrate. b) M_{1a}-M_{1b} in separate well.

The left schematic corresponds to M_{1a}-M_{1b} in a separate well whereas the right schematic corresponds to all N-channel transistors in the same substrate. Note that all the output conductances have been neglected. Since we want to calculate the noise at low-frequency (meaning for $\omega < \omega_2$), we can neglect the parasitic capacitances C_1 and C_2. If a perfect symmetry is assumed, then the two currents generated by transconductances G_{m1a} and G_{m1b}, or G_{ms1a} and G_{ms1b} in the above schematic are equal. If the current mirror is also assumed symmetrical, then the current coming from M1 is mirrored at the output and compensated by the current coming directly from M_{1b}. Therefore, the transconductances G_{m1a} and G_{m1b} (respectively G_{ms1a} and G_{ms1b}) have no effect on the output current. They can therefore be neglected. Assuming again perfect symmetry, the noise currents I_{n3a} and I_{n3b} coming from transistors M_{3a} and M_{3b} split equally between the two branches and produce no net current at the output neither. They can therefore also be neglected. Finally, the output noise current is simply given by

$$I_{nout} = I_{n1a} - I_{n2a} - I_{n2a} + I_{n2b}. \tag{2.37}$$

This means that the transfer functions at low-frequency from each of the noise sources to the output current is simply equal to ± 1. Note that the sign is of no importance since for noise we are only interested by the square of the magnitude of the transfer functions.

The power spectral density (PSD) of the output noise current is then given by

$$S_{nout}(f) = 4kT \cdot G_{nout}(f), \tag{2.38}$$

with

$$G_{nout}(f) = G_{n1a}(f) + G_{n1b}(f) + G_{n2a}(f) + G_{n2b}(f) = 2(G_{n1}(f) + G_{n2}(f)). \tag{2.39}$$

The noise conductances $G_{ni}(f)$ with $i = 1, 2$, are frequency dependent since they include both the thermal and the 1/f noise. They are given by

$$G_{ni}(f) = \gamma_{ni} G_{mi} + G_{mi}^2 \frac{\rho_i}{W_i L_i f}, \tag{2.40}$$

for $i = 1, 2$ where $\rho_1 = \rho_n$ and $\rho_2 = \rho_p$ and

$$\gamma_{ni} = \frac{n_i}{2} \tag{2.41}$$

in weak inversion and saturation and

$$\gamma_{ni} = \frac{2}{3} n_i. \tag{2.42}$$

The noise can be referred to the differential input by dividing G_{nout} by G_{m1}^2, resulting in

$$R_{nin}(f) \triangleq \frac{G_{nout}}{G_{m1}^2} = R_{nt} + R_{nf}(f) \tag{2.43}$$

where R_{nt} is the part of the input-referred noise resistance corresponding to the thermal noise

$$R_{nt} = 2\left(\frac{\gamma_{n1}}{G_{m1}} + \gamma_{n2}\frac{G_{m2}}{G_{m1}^2}\right) = \frac{2\gamma_{n1}}{G_{m1}} \cdot (1 + \eta_{th}), \tag{2.44}$$

where

$$\eta_{th} = \frac{\gamma_{n2}}{\gamma_{n1}}\frac{G_{m2}}{G_{m1}} \tag{2.45}$$

represents the contribution to the input-referred thermal noise of the current mirror relative to that of the differential pair.

The flicker noise resistance $R_{nf}(f)$ is the part corresponding to the 1/f noise

$$R_{nf}(f) = 2\left[\frac{\rho_n}{W_1 L_1 f} + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{\rho_p}{W_2 L_2 f}\right] = \frac{2\rho_n}{W_1 L_1 f} \cdot (1 + \eta_{fl}). \tag{2.46}$$

where

$$\eta_{fl} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{\rho_p}{\rho_n}\frac{W_1 L_1}{W_2 L_2} \tag{2.47}$$

represents the contribution to the input-referred flicker noise of the current mirror relative to the differential pair.

In the same way a noise excess factor γ_n has been defined for a single transistor, a thermal noise excess factor can also be defined for the complete OTA as

$$\gamma_{ota} \triangleq G_m \cdot R_{nt} = \frac{G_{nout,thermal)}}{G_m} = 2\gamma_{n1} \cdot (1 + \eta_{th}) \tag{2.48}$$

where $G_m = G_{m1}$ is the OTA differential transconductance. The total input-referred thermal noise resistance then writes

$$R_{nt} = \frac{\gamma_{ota}}{G_{m1}}. \tag{2.49}$$

The minimum value of the OTA noise excess factor is equal to that of the differential pair only, namely $\gamma_{ota,min} = 2\gamma_{n1}$. In order to limit the contribution of the current mirror to a minimum, the second term in the bracket of (2.48) should be made much smaller than one. This can be achieved by setting the transconductance ratio $G_{m2}/G_{m1} \ll 1$. This can be done by biasing M_{1a}-M_{1b} in weak inversion and M2-M_{2b} in strong inversion, respectively. Replacing G_{m2}/G_{m1} by

$$\frac{G_{m2}}{G_{m1}} = \frac{2n_1 U_T}{n_2 V_{DSsat2}} = \frac{2n_1 U_T}{n_2 V_{P2}} \cong \frac{2n_1 U_T}{V_{G2} - V_{TOp}} \tag{2.50}$$

results in

$$\gamma_{ota} = 2\gamma_{n1}\left(1 + \frac{\gamma_{n2}}{\gamma_{n1}}\frac{2n_1 U_T}{V_{G2} - V_{TOp}}\right) = n_1\left(1 + \frac{8n_2}{3}\frac{U_T}{V_{G2} - V_{TOp}}\right), \tag{2.51}$$

where $\gamma_{n1} = n_1/2$ and $\gamma_{n2} = n_2 2/3$. The OTA thermal noise excess factor is therefore minimized by setting the transconductance ratio $G_{m2}/G_{m1} \ll 1$, which is realized easily if transistors M_{1a}-M_{1b} are biased in weak inversion and M2-M_{2b} in strong inversion and by choosing an overdrive voltage $V_{G2} - V_{TOp}$ of M2-M_{2b} much larger than $8n_2/3U_T \cong 4U_T$ where it has been assumed that $n_2 \cong 3/2$.

The 1/f noise corner frequency f_k is defined as the frequency at which the 1/f noise becomes equal to the thermal noise

$$R_{nf}(f_k) = R_{nt} \tag{2.52}$$

and is given by

$$f_k = \frac{G_{m1}}{\gamma_{ota}}\frac{2\rho_n}{W_1 L_1} \cdot (1 + \eta_{fl}). \tag{2.53}$$

The corner frequency can be reduced by increasing $W_1\,L_1$ and $W_2\,L_2$ at the same time to conserve the same η_{fl} factor. Of course increasing the area of transistors M1 and M2 increases the parasitic capacitance at node 2 and hence decreases the non-dominant pole ω_2.

2.4 Input-referred offset voltage

Mismatch between the two transistors of the differential pair M_{1a}-M_{1b} and of the current mirror M2-M_{2b} causes some current to flow at the output even for a zero differential input voltage $V_{id} = 0$. This output current can be compensated by applying a certain differential input voltage defined as the input-referred offset voltage V_{os}.

The analysis of the mismatch effects for deriving the variance of the input-referred offset voltage can be done similarly to the noise analysis. We can reuse (2.37) with

$$I_{n1a} = +\frac{\Delta I_{D1}}{2}, \tag{2.54}$$

$$I_{n1b} = -\frac{\Delta I_{D1}}{2}, \tag{2.55}$$

$$I_{n2a} = -\frac{\Delta I_{D2}}{2}, \tag{2.56}$$

$$I_{n2b} = +\frac{\Delta I_{D2}}{2}, \tag{2.57}$$

and where ΔI_{D1} and ΔI_{D2} are the current mismatch in the differential pair and in the current mirror, respectively. The output current due to these current mismatches is then given by

$$I_{out} = \Delta I_{D1} + \Delta I_{D2}. \tag{2.58}$$

Of course ΔI_{D1} and ΔI_{D2} are random variables. The variance of the offset output current is then given by

$$\sigma^2_{Iout} = \sigma^2_{\Delta I_{D1}} + \sigma^2_{\Delta I_{D2}} = I_b^2 \cdot \left(\sigma^2_{\Delta I_{D1}/I_{D1}} + \sigma^2_{\Delta I_{D2}/I_{D2}}\right) \tag{2.59}$$

where

$$\sigma^2_{\Delta I_{D1}/I_{D1}} = \sigma^2_{\beta 1} + \left(\frac{G_{m1}}{I_b}\right)^2 \sigma^2_{VT1}, \tag{2.60}$$

$$\sigma^2_{\Delta I_{D2}/I_{D2}} = \sigma^2_{\beta 2} + \left(\frac{G_{m2}}{I_b}\right)^2 \sigma^2_{VT2}. \tag{2.61}$$

with

$$\sigma^2_{\beta i} = \frac{A^2_\beta}{W_i L_i}, \tag{2.62}$$

$$\sigma^2_{V_{T0i}} = \frac{A^2_{VT}}{W_i L_i}. \tag{2.63}$$

for $i = 1, 2$. A_β (usually given in $\%{\cdot}\mu$m) and A_{VT} (usually given in mV$\cdot\mu$m) are the β and threshold matching parameters for the process to be used.

The variance of the output offset current then writes

$$\sigma^2_{Iout} = I_b^2 \cdot \left(\sigma^2_{\beta 1} + \sigma^2_{\beta 2}\right) + G^2_{m1}\, \sigma^2_{VT1} + G^2_{m2}\, \sigma^2_{VT2}. \tag{2.64}$$

The variance of the input-referred offset voltage is obtained by dividing the variance of the output offset current (2.64) by G^2_{m1} resulting in

$$\sigma^2_{Vos} = \left(\frac{I_b}{G_{m1}}\right)^2 \left(\sigma^2_{\beta 1} + \sigma^2_{\beta 2}\right) + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \sigma^2_{VT2} + \sigma^2_{VT1}. \tag{2.65}$$

which can be written as

$$\sigma^2_{Vos} = \sigma^2_{VT} + \sigma^2_{\beta}, \tag{2.66}$$

where σ_{VT} is the V_T-mismatch given by

$$\sigma_{VT}^2 = \sigma_{V_{T1}}^2 \cdot (1 + \xi_{V_T}). \tag{2.67}$$

where ξ_{V_T} represents the V_T-mismatch contribution to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_{V_T} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \cdot \frac{\sigma_{V_{T2}}^2}{\sigma_{V_{T1}}^2} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \cdot \left(\frac{A_{V_{Tp}}}{A_{V_{Tp}}}\right)^2 \cdot \frac{W_1\, L_1}{W_2\, L_2}. \tag{2.68}$$

σ_β is the β-mismatch given by

$$\sigma_\beta^2 = \left(\frac{I_b}{G_{m1}}\right)^2 \cdot \sigma_{\beta_1}^2 \cdot (1 + \xi_\beta), \tag{2.69}$$

where ξ_β represents the β-mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_\beta = \frac{\sigma_{\beta_2}^2}{\sigma_{\beta_2}^2} = \left(\frac{A_{\beta_p}}{A_{\beta_n}}\right)^2 \cdot \frac{W_1\, L_1}{W_2\, L_2}. \tag{2.70}$$

From (2.69), we see that the contribution of the β mismatch to the input-referred offset voltage can be minimized by choosing I_b/G_{m1} as small as possible (or G_{m1}/I_b as large as possible). This can be done by biasing the transistors of the differential pair in weak inversion. Secondly, from (2.68) we see that the contribution of the V_T mismatch of the current mirror ξ_{V_T} an also be minimized by setting $G_{m2}/G_{m1} \ll 1$. Since $\mathrm{M_{1a}}$ and $\mathrm{M_{2a}}$ ($\mathrm{M_{1b}}$ and $\mathrm{M_{2b}}$) share the same bias current $I_{D1} = I_{D2} = I_b$, this can only be done by biasing the current mirror $\mathrm{M_{2a}}$-$\mathrm{M_{2b}}$ in strong inversion. In this case, the transconductances of $\mathrm{M_1}$ and $\mathrm{M_2}$ are then given by $G_{m1} = I_b/(n_1 U_T)$ and $G_{m2} = 2I_b/(n_2 V_{DSsat2})$ with $V_{DSsat} = V_{P2}$, leading to

$$\frac{G_{m2}}{G_{m1}} = \frac{2n_1U_T}{n_2V_{DSsat2}} = \frac{2n_1U_T}{n_2V_{P2}} \cong \frac{2n_1U_T}{V_{G2} - V_{TOp}} \tag{2.71}$$

The overdrive voltage of $\mathrm{M_{2a}}$-$\mathrm{M_{2b}}$ $V_{G2} - V_{TOp}$ has therefore to be chosen much larger than $2n_1U_T$. However, the overdrive voltage $V_{G2} - V_{TOp}$ cannot be made too large since it will lead to a large V_{SG2} voltage that, for a given input common mode voltage, will push $\mathrm{M_{1a}}$ out of saturation.

3 Design

3.1 Physical and process Parameters

The physical parameters are given in Table 3.1, the global process parameters in Table 3.2 and finally the MOSFET parameters in Table 3.3.

> **Warning**
>
> The matching parameters for IHP 130nm are unknown. We will use those from a generic 180nm technology.

Table 3.1: Physical parameters

Parameter	Value	Unit
T	300	K
U_T	25.865	mV

Table 3.2: Process parameters.

Parameter	Value	Unit	Comment
t_{ox}	2.24	nm	SiO_2 oxyde thickness
C_{ox}	15.413	$\frac{fF}{\mu m^2}$	Oxyde capacitance per unit area
V_{DD}	1.2	V	Nominal supply voltage
L_{min}	130	nm	Minimum drawn gate length
W_{min}	150	nm	Minimum drawn gate width
z_1	340	nm	Minimum outer diffusion width
z_2	389	nm	Minimum diffusion width between two fingers

Table 3.3: Transistors parameters.

Parameter	nMOS	pMOS	Unit
Length and width correction parameters for current			
DL	59	51	nm
DW	-20	30	nm
Length and width correction for intrinsic and overlap capacitances			
$DLCV$	93	146	nm
$DWCV$	-10	15	nm
Length and width correction parameter for fringing capacitances			
$DLGCV$	34	96	nm
$DWGCV$	10	-15	nm
Long-channel sEKV parameters parameters			
n	1.22	1.23	-

Table 3.3: Transistors parameters.

Parameter	nMOS	pMOS	Unit
$I_{spec\square}$	708	245	nA
V_{T0}	246	365	mV
Short-channel sEKV parameters parameters			
L_{sat}	7.1	24.9	nm
λ	0.8	6.078	$\frac{V}{\mu m}$
Junction capacitances parameters			
C_J	0.976	0.863	$\frac{fF}{\mu m^2}$
C_{JSWSTI}	0.025	0.032	$\frac{fF}{\mu m}$
C_{JSWGAT}	0.03	0.027	$\frac{fF}{\mu m}$
Overlap capacitances parameters			
C_{GSo}	0.453	0.443	$\frac{fF}{\mu m}$
C_{GDo}	0.453	0.443	$\frac{fF}{\mu m}$
C_{GBo}	0	0.022	$\frac{fF}{\mu m}$
Fringing capacitances parameters			
C_{GSf}	0.2	0.1	$\frac{fF}{\mu m}$
C_{GDf}	0.2	0.1	$\frac{fF}{\mu m}$
Flicker noise parameters			
K_F	3.175e-24	1.2e-23	VAs
AF	1	1	-
ρ	0.01243	0.04697	$\frac{Vm^2}{As}$
Matching parameters			
A_{VT}	5	5	$mV \cdot \mu m$
A_β	1	1	$\% \cdot \mu m$

The threshold voltage of NMOS is 0.246 V.

3.2 Specifications

The OTA specifications are given in Table 3.4.

> **Note**
>
> The specifications given below are simplified specifications. They are mainly targeting the achievement of a certain gain-bandwidth product GBW which sets the differential pair transconductance at minimum current and power consumption. There are additional specifications on random input-referred offset voltage which might eventually require to increase the transistors area. There are no specifications on thermal noise since the transconductance is set by the GBW. There are no specifications on the flicker noise but if the corner frequency was set lower this would required to increase the transistors area. There are also no specifications on the slew-rate, which might be small because of the low-power objective. Finally, there are many more specifications such as CMRR, PSRR, input common-mode voltage range, output-voltage swing, etc... that are not discussed in this example.

> ⚠ Warning
>
> The output conductance of nMOS transistors for the IHP 130nm process is very high. We can therefore not set the DC gain specification too high.

Table 3.4: OTA specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	30	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF
Maximum input-referred offset voltage	$V_{os,max}$	10	mV

3.3 Design procedure

> ❗ Important
>
> For this process, the transistor dimensions are rounded to 10nm. We also will ignore the length and width reduction parameters DL and DW. The main reason is that most of the transistor length and width are sufficiently large that ignoring these parameters has little impact.

3.3.1 Sizing of M_{1a}-M_{1b}

M_{1a}-M_{1b} are biased in weak inversion in order to minimize the input-referred offset. They are sized according to the specification on the GBW and the load capacitance and the required slew-rate.

Recalling that

$$GBW = \frac{G_{m1}}{2\pi C_{out}}, \tag{3.1}$$

where C_{out} is the total output capacitance which includes the parasitic capacitance and the load capacitance C_L. Since we do not yet know the sizes of M_{1a} and M_{2b}, we cannot estimate the total output capacitance. We will start assuming $C_{out} = C_L$.

G_{m1} is the gate transconductance of M_{1a}-M_{1b} which in weak inversion is given by

$$G_{m1} = \frac{I_b}{nU_T}. \tag{3.2}$$

The bias current I_b is the current flowing in each transistor M_{1a}-M_{1b} when the input differential voltage is zero. The bias current provided by M_{3b} is therefore $2I_b$. The bias current must satisfy the following inequality:

$$I_b \geq 2\pi n_{0n} U_T C_L GBW_{min}, \tag{3.3}$$

which for the given specifications gives $I_{b,min} = 198\ nA$. The corresponding slew-rate is then equal to $SR_{min} = 198\ mV/\mu s$ which we will consider as sufficient.

> ❗ Important
>
> If the slew-rate is not sufficient, the bias current I_b should be increased or a dynamic or adaptive biasing OTA should be used.

To have some margin to account for the additional parasitic capacitance at the output due to the junction capacitances that add to the load capacitance C_L, we set $I_b = 250\ nA$ and the inversion coefficient $IC_1 = 0.1$. The transconductance can be calculated from the G_m/I_D function as

$G_{m1} = \frac{I_b}{n_{0n}\, U_T} \cdot gmsid(IC_1) = 7.258\ \frac{\mu A}{V}$.

This leads to a gain-bandwidth product

$GBW = \frac{G_{m1}}{2\pi\, C_L} = 1.2\ MHz$,

which is slightly higher than the target specification offering some margin.

Knowing the drain current I_{D1} and the inversion coefficient, we can calculate the W/L aspect ratio for M_{1a}-M_{1b} as

$\frac{W_1}{L_1} = \frac{I_b}{I_{spec\square n}\, IC_1} = 3.5.$

The degree of freedom left (W_1 or L_1) can be determined by constraints either on the DC gain, the offset voltage or the flicker noise. In this example we will set a minimum DC gain. The latter is given by

$$A_{dc} = \frac{G_{m1}}{G_o} \tag{3.4}$$

where $G_o = G_{ds1b} + G_{ds2b}$ is the conductance to the AC ground at the output node. The output conductances are estimated with the following simple model

$$G_{dsi} = \frac{I_{Di}}{V_{Mi}} \tag{3.5}$$

with $V_{Mi} = \lambda_i \cdot L_i$. Note that this model of the output conductance is only a very rough approximation and that the gain should be checked by simulation. Some margin can be taken to ensure a sufficient DC gain.

A good trade-off for the output conductance is to set $G_{ds1b} = G_{ds2b}$ or since M_{1a}-M_{2b} share the same bias current $V_{M1b} = V_{M2b}$. The minimum length of M_{1a}-M_{2b} is then given by

$L_1 = 2.72\ \mu m.$

which gives the width of M_{1a}-M_{1b}

$W_1 = 9.60\ \mu m.$

We can recompute the transconductance and gain-bandwidth product for the chosen dimensions of M_{1a}-M_{1b}

$I_{spec1} = 2.5\ \mu A$,

$IC_1 = 0.1$,

$G_{spec1} = 79.2\ \mu A/V$,

$G_{m1} = 7.3\ \mu A/V$,

$GBW = 1.2\ MHz$.

3.3.2 Sizing of M_{3a}-M_{3b}

The sizing of M_{3a}-M_{3b} is conditioned by the minimum common-mode input voltage $V_{ic,min}$ to be handled according to

$$V_{ic,min} = V_{GS1} + V_{DSsat3}. \tag{3.6}$$

Because long-channel nMOS transistors have a small threshold voltage in this technology, the minimum common-mode input voltage $V_{ic,min}$ can be low. If we choose an inversion coefficient for M_{3a}-M_{3b} equal to $IC_3 = 20$, we get $V_{DSsat3} = 253\ mV$ and $V_{ic,min} = 430\ mV$, which is low enough. We then get the I_{spec} and W/L ratio

$I_{spec3} = 14.166\ \mu A$ and

$W_3/L_3 = 0.035$.

Since this W/L is rather small, we need to set W_3 to W_{min} and calculate the length L_3

$W_3 = 150\ nm$,

$L_3 = 4.25\ \mu m$.

We can now size the current mirror M_{2a}-M_{2b}.

3.3.3 Sizing of M_{2a}-M_{2b}

The gate voltage of M_{2a} should be set as low as possible for a given maximum common mode input voltage still keeping M_{1a} in saturation. For a maximum input common-mode voltage $V_{ic,max}$ given by

$V_{ic,max} = 0.7\ V$,

the source-to-gate voltage of M_{2a} V_{SG2a} is given by

$$V_{SG2a} = V_{DD} - V_{icmax} + V_{GS1a} - V_{DSsat1a}. \tag{3.7}$$

The saturation voltage of M_{1a}-M_{1b} only depends on IC_1. For the chosen $IC_1 = 0.1$ it is given by

$V_{DSsat1a} = 105\ mV$.

The gate-to-source voltage V_{GS1a} is given by

$$V_{GS1a} = V_{T0n} + (n_{0n} - 1)\, V_{S1} + n_{0n}\, U_T\, (v_p - v_s). \tag{3.8}$$

In this design we have chosen to put M_{1a}-M_{1b} in a separate well, hence $V_{SB1} = 0$ and V_{GS1a} reduces to

$$V_{GS1a} = V_{T0n} + n_{0n}\, U_T\, (v_p - v_s), \tag{3.9}$$

where $v_p - v_s$ can be estimated from the inversion coefficient IC_1. For the chosen $IC_1 = 0.1$, this gives $V_{GS1} \cong 176\ mV$ and for the chosen maximum input common-mode voltage $V_{ic,max} = 0.7\ V$, this results in

$V_{SG2} = 572\ mV$,

which corresponds to an inversion coefficient given by

$IC_2 = 10.3$.

Because V_{SG2} also sets the output quiescent voltage, we could slightly increase V_{SG2} so that the quiescent output voltage is set at $V_{DD}/2 = 0.6\ V$. Choosing

$V_{SG2} = 600\ mV$,

corresponds to an inversion coefficient and a saturation voltage given by

$IC_2 = 12.9$ and

$V_{DSsat2} = 213\ mV$.

The specific current I_{spec}, transconductance G_m and W/L are then given by

$I_{spec2} = 19.41\ nA$,

$G_{m2} = 1.906\ \mu A/V$,

$W_2/L_2 = 0.079$.

The length of M_{2a}-M_{2b} is set by the dc gain similarly to the length of M_{1a}-M_{1b} resulting in

$L_2 = 0.36\ \mu m$.

We can now derive M_{2a}-M_{2b} transistor width

$W_2 = 30\ nm$,

which is smaller than the minimum width $W_{min} = 150\ nm$.

We then set W_2 to the minimum width and deduce the length

$W_2 = W_{min} = 150\ nm$ and

$L_2 = 1.89\ \mu m$.

Since L_2 is longer than the initial value it will not affect the DC gain which should actually be slightly larger. We can evaluate the transconductance G_{m2}

$G_{m2} = 1.906\ \mu A/V$.

Since G_{m2} may become small, we need to check whether the non-dominant pole f_{p2} lies sufficiently high above the GBW to insure the desired phase margin. The non-dominant pole is given by

$$\omega_{p2} = \frac{G_{m2}}{C_2}, \tag{3.10}$$

where C_2 is given by

$$C_2 = 2(C_{GS2} + C_{GB2}) \tag{3.11}$$

Assuming M_2 is in saturation, we have

$$C_{GS2} \cong W_2\, L_2\, C_{ox} \cdot c_{gsi} + (C_{GSop} + C_{GSfp}) \cdot W_2 \tag{3.12}$$

where c_{gsi} is the normalized intrinsic gate-to-source capacitance which is typically equal to 2/3 in strong inversion and is proportionnal to IC in weak inversion. The gate-to-bulk capacitance C_{GB2} is given by

$$C_{GB2} \cong W_2\, L_2\, C_{ox} \cdot c_{gbi} + C_{GBop} \cdot W_2, \tag{3.13}$$

where c_{gbi} is the normalized gate-to-bulk intrinsic capacitance given by

$$c_{gbi} = \frac{n-1}{n} \cdot c_{gsi}. \tag{3.14}$$

The capacitance at node 2 scales with W_2 and L_2 according to

$$C_2 = C_{WL} \cdot W_2\, L_2 + C_W \cdot W_2, \tag{3.15}$$

with

$$C_{WL} = 2\, C_{ox} \cdot (c_{gsi} + c_{gbi}), \tag{3.16}$$

$$C_W = 2(C_{GSop} + C_{GSfp} + G_{GBop}). \tag{3.17}$$

This results in

$C_{GS2} = 2.56\ fF$,

$C_{GB2} = 0.36\ fF$,

$C_2 = 5.83\ fF$,

$f_{p2} = 52.060\ MHz$,

which is much higher than the specified GBW.

In case it would not be, we need to reduce IC_2 which will increase the G_m/I_D and since the current is set by the bias current I_b, it will increase G_{m2}. If W_2 is set to its minimum value W_{min}, decreasing IC_2 keeping the same current, will increase the W_2/L_2. With W_2 set, this leads to a decrease of L_2 and hence a decrease of C_2. The increase of G_{m2} and decrease of C_2 leads to an increase of f_{p2}, as required. We can use the following script to find the required IC for having the non-dominant pole at 10 times the GBW.

Running the optimizer results in

$IC_2 = 38.$

$G_{m2} = 1.180\ \mu A/V$,

$G_{m1}/G_{m2} = 6.151$,

$W_2/L_2 = 0.027$,

$W_2 = 150\ nm$,

$L_2 = 5.53\ \mu m$,

$f_{p2} = 10.000\ MHz$,

$f_{p2}/GBW = 10.$

We see that IC_2 has been increased, increasing G_{m2} and W_2/L_2 for the given current I_b. Since W_2 hits W_{min}, the length L_2 has been slightly increased, increasing C_2 at the same time to set f_{p2} at 10 times the GBW. Now, this has also increased V_{SG2}

$V_{SG2} = 780\ mV$,

which reduces the maximum input common-mode voltage to

$V_{ic,max} = 0.491\ V$,

which is now too low.

Another approach is to take advantage of the margin we have on f_{p2} to limit the flicker noise contribution of M_{2a}-M_{2b}. To do so, we can increase $W_2\,L_2$ while keeping the same IC_2 and W_2/L_2 ratio and therefore also the same V_{SG2} and $V_{ic,max}$. This results in

$W_2 = 350\ nm$,

$L_2 = 4.35\ \mu m.$

We can check the new value of f_{p2} which as expected is given by

$f_{p2} = 10\ MHz$,

$f_{p2}/GBW = 10.$

The sizing process is now finished. The resulting design is summarized in the next section.

3.4 Summary

3.4.1 Specifications

The specifications are recalled in Table 3.5.

Table 3.5: OTA specifications.

Specification	Symbol	Value	Unit
Minimum DC gain	A_{dc}	30	dB
Minimum gain-bandwidth product	GBW	1	MHz
Load capacitance	C_L	1	pF
Maximum input-referred random offset voltage	$V_{os,max}$	10	mV
Phase margin	PM	60	$^\circ$

3.4.2 Bias

The bias information are summarized in Table 3.6.

Table 3.6: OTA bias.

Bias voltage or current	Symbol	Value	Unit
Supply voltage	V_{DD}	1.2	V
Bias current	I_b	250	nA

3.4.3 Transistor information

The transistor sizes and large-signal variables are summarized in Table 3.7, whereas Table 3.8 gives the small-signal and thermal noise parameters. An Excel table is generated with more information (e.g. all the parasitic capacitances).

Table 3.7: Transistor size and bias information.

Transistor	W $[\mu m]$	L $[\mu m]$	I_D $[nA]$	I_{spec} $[nA]$	IC	$V_G - V_{T0}$ $[mV]$	V_{DSsat} $[mV]$
M1a	9.60	2.72	250	2500	0.1	-47	105
M1b	9.60	2.72	250	2500	0.1	-47	105
M2a	0.35	4.35	250	20	12.7	154	211
M2b	0.35	4.35	250	20	12.7	154	211
M3a	0.15	4.25	500	25	20.0	199	253
M3b	0.15	4.25	500	25	20.0	199	253

Table 3.8: Transistor small-signal and thermal noise parameters.

Transistor	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M1a	96.651	8.854	7.258	114.890	0.627
M1b	96.651	8.854	7.258	114.890	0.627
M2a	0.761	2.358	1.917	9.456	0.770
M2b	0.761	2.358	1.917	9.456	0.770
M3a	0.967	3.866	3.169	147.059	0.773

Table 3.8: Transistor small-signal and thermal noise parameters.

Transistor	G_{spec} $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_m $[\mu A/V]$	G_{ds} $[nA/V]$	γ_n
M3b	0.967	3.866	3.169	147.059	0.773

4 OTA Characteristics

In this section, we check whether the specs are achieved.

4.1 Open-loop gain

The calculated OTA features are given in Table 4.1.

Table 4.1: OTA gain variables.

Symbol	Theoretical Value	Unit
A_{dc}	35	dB
G_{m1}	7.258	$\mu A/V$
G_{m2}	1.917	$\mu A/V$
f_0	19.79	kHz
GBW	1.155	MHz
f_{p2}	9.923	MHz
f_{z2}	19.846	MHz

> **Warning**
>
> The slight differences between the value of f_{p2} calculated during the design process and the value shown in Table 4.1 is due to the width and length rounding process.

Using the values given in Table 4.1, we can now plot the gain response shown in Figure 4.1.

4.2 Input-referred noise

We can now compute all the parameters needed for the calculation of the OTA thermal noise excess factor and its input-referred thermal noise resistance. They are given in Table 4.2.

Table 4.2: OTA thermal noise parameters.

Symbol	Theoretical Value	Unit
G_{m1}	7.258	$\mu A/V$
G_{m2}	1.917	$\mu A/V$
G_{m1}/G_{m2}	3.786	-
γ_{n1}	0.627	-
γ_{n2}	0.77	-
η_{th}	0.324	-
R_{nt}	228.847	$k\Omega$
γ_{ota}	1.661	-
$\sqrt{S_{ninth}}$	61.59	$nV/\sqrt{Hz}$
$10 \cdot \log(S_{ninth})$	-144.21	$dBv/\sqrt{Hz}$

Table 4.2: OTA thermal noise parameters.

Symbol	Theoretical Value	Unit

From Table 4.2, we see that $\eta_{th} = 0.324$ and hence that the OTA thermal noise excess factor is only slightly larger than that of the differential pair. This is due to the G_{m1}/G_{m2} ratio as shown in Table 4.2.

We can now compute all the parameters needed for the calculation of the input-referred flicker noise and the corner frequency. They are given in Table 4.3.

Table 4.3: OTA flicker noise parameters.

Symbol	Theoretical Value	Unit
$(G_{m1}/G_{m2})^2$	14.3	-
ρ_p/ρ_n	3.8	-
$\frac{W_1 \cdot L_1}{W_2 \cdot L_2}$	17.2	-
η_{fl}	4.907	-
$\sqrt{S_{ninfl}(1\,Hz)}$	9.7	$\mu V/\sqrt{Hz}$
$10 \cdot \log(S_{ninfl}(1\,Hz))$	-100.2	$dBv/\sqrt{Hz}$
f_k	25	kHz

From Table 4.3, we see that M2a-M2b contributes 4.907 times more than M1a-M1b. This is coming from the fact that $W_1\,L_1$ is 17 times larger than $W_2\,L_2$ and that ρ_p is 3.8 times larger than ρ_n. The flicker noise will therefore be dominated by M2a-M2b.

We can plot the input-reffered noise which is shown in Figure 4.2.

4.3 Input-referred offset

The variance of the input-referred offset is given by (2.66) which is repeated below

$$\sigma_{Vos}^2 = \sigma_{VT}^2 + \sigma_{\beta}^2, \tag{4.1}$$

where σ_{VT} is the V_T-mismatch given by

$$\sigma_{VT}^2 = \sigma_{V_{T1}}^2 \cdot (1 + \xi_{V_T}). \tag{4.2}$$

where ξ_{V_T} represents the V_T-mismatch contribution to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_{V_T} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \cdot \frac{\sigma_{V_{T2}}^2}{\sigma_{V_{T1}}^2} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \cdot \left(\frac{A_{V_{Tp}}}{A_{V_{Tp}}}\right)^2 \cdot \frac{W_1\,L_1}{W_2\,L_2}. \tag{4.3}$$

σ_β is the β-mismatch given by

$$\sigma_\beta^2 = \left(\frac{I_b}{G_{m1}}\right)^2 \cdot \sigma_{\beta_1}^2 \cdot (1 + \xi_\beta), \tag{4.4}$$

where ξ_β represents the β-mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_\beta = \frac{\sigma_{\beta_2}^2}{\sigma_{\beta_2}^2} = \left(\frac{A_{\beta_p}}{A_{\beta_n}}\right)^2 \cdot \frac{W_1\,L_1}{W_2\,L_2}, \tag{4.5}$$

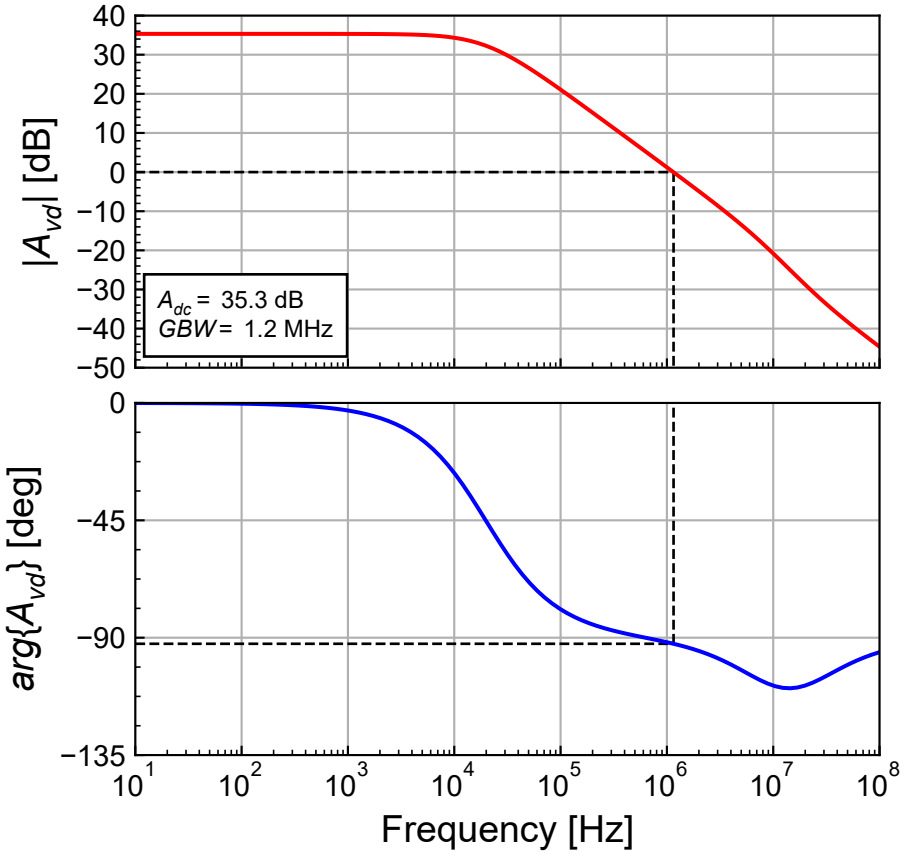

Figure 4.1: OTA theoretical transfer function.

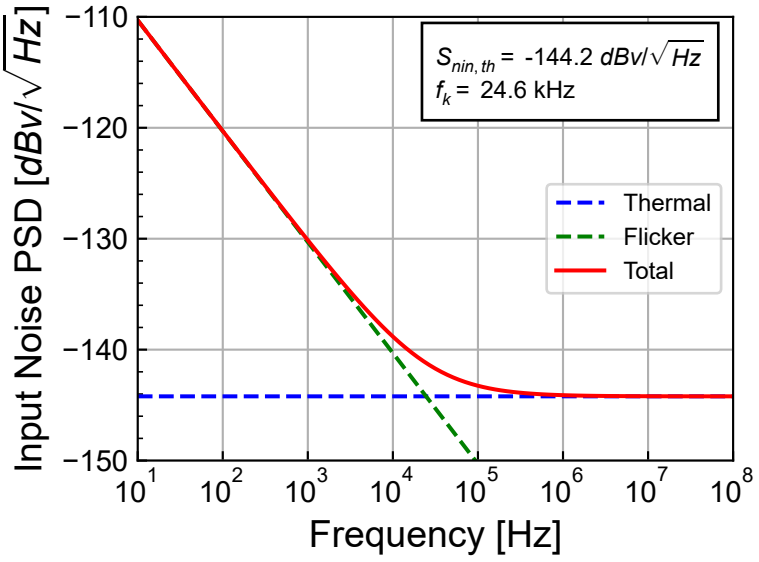

Figure 4.2: OTA theoretical input-referred noise PSD.

where

$$\sigma^2_{\beta_i} = \frac{A^2_\beta}{W_i L_i} \qquad i = 1, 2, \tag{4.6}$$

$$\sigma^2_{V_{T0i}} = \frac{A^2_{VT}}{W_i L_i} \qquad i = 1, 2. \tag{4.7}$$

The parameter for calculating the standard deviation of the input-referred offset voltage are given in Table 4.4.

Table 4.4: OTA input-referred offset parameters.

Symbol	Theoretical Value	Unit
σ_{VT1}	0.978475	mV
σ_{VT2}	4.0522	mV
$\sigma_{\beta 1}$	0.195695	%
$\sigma_{\beta 2}$	0.810441	%
ξ_{VT}	1.19665	-
ξ_β	17.1507	-
$\sigma^2_{V_T}$	2.10311	mV^2
σ_{V_T}	1.45021	mV
σ^2_β	0.0824769	mV^2
σ_β	0.287188	mV
σ_{Vos}	1.478	mV

From Table 4.4, we see that the dominant contribution to the input-referred offset voltage is due to the differential pair M_{1a}-M_{1b}. The resulting total input-referred offset voltage is $\sigma_{Vos} = 1.478\ mV$.

4.4 Current and power consumption

The total current consumption without accounting for the bias string M_{3a} is simply $I_{tot} = 2\, I_b = 500\ nA$, resulting in power consumption $P = V_{DD} \cdot I_{tot} = 0.6\ \mu W$.

5 Simulation results from ngspice

The theoretical results can be validated by comparing them to the results obtained from simulations performed with ngspice. The cells below will run the simulations with ngspice. In order to run the simulations you need to have ngspice installed. Please refer to the ngspice instructions.

> **Note**
>
> The simulations are performed with the PSP 103.6 compact model [1]. For ngspice, we use the Verilog-A implementation given in the IHP package [2] and compiled the OSDI file with OpneVAF [3] to run with ngspice [4].

In addition to the PSP user manual [1] a documentation of PSP and other MOSFET compact models and their parameter extraction can be found in [5].

5.1 Operating point

We first write the parameter file for this specific design for running the ngspice simulations. Before running the AC and NOISE simulations, we first need to check the quiescent voltages and currents and the operating points of all transistors by running an .OP simulation. The node voltages are extracted from the .ic file and presented in Table 5.1.

Table 5.1: OTA node voltages with the OTA in open-loop without offset correction.

Node	Voltage
vdd	1.2
inp	0.6
inn	0.6
id	0
ic	0.6
out	0.619188
1	0.458839
2	0.619211
3	0.486659

From Table 5.1, we see that the ouput voltage $V_{outq} = 619\ mV$ of the open-loop circuit is not extactly equal to the input common-mode voltage $V_{ic} = V_{DD}/2 = 600\ mV$, but sufficiently close. Since the operating point is in the high gain region, we don't need to impose an offset voltage to bring the output voltage in the high gain region.

The operating point information for all transistors coming from the PSP compact model are extracted from the ngspice .op.dat file. The data is split into the large-signal operating informations presented in Table 5.2, the small-signal operating point informations shown in Table 5.3 and the noise operating point informations in Table 5.4.

The sEKV parameters I_{spec} and the inversion coefficient IC calculated from the PSP operating point information are given in Table 5.5. We can compare these valuse to the results of the design given in Table 3.7. We observe that the values are close.

The slope factor and the source transconductance can be calculated from the gate and bulk transconductances as

$$n = \frac{G_{mb}}{G_m} - 1, \tag{5.1}$$

$$G_{ms} = n \cdot G_m. \tag{5.2}$$

They are given in Table 5.6.

The noise parameters calculated from Table 5.4 are given in Table 5.7. The γ_n noise excess factors for the nMOS transistors are close to the theoretical values. However the γ_n noise excess factor for the pMOS device M_{2a}-M_{2b} are about twice the theoretical value. This is a bit questionable because M_{2a}-M_{2b} are long-channel transistors.

We can also check the bias voltages and operating region of each transistor which are presnted in Table 5.8. From Table 5.8, we see that all transistors are biased in saturation. The operating points look fine. We can now proceed with the simulation of the open-loop large-signal transfer characteristic.

Table 5.2: PSP operating point information extracted from ngspice .op file for each transistor.

Transistor	I_D $[nA]$	V_{GS} $[V]$	V_{DS} $[V]$	V_{SB} $[V]$	$V_{GS} - V_T$ $[mV]$	V_{Dsat} $[mV]$
M1a	249.167	0.141	0.160	0.00	-50	110
M1b	249.162	0.141	0.160	0.00	-50	110
M2a	249.162	0.581	0.581	-0.00	241	227
M2b	249.162	0.581	0.581	-0.00	241	227
M3a	499.992	0.487	0.487	0.00	312	271
M3b	498.329	0.487	0.459	0.00	312	271

Table 5.3: PSP small-signal operating point information extracted from ngspice .op file for each transistor.

Transistor	G_m $[\mu A/V]$	G_{mb} $[\mu A/V]$	G_{ds} $[nA/V]$
M1a	7.348	0.980	223.009
M1b	7.348	0.980	223.008
M2a	1.932	0.359	5.185
M2b	1.932	0.359	5.185
M3a	3.263	0.448	58.544
M3b	3.253	0.446	61.064

Table 5.4: PSP noise operating point information extracted from ngspice .op file for each transistor.

Transistor	$S_{ID,th}$ $[A^2/Hz]$	$S_{ID,fl}$ at 1Hz $[A^2/Hz]$
M1a	7.467e-26	4.179e-22
M1b	7.467e-26	4.179e-22
M2a	4.656e-26	2.128e-21
M2b	4.656e-26	2.128e-21
M3a	4.106e-26	4.120e-21
M3b	4.093e-26	4.101e-21

Table 5.5: sEKV parameters calculated from the values extracted from the simulation.

Transistor	W_{eff} $[\mu m]$	L_{eff} $[\mu m]$	W_{eff}/L_{eff}	I_{spec} $[\mu A]$	IC
M1a	9.620	2.661	3.615	2.560	0.097
M1b	9.620	2.661	3.615	2.560	0.097
M2a	0.320	4.396	0.073	0.018	13.993
M2b	0.320	4.396	0.073	0.018	13.993
M3a	0.170	4.191	0.041	0.029	17.403
M3b	0.170	4.191	0.041	0.029	17.345

Table 5.6: sEKV small-signal parameters calculated from the values extracted from the simulation.

Transistor	G_{spec} $[\mu A/V]$	n	G_m $[\mu A/V]$	G_{ms} $[\mu A/V]$	G_{ds} $[nA/V]$
M1a	98.995	1.133	7.348	8.328	223.009
M1b	98.995	1.133	7.348	8.328	223.008
M2a	0.688	1.186	1.932	2.290	5.185
M2b	0.688	1.186	1.932	2.290	5.185
M3a	1.111	1.137	3.263	3.711	58.544
M3b	1.111	1.137	3.253	3.700	61.064

Table 5.7: sEKV noise parameters calculated from the values extracted from the simulation.

Transistor	$\sqrt{S_{nin,th}}$ $[nV/\sqrt{Hz}]$	$R_{nin,th}$ $[k\Omega]$	γ_n $[-]$	$\sqrt{S_{nin,fl}}$ $[nV/\sqrt{Hz}]$
M1a	37.190	83.437	0.613	2782.233
M1b	37.190	83.439	0.613	2782.259
M2a	111.696	752.655	1.454	23876.535
M2b	111.696	752.654	1.454	23876.531
M3a	62.097	232.625	0.759	19671.380
M3b	62.181	233.259	0.759	19684.838

Table 5.8: Bias voltages and operating regions of each transistor.

Trans.	Type	Funct.	V_G $[V]$	V_S $[V]$	V_D $[V]$	V_{DS} $[mV]$	V_{DSsat} $[mV]$	Reg.	Sat.
M1a	n	DP	0.141	0.000	0.160	160	110	WI	sat
M1b	n	DP	0.141	0.000	0.160	160	110	WI	sat
M2a	p	CM	0.581	0.000	0.581	581	227	SI	sat
M2b	p	CM	0.581	0.000	0.581	581	227	SI	sat
M3a	n	CM	0.487	0.000	0.487	487	271	SI	sat
M3b	n	CM	0.487	0.000	0.459	459	271	SI	sat

5.2 Large-signal differential transfer characteristic

We now simulate the large-signal DC input-output transfer characteristic. The simulation result is presented in Figure 5.1.

We can now zoom into the high gain region and estimate the offset voltage and the output swing. The simulation results are presented in Figure 5.2.

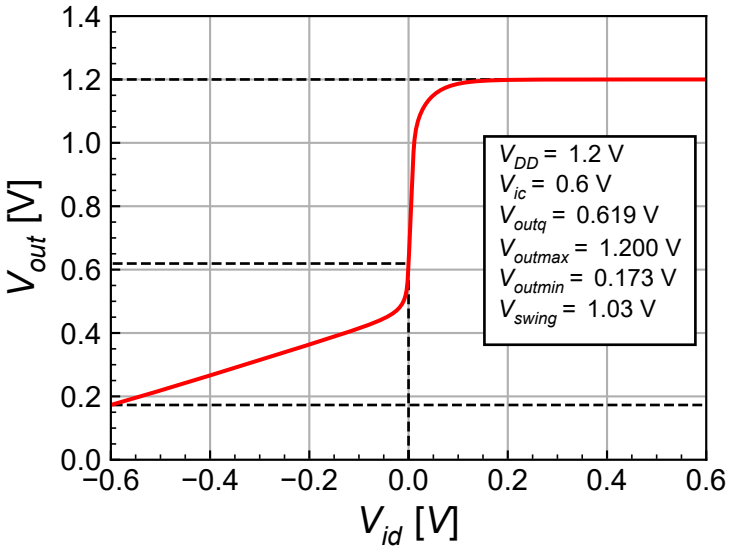

Figure 5.1: Simulated large-signal input-output characteristic.

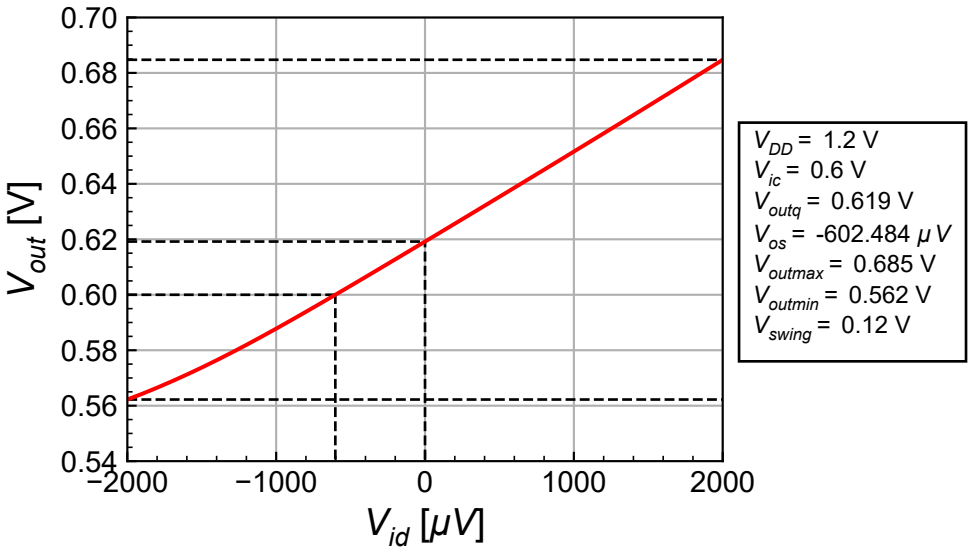

Figure 5.2: Zoom of the simulated large-signal input-output characteristic in the gain region.

We see that the required offset voltage to bring the output voltage to $V_{ic} = 600\ mV$ is equal to $V_{os} =$ -602 μV, which is rather large. On the other hand, we don't need to introduce this offset voltage because the quiescent output voltage $V_{outq} = 619\ mV$ is in the high gain region (the OTA does not saturate).

5.3 Open-loop gain

After having checked the operating point information and making sure that the OTA output is not saturated and in the high gain region, we can now perform the AC simulation. The simulation results are compared to the theoretical estimations in Figure 5.3.

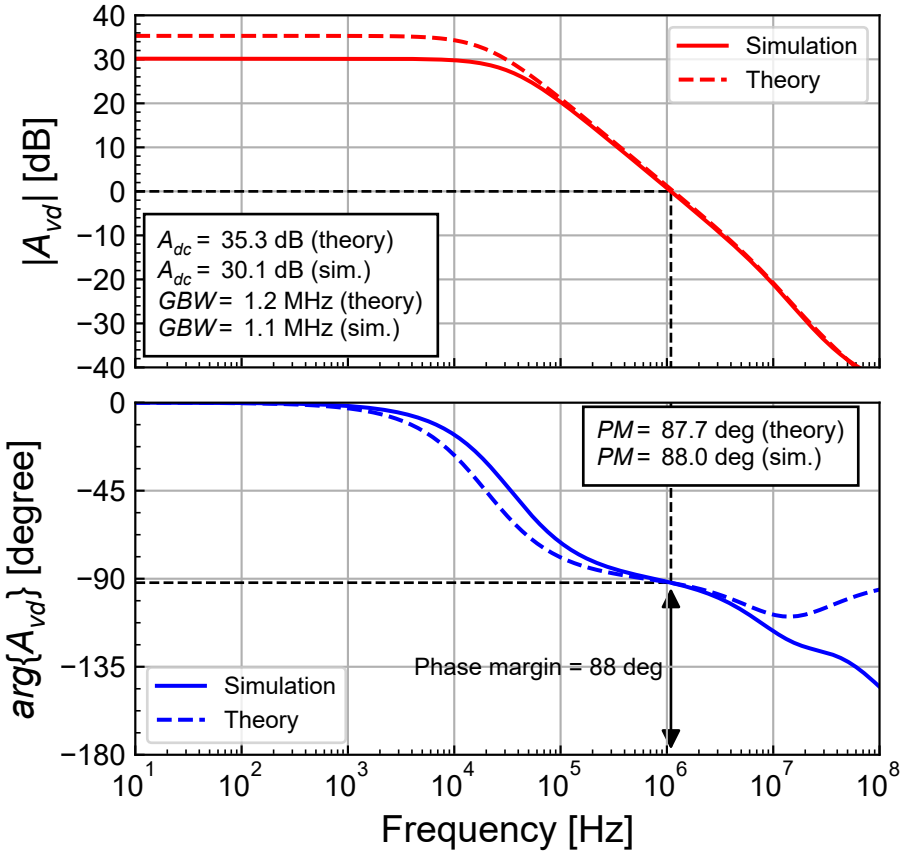

Figure 5.3: Simulated gain response compared to theoretical estimation.

We see a good match between the small-signal simulations and the theoretical results except for the simulated DC gain which is lower than the estimation. We also see some discrepancy at higher frequency where additional poles due to parasitic capacitances that have not been accounted for introduce additional phase shift. We now will peform the noise simulations.

5.4 Input-referred noise

We can compare the theoretical input-referred noise to that obtained from simulations. The simulation results are presented in Figure 5.4.

The contributions of M_{1a}-M_{1b} and M_{2a}-M_{2b} to the input-referred white noise PSD are detailed in Figure 5.5 and compared to the theoretical white noise. We can observe that the white noise is dominated by the differential pair M_{1a}-M_{1b} while the contribution of M_{2a}-M_{2b} is 2 dB lower. The

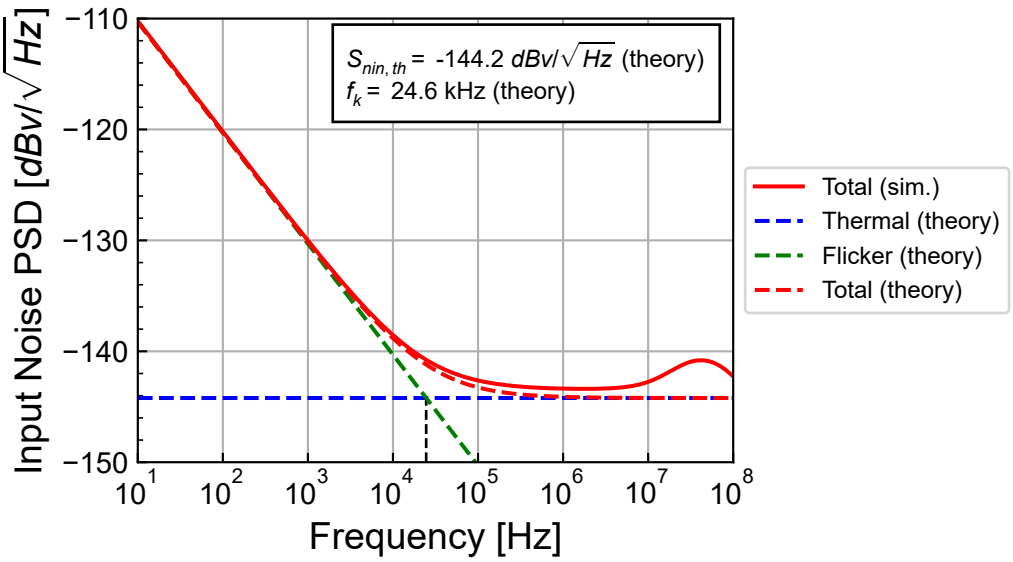

Figure 5.4: Simulated input-referred noise PSD compared to theoretical estimation.

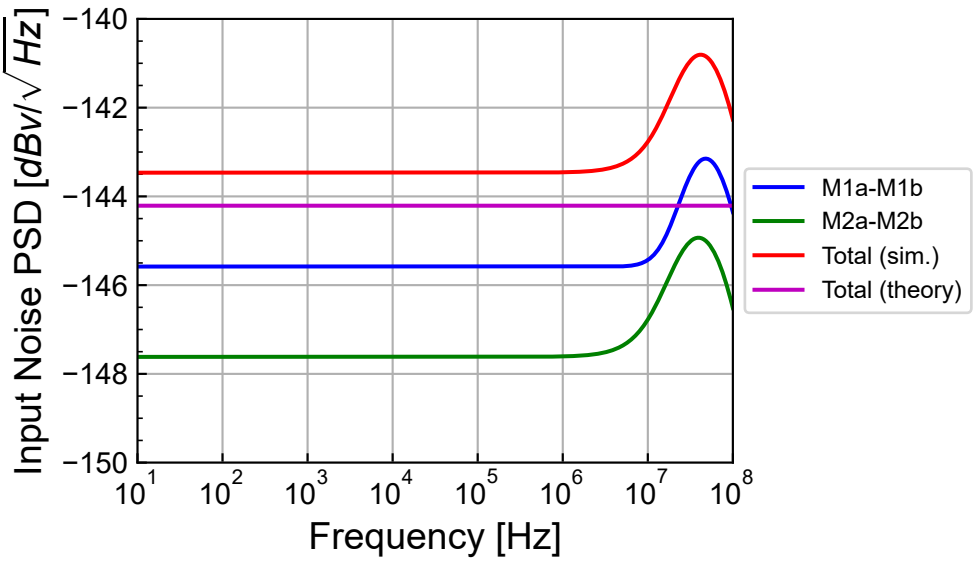

Figure 5.5: Breakdown of the contributions to the simulated input-referred white noise PSD.

total simulated white noise is slightly higher (about 1.25 dB) than the theoretical estimation, which is acceptable. This results in an OTA thermal noise excess factor $\gamma_{n,ota} = 1.996$ that is slightly larger than the predicted value $\gamma_{n,ota} = 1.661$.

Figure 5.6 presents the breakdown of the contributions of M_{1a}-M_{1b} and M_{2a}-M_{2b} to the input-referred flicker noise. Contrary to the white noise, the flicker noise is largely dominated by the contribution of the current mirror M_{2a}-M_{2b}. This is consistent with what was already observed in the OTA characteristic section. It is due to the fact that $W_1 L_1$ is 17 times larger than $W_2 L_2$ and that ρ_p is 3.8 times larger than ρ_n.

The breakdown of the contributions of M_{1a}-M_{1b} and M_{2a}-M_{2b} to the total input-referred noise is presented in Figure 5.6. We can observe that the simulation is close to the theoretical estimation.

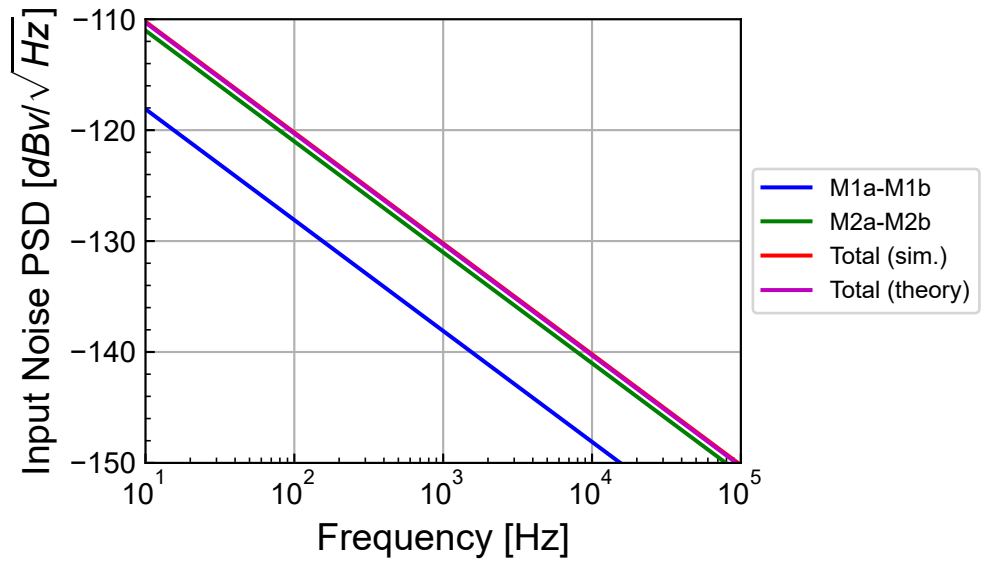

Figure 5.6: Breakdown of the contributions to the simulated input-referred flicker noise PSD.

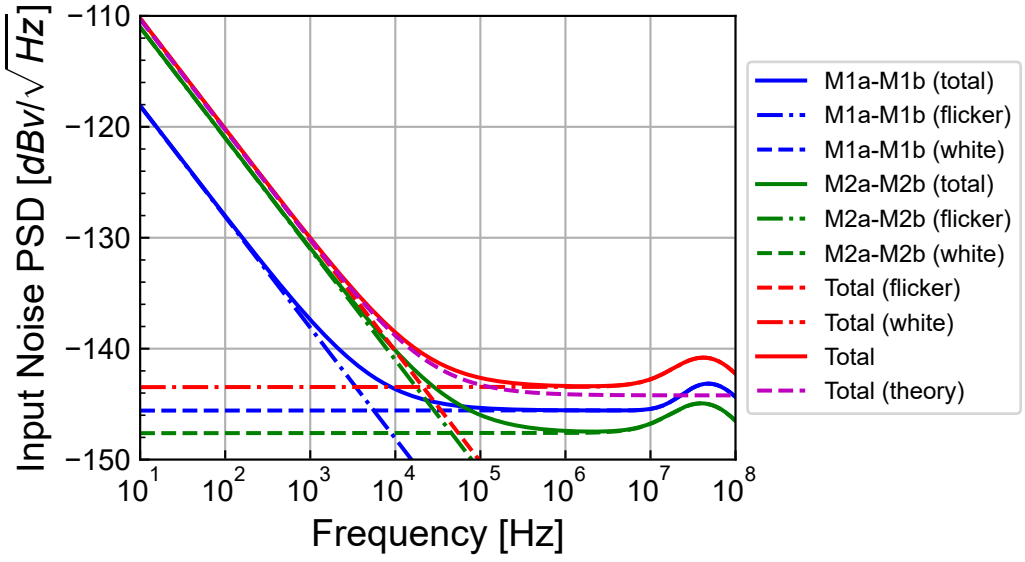

Figure 5.7: Breakdown of the contributions to the simulated input-referred noise PSD.

5.5 Input common-mode voltage range

We can check the input common-mode voltage range by connecting the OTA as a voltage follower and sweeping the positive input. As shown in Figure 5.8, the output follows the input voltage up to $0.8\,V$. So the input common-mode voltage range is about $0.8\,V$.

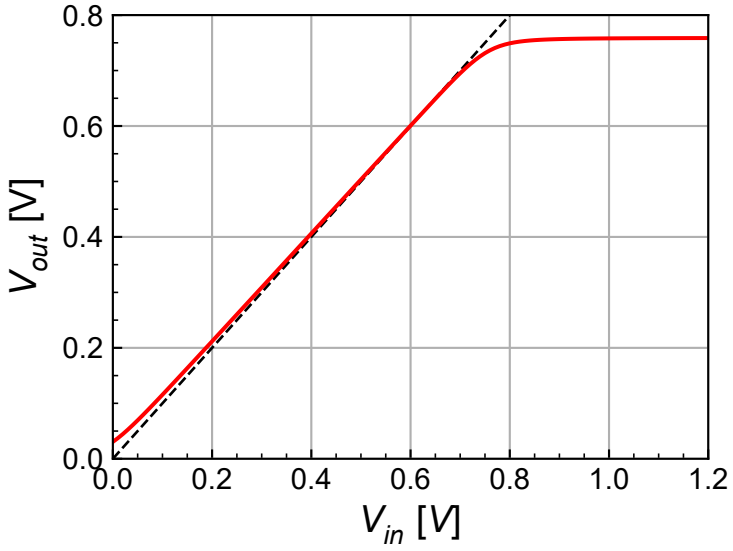

Figure 5.8: Simulated input common-mode voltage range.

5.6 Step-response

In this section we will check the step response of the OTA operating as a voltage follower (output connected to the negative input) with the same load capacitance $C_L = 1\ pF$. According to the input common-mode voltage range established above, we will set the input common-mode voltage to $V_{ic} = 0.3\ V$ to leave enough room for the large step.

5.6.1 Small-step

We start by imposing a small step $\Delta V_{in} = 10\ mV$ on top of a common mode voltage $V_{ic} = 0.3\ V$. The simulation results are shown in Figure 5.9 where $\Delta V_{in}(t) \triangleq V_{in+}(t) - V_{ic}$ and $\Delta V_{out}(t) \triangleq V_{out}(t) - V_{outq}$ with $V_{outq} \cong V_{ic}$ is the quiescent output voltage. ΔV_{in} and ΔV_{out} are compared to the response of a single pole circuit having a cut-off frequency equal to the GBW. We can observe that the output voltage does not settler to the correct value but slightly below. This is due to the very limited DC gain. The output voltage will settle to

$$\lim_{t\to\infty} \Delta V_{out}(t) \cong \Delta V_{in} \cdot \left(1 - \frac{1}{A_{dc}}\right) \tag{5.3}$$

which is respresented in Figure 5.10 by an horizontal dashed line. Differences can also be observed at the beginning which are due to the higher order poles.

5.6.2 Large step

We now impose a larger step $\Delta V_{in} = 300\ mV$ on top of a common mode voltage $V_{ic} = 300\ mV$. The simulation results are shown in Figure 5.10 where $\Delta V_{in}(t) \triangleq V_{in+}(t) - V_{ic}$ and $\Delta V_{out}(t) \triangleq V_{out}(t) - V_{outq}$

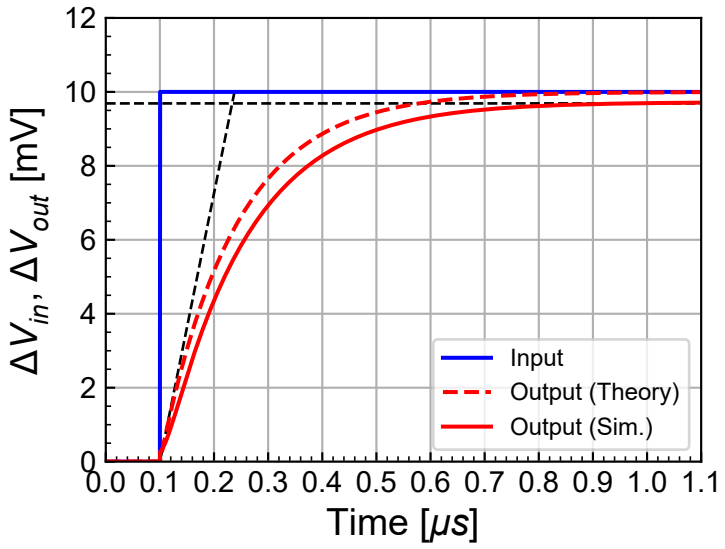

Figure 5.9: Step response of the OTA as a voltage follower for a small input step.

with $V_{outq} \cong V_{ic}$ is the quiescent output voltage. ΔV_{in} and ΔV_{out} are compared to the response of a single pole circuit having a cut-off frequency equal to the GBW. We now observe the effect of slew-rate which increases the settling time.

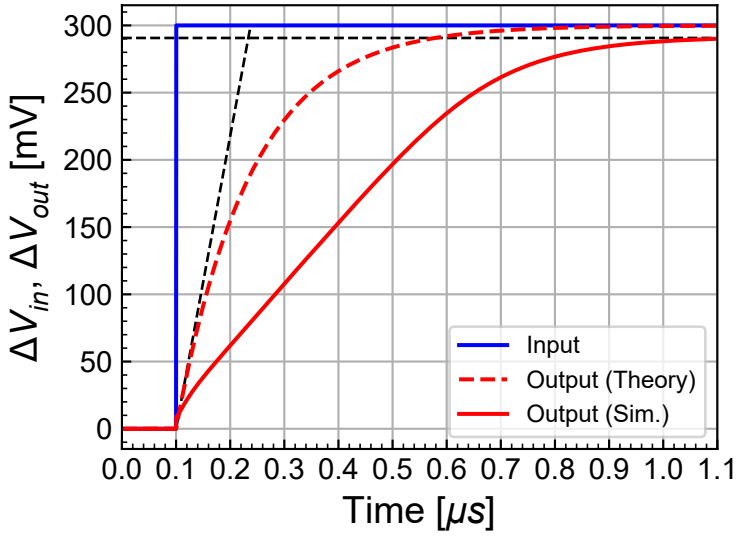

Figure 5.10: Step response of the OTA as a voltage follower for a large input step highlighting the slew-rate effect.

5.7 Current and power consumption

The total current consumption without accounting for the bias string M_{3a} is simply $I_{tot} = 2\,I_b = 500$ nA, resulting in power consumption $P = V_{DD} \cdot I_{tot} = 0.6$ μW.

6 Conclusion

This notebook presented the analysis, design and verification of the simple 5 transistors OTA for the IHP 130nm SG13G2 open source PDK. The detailed analysis provided all the equations that were then used in the design phase to reach the target specifications. The design was then performed using the inversion coefficient approach with the sEKV transistor model. The theoretical performance resulting from the design were then evaluated. The design was then verified by simulation using ngspice with the PSP compact model and the parameters provided by the IHP 130nm SG13G2 open source PDK. After carefully checking the operating point, the large-signal transfer characteristic was simulated. Then the small-signal open-loop transfer fucntion was simulated. The target gain-bandwidth GBW is achieved. The DC gain is also achieved despite the simulated DC gain is lower than the theoretical estimation. The input-referred noise was then simulated and compared to the theoretical estimation. It was shown that the flicker noise is dominated by the pMOS current mirror, while the white noise is dominated by the differential pair. The input common-mode voltage range was then simulated with the OTA connected as a voltage follower.The input voltage is limited to $0.8\,V$. Finally, the small-signal step response was simulated highlighting the effect of the low DC gain. The step-response with a large input step highlighted the effect of slew-rate.

This design has highlighted an important drawback of this technology, namely the high output conductance of nMOS transistors and even for long-channel.

Despite the compact model that was used for the simulation is not the EKV compact model but the PSP model, the simulation results are reasonably close to the the theoretical estimation made with the sEKV model. Of course this required to extract the sEKV parameters for the IPHP SG13G2 technology.

[1] G.D.J. Smit, A.J. Scholten, D.B.M. Klaassen, O. Rozeau, S. Martinie, T. Poiroux and J.C. Barbé, "PSP 103.6 - The PSP model is a joint development of CEA-Leti and NXP Semiconductors." https://www.cea.fr/cea-tech/leti/pspsupport/Documents/psp103p6_summary.pdf, 2017.

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