Release Notes
88E6208 and 88E6218 Revision B0 SOHO Gateway SOC

1. Overview

This document is an update/supplement to the *Link Street™ 88E6208/88E6218 Datasheet SOHO Gateway SOC with ARM9E™ CPU, 10/100 Switch and PHYs Datasheet:*

- *Part 1 of 3: Overview, Pinout, & Electrical Specifications* (Doc. No. MV-S101300-01, Rev. -)
- *Part 2 of 3: CPU & Peripherals* (Doc. No. MV-S101300-02, Rev. -)
- *Part 3 of 3: Switch Core, PHYs, & Related Registers* (Doc. No. MV-S101300-03, Rev. -).

It contains the following sections:

Revision Identification: This section describes how to identify the revision of the device covered in this document.

Revision Updates: This section summarizes the bugs closed and new features added, when compared to the previous revision (if applicable).

Errata: This section summarizes the known errata for the 88E6208 and 88E6218 Rev B0 devices.

Customer Information: This information section discusses certain features and modes of the part that are very important to know about. They might be additional features that are not common in similar parts, or modes of operation that are different than what the customer might be accustomed to. It is critical that the customers read this carefully.

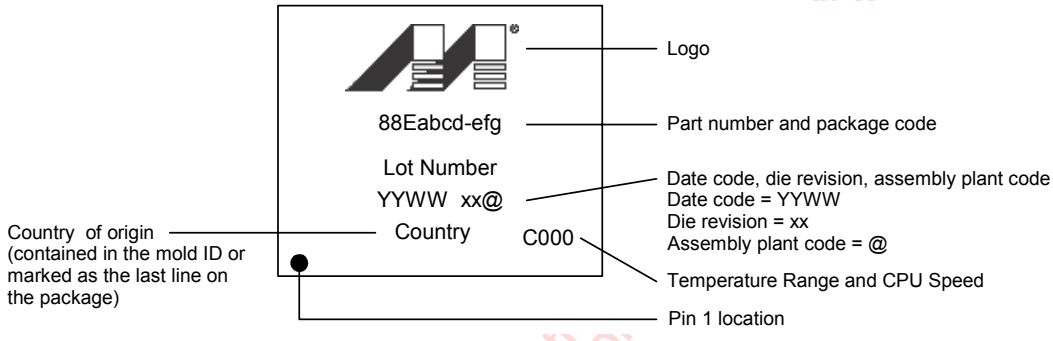
Datasheet Revisions: This section contains the latest changes made to the datasheet or changes that will be made in the next revision of the datasheet. Refer to the relevant sections in the datasheet, as well.

2. Revision Identification

The 88E6208 Rev B0 device can be identified in software by reading a value of 0xF911 from the Switch Identification Register, at offset 0x03, bits 15:0. The 88E6218 Rev B0 device can be identified by reading a value of 0xF931 from the same bits.

The package identifies the revision of the device in the 'xx' fields shown in Figure 1.

Figure 1: Generic Package Markings



The 88E6208/88E6218 Rev B0 devices are speed code marked.

3. Revision Updates

Errata fixed: All errata issues from 88E6208 and 88E6218 Rev. A0 devices were fixed in Rev. B0 of these devices.

New Features: Rev. B0 of the 88E6208 and 88E6218 devices adds a new, internal Watchdog circuitry and provides a watchdog expired indication as a reset option on pin GPIO[12]. This feature was not available in 88E6208 and 88E6218 Rev. A0 devices.

4. Errata

None

5. Customer Information

5.1 CPU Clock Speed

CPU speed is set by resistors on CLKSEL[1]/M_A[22] and CLKSEL[0]/M_A[23] (on pins 59 and 58, for the 88E6208/88E6218 devices, respectively) and M_A[10] (on pin 90, for both the 88E6208 and 88E6218 devices). The 88E6208 and 88E6218 Rev. B0 devices contain internal pull-up resistors on both M_A[10] and CLKSEL[0]/M_A[23], and an internal pull-down resistor on CLKSEL[1]/M_A[22] — these three pins select the 133 MHz speed (see Table 1).

Table 1: 88E6208 and 88E6218 Revision B0 CPU Clock Options

For the 88E6208 Device: **M_A[10], CLKSEL[1:0]** *For the 88E6218 Device:* **M_A[10], M_A[22:23]**	**Core CPU Frequency**
000	Reserved
001	Reserved
010	83 MHz
011	100 MHz
100	125 MHz
101	133 MHz (default)
110	150 MHz
111	Reserved

5.2 Designs Using Warm Resets and an 8-bit Boot Device

Full Page SDRAM Burst mode cannot be used if warm resets are needed in a design, and an 8-bit boot device is used.

A warm reset is one that activates the 88E6208 or 88E6218 Rev B0 device's RESETn pin without a power cycle (like a hardware reset button or Watchdog circuit). If Full Page SDRAM Burst mode is used and a warm reset occurs during an SDRAM Page Read, the SDRAM Page remains open after the reset and causes contention with the boot device read. This contention will only occur if an 8-bit boot device is used in the design.

This contention will not occur for an SDRAM burst size of 8 bytes, because the SDRAM Page Read will finish within 10 clock cycles. However, since using an SDRAM burst size of 8 bytes impacts on performance, it is not recommended if high performance (fast access) is required.

5.3 Board Design Guidelines

Refer to the application note AN-133 *Board Design and Layout Guidelines for 88E6208 and 88E6218 Revision B0 Devices* (Document number MV-S300456).

6. Datasheet Revision Information

1. Rev B0 of the 88E6208 and 88E6218 devices add a new Watchdog reset option to GPIO[12]. (See Table 118: GPIO Select [15:8] Register and Table 152: Watchdog Enable Register in the *88E6208/88E6218 Datasheet Part 2*, Rev. -, Document number MV-S101300-02). This feature was not available in 88E6208 and 88E6218 Rev A0 devices.
2. M_A[21] has an internal pull down in Rev B0, instead of an the internal pull up that existed in Rev A0 (see Table 13 Switch/CPU Interface Configuration Pins in the *88E6208/88E6218 Datasheet Part 1*, Rev. -, Document number MV- S101300-01).
3. For 88E6218 device, the IDMA channels Direction (Src and Des) and the Burst Limit:
   IDMA operation is guaranteed for Increment mode only, and for a Burst Limit that is greater or equals to 4 bytes. Decrement mode and Burst Limits of under 4 bytes are not supported. An explanation of this can be found in Part 2 of the 88E6208/88E62188 Datasheet, in Section A.5.3, which describes how the Channel 0 /1 control registers BurstLimit bits [8:6] can be configured as 4 bytes or more, and the DesDir and SrcDir, bits [5:4] and bits [3:2], respectively, can be configured to increment or hold the address, but not to decrement it.
4. The recommended operating conditions for using 2.5V PNP appears in Part 1 of the *88E6208/88E6218 Datasheet*, Rev. - (Document number MV-S101300-01), in Table 18 in the row for symbol $V_{DD(2.5V)}$. It is recommended to operate as follows: Minimum: 2.375V, Typical: 2.5V, and Maximum: 2.75V. (As indicated here, the Maximum value can be higher than what currently appears in the datasheet).

Note

Items 1, 2, and 3 listed above already appear in the latest release of Parts 1 and 2 of the *88E6208/88E6218 Datasheet*, Rev. - (Document numbers MV-S101300-01 and MV-S101300-02, respectively).

7. Revision History

Table 2: Revision History

Document Type	Rev. #	Date
Preliminary	Rev. A	April 6, 2003
First release of this document		
Preliminary	Rev. B	July 8, 2003
1. Changed the "Revision Identification" to indicate that the Rev B0 devices can be identified by reading a value of 0xF911 for the 88E6208 device or 0xF931 for the 88E6218 device.		
Preliminary	Rev. C	December 16, 2003
1. Revised Section 5.1 CPU Clock Speed and Table 1, "88E6208 and 88E6218 Revision B0 CPU Clock Options," on page 2. 2. Revised Section 5.2 Designs Using Warm Resets and an 8-bit Boot Device.		

Disclaimer

This document provides preliminary information about the products described, and such information should not be used for purpose of final design. Visit the Marvell® web site at www.marvell.com for the latest information on Marvell products.

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