Release Notes
88E6208 and 88E6218 Revision B1
SOHO Gateway SOC

1. Overview

This document is an update/supplement to the datasheet. It contains the following sections:

Revision Identification: This section describes how to identify the revision of the device covered in this document.

Revision Updates: This section summarizes the bugs closed and new features added, when compared to the previous revision (if applicable).

Errata: This section summarizes the known errata for the 88E6208 and 88E6218 Rev B1 devices.

Customer Information: This information section discusses certain features and modes of the part that are very important to know about. They might be additional features that are not common in similar parts, or modes of operation that are different than what the customer might be accustomed to. It is critical that the customers read this carefully.

Datasheet Revision Information: This section contains the latest changes made to the datasheet or changes that will be made in the next revision of the datasheet. Refer to the relevant sections in the datasheet, as well.

Related Documents:

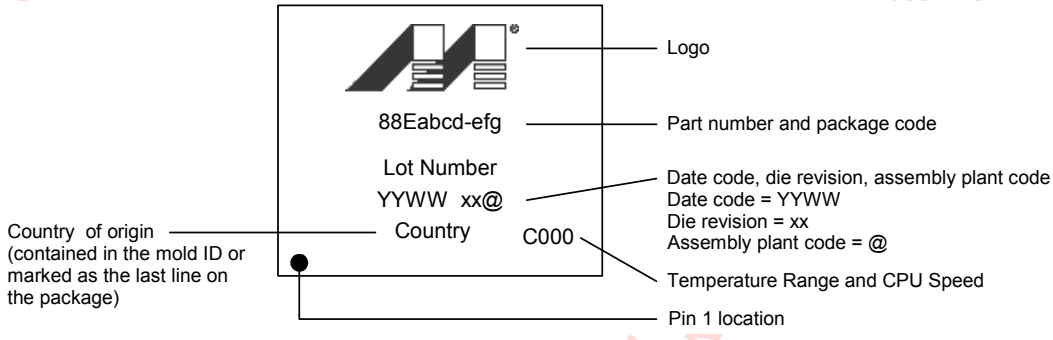
- *Link Street™ 88E6208/88E6218 Datasheet SOHO Gateway SOC with ARM9E™ CPU, 10/100 Switch and PHYs* Parts 1, 2, and 3 (Document numbers MV-S101300-01, MV-S101300-02, and MV-S101300-03, respectively)
- AN-133 *Board Design and Layout Guidelines for 88E6208 and 88E6218 Revision B0 and B1 Devices*, Rev. B (Document number MV-S300456-00)

2. Revision Identification

The 88E6208 Rev. B1 device can be identified in software by reading a value of 0xF912 from the Switch Identification Register, at offset 0x03, bits [15:0]. The 88E6218 Rev. B1 device can be identified by reading a value of 0xF932 from the same bits.

The package identifies the revision of the device in the 'xx' fields shown in Figure 1.

Figure 1: Generic Package Markings



The 88E6208 and 88E6218 Rev. B1 devices are speed code marked.

3. Revision Updates

3.1 Errata Fixed

The following errata were fixed in 88E6208 and 88E6218 Rev. B1 devices:

- Support 8-bit in full page mode: To enable this feature, pull down M_A[7].
- To ensure stability at the output of the RESET generator circuit, pull down pin M_A[8].

Note

Pins M_A[7] and M_A[8] are both internally pulled up to be compatible with 88E6208 and 88E6218 Rev. B0 devices.

3.2 New Features

Rev. B1 of the 88E6208 and 88E6218 devices have a modified Watchdog mechanism that does not allow disabling by the software once the Watchdog is enabled. The Watchdog activity is disabled only by cold reset. (In Rev. B0, disabling the Watchdog using the software was allowed.)

4. Errata

None

5. Customer Information

5.1 CPU Clock Speed

CPU speed is set by resistors on CLKSEL[1]/M_A[22] and CLKSEL[0]/M_A[23] (on pins 59 and 58, for the 88E6208/88E6218 devices, respectively) and M_A[10] (on pin 90, for both the 88E6208 and 88E6218 devices). The 88E6208 and 88E6218 Rev. B1 devices contain internal pull-up resistors on both M_A[10] and CLKSEL[0]/M_A[23], and an internal pull-down resistor on CLKSEL[1]/M_A[22] — these three pins select the 133 MHz speed (see Table 1).

Table 1: 88E6208 and 88E6218 Revision B0 CPU Clock Options

For the 88E6208 Device: M_A[10], CLKSEL[1:0] *For the 88E6218 Device:* M_A[10], M_A[22:23]	Core CPU Frequency
000	Reserved
001	Reserved
010	83 MHz
011	100 MHz
100	125 MHz
101	133 MHz (default)
110	150 MHz
111	Reserved

5.2 Board Design Guidelines

Refer to the application note AN-133 *Board Design and Layout Guidelines for 88E6208 and 88E6218 Revision B0 and B1 Devices*, Rev. B (Document number MV-S300456-00).

5.3 Augmented VCT operation

VCT operation has been augmented to refine the accuracy of cable diagnostic results with cables that are equal to or less than 15 meters in length.

6. Datasheet Revision Information

1. For 88E6208 and 88E6218 Rev. B1 devices, the IDMA channels Direction (Src and Des) and the Burst Limit: IDMA operation is guaranteed for Increment mode only, and for a Burst Limit that is greater or equals to 4 bytes. Decrement mode and Burst Limits of under 4 bytes are not supported. An explanation of this can be found in Part 2 of the *88E6208/88E6218 Datasheet*, Rev. - (Document number MV-S101300-02), in Section A.5.3, which describes how the Channel 0 /1 control registers BurstLimit bits [8:6] can be configured as 4 bytes or more, and the DesDir and SrcDir, bits [5:4] and bits [3:2], respectively, can be configured to increment or hold the address, but not to decrement it.
2. The recommended operating conditions for using 2.5V PNP appears in Part 1 of the *88E6208/88E6218 Datasheet*, Rev. - (Document number MV-S101300-01), in Table 18 in the row for symbol $V_{DD(2.5V)}$. It is recommended to operate as follows: Minimum: 2.375V, Typical: 2.5V, and Maximum: 2.75V. (As indicated here, the Maximum value can be higher than what currently appears in the datasheet).

Note

Item 1 listed above already appears in the latest release of Part 2 of the *88E6208/88E6218 Datasheet*, Rev. - (Document numbers MV-S101300-02).

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