Release Notes - 88E6218 Rev A0

Overview

This document is an update/supplement to the datasheet. It contains the following sections.

Revision Identification: This section describes how to identify the revision of the device covered in this document.

Revision Updates: This section summarizes the bugs closed and new features added, when compared to the previous revision (if applicable).

Errata: This section summarizes the known errata for the 88E6218 Rev A0.

Customer Information: This information section discusses certain features and modes of the part that are very important to know about. They might be additional features that are not common in similar parts, or modes of operation that are different than what the customer might be accustomed to. It is critical that the customers read this carefully.

Datasheet Revisions: This section contains the latest changes made to the datasheet or changes that will be made in the next revision of the datasheet. Please refer to the relevant sections in the datasheet as well.

1. Revision Identification

The 88E6218 Rev A0 can be identified in software by reading a value of 0xF930 from the Switch Identification Register at 3.15:0.

The package identifies the revision of the device in the 'xx' fields shown in Figure 1.

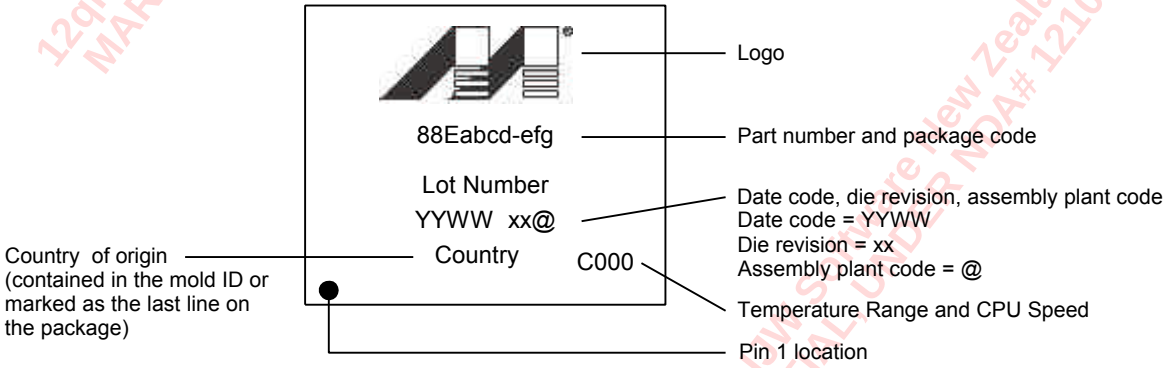


Figure 1: Generic Package Markings

The 88E6218 Rev A0 devices are not speed code marked.

2. Revision Updates

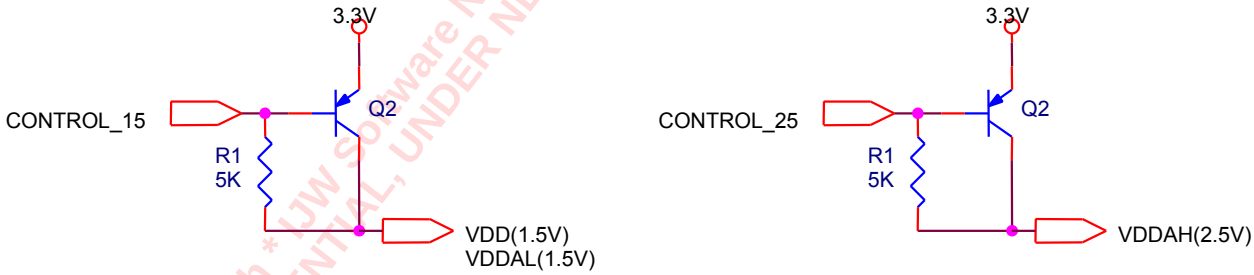
Errata fixed: This is the first revision of the device.

New features: This is the first revision of the device.

3. Errata

3.1 The 1.5V VDD regulator will not always start up.

Work around: Use external 5K resistors and connect between the base and collector on both of the PnPs to jump start the internal regulators. Another work around is to use external regulators and by-pass the internal regulators for generating 1.5V and 2.5V.



Plan: Will be fixed in Rev B0.

3.2 Purged Multicast entries cannot be re-used in the ATU's address database without a Flush.

This errata is only applicable to systems that will Load and Purge multicast addresses in the ATU address database. Systems that run spanning tree will not have a problem since they will Load the BPDU multicast address into the ATU but will not Purge it. The only systems that will encounter this errata are those that perform multicast address filtering.

Work around: When the ATU Full Interrupt occurs, perform an ATU Flush operation and reload the locked addresses.

Plan: Will be fixed in Rev B0.

3.3 Bits 11:8 of PortControl Register for ports 5 & 6 do not report the correct information.

Because of this, it is not possible to see if the 200BASE mode is enabled.

Work around: None.

Plan: Will be fixed in Rev B0.

3.4 An Access to an unmapped address might cause the system to hang.

Accesses to unmapped internal addresses in the range of 0x8000c000 - 0x8000dfff (LBU) with bits [7:5] of the address equals 0b110, might cause mapping to undefined registers and eventually might lead the system to hang.

Work around: Do not access these addresses.

Plan: Will be fixed in Rev B0.

4. Customer Information

1. CPU speed is set by resistors on M_A[10], M_A[22] and M_A[23] (on pins 90, 59 & 58). 88E6218 Rev A0 contains internal pull-up resistors on these pins which selects an undefined speed (used for test mode purposes - see Table 1). The next revision of the 88E6218 (Rev B0), the default CPU clock frequency will be changed to 133 MHz. This is done by changing M_A[22] to have an internal pull-down resistor (instead of an intern pull-up resistor - see Table 2).

Note:	M_A[22] will have a pull-down resistor instead of a pull-up resistor in Rev B0. For 133 MHz operation this is a don't care. For other frequency operation the PCB's artwork may need to change.

M_A[10], M_A[22], M_A[23]	Core CPU Frequency
000	Reserved
001	75 MHz (becomes 143 MHz on Rev B0)
010	83 MHz
011	100 MHz
100	125 MHz
101	133 MHz
110	150 MHz[1]
111	Reserved (default)

Table 1: Rev A0 CPU Clock Options

M_A[10], M_A[22], M_A[23]	Core CPU Frequency
000	Reserved
001	143 MHz[1]
010	83 MHz
011	100 MHz
100	125 MHz
101	133 MHz (default)
110	150 MHz[1]
111	Reserved

Table 2: Rev B0 CPU Clock Options

1 = Speeds above 133 MHz are not guaranteed unless the part is marked for 150 MHz speed.

2. Port 5's speed is set by resistors on M_A[20] and M_A[21] (on pins 62 & 61). 88E6218 Rev A0 contains internal pull-up resistors on these pins which selects the UniMAC's speed to be 200BASE mode. The next revision of the 88E6218 (Rev B0), the default UniMAC speed will be changed to 100BASE mode. This is done by changing M_A[21] to have an internal pull-down resistor (instead of an intern pull-up resistor - see Table 2).

Note:	M_A[21] on Rev B0 will have an internal pull-down resistor instead of an internal pull-up resistor as in Rev A0. For 100BASE UniMAC operation this is a don't care. For 200BASE UniMAC operation the PCB's artwork may need to change.

3. Full Page SDRAM burst mode cannot be used if warm Resets are needed in a design. Use an SDRAM burst size of 8 instead. A warm Reset is one that activates the 88E6218 Rev A0's RESETn pin without a power cycle (like a hardware reset button or Watchdog circuit). If Full Page SDRAM burst mode is used and a Reset occurs during an SDRAM Page Read, the SDRAM Page remains open after the Reset and causes a conflct with the Flash read cycles. This conflict will not occur for an SDRAM burst size of 8 because the SDRAM Page Read will finish within 10 clocks.
4. Packets with invalid /T/R are being forwarded instead of being filtered (T and R are MLT-3 symbols used by the PHY to decode the end of frame). If an error occurred in the data portion of the frame the frame's CRC would be incorrect and the frame will be discarded by the switch for this reason. If the error occurred only outside the frame (i.e., in the/ T/R portion) then the data portion of the frame is valid if its CRC is good. Also, there is no IEEE spec calling for dropping such packets.

5. Datasheet Revision Information

1. TRSTn (pin 44) was previously documented that it could be left floating (high) if not being used. This is not the case and will be corrected in the next revision of the datasheet. TRSTn must be low if not being used. An external 10K Ohm resistor to VSS can be used or TRSTn can be tied to VSS.
2. Rev B0 of the 88E6218 adds a new Watch Dog reset option to GPIO[12]. This feature is not available in 88E6218 Rev A0.