GATEWAYS

Link Street™ 88E6208/88E6218 Datasheet

SOHO Gateway SOC with
ARM9E™ CPU, 10/100 Switch and PHYs

Part 3 of 3: 7-Port QoS Switch and PHYs

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Preface

About this Document

This datasheet volume, 88E6208/88E6218 Datasheet, *Part 3, 7-Port QoS Switch and PHYs,* describes the switch core, PHYs and their associated register tables. This volume is part of a three-volume set that describes the hardware features, the CPU and peripheral interfaces and the switch core and PHYs of the 88E6208/88E6218 device.

The details of the other two datasheets in this set are:

- 88E6208/88E6218 Datasheet, Part 1: *Overview, Pinout, and Electrical Specifications*, Document Number MV-S101300-01, provides a features list, overview, pin description, pin map, and electrical specifications for this part.
- 88E6208/88E6218 Datasheet, Part 2*: CPU & Peripherals*, Document Number MV-S101300-02, provides a description of the CPU and each of the peripheral interfaces of the 88E6208/88E6218 device

Document Conventions

Table 1: Document Conventions

Document Conventions The following name and usage conventions are used in this document:	
Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_Addr[12:0]
Active Low Signals n	A lower-case n symbol at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated in courier blue font. Example: `RegInit` OR Example: Global_Control<DevEn>, Where Global Control represents the register name, and <DevEn> represents the register field name. Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use.

Overview

Note

This document applies to both the Marvell Link Street™ 88E6208 and 88E6218 devices. Any reference to the 88E6218 also applies to the 88E6208 devices unless specified otherwise. A summary of the differences between the two devices appears in Table 2 on page 12.

The 88E6208 and 88E6218 devices offer single-chip integrated SOHO gateway router solutions to reach full-wire-speed 100 Mbps WAN/LAN routing . Marvell is the first to implement this highly-integrated gateway router design on a two-layer PCB reference design which passes FCC Class B EMI conformance and which achieves the most cost-effective form factor ready for manufacturing. The Marvell Link Street™ 88E6208/88E6218 SOHO gateway router devices enable OEM customers to expand their product offerings, addressing a worldwide home networking and residential gateway market.

The Marvell Link Street 88E6218 gateway router provides single chip integration, integrating the Company's Link Street 7-port Fast Ethernet (FE) switch to enhance network reliability, an ARM946E-S™ CPU to execute the router software and configure the switch, and a software architecture for enhanced routing performance. In the 88E6208 gateway router, the Fast Ethernet (FE) switch has six ports. The Marvell Link Street devices also leverage the Company's newest generation 0.15-micron PHY transceiver technology, which interfaces the chip to external cables. The Marvell PHYs incorporate Virtual Cable Tester™ (VCT) technology, which provides built-in cable diagnostic testing capability, quickly resolving cable problems and decreasing downtime.

The highly integrated Marvell Link Street gateway routers achieve the highest level of performance available—100 Mbps full-wire-speed WAN/LAN routing. The devices utilize the Company's UniMAC™ architecture to accelerate routing performance with pre-packet processing, speeding IP routing and increasing CPU performance. UniMAC also enhances security by providing port isolation for WAN, LAN and De-Militarized Zone (DMZ) ports. System products integrating the Marvell Link Street 88E6218 device add quality-of-service (QoS) for converged voice/video/data networks, allowing IP services such as IP telephony and video-over-the-Internet.

The Marvell Link Street 88E6208/88E6218 gateway routers provide full-wire-speed routing and the lowest system cost implementation—enabling OEMs fast entry into the rapidly-growing SOHO networking market. In addition, the Link Street gateway routers achieve extremely low power consumption, providing OEMs with a complete gateway router design that runs much cooler and achieves a longer life span, resulting in higher reliability.

Link Street SOHO Gateway Router Features

The Link Street 88E6208/88E6218 SOHO gateway routers include a high-speed ARM946E-S™ processor, the Marvell Link Street FE 6-port/7-port switches, and five Marvell 0.15-micron FE transceivers, providing OEMs with a high-performance, cost-effective, low power solution.

Link Street 88E6208 SOHO Gateway Router

The cost-effective Link Street **88E6208** SOHO gateway router includes the following features:

- Full-wire-speed 100 Mbps WAN/LAN routing
- ARM946E-S™ CPU (with DSP Processor instruction extensions) @ 133 MHz
- High-performance cache memory architecture with 8 KB instruction cache, 8 KB data cache

- 2-layer PCB reference design which passes FCC Class B EMI conformance testing, achieving lower system-cost router design
- 16 bit Memory Controller interface including 3 memory device banks (one boot Flash/ROM and two others)
- Enhanced 6-port FE switch with UniMAC™ IP routing acceleration
- One UART interface for debugging and for backup phone line WAN connection
- Pin-compatible with the 88E6218 device

Link Street 88E6218 SOHO Gateway Router

The Link Street 88E6218 SOHO gateway router offers these additional features:

- Full-wire-speed 100 Mbps WAN/LAN routing, plus a faster CPU providing bandwidth for software VPN services
- ARM946E-S™ CPU (with DSP Processor instruction extensions) at up to 150 MHz
- High-performance cache memory architecture with 8 KB instruction cache, 8 KB data cache, and 8 KB tightly coupled memory
- 32 bit Memory Controller interface including 4 memory device banks (one boot Flash/ROM and three others)
- Quality-of-Service (QoS) enhanced 7-port FE switch including UniMAC IP routing acceleration, for video-over-the-Internet and audio-over-the-Internet delivery
- External MII port, which can run at up to 200 Mbps full-duplex, providing network expansion capability to an additional multi-port switch or wireless LAN

Table 2 on page 12 summarizes the feature differences between the pin compatible 88E6218 and 88E6208 devices

Table 2: Feature Differences Between 88E6218 and 88E6208 Devices

Feature	88E6208	88E6208
CPU		
Maximum CPU Speed	133 MHz	150 MHz
8K Data Tightly-Coupled Memory SRAM	No	Yes
Internal DMA	No	Yes
External Memory Width	16-bits	32-bits
Maximum Flash Size	8 MB	64 MB
External Chip Selects	3 - BootCSn, M_CSn[1:0]	4 - BootCSn, M_CSn[2:0]
M_STATUS pin for Flash Memory	No[1]	Yes
Address Bus pins	M_A[21:0]	M_A[23:0]
UniMAC™ QoS	No	Yes - 4 Queues
UniMAC DA Filter	No	Yes
SWITCH		
# of Switch Ports	6	7
External MII interface	No	Yes
Switch QoS	No	Yes - 4 Queues
Ingress Rate Limiting	No	Yes
Egress Rate Shaping	No	Yes
Max. UniMAC Speed	100 Mbps FD	200 Mbps FD
Embedded Memory	0.5 Mb	1 Mb

1 A GPIO pin can be used instead.

Section 1. Functional Description

This section describes the wire-speed, non-blocking -port 10/100-Mbps Fast Ethernet QoS (Quality-of-Service) switch core that is integrated into the 88E6218 device. The seven ports include PHY, MII/SNI, and internal MII ports, as described below. The wirespeed, non blocking, 10/100 Fast Ethernet switch core is also described. This core is integrated into the 88E6208 device.

1.1 Switch Data Flow

The 88E6208/88E6218 device accepts IEEE 802.3 frames and either discards them or transmits them out of one or more of the switchports. The decision on what to do with each frame is one of the many jobs handled inside the switch. Figure 1 shows the data path inside the switch along with the major functional blocks that process the frame as it travels through the 88E6208/88E6218 device.

Figure 1: 88E6218 Device Switch Data Flow

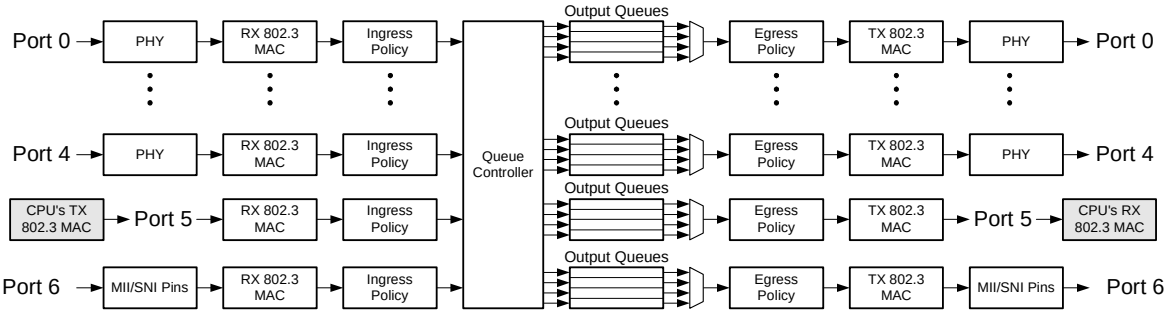
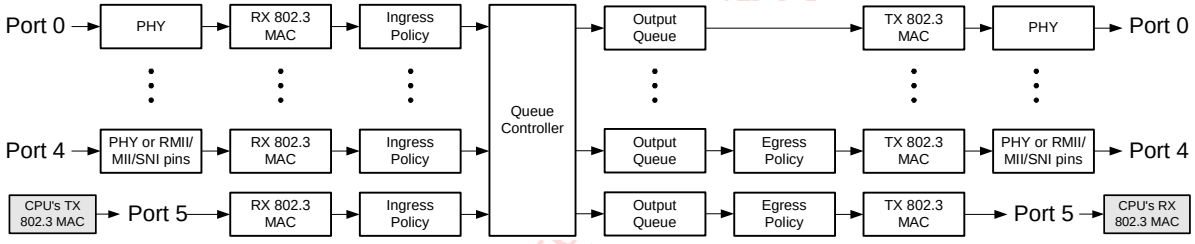


Figure 2: 88E6208 Device Switch Data Flow



The PHY, or physical layer interface, is used to receive and transmit frames over CAT 5 twisted pair cable or fiber-optic cables (only Port 0 supports a fiber option). The 88E6208/88E6218 device contains five PHYs connected to Port 0 to Port 4. The PHY block is covered in detail in section 2.

Port 5 and Port 6 (absent in the 88E6208 device) do not contain PHYs. Port 6 supports a short-distance industry-standard digital interface generically called the port's MII interface. Many interface modes and timings are supported so that a large number of external device types can be used. Port 5 is internal and connected to the CPU subsystem (see Part 1 of this Datasheet set for more information).

.The 88E6208/88E6218 device contains seven independent MACs (the 88E6208 contains six) that perform all of the functions specified in the 802.3 protocol, which include, among others:

- Frame formatting
- CRC checking
- CSMA/CD enforcement
- Collision handling

The switch portion of the 88E6208/88E6218 device receives good packets from the MACs, processes them, and forwards them to the appropriate MACs for transmission. Processing frames is the key activity, and it involves the Ingress Policy block, the Queue Controller, the Output Queues, and the Egress Policy blocks shown in Figure 3. These blocks modify the normal or default packet flow through the switch and are discussed in section 1.6 to section 1.8.

The 88E6208 device has only one output queue per port.

Figure 3: Switch Operation — 88E6218

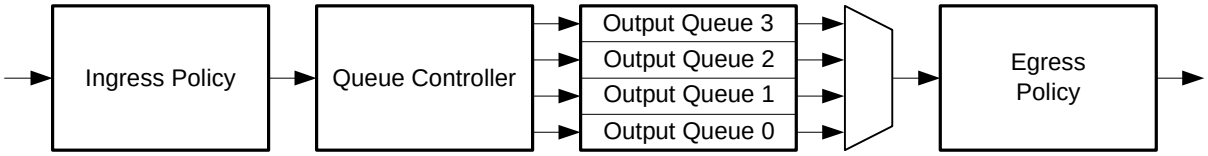
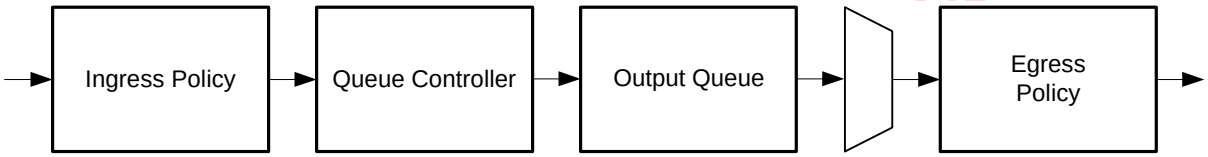


Figure 4: Switch Operation — 88E6208



1.2 Internal CPU Interface

The CPU interface of the 88E6218 allows for three link speeds, 10 Mbps, 100 Mbps, and 200 Mbps. For the 88E6208 device, it allows for two link speeds, 10 Mbps and 100 Mbps. See Part 1 of this document set for more information on this interface.

1.3 MII/SNI Interface (88E6218 only)

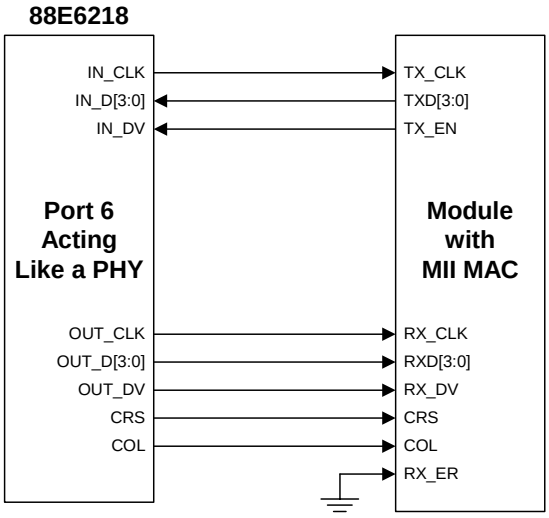
The MII interface supports four major modes of operation:

- MII PHY Mode
- MII MAC Mode
- SNI PHY Mode

1.3.1 MII PHY Mode

The MII PHY Mode, (Reverse MII), configures the selected MAC inside the 88E6218 device to emulate a PHY. This enables the 88E6218 device to be directly connected to an external MAC (for example, one inside a Router CPU). In this mode, the 88E6218 device drives the interface clocks (Px_INCLK and Px_OUTCLK); therefore, the required frequency needs to be selected. Both full-duplex and half-duplex modes are supported and need to be selected to match the mode of the link partner's MAC. The MII PHY interface is compliant with the IEEE 802.3u clause 22.

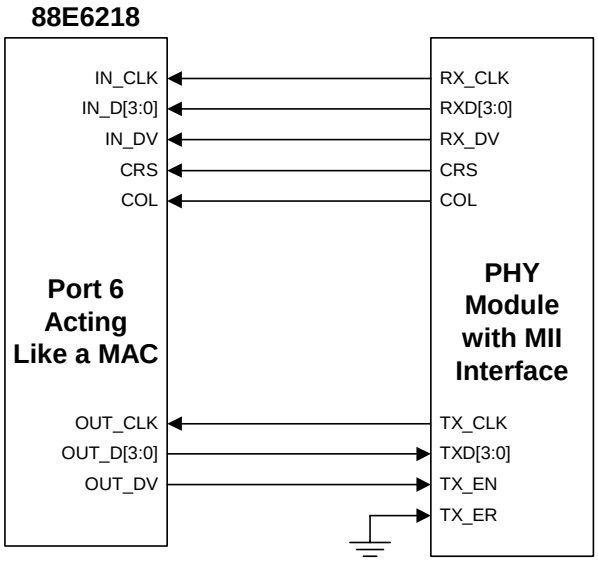
Figure 5: MII PHY Interface Pins



1.3.2 MII MAC Mode

The MII MAC Mode (Forward MII) configures the required MAC inside the 88E6218 device to act as a MAC so that it can be directly connected to an external PHY. In this mode, the 88E6218 device receives the interface clocks (Px_INCLK and Px_OUTCLK) and works at any frequency from DC to 25 MHz or 50 MHz (dependent upon the external source). The two clocks can be asynchronous with respect to each other. Both full-duplex and half-duplex modes are supported and need to be selected to match the mode of the link partner's MAC. The MII MAC interface is compliant with clause 22 of the IEEE 802.3u specification.

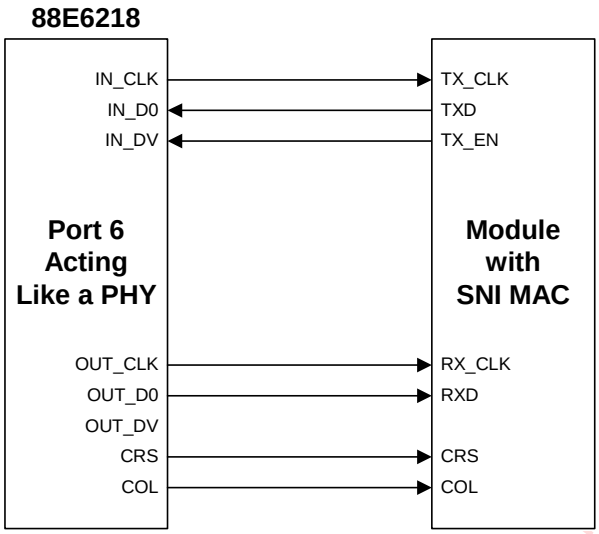
Figure 6: MII MAC Interface Pins



1.3.3 SNI PHY Mode

The SNI PHY Mode, 7-Wire interface, configures the selected MAC inside the 88E6218 device to act as a 10 Mbps PHY, enabling it to be directly connected to an external 10 Mbps-only MAC (such as one inside a Router CPU). In this mode, only one data bit is used on each of input and output (Px_IND0 and Px_OUTD0). The interface clocks, Px_INCLK and Px_OUTCLK, are driven by the 88E6218 device. Since SNI was never standardized, the 88E6218 device supports various SNI modes. The active edge of the clock (either rising or falling) and the active level on the collision signal (either active high or low) can be selected.

Figure 7: SNI PHY Interface Pins



1.3.4 MII/SNI Configuration

MII/SNI interfaces in the 88E6218 device are configured at the rising edges of RESETn. During reset the P6_OUTD[3:0]/P6_MODE[3:0] pins become tri-stated, and the values found on these pins become the interface's mode as defined in Table 3(the Reset and Initialization section in Part 1 of this datasheet publication).

Table 3: RMII/MII/SNII Configuration Options for Port 6

P6 MODE[3:0] (at Reset)	PHY/ MAC Mode	Duplex	MII/SNI Mode	Description
0 0 0 0	PHY	Half-Duplex	SNI 10 Mbps	Falling edge clock with collision active low
0 0 0 1	PHY	Half-Duplex	SNI 10 Mbps	Falling edge clock with collision active high
0 0 1 0	PHY	Full-Duplex	SNI 10 Mbps	Falling edge clock (collision is don't care)
0 0 1 1	MAC	Full-Duplex	MII 200 Mbps	50 MHz MII input clock mode
0 1 0 0	PHY	Half-Duplex	SNI 10 Mbps	Rising edge clock with collision active low
0 1 0 1	PHY	Half-Duplex	SNI 10 Mbps	Rising edge clock with collision active high
0 1 1 0	PHY	Full-Duplex	SNI 10 Mbps	Rising edge clock (collision is don't care)
0 1 1 1	PHY	Full-Duplex	MII 200 Mbps	50 MHz MII output clock mode
1 0 0 0	MAC	Half-Duplex	MII 0 - 100 Mbps	DC to 25 MHz MII input clock mode
1 0 0 1	-	-	-	Reserved for future use
1 0 1 0	MAC	Full-Duplex	MII 0 - 100 Mbps	DC to 25 MHz MII input clock mode
1 0 1 1				Reserved for future use
1 1 0 0	PHY	Half-Duplex	MII 10 Mbps	2.5 MHz MII output clock mode
1 1 0 1	PHY	Half-Duplex	MII 100 Mbps	25 MHz MII output clock mode
1 1 1 0	PHY	Full-Duplex	MII 10 Mbps	2.5 MHz MII output clock mode
1 1 1 1	PHY	Full-Duplex	MII 100 Mbps	25 MHz MII output clock mode

1.3.5 Enabling the MII/SNI Interfaces

Port 6 (the 7th port) is enabled when the DISABLE_P6 configuration pin is low at reset (See Part 1 of this datasheet publication.

1.3.6 Port Status Registers

Each switch port of the 88E6208/88E6218 device has a status register that reports information about that port's PHY or MII/SNI interface. See Section 3.2.1 "Switch Core Register Map" for more information.

1.3.7 MII 200 Mbps Mode

The 88E6218 device MII interfaces can run at a data rate of 200 Mbps in full-duplex mode. Do not select this mode unless the MAC on the other end of the MII interface can also run at this doubled rate. Both PHY (Reverse MII) and MAC (Forward MII) 200 Mbps modes are supported on Port 6. When the 200 Mbps PHY mode is selected, the output MII clocks (OUTCLK and INCLK) run at a 50 MHz rate. There is no change in the format of the data. When the 200 Mbps MAC mode is selected, the input MII clocks (OUTCLK and INCLK) must be 50 MHz +/-50 ppm. This mode can be used to connect a 88E6218 device to another Marvell Link Street™ switch product with 200 Mbps of bandwidth in each direction using only one MII port on each device.

1.4 Media Access Controllers (MAC)

The 88E6218 device contains seven (six in the 88E6208) independent MACs that perform all of the functions in the 802.3 protocol that include, among others, frame formatting, frame stripping, CRC checking, CSMA/CD enforcement, and collision handling.

Each MAC receive block checks incoming packets and discards packets with CRC errors, alignment errors, short packets (fewer than 64 bytes)[1], or long packets (more than 1518 bytes for un-Tagged frames and more than 1522 bytes for IEEE 802.3ac Tagged[2] frames)[3]. Each MAC constantly monitors its receive lines waiting for preamble bytes followed by the Start of Frame Delimiter (SFD). The first six bytes after the SFD are used as the packet's Destination Address (DA), and the next six bytes are used as the packet's Source Address (SA). These two addresses are fundamental to the operation of the switch (see section 1.5). The next two to eight bytes are examined and potentially used for QoS (Quality of Service) decisions (88E6218 only) made inside the switch (see section 1.6.1 and section 1.6.6). The last four bytes of the packet contain the packet's Frame Check Sequence (FCS). The packet is discarded if the FCS does not meet the IEEE 802.3 CRC-32 requirements.

Before a packet can be sent out, the transmit block must check whether the line is available for transmission. The transmit line is available all the time when the port is in full-duplex mode, but the line could be busy receiving a packet when the port is in half-duplex mode. In this case, the transmitter defers its transmission until the line becomes available, when it ensures that a minimum interpacket gap of at least 96 bits occurs before transmitting a 56-bit preamble and an 8-bit Start of Frame Delimiter (SFD) ahead of the basic frame. Transmission of the frame begins immediately after the SFD.

For the half-duplex mode, the 88E6208/88E6218 device also monitors the collision signal while it is transmitting. When a collision is detected (i.e., both transmitter and receiver of a half-duplex MAC are active at the same time), the MAC transmits a JAM pattern and then delays the retransmission for a random time period determined by the IEEE 802.3 backoff algorithm. In full-duplex mode, the collision signal and backoff algorithm are ignored.

1.4.1 Backoff

In half-duplex mode, the 88E6208/88E6218 device's MACs implement the truncated binary exponential backoff algorithm defined in the IEEE 802.3 standard. This algorithm starts with a randomly-selected small backoff time and follows by generating progressively longer random backoff times. The random times prevent two or more MACs from always attempting re-transmission at the same time. The progressively longer backoff times give a wider random range at the expense of a longer delay, giving congested links a better chance of finding a winning transmitter. Each MAC in the 88E6208/88E6218 device resets the progressively longer backoff time circuit after 16 consecutive retransmit trials. Each MAC then restarts the backoff algorithm with the shortest random backoff time and continues to retry and retransmit the frame. A packet that successively collides with a retransmit signal is re-transmitted until transmission is successful. This algorithm prevents packet loss in highly-congested environments.

1.4.2 Half-Duplex Flow Control

Half-duplex flow control is used to throttle the end station to avoid dropping packets during network congestion. It is enabled on all half-duplex ports when the BA[0]/M_A[13] pin is low (see Part 1 of this datasheet publication) at the rising edge of RESETn. The 88E6208/88E6218 device uses a collision-based scheme to perform half-duplex flow control. When the free buffer space is almost exhausted, the MAC forces a collision in the input port when the

1. When Ingress Double Tagging is enabled, the minimum frame size for Tagged frames is 68 bytes.
2. IEEE 802.3ac VLAN Tagged frames are four bytes longer than normal IEEE 802.3 frames. The extra four bytes are used to support Tagging information for IEEE 802.1p and IEEE 802.1Q.
3. A maximum frame size of 1535 bytes is supported by setting the MaxFrameSize bit in the Global Control register—see section 3.2.3.

88E6208/88E6218 device senses an incoming packet. Only those ports that are involved in the congestion are flow controlled. When the half-duplex flow control mode is not set and no packet buffer space is available, the incoming packet is discarded.

1.4.3 Full-Duplex Flow Control

The purpose of full-duplex flow control is the same as that of flow control in the half-duplex case—to avoid dropping packets during congestion. Full-duplex flow control is enabled on all full-duplex ports when:

- BA[1]/M_A[14] pin is low at the rising edge of RESETn (see Part 1), and
- Auto-Negotiation is enabled on the port (see section 2.2.13), and
- The link partner 'advertises' that it supports pause during Auto-Negotiation[1]

Full-duplex flow control is not automatically supported on Port 0 when it is configured for 100BASE-FX operation, nor for Port 5 and Port 6. This is because Auto-Negotiation is not defined for 100BASE-FX or MII. Therefore, the link partners cannot advertise that they support Pause. It can be forced, however—see section 1.4.4. When the full-duplex flow control mode is not set and no packet buffer space is available, the incoming packet is discarded.

In full-duplex mode, the 88E6208/88E6218 MACs support the standard flow control defined in the IEEE 802.3x specification. This flow control enables stopping and restoring the transmission from the remote node. The basic mechanism for performing full-duplex flow control is by means of a Pause frame. The format of the Pause frame is shown in Table 4.

Table 4: Pause Frame Format

Destination Address (6 Bytes)	Source Address (6 Bytes)	Type (2 Bytes)	Op Code (2 Bytes)	Pause Time (2 Bytes)	Padding (42 Bytes)	FCS (4 Bytes)
01-80-C2-00-00-01	See text	88-08	00-01	See text	All zeros	Computed

Full-duplex flow control functions as follows. When the free buffer space is almost exhausted, the 88E6208/88E6218 device sends out a Pause frame with the maximum pause time (a value of all ones—0xFFFF) to stop the remote node from sending more frames into the switch. Only the node that is involved in the congestion is paused. When the event that invoked flow control disappears, the 88E6208/88E6218 device sends out a Pause frame with the pause time equal to zero, indicating that the remote node can resume transmission. The 88E6208/88E6218 device also responds to the Pause command in the MAC receiving block. When the Pause command is detected, the MAC responds within one slot time to stop transmission of the new data frame for the amount of time defined in the pause time field of the Pause command packet.

The Source Address of received Pause frames is not learned (see section 1.5.3 "Address Learning") since it may not represent the Source Address of the transmitting port. This is generally the case if the link partner is an unmanaged switch. The 88E6208/88E6218 device can be configured to transmit a switch-specific Source Address on Pause frames that it transmits (the default is all zeros). Global Switch MAC Address registers 1, 2, and 3 (see Table 33, Table 34, and Table 35) can be set to the required Source Address to use. A single fixed Source Address can be used for all ports, or a unique Source Address per port can be selected by changing the value of the DiffAddr bit in Global register 1.

The MACs always discard all IEEE 802.3x Pause frames that they receive, even when full-duplex flow control is disabled or even when the port is in half-duplex mode.

1. Full-duplex flow control is not automatically supported on Port 0 when it is configured for 100BASE-FX operation since Auto-Negotiation is not defined for 100BASE-FX, and hence, the link partners cannot advertise that they support PAUSE. It can be forced, however – see section 3.3.4.

1.4.4 Forcing Flow Control

When flow control is enabled using the device's pins, it is enabled for all ports of the same type (i.e., on all half-duplex ports or on all full-duplex ports that have a flow-controllable link partner). It may be required to have flow control enabled on only one or two ports and have all the other ports disabled. In this case, flow control should be disabled using the appropriate device pins. Ensure that BA[1]/M_A[14] and BA[0]/M_A[13] are high at the rising edge of RESETn and then set the required port's ForceFlowControl bit to a one (see Port Control Register description in section 3.2.2). This is the only way to enable full-duplex flow control on Port 5, Port 6, and Port 0 when it is in 100BASE-FX mode.

1.4.5 Statistics Counters

Sometimes it is necessary to debug network occurrences. For example, a technician may want to view the network remotely to solve a customer problem or a software programmer may want to trace transmitted frames. In these situations, two basic types of data are important:

- Number of good frames entering and leaving each port of the switch
- Quality of network segment performance

Frame size and the distribution of frames between multicast and unicast types are less important in this kind of debugging for an edge switch.

The 88E6208/88E6218 Statistics Counter support basic debugging needs. Each port can capture two kinds of statistics:

- A count of the number of good frames received with the number of frames transmitted
- A count of the number of bad frames received with the number of collisions encountered

The first statistic answers the question "Where did all the frames go?", while the second statistic answers the question "Does the network segment have any performance problems?". These counters are described in Table 30 on page 76, and in Table 31 on page 76. The counters can be cleared, and their mode chosen by the CtrMode bit in the Switch Global Control register (section 3.2.3).

1.5 Address Management

The primary function of the switch portion of the 88E6208/88E6218 is to receive good packets from the MACs, processes them, and forward them to the appropriate MACs for transmission. This frame processing involves the Ingress Policy, Queue Controller, Output Queues, and Egress Policy blocks shown in Figure 3. These blocks modify the normal or default packet flow through the switch and are discussed following section 1.6. The normal packet flow and processing is discussed first.

The normal packet flow involves learning how to switch packets only to the correct MACs. The switch learns which port an end station is connected to by remembering each packet's Source Address along with the port number on which the packet arrived.

When a packet is directed to a new, currently unlearned MAC address, the packet is transmitted out of all of the ports[1] except for the one on which it arrived[2]. Once a MAC address/port number mapping is learned, all future packets directed to that end station's MAC address (as defined in a frame's Destination Address field) are directed

1. Port-based VLANs modify this operation (section 1.6.2).
2. The 88E6208/88E6218 device can be configured to transmit frames from the same port that they came in on—see Table 27 on page 72.

to the learned port number only. This ensures that the packet is received by the correct end station (if it exists), and when the end station responds, its address is learned by the switch for the next series of packets.

Owing to the limitation of physical memory, switches learn only the currently “active” MAC addresses—a small subset of the 2^{48} possible MAC addresses. When an end station is moved from one port to another, a new MAC address/port number association must be learned, and the old one replaced. These issues are handled by the ‘Aging’ and ‘Station Move Handling’ functions. A MAC address/port number association is allowed to be “active” for only a limited time. This time limit is typically set to five minutes.

1.5.1 Address Translation Unit

The 88E6208/88E6218 device’s Lookup Engine or Address Translation Unit (ATU) gets the DA and SA from each frame received from each port. It performs all address searching, address learning, and address aging functions for all ports at “wire speed” rates. For example, a DA and an SA lookup/learn function can be performed for all ports in less time than it takes to receive a 64-byte frame on that port.

The address database uses a hashing technique for quick storage and retrieval. Hashing a 48-bit address into fewer bits results in some MAC addresses having the same hash address. This situation is called a hash collision and is solved in the 88E6208/88E6218 device by using a four entry bin per hash location that can store up to four different MAC addresses at each hash location. The four-entry bin is twice as deep as that of many competing switching devices and allows for a reduced size of address database while still holding the same number of active random value MAC addresses.

The address database is stored in the embedded SRAM and has a default size of 1024 entries with a default aging time of about 300 seconds (5 minutes). The size of the address database can be modified to a maximum of 512, 1024, or 2048 entries (88E6218 only). Increasing the size of the address database reduces the number of buffers available for frames, however (see Figure 8). The age time can be modified in 16 second increments from 0 seconds (aging disabled) to 4080 seconds (68 minutes). These options are set in the ATU Control register (Table 37 on page 80).

Note

Changing the ATU size must be done very carefully since it affects the frame buffer area—see ATUSize and SWReset register descriptions in Table 37 on page 80.

Figure 8: ATU Size Tradeoffs—88E6218

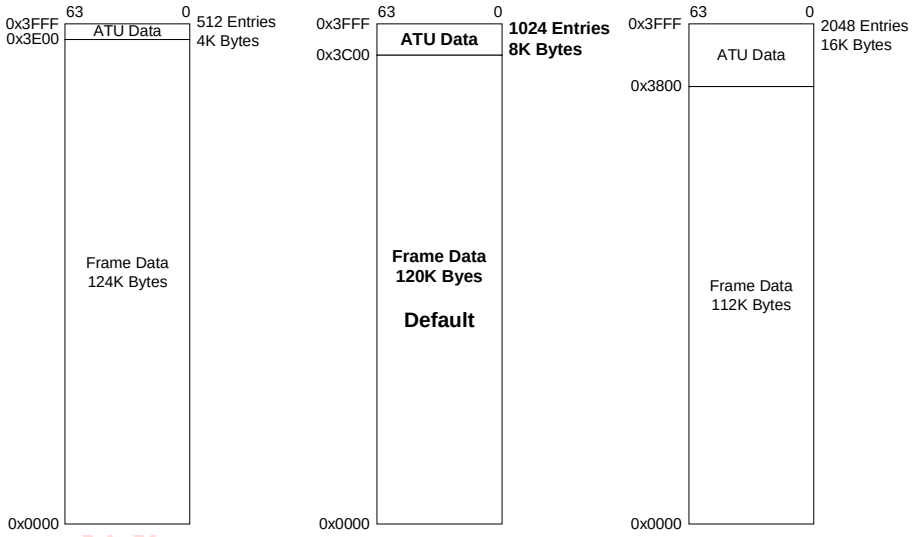
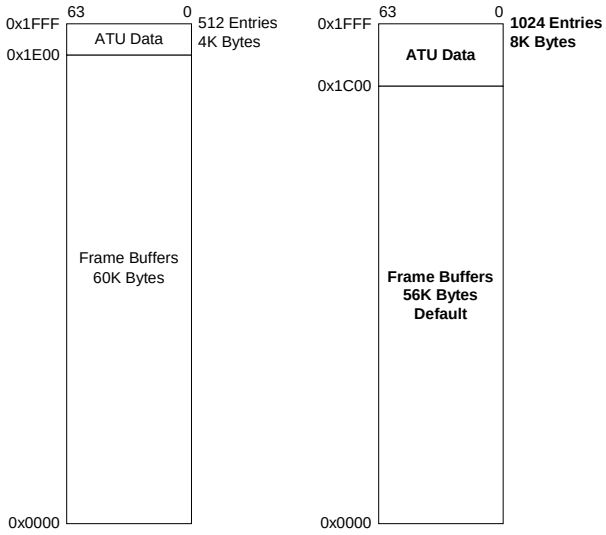


Figure 9: ATU Size Tradeoffs—88E6208



1.5.2 Address Searching or Translation

The address search engine searches the address database to get the output port number(s), called the Destination Port Vector (DPV), for each frame's Destination Address (DA). When an address is found, it can switch the frame instead of flooding it. Flooding refers to the action of sending frames out all the ports of the switch except for the port the frame came in on. The switch arbitrates destination address lookup requests from the seven ports (six for the 88E6208) and grants one lookup at a time. The MAC address is hashed, and then data is read from the

SRAM table and compared to the MAC address for a match. Four different addresses can be stored at each hash location. When a match is found, the Address Translation Unit (ATU) returns the DPV to the Ingress Policy block where it may get modified before the packet is queued to the output port(s). The DPV returned from the ATU may get modified by the VLANTable data - see section 1.6.2. When no MAC address match is found, the Ingress Policy block uses a unique default DPV for each Ingress port, which typically floods the frame. The default DPV for each port is the Port's VLANTable data – see Table 27 on page 72. When the destination address in the frame is a multicast address or broadcast address, the address is searched in the same way as a unicast address, and the frame is processed identically. Multicast addresses cannot be learned, so they appear in the address database only when they are loaded into it by a CPU—see section 1.5.5.3. This feature is used for multicast filtering and Bridge Protocol Data Unit (BPDU) handling. BPDU frames are special frames used for Spanning Tree or bridge loop detection. Multiple separate address databases are supported in the 88E6208/88E6218. In this device the database that is searched is controlled by the port's database number setting (DBNum - Table 27 on page 72). MAC addresses that are not members of the port's DBNum cannot be found.

1.5.3 Address Learning

The address learning engine learns source addresses of incoming frames. Up to 2048 MAC address/port number mappings (1024 in the 88E6208) can be stored in the address database. See section 1.5.1. When the source address from an input frame cannot be found in the address database, the ATU enters the self-learning mode, places the new MAC address/port number mapping into the database, and refreshes its Age time. The Age time on a MAC Address entry is refreshed by setting its Entry_State field to 0xE. When the MAC address is already in the database, the port number and Age associated with the entry is updated and/or refreshed. The port number is updated in case the end station has moved, and the port number needs to be corrected. The entry's Age is refreshed since the MAC address is still "active". This refreshing prevents the MAC address/port number mapping from being prematurely removed as being "inactive".

When an address is added to the database it is hashed and stored in the first empty bin found at the hashed location. When all four address bins are full, a "least recently used" algorithm scans each entry's Age time in the Entry_State field. This field is described in section 1.5.5.1. If all four address bins have the same Age time, the first unlocked bin is used (see section 1.5.5.1 for more information about locked, i.e. static, addresses). If all four bins are locked, the address is not learned and an ATUFull interrupt is generated. See the Switch Global Status register—Table 32 on page 77. Multiple separate address databases are supported in the 88E6208/88E6218 device.

In this device, the port's database number (DBNum—Table 27 on page 72) determines the address database into which the learned MAC address is stored. The same MAC address can be learned multiple times with different port mappings if different DBNum values are used.

Learning can be disabled for all ports by setting the LearnDis bit to a one in the ATU Control register (Table 37 on page 80). Learning is disabled on any port that has a PortState of Disabled or Blocking/Listening (see the Port Control register—Table 26 on page 70).

1.5.4 Address Aging

Address aging makes room for new active addresses by ensuring that when a node is disconnected from the network segment or when it becomes inactive, its entry is removed from the address database. An address is removed from the database after a predetermined interval from the time it last appeared as an Ingress frame's source address (SA). This interval is programmable in the 88E6208/88E6218 device. The default Aging interval is about 5 minutes (282 to 304 seconds), but it can be set from 0 seconds (i.e., aging is disabled) to 4,080 seconds in 16 second increments. See AgeTime in ATU Control register – Table 37 on page 80.

The 88E6208/88E6218 device runs the address aging process continuously unless disabled by clearing the AgeTime field in the ATU Control register to zero. Aging is accomplished by a periodic sweeping of the address database. The speed of these sweeps is determined by the AgeTime field. On each aging sweep of the database, the

ATU reads each valid entry and updates its Age time by decrementing its Entry_State field as long as the entry is not locked. The Entry_State field is described in section 1.5.5.1. When the Entry_State field reaches zero, the entry is considered invalid and purged from the database.

The time taken to age out any entry in the MAC address database is a function of the AgeTime value in the ATU Control register and the value in the Entry_State field. A new or just-refreshed unicast MAC address has an Entry_State value of 0xE. See section 1.5.2. A purged or invalid entry has an Entry_State value of 0x0. The values from 0xD to 0x1 indicate the Age time on a valid unicast MAC address with 0x1 being the oldest. This scheme provides 14 possible age values in the Entry_State field which increases precision in the age of entries in the MAC address database. This precision is relayed to the “least recently used” algorithm that is employed by the address learning process. An address is purged from the database within 1/14th of the programmed AgeTime value in the ATU Control register.

1.5.5 Address Translation Unit Operations

The ATU in the 88E6208/88E6218 device supports user commands to access and modify the contents of the MAC address database.

All ATU operations have the same user interface and protocol. Five Global registers are used and are shown in Table 5 below. The protocol for an ATU operation is as follows:

1. Ensuring the ATU is available by checking the ATUBusy bit in the ATU Operation register. The ATU can only perform one user command at a time.
2. Loading the ATU Data and ATU MAC registers, if required by the required operation.
3. Starting the ATU operation by defining the required DBNum, ATUOp, and setting the ATUBusy bit to a one in the ATU Operation register. The DBNum, ATUOp and the ATUBusy bits setting can be done at the same time.
4. Waiting for the ATU operation to complete. Completion can be verified by polling the ATUBusy bit in the ATU Operation register or by receiving an ATUDone interrupt. See Switch Global Control register Table 36 on page 79 and Switch Global Status register, Table 32 on page 77.
5. Reading the required results, if appropriate.

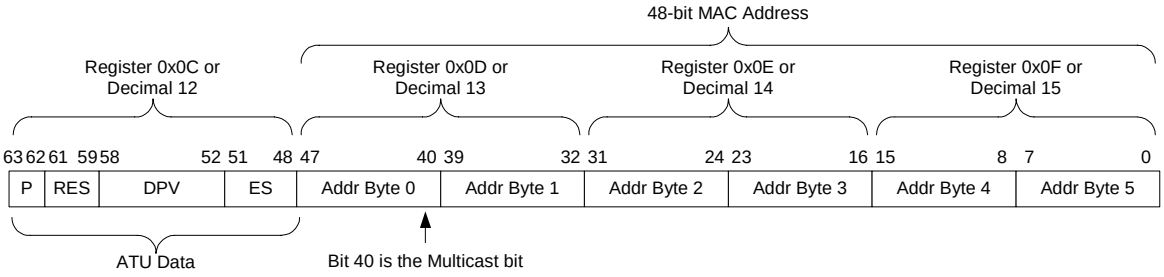
Table 5: ATU Operations Registers

Register	Offset	Section	Before the Operation Starts	After the Operation Completes
ATU Operation	0x0B or Decimal 11	Table 38 on page 81	Used to define the required operation (including which database to search, i.e., the DBNum field) and start it.	Used to indicate the ATU’s Busy status.
ATU Data	0x0C or Decimal 12	Table 39 on page 82	Used further to define the required operation and used as the required ATU Data that is to be associated with the required MAC address below.	Returns the ATU Data that is associated with the resulting MAC address below.
ATU MAC (3 registers)	0x0D to 0x0F or Decimal 13 to 15	Table 40 on page 82	Used to define the required MAC address upon which to operate	Returns the resulting MAC address from the required operation.

1.5.5.1 Format of the ATU Database

Each MAC address entry in the ATU database is 64 bits in size. The lower 48 bits contain the 48-bit MAC address, and the upper 16 bits contain information about the entry as shown in Figure 10. The database is accessed 16 bits at a time via the Switch Global registers shown in the figure. For more information about these registers, see Table 40 through Table 42

Figure 10: Format of an ATU Entry



The upper 16 bits of the ATU entry are called the ATU Data which are separated into four fields—see Table 6 and Table 39 on page 82.

Note

The DPV resides in bits 57 to 52 in the 88E6208 device since there is no Port 6

Table 6: ATU Data Fields

Field	Bits	Description
Entry_State	51:48	The Entry_State field, together with the entry's Multicast bit (bit 40) is used to determine the entry's age or its type as follows: For unicast MAC addresses (bit 40 = 0): 0x0 = Invalid, empty, or purged entry. 0x1 to 0xE = Valid entry where the Entry_State = the entry's age, and the DPV indicates the port or ports mapped to this MAC address. 0xF = Valid entry that is locked and does not age. The DPV indicates the port or ports mapped to this MAC address, and the Priority bits indicate the priority to use overriding any other priorities (88E6218 device only). For multicast MAC addresses (bit 40 = 1): 0x0 = Invalid, empty, or purged entry. 0x5 = Valid entry that is locked and does not age. The DPV indicates the port or ports mapped to this MAC address. Frames with this MAC address are NOT limited by Multicast Rate Limiting (88E6218 device only)—see section 1.6.6. 0x7 = Valid entry that is locked does not age. The DPV indicates the port or ports mapped to this MAC address. Used for multicast filtering. 0xE = Valid entry that is locked and does not age. The DPV indicates the port or ports mapped to this MAC address. Frames with this MAC address are considered MGMT (management) frames and are allowed to tunnel through blocked ports (see section 1.6), and the Priority bits indicate the priority to use overriding any other priorities. Used for BPDU handling.
DPV	58:52 (88E6218) 57:52 (88E6208)	The Destination Port Vector. These bits indicate which port or ports are associated with this MAC address (i.e., where frames should be switched to) when they are set to a one. A DPV of all zeros indicates that frames with this DA should be discarded. Bit 52 is assigned to physical Port 0, 53 to Port 1, 54 to Port 2, and so on.
Reserved	61:59 (88E6218) 61:58 (88E6208)	Reserved for future use.
Priority	63:62	These priority bits can be used as a frame's priority depending upon the value of the Entry_State (bits 51:48 above). When these bits are used, they override any other priority determined by the frame's data—88E6218 device only; these bits are reserved in the 88E6208 device.

1.5.5.2 Reading the Address Database

The contents of the address database can be dumped or searched. The Get Next operation returns the active contents of the address database in ascending network byte order. A search operation can also be done using the Get Next operation. If multiple address databases are being used, the Get Next function returns all unique MAC

addresses from all of the databases. If the same MAC address appears in multiple address databases, only one instance of that MAC address is returned from the Get Next operation.

The Get Next operation starts with the MAC address contained in the ATU MAC registers and returns the next higher active MAC address currently active in the address database. Use an ATU MAC address of all zeros to get the first or lowest active MAC address. The returned MAC address and its data is accessible in the ATU MAC and the ATU Data registers. To get the next higher active MAC address, the Get Next operation can be started again without setting the ATU MAC registers since they already contain the 'last' address. A returned ATU MAC address of all ones indicates that no higher active MAC addresses was found. This result indicates that the end of the database has been reached. A summary of how the Get Next operation uses the ATU's registers is shown in Table 7.

Table 7: ATU Get Next Operation Register Usage

Register	Offset	Section	Before the Operation Starts	After the Operation Completes
ATU Operation	0x0B or Decimal 11	Table 38 on page 81	Used to define the required operation (including which database to search, i.e., the DBNum field) and start it.	Used to indicate the ATU's Busy status.
ATU Data	0x0C or Decimal 12	Table 39 on page 82	Ignored.	Returns the ATU Data that is associated with the resulting MAC address below. If Entry_State = 0x0 the returned data is not a valid entry.
ATU MAC (3 registers)	0x0D to 0x0F or Decimal 13 to 15	Table 40 through Table 42	Used to define the starting MAC address to search. Use an address of all zeros to find the first or lowest MAC address. Use the last address to find the next address. There is no need to write to this register in this case.	Returns the next higher active MAC address if found, or all ones are returned indicating the end of the table has been reached.

To search for a particular MAC address, start the Get Next operation with a MAC address one less than the required MAC address to search using the DBNum of the database you want to search. When the searched MAC address is found, it is returned in the ATU MAC registers along with its associated data in the ATU Data register. When the searched MAC address is not found active, then the ATU MAC registers will not equal the required searched address.

1.5.5.3 Loading and Purging an Entry in the Address Database

Any MAC address (unicast or multicast) can be loaded into, or removed from, the address database by using the Load operation. An address is loaded into the database if the Entry_State in the ATU Data register (Table 39 on page 82) is non-zero. A value of zero indicates the required ATU operation is a purge.

The load operation searches the address database indicated by the database number, DBNum (in the ATU Operation register), for the MAC address contained in the ATU MAC registers. When the address is found, it is updated by the information found in the ATU Data register.

Note

A load operation becomes a purge operation when the ATU Data's Entry_State equals zero. Also, locked addresses can be modified without their needing to be purged first.

If the address is not found and if the ATU Data's Entry_State does not equal zero, the address is loaded into the address database using the same protocol as is used by automatic Address Learning. See section 1.5.3. The 16 bits of the ATU Data register are written into bits 63:48 of the ATU entry. See section 1.5.5.1.

A summary of how the Load operation uses the ATU's registers is shown in Table 8.

Table 8: ATU Load/Purge Operation Register Usage

Register	Offset	Section	Before the Operation Starts	After the Operation Completes
ATU Operation	0x0B or Decimal 11	Table 38 on page 81	Used to define the required operation (including which database to load or purge, i.e., the DBNum field) and start it.	Used to indicate the ATU's Busy status.
ATU Data	0x0C or Decimal 12	Table 39 on page 82	Used to define the associated data that is loaded with the MAC address below. When Entry_State = 0, the load becomes a purge.	No change.
ATU MAC (3 registers)	0x0D to 0x0F or Decimal 13 to 15	Table 40 through Table 42	Used to define the MAC address to load or purge.	No change.

1.5.5.4 Flushing Entries

All MAC addresses, or just the unlocked MAC addresses, can be purged from the entire set of address databases using single ATU operations. These ATU operations are:

- Flush all Entries
- Flush all Unlocked Entries

The ATU Data and ATU MAC Address registers are not used for these operations and they are left unmodified.

1.6 Ingress Policy

The Ingress Policy block modifies the normal packet flow through the switch. All ports have identical capabilities. The content of each frame is examined more deeply for Quality of Service (QoS) priority information (88E6218 only), the frames are prevented from exiting from certain ports by the use of port-based VLANs and frames are prevented from entering the switch by the use of switch management Port States. An optional Trailer mode enables a management CPU to override the switch giving the CPU complete control over those frames that it selects. Rate limiting is also supported along with a Double Tagging option (88E6218 only).

1.6.1 Quality of Service (QoS) Classification (88E6218 only)

The Ingress Policy block does not perform QoS switching policy; this task is performed by the Queue Controller. Instead, the Ingress Policy block determines the priority of each frame for the Queue Controller. The priority of a frame is determined in priority order by:

1. The CPU's Trailer when enabled on the port; See section 1.6.8.
2. The frame's DA; when that DA is in the address database with a defined priority. See section 1.5.5.
3. The IEEE 802.3ac Tag containing IEEE 802.1p priority information; this IEEE 802.1p priority information is used in determining frame priority when IEEE 802.3ac tagging is enabled on the port. See section 1.6.1.2.
4. The IPv4 Type of Service (TOS)/DiffServ field or IPv6 Traffic Class field when enabled on the port. IPv4/IPv6's priority classification can be configured on a per port basis to have a higher priority than IEEE Tag. The default state is "enabled" on all of the ports. See section 1.6.1.3.
5. The Port's default priority defined in DefPri in the Rate Control register (see Table 29 on page 74).

The designer can enable these classifications individually or in combination. For instance, if a 'hot', higher priority port is required for a switch design, priority classifications 1 to 4 can be disabled. This setting leaves only priority classification 5 active (the Port's default), which results in all ingress frames being assigned the same priority on that port.

- The priority classifications, except for #2, the DA, can be disabled separately on a per-port basis. These settings enable each port in the switch to be configured to use different rules for priority classification. See the UseTag and UseIP bits in the Port Control registers—Table 26 on page 70
- Priority classification #3 (IEEE Tag) and #4 (IP) can also be reversed on a per port basis using the TagIfBoth bit in the Port Control register. This feature enables priority to be selected both for Tagged frames and for IP frames.

The CPU's Trailer, when enabled on the port, supersedes any other priority that may apply to the frame. Thus the CPU can have ultimate control over every frame that it transmits into the switch. The DA priority is used to set the highest priority on BPDUs or other MGMT frames since these frames should never be dropped.

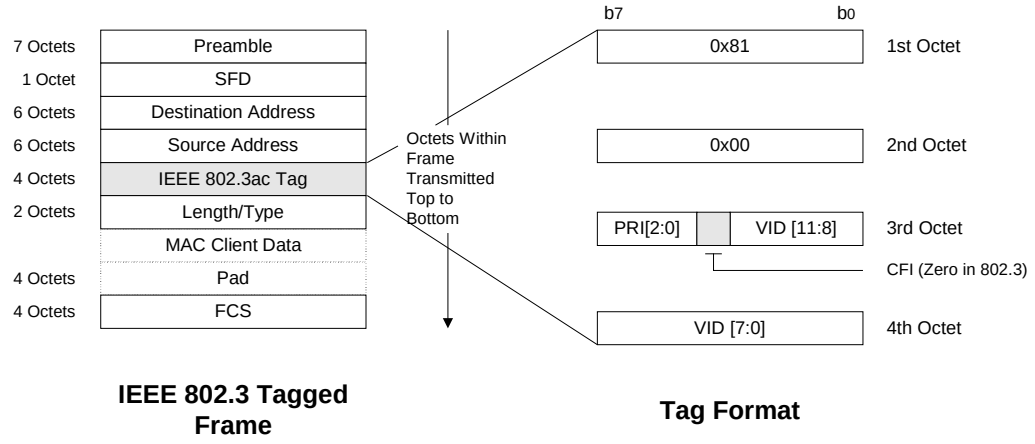
1.6.1.1 Forced Priority

All IEEE tagged frames entering a port can have their priority overridden and set to the port's default priority if none of the other priority classification rules are enabled on the port (i.e., UseIP and UseTag should be zero on the port—see Port Control Register— Table 26 on page 70. If these tagged frames egress the switch tagged, their 3-bit priority field in the tag is modified to the ingress port's default priority. This prevents an end user from using an unauthorized higher priority than that allocated.

1.6.1.2 IEEE Tagged Frames (88E6218 only)

The format of an IEEE Tagged frame is shown in Figure 11.

Figure 11: IEEE Tag Frame Format



The 88E6218 device captures the frame's PRI[2:0] bits and uses them as the frame's priority. The IEEE Tag supports eight priorities, while the 88E6218 device supports four. The Ingress Policy block takes PRI[2:0] and maps them into the two priority bits passed to the Queue Controller. This is done using the data found in the IEEE-PRI register (Table 51 on page 88). The CFI and VID bits of the IEEE Tag are ignored by the 88E6218 device. The device's default is to capture and use IEEE Tagged frame priority data over IP priority data on all ports.

1.6.1.3 IPv4 & IPv6 Frames (88E6218 only)

The format of an IPv4 TOS/DiffServ frame is shown in Figure 12, and an IPv6 Traffic Class frame is shown in Figure 13.

Figure 12: IPv4 Frame Format

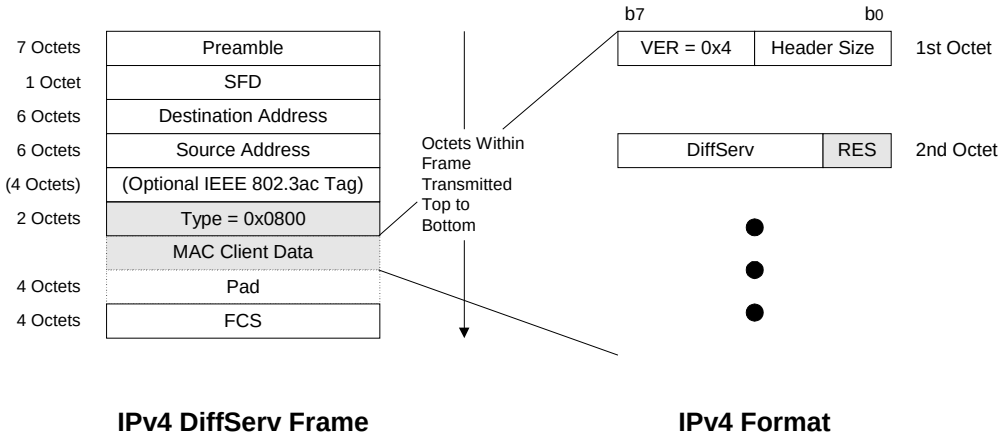
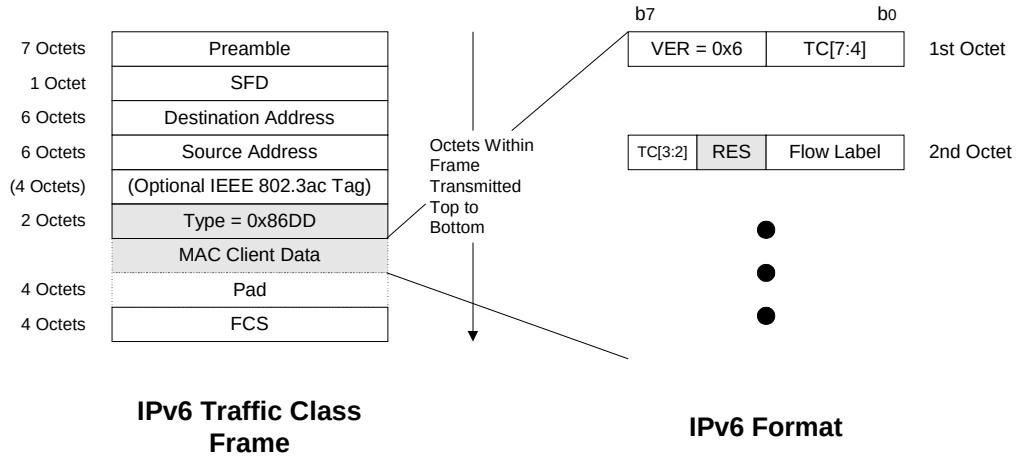


Figure 13: IPv6 Frame Format



The 88E6218 device capture the frame's DiffServ bits when it is an IPv4 frame or the frame's TC[7:2] bits when it is an IPv6 frame and uses them as the frame's priority. The DiffServ/TC bits support 64 priorities, while the 88E6218 device supports four. The Ingress Policy block takes DiffServ/TC bits and maps them into the two priority bits passed to the Queue Controller. This is done using the data found in the IP-PRI registers (see Table 43 on page 84 and those following). The rest of the frame's IP bits are ignored by the 88E6218 device. The device's default is to capture and use IP frame priority data in the absence of IEEE Tag priority data on all ports.

1.6.2 VLANs

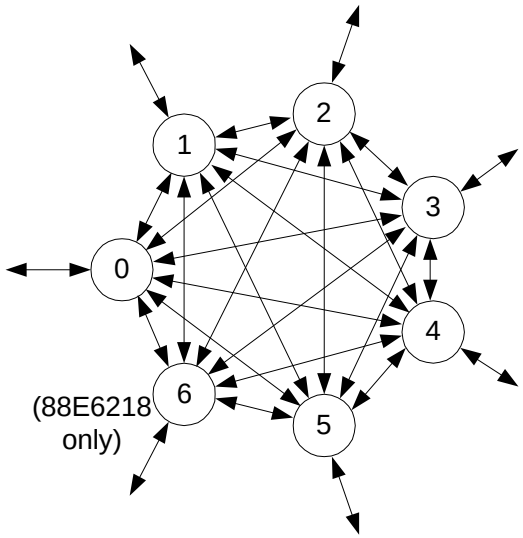
The 88E6208/88E6218 devices support port-based VLANs.

1.6.2.1 Port Based VLANs

The 88E6208/88E6218 device supports a very flexible port-based VLAN feature.

Each Ingress port is associated with the VLANTable field of the Port-based VLAN Map register that restricts which egress ports its frames may use. (see Table 27 on page 72). When bit 0 of a port's VLANTable field is set to a one, that port is allowed to send frames to Port 0. When bit 1 of this field is set to a one, that port is allowed to send frames to Port 1. If bit 2 equals 1, Port 2 may receive frames, etc. At reset the VLANTable field value for each port is set to all ones, except for each port's own bit, which is cleared to a zero. This prevents frames from going back out of the port at which they arrived. This default VLAN configuration allows all of the ports to send frames to all of the other ports as shown in Figure 14.

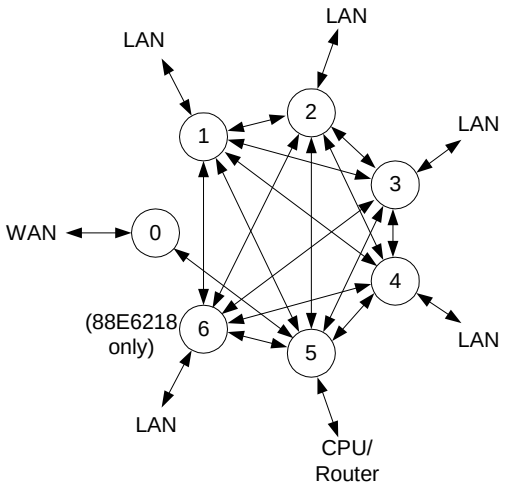
Figure 14: Switch Operation with VLANs Disabled



For unusual situations that require ingress frames to be reflected out of their ingress port, that port's own bit in the VLANTable field of the Port-based VLAN Map register can be set to a one—see section 1.6.3 and the register table listed above.

One reason for VLAN support in the 88E6208/88E6218 device is to isolate a port for firewall router applications. Figure 15 shows a typical VLAN configuration for a firewall router. Port 0 is the WAN port (since it can be either fiber, or copper with Auto-Crossover—section 2.4.1). The frames arriving at this port must not go out to any of the LAN ports, but they must be able to go to the router CPU. All the LAN ports are able to send frames directly to each other without the need for CPU intervention but they cannot send frames directly to the WAN port. To accomplish routing, the CPU is able to send frames to all of the ports.

Figure 15: Switch Operation with a Typical Router VLAN Configuration



This specific VLAN configuration is accomplished by setting the port's VLANTable registers as follows:

Table 9: VLANTable Settings for Figure 15

Port #	Port Type	VLANTable Setting
0	WAN	0x20
1	LAN	0x7C
2	LAN	0x7A
3	LAN	0x76
4	LAN	0x6E
5	CPU	0x5F
6 (88E6218 only)	LAN	0x3E

1.6.2.2 Tunneling Frames Through Port-Based VLANS

Normally frames cannot pass through the port based VLAN barriers. However, some frames can be made to pass through the VLAN barriers on the 88E6208/88E6218 device. Before a frame can tunnel through a port based VLAN barrier, its destination address (DA) must be locked into the address database (section 1.5.5.1), and the VLANTunnel bit on the frame's Ingress port must be set to a one (Table 26 on page 70). When both of these conditions are met, the frame is sent out of the port or ports indicated in the locked address's DPV field for the DA entry in the address database. The VLANTable data is ignored in this case. This feature is enabled only on those ports that have their VLANTunnel bit set to a one and Port Based VLANs are being used on the frame.

1.6.3 Switching Frames Back to their Source Port

The 88E6208/88E6218 device supports the ability to return frames to the port at which they arrived. While this is not a standard way to handle Ethernet frames, some applications may require this ability on some ports. This feature can be enabled on a port-by-port basis by setting the port's own bit in its VLANTable register to a one. See section 1.6.2 and Table 27 on page 72.

1.6.4 Port States

The 88E6208/88E6218 device supports four Port States per port as shown in Table 10. The Port States are used by the Queue Controller (section 1.7) in the 88E6208/88E6218 device to adjust buffer allocation. They are used by the Ingress Policy blocks to control which frame types are allowed to enter and leave the switch, so that Spanning Tree or other bridge loop detection software can be supported. The PortState bits in the Port Control register (Table 26 on page 70) determine each port's Port State, and they can be modified at any time.

Table 10 below lists the Port States and their function. Two of the Port States require the detection of MGMT frames. MGMT frames in the 88E6208/88E6218 are any multicast frame whose DA address is locked into the address database with an Entry_State value of 0xE (section 1.5.5.1).These MGMT frames are typically used for 802.1D Spanning Tree Bridge Protocol Data Units (BPDUs), but any multicast address can be used supporting new and/or proprietary protocols.

Table 10: Port State Options

Port State	Description
Disabled	Frames are not allowed to enter (ingress) or leave (egress) a disabled port. Learning does not take place on disabled ports.
Blocking/ Listening	Only MGMT frames are allowed to enter or leave a blocked port. All other frame types are discarded. Learning is disabled on blocked ports.
Learning	Only MGMT frames are allowed to enter or leave a learning port. All other frame types are discarded, but learning takes place on all good frames even if they are not MGMT frames.
Forwarding	Normal operation. All frames are allowed to enter and leave a forwarding port. Learning takes place on all good frames.

The default Port State for all of the ports in the switch can be either Disabled or Forwarding depending upon the value of the M_A[0] pins (see Pin Description in Part 1 of this datasheet). The ports should come up in the Disabled Port State.

Note

Configuring the ports in the forwarding mode is for debug purposes only. If the ports are so configured in production, WAN to LAN traffic occurs without routing until the software has time to initialize the port-based VLANs.

1.6.5 Ingress Double VLAN Tagging (88E6218 only)

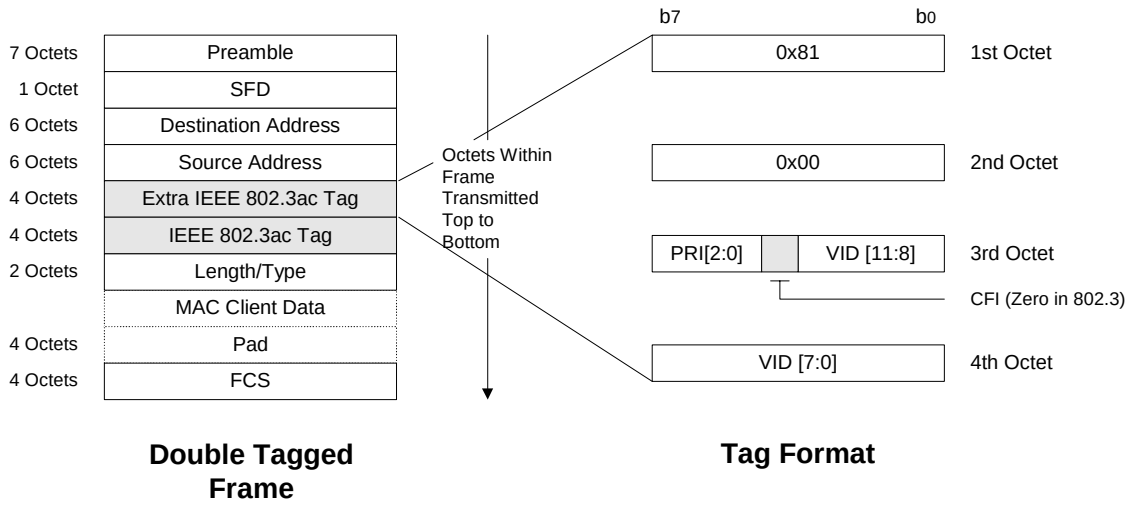
Double Tagging is a way to isolate one IEEE 802.1Q VLAN from other IEEE 802.1Q VLANs in a hierarchical fashion that is compatible with IEEE 802.1Q-aware switches as long as those switches support a maximum frame size of 1526 bytes or more. This method places an extra or Double Tag in front of a frame's normal Tag (assuming the

frame were already tagged), increasing the frame size by 4 bytes. The Double Tag frame format is shown in Figure 16.

Ingress Double Tagging is selectable on a port-by-port basis by setting the port's IngressMode bits in its Port Control register (Table 26 on page 70). Typically any port that has Ingress Double Tagging enabled also has Egress Double Tagging enabled (see section 1.8.2).

An Ingress port that has Double Tagging enabled expects all ingress frames to contain an extra Tag that needs to be removed from the frame prior to performing the port's ingress policy on the frame. In this mode, the ingress port removes the first IEEE 802.3ac Tag that appears after the Source Address in every frame. If the frame is untagged, it is not modified. When the frame has a single Tag, it is removed. If the frame has two Tags, the first Tag is removed. The CRC on modified frames is updated. The port's ingress policies of frame size checking and priority determination are performed *after* the first Tag is removed (if it were present). Thus, Tagged frames must be at least 68 bytes in size, so as not to be considered undersized frames after the Tag is removed. Frame padding is not performed on Ingress Double Tagging. All data from the removed Tags is ignored by the switch.

Figure 16: Double Tag Format



1.6.6 Ingress Rate Limiting (88E6218 only)

A switch design may need to limit the reception rate of multicast frames along with unknown or flooded unicast frames, or it may need to limit the rate for all frames but still keep QoS. The 88E6218 device supports this feature on a per port basis by setting bits in the port's Rate Control register (Table 29 on page 74). The process to arrive at such a design is shown as follows:

1. The types of frames to limit must be determined. The 88E6218 device can limit all frames, only multicast and flooded unicast frames (including broadcast frames), only multicast frames (including broadcast), or just broadcast frames. Specific multicast addresses can override this limit setting if they are locked into the address database with an Entry_State value of 0x5 (section 1.5.5 and Table 6). MGMT (management[1]) frames can also be specifically excluded by clearing the port's LimitMGMT bit to a zero in the Rate Control

1. BPDU frames are MGMT frames (section 1.5.5.1).

register. Any frame that is not limited by the above rules is ignored in the rate calculations (i.e., their size is not counted towards the limit total).

2. The required maximum rate must be selected. the 88E6218 device supports seven different rate limits from 128 Kbps to 8 Mbps. Ingress rate limiting can be disabled on this port by selecting the Not Limited option.
3. The maximum rate for higher priority frames must be selected. The 88E6218 device supports four different QoS priorities and each higher priority can be limited to the same rate as the next lower priority or its limit can be twice as much. This feature supports a maximum limit of 64 Mbps for priority-3 frames.
4. The bytes to count for limiting must be determined. The default setting is to include the frame's bytes from the beginning of the Preamble field to the end of the frame check sequence (FCS) field and including a 96-bit inter frame gap (IFG). The frame's preamble bytes (the 8 bytes prior to the DA) are included if the CountPre bit is set to a one in the port's Rate Control register. The frame's minimum IFG bytes (the 12-byte inter-frame gap after the FCS) are included if the CountIFG is set to a one so either or both of these can be excluded if required.

1.6.7 Switch's Ingress Header

The CPU in a router must perform many functions. One of those functions is routing IP frames, and another is bridging frames between WAN ports and LAN ports. The 88E6208/88E6218 device's Ingress Header mode increases the performance of both of these functions. Any 88E6218 port can be configured to support an Ingress Header by setting the Header bit in the port's Port Control register (Table 26 on page 70), but only the CPU's port should be configured in this way[1]. The 88E6208 only supports the header mode on Port 5, the CPU port.

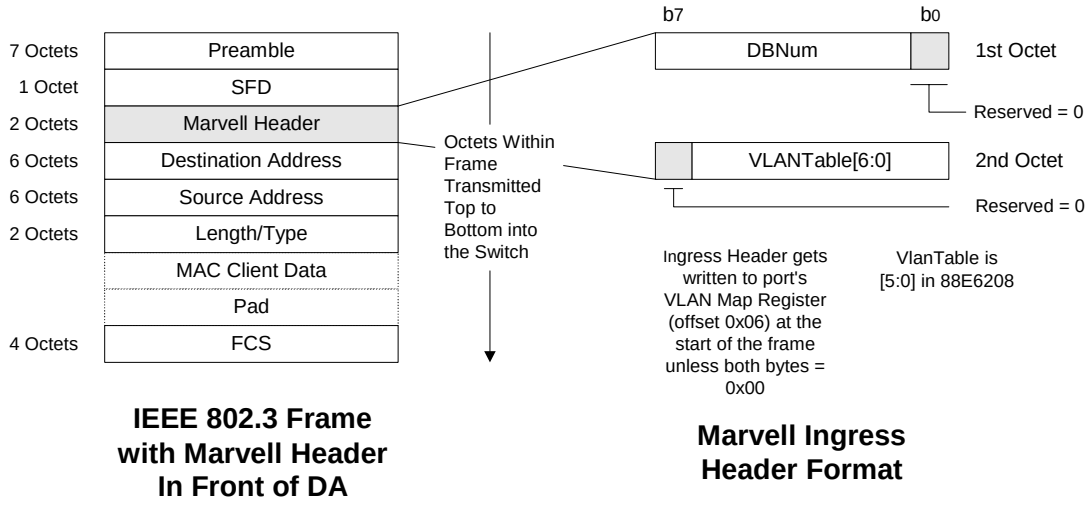
The Ingress Header accelerates the CPU's performance when routing IP frames by aligning the IP portion of the frame with 32-bit boundaries. This is accomplished by prepending the frame with two extra bytes of zeros. Bridging between WAN and LAN ports sometimes requires the switch to support multiple address databases (one for the LAN and one for the WAN) so the same MAC address can be used on multiple ports. Since the CPU is generally a member of all VLANs, it must notify the switch which VLAN to use for a given frame (and thus which address database to use). This is accomplished by using an Ingress Header with a non-zero value as defined in Figure 17[2]. When the Ingress Header is seen with a non-zero value, its contents are written to the port's Port Based VLAN Map register (Table 27 on page 72) prior to the start of the rest of the frame. The frame is then processed by the switch using this new information. In this way the CPU can direct which VLAN and address database to use on every frame at wire speed.

When the Ingress Header mode is enabled on a port, the first two bytes of the frame (just before the DA) are used to direct the switch action. The Ingress Policy block removes the Header from the frame and overwrites the frame's CRC with a new one (causing the frame to be two bytes smaller in size). This adjustment makes the frame "normal" for the rest of the network since the Header's data is intended for the switch only. Frame size checking is performed on the adjusted frame size. This means that the CPU must always add two bytes of data to the beginning of every frame that it sends into the switch (if the Header mode is enabled).

The Ingress Header gives the CPU the ability to control which VLAN, VLAN Mode, and address database to use on the frame it just received. However, the switch's register may not need to be changed by the CPU. If the CPU notifies the switch to process the frame based upon the switch's current ingress policy, the CPU sets the Header data in the frame to all zeros (i.e., it prepends the frame with two extra bytes of zeros). This zero padding notifies the switch to ignore the header's data and process the frame normally (after the header is removed from the frame).

1. The Header bit enables the Header mode for both Ingress and Egress.
2. Reserved bits in the Header must always be zeros.

Figure 17: Ingress Header Format



IEEE 802.3 Frame with Marvell Header In Front of DA

Marvell Ingress Header Format

Note

See UniMAC device description in Part 1 of this datasheet set.

1.6.8 Switch's Ingress Trailer

When a CPU needs to perform Spanning Tree or other bridge loop detection or when it must be able to send frames out of a special port or ports, the CPU's port must be configured for Ingress Trailer mode. Any port can be configured in this way by setting the IngressMode bits in the port's Port Control register (Table 26 on page 70), but only the CPU's port should be configured in this way. The 88E6208 only supports the trailer mode on port 5, the CPU port.

When the Ingress Trailer mode is enabled on a port, the last four bytes of the data portion of the frame are used to configure the switch—see Figure 18. The Ingress Policy block removes the Trailer from the frame and overwrites it with a new CRC, causing the frame to be four bytes smaller in size. This adjustment makes the frame 'normal' for the rest of the network since the Trailer's data is intended for the switch only. Frame size checking is performed on the adjusted frame size. This means the CPU must always add four bytes of data to the end of every frame it sends into the switch when the Trailer mode is enabled.

The Ingress Trailer gives the CPU the ability to override normal switch operation on the frame that it just transmitted but this override may not always be necessary. When the CPU requires the switch to process the frame with the switch's current ingress policy, the CPU sets the Trailer data in the frame to all zeros by inserting a four-byte pad there. This zero padding clears the Override bit in the Trailer causing the switch to ignore the Trailer's data and process the frame normally after removing the Trailer from the frame.

When the CPU overrides all of the switch's Ingress policy, including priorities and Port Based VLANs among other functions, it sets the fields in the Trailer as shown in Figure 18 and defined in Table 11.

Figure 18: Ingress Trailer Format

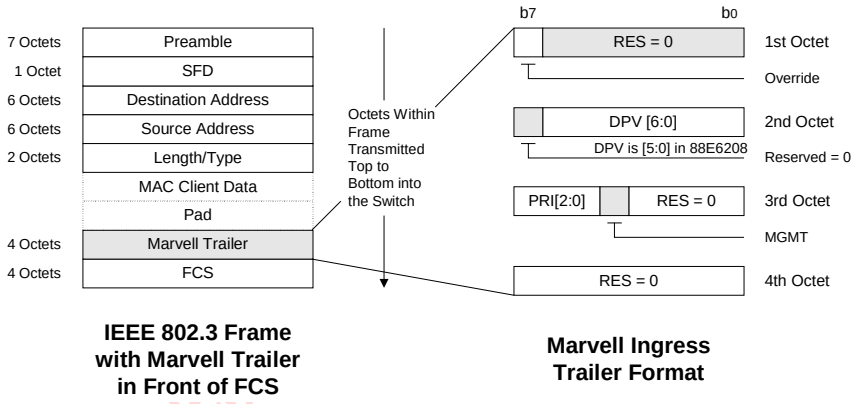


Table 11: Ingress Trailer Fields

Port State	Description
Override	When this bit is set to a one, the Trailer data is used to override the switch's operation. When this bit is cleared to a zero, the Trailer data is ignored.
DPV[6:0] (88E6218) DPV[5:0] (88E6208)	The Destination Port Vector. These bits indicate which port or ports the frame is to be sent to if the Override bit is set to a one. A DPV of all zeros discards the frame. Bit 0 is assigned to physical Port 0 and must be set to a one for this frame to egress from that port, bit 1 for Port 1, bit 2 for Port 2, etc.
PRI[2:0] (88E6218 only)	The frame's priority. PRI[2:1] indicate the frame's priority of the Override bit is set to a one. PRI[0] is reserved for future use and it is ignored in this device.
MGMT	The frame's management bit. When this bit is set to a one (along with the Override bit) indicates the frame is a MGMT frame and is allowed to Ingress and Egress through Blocked ports (section 1.6.4). Must be set on BPDU frames.
RES = 0	These fields are reserved for future use and are ignored in this device.

1.7 Queue Controller

The 88E6208/88E6218 device's queue controller uses an advanced non-blocking, four-priority (88E6218 only), output-port queue architecture with Resource Reservation. As a result, the 88E6208/88E6218 device supports definable frame latencies with guaranteed frame delivery (for high priority frames)—88E6218 only—without head-of-line blocking problems or non-blocked flow disturbances in any congested environment (for all frame priorities).

1.7.1 Frame Latencies (88E6218 only)

The 88E6218 device can guarantee frame latencies owing to its unique, high-performance, four-priority queuing system. A higher-priority frame is always the next frame to egress a port when lower priority. frames are currently egressing the port. This is true regardless of the two priorities of the frames and the Scheduling[1] mode of the switch.

1.7.2 No Head-of-Line Blocking

An output port that is slow or congested never affects the transmission of frames to ports that are not congested. The 88E6208/88E6218 device is designed to ensure that all flows that are not congested traverse the switch without degradation regardless of the congestion elsewhere in the switch

1.7.3 QoS with and without Flow Control (88E6218 only)

The Queue Controller is optimized for two modes of operation – with and without Flow Control. When Flow Control is enabled, no frames are dropped, and higher priority flows receive higher bandwidth through the switch. These flows are less constrained if there is congestion between a higher and a lower priority flow. The percentage of bandwidth they receive is determined by the Scheduling mode (section 1.7.5). Flow Control prevents frames from being dropped, but it can greatly impact the available bandwidth on any network segment that is subject to flow control. The latency of higher priority data on flow-constrained network segments also increases since industry standard flow control mechanisms stop all frames from being transmitted. Therefore, flow control may not be acceptable in a QoS switch environment. For this reason, the 88E6218 device is optimized to work properly without Flow Control.

When Flow Control is disabled and congestion occurs for an extended period of time, frames are dropped. This is true in all switches. The 88E6218 drops the correct frames, i.e., the lower priority frames. In this case, the higher priority flows get a higher percentage of the free buffers. The percentage of buffers they get is determined by the Scheduling mode (section 1.7.5).

1.7.4 Guaranteed Frame Delivery without Flow Control (88E6218 only)

The 88E6218 device can guarantee high-priority frame delivery[2], even with Flow Control disabled, owing to its intelligent Resource Reservation system. Having an output queue with multiple priorities is not a sufficient condition to support Quality of Service (QoS) when the higher priority frames cannot enter the switch owing to a lack of buffers. The 88E6218 device reserves buffers for higher priority frames so that they can be received and then switched. These high-priority buffers are replenished first from the Free Queue, which gets the switch ready for the next high priority frame.

1. The Scheduling mode selects either a Fixed priority or an 8-4-2-1 Weighted Fair Queuing - section 1.7.5.
2. If the frames entering a port are all of high priority at wire speed, their delivery cannot be guaranteed.

1.7.5 Fixed or Weighted Priority (88E6218 only)

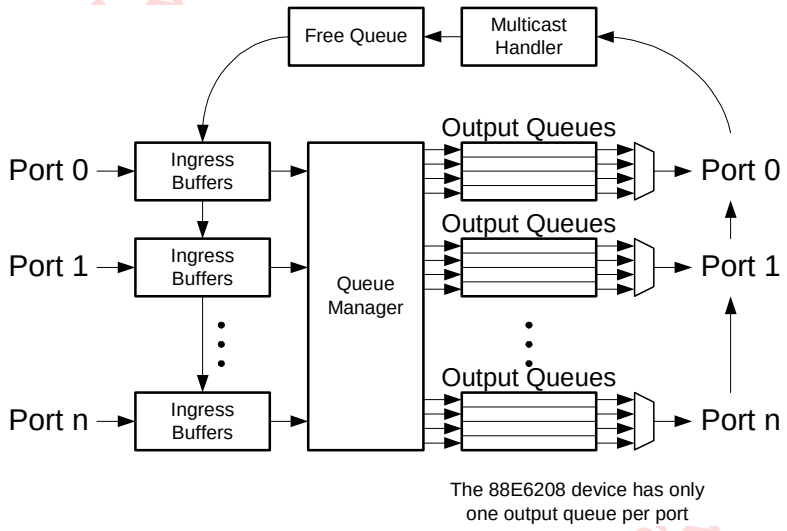
The 88E6208/88E6218 device supports either a fixed-priority or weighted fair-queuing scheme. The selection is made by the Scheduling bit in the Switch Global Control register (Table 36 on page 79).

In the fixed-priority scheme, all top-priority frames egress a port until that priority's queue is empty, then the next lower priority queue's frames egress. This approach can cause the lower priorities to be starved of opportunity for transmitting any frames but ensures all high priority frames egress the switch as soon as possible. In the weighted fair scheme, an 8, 4, 2, 1 weighting is applied to the four priorities. This approach prevents the lower priority frames from being starved of opportunity for transmission with only a slight delay to the higher priority frames.

1.7.6 The Queues

The queues in the 88E6208/88E6218 device are shown in Figure 19.

Figure 19: Switch Queues



1.7.7 Queue Manager

At reset[1], the Queue Manager initializes the Free Queue by setting all of the buffer pointers to point into it and ensuring that all of the other queues are empty. The Queue Manager then takes the first available free buffer pointers from the Free Queue and assigns them to any Ingress port that is not disabled[2] and whose link[3] is up. When these conditions are met, the switch is ready to accept and switch packets. Whenever any port's link goes down or the port is set to the Disabled Port State, the port's Ingress buffers and Output Queue buffers are immediately returned to the Free Queue. This feature prevents "stale buffers" or "lost buffers" conditions and maximizes the size of the Free Queue so that of momentary congestion can be handled. When an enabled port's link comes back up, the port gets its Ingress Buffers back and it can start receiving frames again.

1. The Queue Manager is reset either by toggling the hardware RESETn pin, a software reset by the SWReset bit, or by an ATUSize change (both in the ATU Control register – Table 37 on page 80).
2. When a port is in the Disabled Port State (section 3.5.3), its Ingress buffers are left in the Free Queue for other ports to use.
3. PHY based ports need to get a Link Up signal from the PHY. MII based ports have a link up state if they are enabled.

When a MAC receives a packet, it places it into the embedded memory at the address indicated by the input pointers that the MAC received from the Queue Manager. When packet reception is complete, the MAC transfers the pointers to the Queue Manager and requests new buffers from the Free Queue. When the Free Queue is empty, the MAC is not allocated any pointers until they become available. If the MAC starts to receive a packet when it has no pointers allocated, the packet is dropped. If flow control is enabled, it prevents this condition from occurring.

The Queue Manager uses the data returned from the Lookup Engine (section 1.5.1) and the Ingress Policy block (section 1.6) to determine to which output queues the packet's pointers should point and at what priority (88E6218 only). At this point, the Queue Manager modifies the required mapping of the frame, depending upon the mode of the switch and its level of congestion.

Two modes are supported, with and without Flow Control. Both modes are handled at the same time and can be different per port. One port can have Flow Control enabled, while another has it disabled.

When Flow Control is enabled on an ingress port, the frame is switched to the required output queue without modification. This operation is done so that frames are not dropped. The Queue Manager monitors which output queues are congested and enables or disables flow control on the ingress ports that are causing the congestion. This approach allows flows that are not congested to progress through the switch without degradation.

When Flow Control is disabled on an ingress port, the frame can be discarded instead of being switched to the required Output Queue. If a frame is destined for more than one output queue, it can be switched to some queues and not to others. The decisions are quite complex because the Queue Manager takes many pieces of information into account before the decision is made.

The Queue Manager monitors the priority of the current frame (88E6218 only), the current level of congestion in the output queues to which the frame is being switched, and the current number of free buffers in the Free Queue. As a result, uncongested flows traverse the switch unimpeded, and higher priority frames traverse the switch more quickly (88E6218 only) even when there is congestion elsewhere in the switch.

1.7.8 Output Queues

The Output Queues receive and transmit packets in the order received for any given priority. This is very important for some forms of Ethernet traffic. The Output Queues are emptied as fast as possible, but they can empty at different rates, possibly owing to a port's being configured for a slower speed, or because of network congestion (collisions or Flow Control).

Each 88E6208 port contains a single output queue. The frames are transmitted from the output port in the order in which they were placed in the output queue.

Each 88E6218 port contains four independent Output Queues, one for each priority. The order in which the frames are transmitted out of each port is controlled by the Scheduling bit in the Switch Global Control registers (Table 36 on page 79). A fixed or a weighted priority can be selected (see section 1.7.5).

After a packet has been completely transmitted to the MAC, the Output Queue passes the transmitted packet's pointers to the Multicast Handler for processing, after which the MAC begins transmitting the next packet.

1.7.9 Multicast Handler

The Multicast Handler receives the pointers from all of the packets that are transmitted. It looks up each pointer to determine whether each packet were directed to more than one output queue. If not, the pointer is returned to the Free Queue where it can be used again. When the frame is switched to multiple output queues, the Multicast Handler ensures that the frame has exited all of the ports to which it was switched before returning the pointers to the Free Queue.

1.8 Egress Policy

The Egress Policy block is used to modify frames, if so directed, as they exit the switch. IEEE Tags can be added or removed (88E6218 only) or specific switch information can be added to the frame for the switch's CPU.

1.8.1 Tagging and Untagging Frames (88E6218 only)

Each Egress port on the 88E6218 device can be independently configured to add or remove IEEE 802.3ac Tags by using the port's EgressMode bits (in the Port Control register – Table 26 on page 70) as follows:

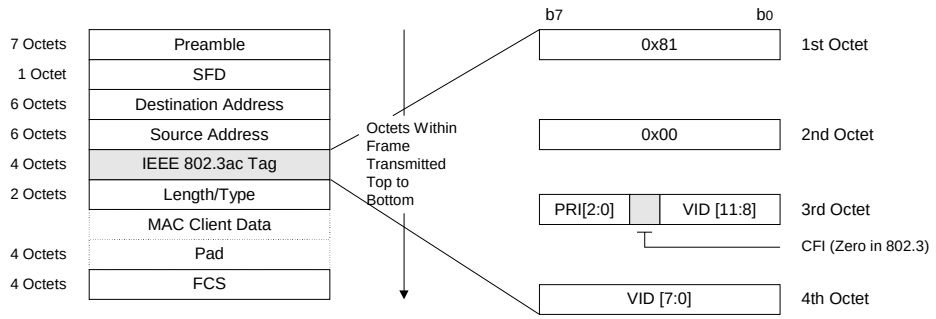
Table 12: Egress Port Configuration

Configuration	Result	
Leave the frames unmodified. This is the default setting so the switch acts as a transparent switch.	UnTagged frames egress the port UnTagged.	Tagged frames egress the port Tagged.
Transmit all frames UnTagged. Needed when switching frames to end stations that do not recognize Tags.	UnTagged frames egress the port unmodified.	The IEEE Tag on Tagged frames is removed, the frame is zero padded if needed, and a new CRC is computed for the frame.
Transmit all frames Tagged[1]. Typically used when switching frames into the core or up to a server.	An IEEE Tag is added to UnTagged frames and a new CRC is computed.	Tagged frames egress the port unmodified.
Transmit all frames Double Tagged.	See section 1.8.2	

1. Tagged frames egressing tagged can be forced to be modified to use the source port's Default (see section 3.5.2.4) and/or the source port's Default Priority (see section).

The format of an IEEE Tagged frame is shown in Figure 20.

Figure 20: IEEE Tag Frame Format



IEEE 802.3 Tagged Frame **Tag Format**

When a Tag is added to an UnTagged frame, the Tag is inserted after the frame's Source Address. The four bytes of added data are:

- The first octet is always 0x81.

- The second octet is always 0x00.
- PRI[2:1] indicate the Egress Priority Queue that the frame was switched through (section 1.7).
- The CFI bit is always set to a zero.
- PRI0 and VID come from the frame's source port's Default Port VLAN ID & Priority register (Table 28 on page 73). The frame's source port determines the Tag data so that when multiple ports are switching to one port, different Tags can be added.

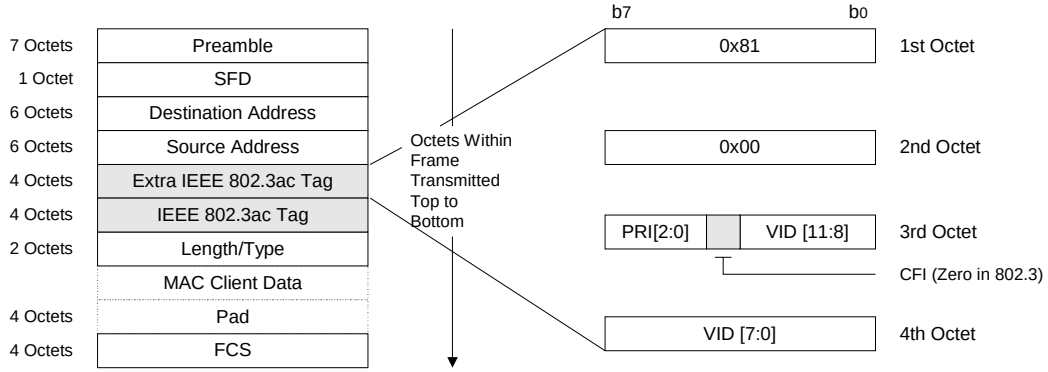
1.8.2 Egress Double VLAN Tagging (88E6218 only)

Double Tagging is a way to isolate one IEEE 802.1Q VLAN from other IEEE 802.1Q VLANs in a hierarchical fashion that is compatible with IEEE 802.1Q-aware switches as long as those switches support a maximum frame size of 1526 bytes or more. This method places an extra or Double Tag in front of a frame's normal Tag (assuming the frame were already Tagged) increasing the frame size by 4 bytes. The Double Tag frame format is shown in Figure 21.

Egress Double Tagging is selectable on a port-by-port basis by setting the port's EgressMode bits in its Port Control register (Table 26 on page 70). Typically, any port that has Egress Double Tagging enabled also has Ingress Double Tagging enabled (see section 1.6.5).

An Egress port that has Double Tagging enabled transmits all Egress frames with an extra Tag. When a frame is UnTagged, it egresses Tagged. If a frame is Tagged, it egresses Double Tagged. The extra or Double Tag is inserted just after the frame's Source Address. This new Tag becomes the frame's first Tag. The Frame's Tag data comes from the same sources as a normal tag insertion described in section 1.8.1.

Figure 21: Double Tag Format



1.8.3 Egress Rate Limiting (88E6218 only)

A switch design may need to limit the transmission rate of frames but still keep QoS. The 88E6218 device supports this capability on a per-port basis by setting bits in the port's Rate Control register (Table 29 on page 74). Egress rate limiting is performed by shaping the output load.

1. The type of frame that is to be limited must be determined. The 88E6218 device can limit all frames, or just multicast and flooded unicast frames (including broadcast frames), or just multicast frames (including broadcast), or just broadcast frames. MGMT (management[1]) frames can also be specifically excluded by clearing the port's LimitMGMT bit to a zero in the Rate Control register. Any frame that is not limited by the above rules is ignored in the rate calculations (i.e., its size is not counted toward the limit total).
2. The required maximum rate must be selected. The 88E6208/88E6218 device supports seven different rate limits from 128 Kbps to 8 Mbps. The selected rate will not be exceeded. Egress rate limiting can be disabled on this port by selecting the Not Limited option.
3. The bytes to count for limiting must be determined. The default setting is to include the frame's bytes from the beginning of the destination address (DA) field to the end of the frame check sequence (FCS) field. The frame's preamble bytes (the eight bytes prior to the DA) are included if the CountPre bit is set to a one in the port's Rate Control Register. The frame's minimum inter-frame gap (IFG, the 12 byte inter frame gap after the FCS) are included if the CountIFG bit is set to a one.

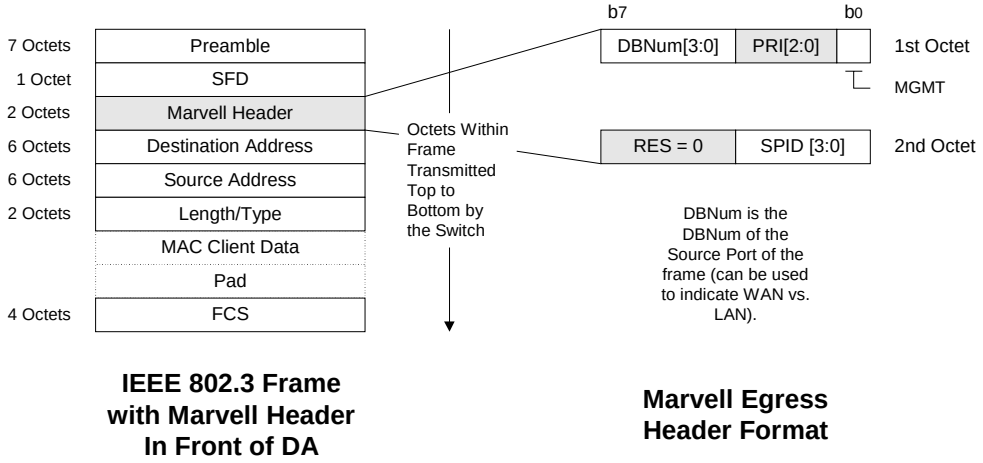
1.8.4 Switch's Egress Header

If a CPU must have the IP frame data of the Ethernet frame aligned to 32-bit boundaries for faster routing, the switch supports a Marvell Header that inserts two bytes into the frame just before the frame's Destination Address. Any po88E6218 device can be configured in this way by setting the Header bit in the port's Port Control register (see Table 26 on page 70). In practice, only the CPU's port should be configured in this way[2]. Only port 5, the CPU port, supports header mode in the 88E6208 device.

When the Egress-Header mode is enabled on a port, two extra bytes are added to the beginning of the frame just before the frame's DA and a new CRC is calculated for the frame. When the frame is received by the CPU its MAC removes the CRC so that Header occupies the first two bytes of the frame. If the CPU's MAC must process the frame for filtering or for other reasons, the MAC must be aware that the frame data has been shifted down by two bytes. The MAC inside the CPU block can be configured to support the Marvell Header (software needs to configure the CPU's MAC mode independently of the switch MAC mode).

The format of the Egress Header is shown in Figure 22 and its fields are defined in Table 13.

Figure 22: Egress Header Format



1. BPDU frames are MGMT frames (section 1.5.5.1 and 1.9).
2. The Header bit enables the Header mode for both ingress and egress.

Note

See UniMAC device description in Part 1 of this datasheet set.

Table 13: Egress Header Fields

Field	Description
DBNum[3:0]	Database Number. This field represents the address database assigned to this frame at ingress into the switch (i.e., it is assigned by the source port). DBNum can be used to indicate the port based VLAN number of the source port.
PRI[2:0]	The frame's priority in the 88E6218 device. PRI[2:1] indicate the frame's Egress Priority Queue the frame was switched through (section 1.7). PRI0 comes from the frame's source port's Default Port VLAN ID & Priority register (Table 28 on page 73). In the 88E6208, PRI[2:0] = 0x6.
MGMT	The frame management bit. When this bit is set to a one, it indicates that the frame is a MGMT frame which is allowed to ingress and egress through blocked ports (section 1.6.4).
RES	Reserved for future use. Currently set to 0x0.
SPID[3:0]	The Source Port ID. These bits indicate the physical port of entry of the frame. An SPID of all zeros indicates Port 0. An SPID of 0x1 indicates Port 1. 0x2 indicates Port 2, etc.

1.8.5 Switch's Egress Trailer

If a CPU needs to perform Spanning Tree or other bridge loop detection, the CPU must have information about the originating physical source ports of its received frames, since just those frames' SA information cannot be relied upon. To get this physical source port data, the CPU's port needs to be configured for Egress Trailer mode. Any port in the 88E6218 device can be configured in this way by setting the TrailerMode bit in the port's Port Control register (Table 26 on page 70), but only the CPU's port should be configured this way. In the 88E6208, only port 5, the CPU port, supports the egress trailer mode.

When the Egress Trailer mode is enabled on a port, four extra bytes are added to the end of the frame before the frame's CRC or FCS, and a new CRC is appended to the end of the frame. When the frame is received by the CPU, the MAC removes the CRC, so the Trailer occupies the last four bytes of the frame. The CPU's software can examine portions of the frame to determine if it needs the frame's source port information. Generally it is needed only on MGMT/Spanning Tree frames. If the information is not needed, the CPU reduces the frame size variable by four and passes the frame to the appropriate routines for processing. Removing the Trailer from a frame essentially a subtraction operation without the need to move any data. Consequently CPU overhead is kept to a minimum.

The format of the Egress Trailer is shown in Figure 23 and its fields are defined in Table 14.

Figure 23: Egress Trailer Format

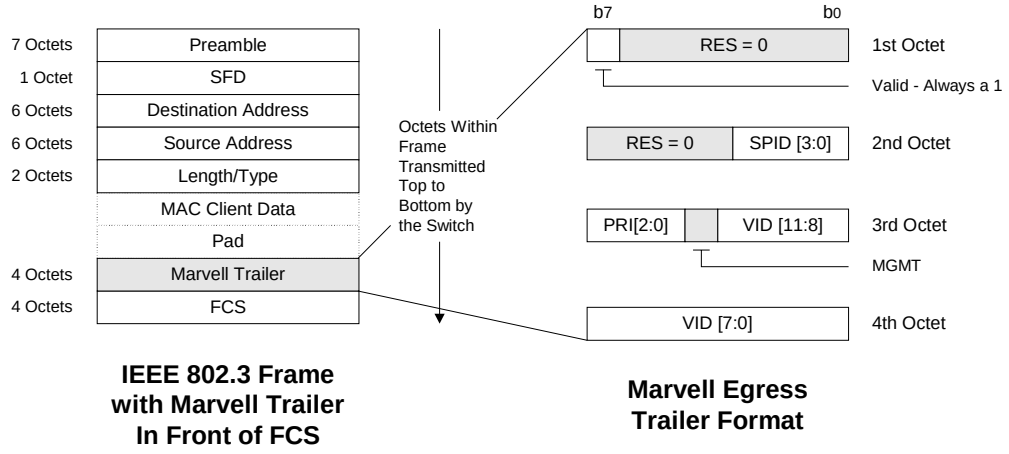


Table 14: Egress Trailer Fields

Field	Description
Valid	Always set to a one, indicating that Trailer data is present.
SPID[3:0]	Source Port ID. These bits indicate the physical port of entry of the frame. SPID[3:0] = 0 indicates Port 0. SPID[3:0] = 0x1 indicates Port 1, SPID[3:0] = 0x2 indicates Port 2, etc.
PRI[2:0]	The frame priority. in the 88E6218 device, PRI[2:1] indicate the frame's Egress Priority Queue that the frame was switched through (section 1.7). PRI[0] comes from the frame's source port Default Port VLAN ID & Priority register (Table 28 on page 73). In the 88E6208, PRI[2:0] = 0x6
MGMT	The frame management bit. When this bit is set to a one, it indicates that the frame is a MGMT frame which is allowed to ingress and egress through blocked ports (section 1.6.4).
VID[11:0]	The VID field, in the 88E6218 device, comes from the frame's source port Default Port VLAN ID & Priority register (Table 28 on page 73). In the 88E6208 device, VID[11:0] = 0x001.
RES = 0	These fields are reserved for future use and must be set to zeros.

1.9 Spanning Tree Support

IEEE 802.1D Spanning Tree is supported in the 88E6208/88E6218 device with the help of an external CPU that runs the Spanning Tree algorithm. The 88E6208/88E6218 device supports Spanning Tree by:

- Detection of Bridge Protocol Data Unit (BPDU) frames. These frames are called MGMT (management) frames in the 88E6208/88E6218 device. They are detected by loading the BPDU's multicast address (01:80:C2:00:00:00) into the address database with a MGMT Entry_State indicator (see section 1.5.5.1).
- Tunnelling of BPDU frames through Blocked ports. Blocked ports are controlled by the Port's PortState bits (section 3.5.3). When a port is in the Blocked state, all frames are discarded except for multicast frames with a DA that is contained in the address database with a MGMT indicator (see above).
- Redirection of BPDU frames. BPDU frames need to go to the CPU only, even though they are multicast frames. This is handled in the detection of BPDU frames above by mapping the BPDU's multicast address to the CPU port. (The value of the DPV bits when the address is loaded).
- Source Port information. The CPU needs information of the physical source port of origin of the BPDU frame. The source port is supplied in the frame's Egress Trailer that is sent to the CPU (section 1.8.5).
- CPU transmission of BPDU frames. The CPU needs to be able to transmit BPDU frames out of any physical port of the switch. This is supported in the Ingress Trailer data that is supplied by the CPU (section 1.6.8).

The 88E6208/88E6218 device can support 802.1D Spanning Tree, or it can be used to perform simpler bridge loop detection on new link up. These different options are accommodated by running appropriate software on the attached CPU.

Any vendor's proprietary protocol units can be handled with the same mechanism.

1.10 Embedded Memory

The 88E6218 device contains an embedded 1 Mb (16K x 64) Synchronous SRAM (SSRAM) that runs at 50 MHz, on a 64-bit wide data bus. The 88E6208 contains 1/2 Mb (8K x 64) of SRAM that also runs at 50 MHz. The memory interface provides up to 3.2 Gbps bandwidth for packet reception and transmission and address mapping of data accesses. This memory bandwidth is enough for all of the ports running at full wire speed in full-duplex mode with minimum size frames.

1.11 Interrupt Controller

The 88E6208/88E6218 device contains a switch Interrupt Controller that is used to merge various interrupts on to the CPU's interrupt signal—see the section on the CPU Interrupt Controller in part 2 of this datasheet set. Each switch interrupt can be individually masked by an enable bit contained in the Switch Global Control register (Table 36 on page 79). When an unmasked interrupt occurs and the interrupt pin goes active low, the CPU needs to read the Switch Global Status register (Table 32 on page 77) to determine the source of the interrupt. When the interrupt comes from the switch core (from ATUFull, ATUDone or EEInt), the switch's interrupt pin goes inactive after the Switch Global Status register is read. The interrupt status bits are cleared on read. If the interrupt comes from the PHY (PHYInt), then the switch's interrupt pin goes inactive only after the PHY's interrupt is cleared by reading the appropriate registers in the PHY. See section 3.2.1 for details.

Section 2. Physical Interface (PHY) Functional Description

The 88E6208/88E6218 device contains five IEEE 802.3 100BASE-TX and 10BASE-T compliant media-dependent interfaces for support of Ethernet over unshielded twisted pair (UTP) copper cable. DSP-based advanced mixed signal processing technology supports attachment of up 150 meters of CAT 5 cable to each of these interfaces. An optional, per port, automatic MDI/MDIX crossover detection function gives true “plug and play” capability without the need for confusing crossover cables or crossover ports.

The port 0 interface can be configured to support IEEE 802.3 100BASE-FX by utilizing a pseudo-ECL (PECL) interface for fiber-optics.

Figure 24: 88E6208/88E6218 Device Transmit Block Diagram

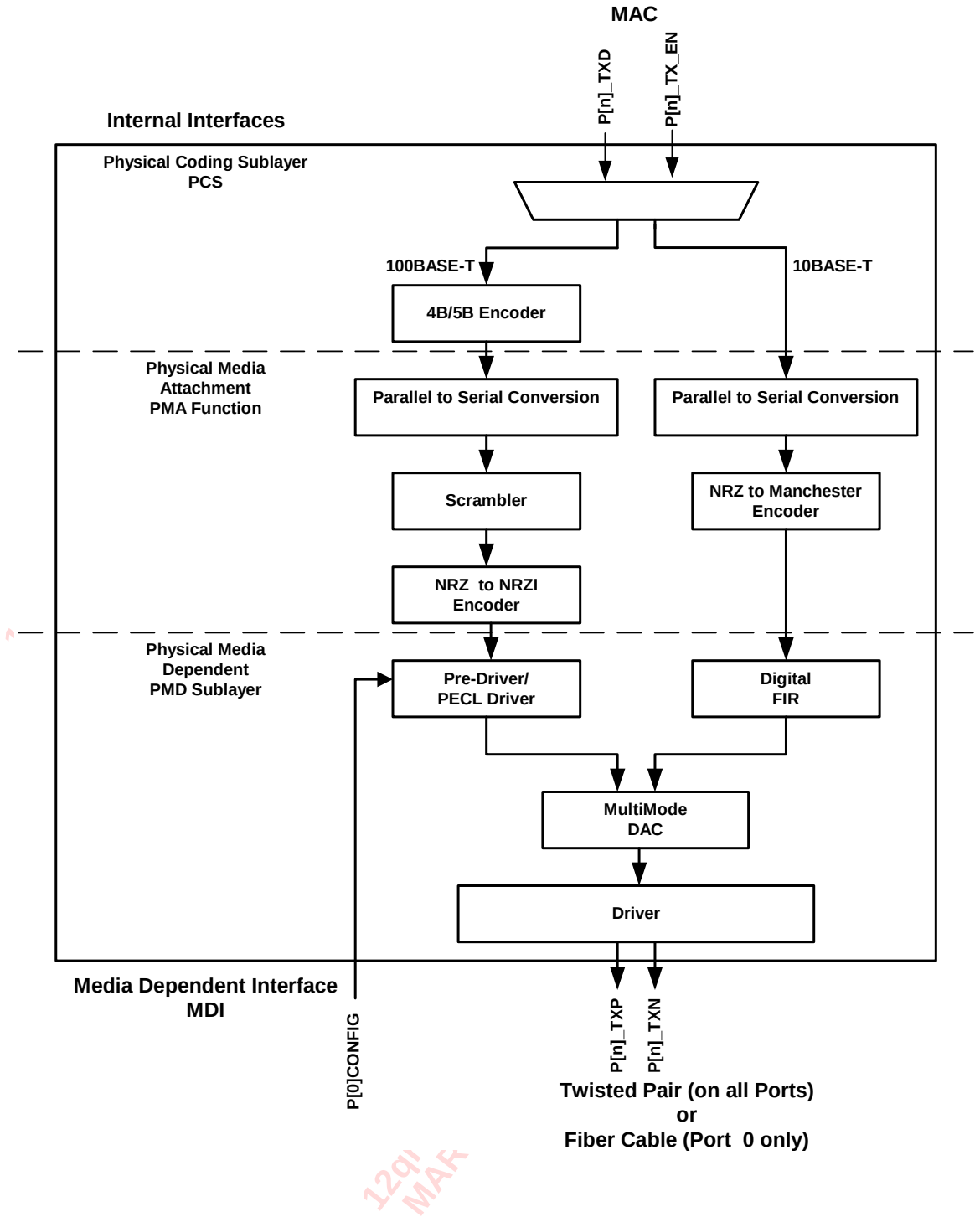
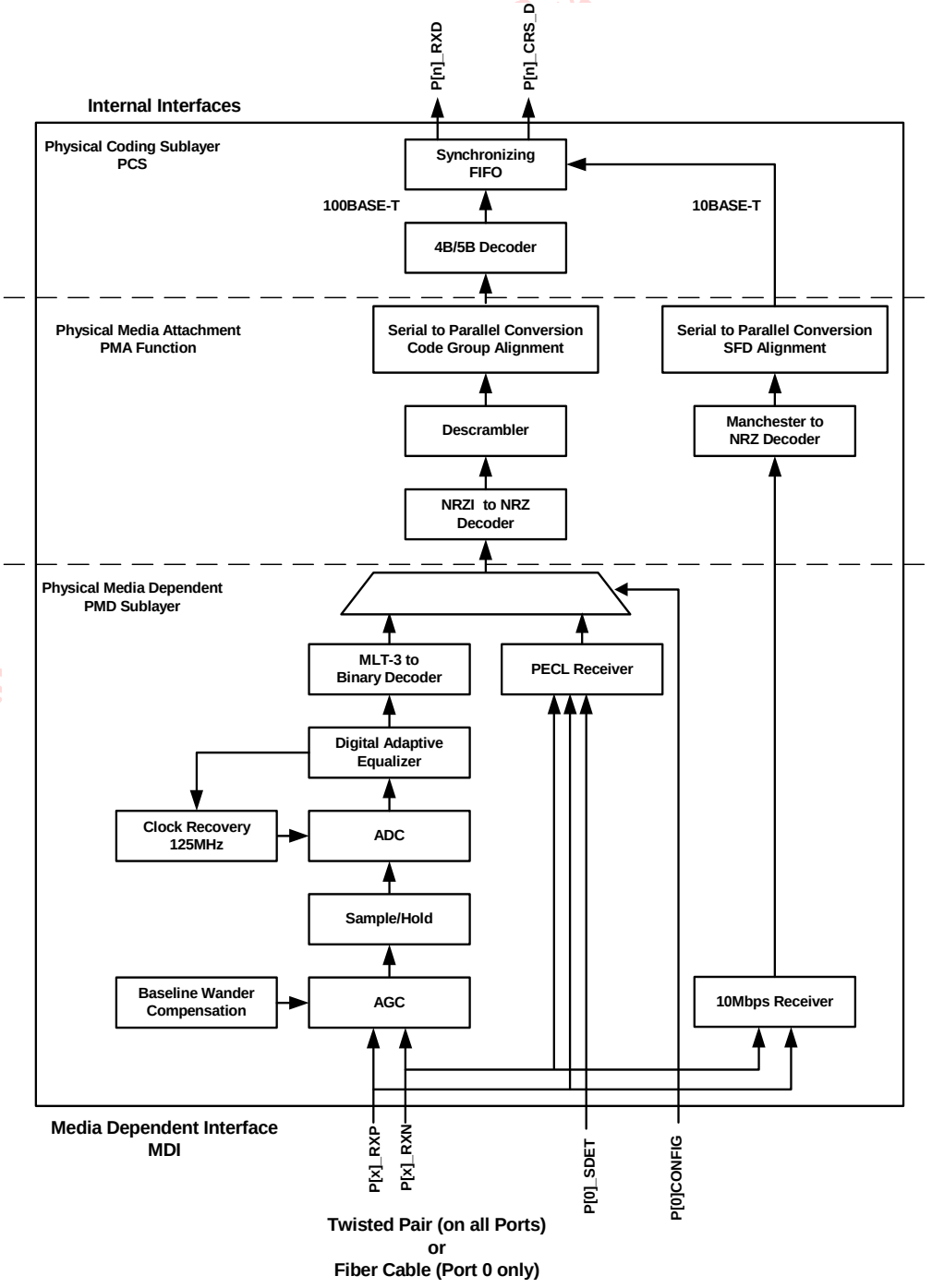


Figure 25: 88E6208/88E6218 Device Receive Block Diagram



2.1 Transmit PCS and PMA

2.1.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks that convert synchronous 4-bit nibble data to a scrambled MLT-3 125 Mbps serial data stream.

2.1.2 4B/5B Encoding

For 100BASE-TX mode, the 4-bit nibble is converted to a 5-bit symbol with /J/K/ start-of-stream delimiters and /T/R/ end-of-stream delimiters inserted as needed. The 5-bit symbol is then serialized and scrambled.

2.1.3 Scrambler

In 100BASE-TX mode, the transmit data stream is scrambled in order to reduce radiated emissions on the twisted pair cable. The data is scrambled by exclusive ORing the NRZ signal with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit repeating pseudo-random sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies.

Note

The enabling and disabling of the scrambler and the far end fault generator are controlled in the same way as for the descrambler detection and far end fault detection on the receive side.

2.1.4 NRZ to NRZI Conversion

The data stream is converted from NRZ to NRZI.

2.1.5 Pre-Driver and Transmit Clock

The 88E6208/88E6218 device uses an all-digital clock generator circuit to create the various receive and transmit clocks necessary for 100BASE-TX, 100BASE-FX, and 10BASE-T modes of operation.

For 100BASE-TX mode, the transmit data is converted to MLT3-coded symbols. The digital time base generator (TBG) produces the locked 125 MHz transmit clock.

For 100BASE-FX mode, NRZI data is presented directly to the multimode DAC.

For 10BASE-T mode, the transmit data is converted to Manchester encoding. The digital time base generator (TBG) produces the 10 MHz transmit reference clock as well as the over-sampling clock for 10BASE-T waveshaping.

2.1.6 Multimode Transmit DAC

The multimode transmit digital to analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode, NRZI symbols in 100BASE-FX mode, and Manchester-coded symbols in 10BASE-T mode. The transmit DAC utilizes a direct-drive current driver which is well balanced to produce very low common mode transmit noise.

In 100BASE-TX mode, the multimode transmit DAC performs slew control to minimize high frequency EMI.

In 100BASE-FX mode, the pseudo ECL level is generated through external resistive terminations.

In 10BASE-T mode, the multimode transmit DAC generates the needed pre-equalization waveform. This pre-equalization is achieved by using a digital FIR filter.

2.2 Receive PCS and PMA

2.2.1 10-BASE-T/100BASE-TX Receiver

The differential RXP and RXN pins are shared by the 100BASE-TX, 100BASE-FX (supported on Port 0), and 10BASE-T receivers.

The 100BASE-TX receiver consists of several functional blocks that convert the scrambled MLT-3 125 Mbps serial data stream to the synchronous 4-bit nibble data presented to the RMII interfaces.

2.2.2 AGC and Baseline Wander

In 100BASE-TX mode, after input to the AGC block, the signal is compensated for baseline wander by means of a digitally controlled Digital to Analog converter (DAC). It automatically removes the DC offset from the received signal before it reaches the input to the sample and hold stage of the ADC.

2.2.3 ADC and Digital Adaptive Equalizer

In 100BASE-T mode, an analog to digital converter (ADC) samples and quantizes the input analog signal and sends the result into the digital adaptive equalizer. This equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from the ADC output and uses a combination of feed-forward equalizer (FFE) and decision feedback equalizer (DFE) for the best optimized signal-to-noise (SNR) ratio.

2.2.4 Digital Phased Locked Loop (DPLL)

In 100BASE-TX mode, the receive clock is locked to the incoming data stream and extracts a 125 MHz reference clock. The input data stream is quantized by the recovered clock and sent through to the digital adaptive equalizer from each port.

Digital interpolator clock recovery circuits are optimized for MLT-3, NRZI, and Manchester modes. A digital approach makes the 88E6208/88E6218 receiver path robust in the presence of variations in process, temperature, on-chip noise, and supply voltage.

2.2.5 NRZI to NRZ Conversion

In 100BASE-TX mode, the recovered 100BASE-TX NRZI signal from the receiver is converted to NRZ data, descrambled, aligned, parallelized, and 5B/4B decoded.

2.2.6 Descrambler

The descrambler is initially enabled upon hardware reset if 100BASE-TX is selected. The scrambler can be enabled or disabled via software by setting the scrambler bit (Table 63 on page 100).

The descrambler “locks” to the descrambler state after detecting a sufficient number of consecutive idle code-groups. The receiver does not attempt to decode the data stream unless the descrambler is locked. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization.

The receiver descrambles the incoming data stream by exclusive ORing it with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence.

The descrambler is always forced into the “unlocked” state when a link failure condition is detected or when insufficient idle symbols are detected.

2.2.7 Serial-to-Parallel Conversion and 5B/4B Code-Group Alignment

The Serial-to-Parallel /Symbol Alignment block performs serial to parallel conversion and aligns 5B code-groups to a nibble boundary.

2.2.8 5B/4B Decoder

The 5B/4B decoder translates 5B code-groups into 4B nibbles to be presented to the MAC interfaces. The 5B/4B code mapping is shown in Table 6.

2.2.8.1 FIFO

The 100BASE-X or 10BASE-T packet is placed into the FIFO in order to correct for any clock mismatch between the recovered clock and the reference clock REFCLK.

2.2.8.2 100BASE-FX Receiver

In 100BASE-FX mode, a pseudo-ECL (PECL) receiver is used to decode the incoming NRZI signal passed to the NRZI-NRZ decoder. The NRZI signal from the receiver is converted to NRZ data, aligned, parallelized, and 5B/4B decoded as in the 100BASE-TX mode.

2.2.8.3 Far End Fault Indication (FEFI)

When 100BASE-FX is selected and Bit 0 of CONFIG8 is low at hardware reset, the far end fault detect (FEFD) circuit is enabled. The FEFD enable state can be overridden by programming the FEFI bit (Table 63 on page 100).

Note

The FEFI function is always disabled if 100BASE-TX is selected.

2.2.8.4 10BASE-T Receiver

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ and then aligned. The alignment is necessary to ensure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

In 10BASE-T mode, a receiver is used to decode the differential voltage offset of the Manchester data. Carrier sense is decoded by measuring the magnitude of the voltage offset.

In this mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ data. The data stream is converted from serial to parallel format and aligned. The alignment is necessary to ensure that the start of frame delimiter (SFD) is aligned to a byte or nibble boundary. For cable lengths greater than 100 meters, the incoming signal has more attenuation. Hence, the receive voltage threshold should be lowered via the ExtendedDistance bit in the PHY Specific Control Register (Table 63 on page 100)

Table 15: 5B/4B Code Mapping

PCS Code-Group [4:0] 4 3 2 1 0	Name	TXD/RXD <3:0> 3 2 1 0	Interpretation
1 1 1 1 0	0	0 0 0 0	Data 0
0 1 0 0 1	1	0 0 0 1	Data 1
1 0 1 0 0	2	0 0 1 0	Data 2
1 0 1 0 1	3	0 0 1 1	Data 3
0 1 0 1 0	4	0 1 0 0	Data 4
0 1 1 1 0	6	0 1 1 0	Data 6
0 1 1 1 1	7	0 1 1 1	Data 7
1 0 0 1 0	8	1 0 0 0	Data 8
1 0 0 1 1	9	1 0 0 1	Data 9
1 0 1 1 0	A	1 0 1 0	Data A
1 0 1 1 1	B	1 0 1 1	Data B
1 1 0 1 0	C	1 1 0 0	Data C
1 1 0 1 1	D	1 1 0 1	Data D
1 1 1 0 0	E	1 1 1 0	Data E
1 1 1 0 1	F	1 1 1 1	Data F
1 1 1 1 1	I	Undefined	IDLE; used as inter-stream fill code
1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
0 1 1 0 1	T	Undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
0 0 1 1 1	R	Undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
0 0 0 0 0	V	Undefined	Invalid code
0 0 0 0 1	V	Undefined	Invalid code
0 0 0 1 0	V	Undefined	Invalid code
0 0 0 1 1	V	Undefined	Invalid code
0 0 1 0 1	V	Undefined	Invalid code
0 0 1 1 0	V	Undefined	Invalid code
0 1 0 0 0	V	Undefined	Invalid code
0 1 1 0 0	V	Undefined	Invalid code
1 0 0 0 0	V	Undefined	Invalid code
1 1 0 0 1	V	Undefined	Invalid code

2.2.9 Setting Cable Characteristics

Since cable characteristics differ between unshielded twisted pair and shielded twisted pair cable, optimal receiver performance can be obtained in 100BASE-TX and 10BASE-T modes by setting the TPSelect bit in the PHY Specific Control Register (Table 63 on page 100) for cable type.

2.2.10 Scrambler/Descrambler

The scrambler block is initially enabled upon hardware reset if 100BASE-TX is selected. If 100BASE-FX or 10BASE-T is selected, the scrambler is disabled by default. The scrambler is controlled by programming the DisScrambler bit in the PHY Specific Control Register (Table 63 on page 100).

The scrambler setting is also controlled by hardware configuration at the end of hardware reset. Table 16 shows the effect of various configuration settings on the scrambler.

Table 16: Scrambler Settings

P[1:0]_CONFIG (If FX is selected)	Scramble Bit ()	Scrambler/ Descrambler
High	HW reset to 1	Disabled
Low	HW reset to 0	Enabled
X	User set to 1	Disabled
X	User set to 0	Enabled

2.2.11 Digital Clock Recovery/Generator

The 88E6208/88E6218 device uses an all-digital clock recovery and generator circuit to create all of the needed receive and transmit clocks. The digital time base generator (TBG) takes the 25 MHz or 50 MHz reference input clock (XTAL_IN) and produces the locked 25 MHz transmit clock for the MAC in 100BASE-TX mode. It produces a 2.5 MHz transmit clock for the MAC in 10BASE-T mode as well as producing the over-sample clock for 10BASE-T waveshaping

2.2.12 Link Monitor

The link monitor is responsible for determining whether link is established with a link partner.

In 10BASE-T mode, link monitor function is performed by detecting the presence of the valid link pulses on the RXP/N pins.

In 100BASE-TX mode, the link is established by scrambled idles

In 100BASE-FX mode, the external fiber-optic receiver performs the signal detection function and communicates this information with the 88E6208/88E6218 device through SDETP/N pins for Port 0.

If Force Link Good is asserted (ForceLink bit is set high - PHY Specific Control Register, Table 63 on page 100), the link is forced to be good, and the link monitor is bypassed. Pulse checking is disabled if Auto-Negotiation is disabled, and DisNLPCheck (PHY Specific Control Register, Table 63 on page 100) is set high. If Auto-Negotiation is disabled and DisNLPGen (PHY Specific Control Register, Table 63 on page 100) is set high, then the link pulse transmission is disabled.

2.2.13 Auto-Negotiation

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset
- Restart Auto-Negotiation
- Transition from power down to power up
- Change from the *linkfail* state to the *link-up* state

If Auto-Negotiation is enabled, the 88E6208/88E6218 device negotiates with its link partner to determine the speed and duplex mode at which to operate. If the link partner is unable to Auto-Negotiate, the 88E6208/88E6218 device goes into the parallel detect mode to determine the speed of the link partner. Under parallel detect mode, the duplex mode is fixed at half-duplex.

After hardware reset, Auto-Negotiation can be enabled and disabled via the AnegEn bit (PHY Control Register - Table 53 on page 91). When Auto-Negotiation is disabled, the speed and duplex can be changed via the SpeedLSB and Duplex bits (PHY Control Register - Table 53 on page 91), respectively. The abilities that are advertised can be changed via the Auto-Negotiation Advertisement Register (Table 57 on page 95).

2.2.14 Register Update

Changes to the AnegEn, SpeedLSB, and Duplex bits (Table 57 on page 95) do not take effect unless one of the following takes place:

- Software reset (SWReset bit - Table 57 on page 95)
- Restart Auto-Negotiation (RestartAneg bit - Table 57 on page 95)
- Transition from power down to power up (PwrDwn bit - Table 57 on page 95)
- Loss of the link

The Auto-Negotiation Advertisement register (Table 57 on page 95) is internally latched once every time Auto-Negotiation enters the *ability detect* state in the arbitration state machine. Hence, a write into the Auto-Negotiation Advertisement Register has no effect once the 88E6208/88E6218 device begins to transmit Fast Link Pulses (FLPs). This guarantees that a sequence of FLPs transmitted is consistent with one another.

The Next Page Transmit register (Table 61 on page 99) is internally latched once every time Auto-Negotiation enters the *next page exchange* state in the arbitration state machine.

2.2.15 Next Page Support

The 88E6208/88E6218 device supports the use of next page during Auto-Negotiation. By default, the received base page and next page are stored in the Link Partner Ability register - Base Page (Table 58 on page 97). The 88E6208/88E6218 device has an option to write the received next page into the Link Partner Next Page register - Table 62 on page 99 - (similar to the description provided in the IEEE 802.3ab standard) by programming the Reg8NxtPg bit (PHY Specific Control Register - Table 63 on page 100).

2.2.16 Status Registers

Once the 88E6208/88E6218 device completes Auto-Negotiation it updates the various status in the PHY Status (Table 64 on page 103), Link Partner Ability (Next Page) (Table 59 on page 97), and Auto-Negotiation Expansion (Table 60 on page 98) registers. Speed, duplex, page received, and Auto-Negotiation completed status are also

available in the PHY Specific Status (Table 64 on page 103) and PHY Interrupt Status registers (Table 66 on page 106).

2.3 Far End Fault Indication (FEFI)

Far-end fault indication provides a mechanism for transferring information from the local station to the link partner that a remote fault has occurred in 100BASE-FX (Port 0 only) mode.

A remote fault is an error in the link that one station can detect while the other one cannot. An example of this is a disconnected wire at a station's transmitter. This station is receiving valid data and detects that the link is good via the link monitor, but is not able to detect that its transmission is not propagating to the other station.

A 100BASE-FX station that detects this remote fault modifies its transmitted idle stream pattern from all ones to a group of 84 ones followed by one zero. This is referred to as the FEFI idle pattern.

The FEFI function is controlled by CONFIG_A connection and the DisFEFI bit (Table 63 on page 100).

Table 17 shows the various configuration settings affecting the FEFI function on hardware reset.

Table 17: FEFI Select

CONFIG_A Connection	LEDMode	FEFI	FEFI Bit ()
VSS	0	Disabled	HW reset to 1
P0_LED0	0	Enabled	HW reset to 0
P0_LED1	1	Disabled	HW reset to 1
P0_LED2	1	Enabled	HW reset to 0
P1_LED0	2	Disabled	HW reset to 1
P1_LED1	2	Enabled	HW reset to 0
P1_LED2	3	Disabled	HW reset to 1
VDDO	3	Enabled (default)	HW reset to 0
X	X	Disabled	User set to 1
X	X	Enabled	User set to 0

2.4 Virtual Cable Tester™

The 88E6208/88E6218 PHY Virtual Cable Tester™ feature uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatches, bad connectors, termination mismatches, and bad magnetics.

The 88E6208/88E6218 Switch Core conducts a cable diagnostic test by transmitting a signal of known amplitude (+1V) sequentially along each of the TX and RX pairs of an attached cable. The transmitted signal continues along the cable until it is reflected from a cable imperfection. The magnitude this echo signal and its return time are shown in the VCT registers (Table 72 on page 111 and Table 73 on page 112) on the AmpRfln and DistRfln bits respectively.

Using the information from these registers, the VCT registers (Table 72 on page 111 and Table 73 on page 112), the distance to the problem location and the type of problem can be determined. For example, the echo time can be converted to distance using Table 72 on page 111 and Figure 27 . The polarity and magnitude of the reflection together with the distance indicates the type of discontinuity. For example, a +1V reflection indicates an open close to the PHY and a -1V reflection indicates a short close to the PHY.

When the cable diagnostic feature is activated by setting the ENVCT bit to one (Table 72 on page 111), a pre-determined amount of time elapses before a test pulse is transmitted. This is to ensure that the link partner loses link, so that it stops sending100BASE-TX idles or 10 Mbit data packets. This is necessary to be able to perform the TDR test. The TDR test can be performed either when there is no link partner or when the link partner is Auto-Negotiating or sending 10 Mbit idle link pulses. If the 88E6208/88E6218 device receives a continuous signal for 125 ms, it declares a test failure because it cannot start the TDR test. In the test failure case, the received data is not valid. The results of the test are also summarized in the VCTTst bits (Table 72 on page 111 and Table 73 on page 112).

- 11 = Test fail (The TDR test could not be run for reasons explained above)
- 00 = valid test, normal cable (no short or open in cable)
- 10 = valid test, open in cable (Impedance > 333 ohms)
- 01 = valid test, short in cable (Impedance < 33 ohms)

The definition for shorts and opens is arbitrary and can be user-defined using the information in the VCT registers The impedance mismatch at the location of the discontinuity can also be calculated knowing the magnitude of the echo signal. Refer to the Application Note “Virtual Cable Tester -- How to use TDR results” for details.

2.4.1 Auto MDI/MDIX Crossover

The 88E6208/88E6218 device automatically determines whether or not it needs to interchange cable sense between pairs so that an external crossover cable is not required. If the 88E6208/88E6218 device interoperates with a device that cannot automatically correct for crossover, the 88E6208/88E6218 PHY makes the necessary adjustment prior to commencing Auto-Negotiation. If the 88E6208/88E6218 device interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 section 40.4.4 determines which device performs the crossover.

When the 88E6208/88E6218 device interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, it follows the same algorithm as described above since link pulses are present. However, when inter-operating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the 88E6208/88E6218 device uses signal detect to determine whether to implement crossover.

The Auto MDI/MDIX crossover function can be disabled via the AutoMDI[X] bits (Table 63 on page 100).

The 88E6208/88E6218 device is set to MDIX mode by default if auto MDI/MDIX crossover is disabled at hardware reset.

The pin mapping in MDI and MDIX modes is specified in Table 18.

Table 18: MDI/MDIX Pin Functions

Physical Pin	MDIX		MDI	
	100BASE-TX	10BASE-T	100BASE-TX	10BASE-T
TXP/TXN	Transmit	Transmit	Receive	Receive
RXP/RXN	Receive	Receive	Transmit	Transmit

2.5 LED Interface

The LED interface pins can either be controlled by a port's PHY or controlled directly, independently of the state of the PHY. Four display options are available and both interfaces (PHY or direct control) can be used together to provide even more LED combinations.

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Direct control is achieved by writing to the PHY Manual LED Override register (Table 71 on page 110). Any of the LEDs can be turned on, off, or made to blink at variable rates independent of the state of the PHY.

When the LEDs are controlled by a port's PHY, their activity is determined by the PHY's state. Each LED can be programmed to indicate various PHY states, with variable blink rate.

Some port PHY events configured to drive LED pins are too short to result in an observable change in LED state. For these events, pulse stretching is provided to translate a short PHY event into an observable LED response. The duration of a pulse stretch can be programmed via the PulseStretch bits (Table 70 on page 110). The default pulse stretch duration is set to 170 to 340 ms. The pulse stretch duration applies to all applicable LED interface pins.

Some of the status indicators signal multiple events by toggling LED interface pins resulting in a blinking LED. The blink period can be programmed via the BlinkRate bits (Table 70 on page 110). The default blink period is set to 84 ms. The blink rate is true for all applicable LEDs.

These LED interface pins can be used to display port status information. The LED interface has three different status indicators for each port with four different display options, using the Px_LED2, Px_LED1, and Px_LED0 pins.The LED Parallel Select Register (Table 69 on page 108) specifies which single LED mode status to display on the LED interface pins. The default display for each mode is shown in Table 19 and the default mode that applies depends upon the hardware configuration established using the CONFIG_A pin—see table "Switch PHY Configuration" in part 1 of the this datasheet set).

Table 19: Parallel LED Hardware Defaults

LED Mode —set by CONFIG_A at reset	P[4:0]_LED2	P[4:0]_LED1	P[4:0]_LED0
0	LINK	RX	TX
1	LINK	ACT	SPEED
2	LINK/RX	TX	SPEED
3	LINK/ACT	DUPLEX/COLX	SPEED

Table 69 on page 108 shows additional display modes that can be set up by software after startup. Table 20 includes these extra modes that cannot be set up by hardware configuration pins at reset.

Table 20: Parallel LED Display Interpretation

Status	Description
COLX	Low = collision activity High = no collision activity This status is pulse stretched to 170ms.
ERROR	Low = Jabber, received error, false carrier, or FIFO over/underflow occurred High = none of the above occurred This status is pulse stretched to 170ms.
DUPLEX	Low = full-duplex High = half-duplex
LINK	Low = link up High = link down
RX	Low = receive activity High = no receive activity This status is pulse stretched to 170ms.
TX	Low = transmit activity High = no transmit activity This status is pulse stretched to 170ms.
ACT	Low = transmit or received activity High = no transmit or receive activity This status is pulse stretched to 170ms.
SPEED	Low = speed is 100 Mb/s High = speed is 10 Mb/s
LINK/RX	Low = link up High = link down Blink = receive activity (blink rate is 84ms active then 84ms inactive) The receive activity is pulse stretched to 84ms.
LINK/ACT	Low = link up High = link downBlink = transmit or receive activity (blink rate is 84ms active then 84ms inactive) The transmit and receive activity is pulse stretched to 84ms
DUPLEX/COLX	Low = full-duplex High = half-duplex Blink = collision activity (blink rate is 84ms active then 84ms inactive) The collision activity is pulse stretched to 84ms.

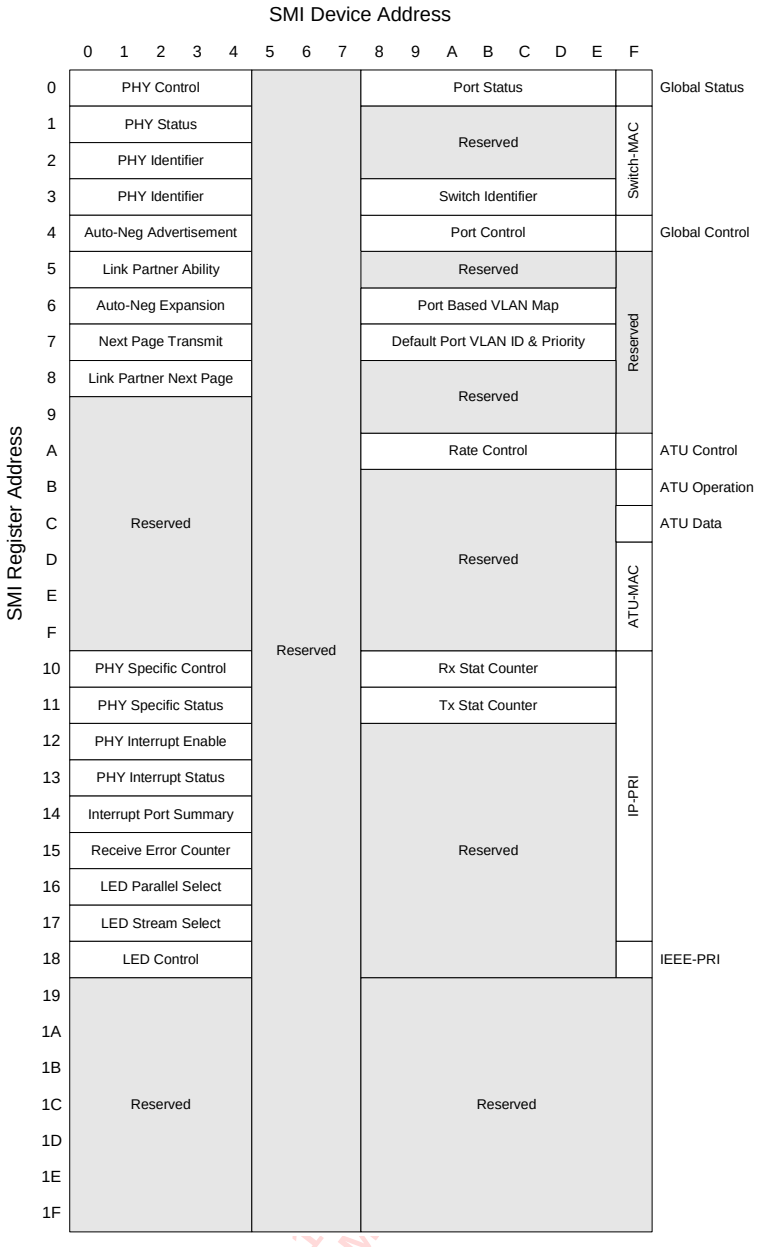
Table 21: LED Display Mode

Status	Description
DUPLEX/COLX	Low = full-duplex High = half-duplex Blink = collision activity (blink rate is 84ms active then 84ms inactive) The collision activity is pulse stretched to 84ms.
SPEED	Low = speed is 100 Mbps High = speed is 10 Mbps
LINK	Low = link up High = link down
TX	Low = transmit activity High = no transmit activity This status is pulse stretched to 170ms.
RX	Low = receive activity High = no receive activity This status is pulse stretched to 170ms.
ACT	Low = transmit or received activity High = no transmit or receive activity This status is pulse stretched to 170ms.
LINK/RX	Low = link up High = link down Blink = receive activity (blink rate is 84ms active then 84ms inactive) The receive activity is pulse stretched to 84ms.
LINK/ACT	Low = link up High = link down Blink = transmit or receive activity (blink rate is 84ms active then 84ms inactive) The transmit and receive activity is pulse stretched to 170ms.
ACT (Blink Mode)	Low = No activity High = activity Blink = transmit or receive activity (blink rate is 84ms active then 84ms inactive) The transmit and receive activity is pulse stretched to 170ms.

Section 3. Register Description

All of the 88E6208/88E6218 registers are accessible using the IEEE Serial Management Interface (SMI) used for PHY devices. The 88E6208/88E6218 uses 16 of the 32 possible Device Addresses. The16 Device Addresses are configurable at RESETn by use of the MA_[3] configuration pin (see Part 1 of the 88E6208/88E6218 datasheet). Figure 26 below shows the register map assuming the lower 16 SMI Device Addresses are being used.

Figure 26: 88E6208/88E6218 Register Map



3.1 Register Types

The registers in the 88E6208/88E6218 device are made up of one or more fields. The way in which each of these fields operate is defined by the field's Type. The function of each Type is described in Table 22.

Table 22: Register Types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to a one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or until a reset occurs.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only.
ROC	Read only clear. After read, register field is cleared to zero.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register is read, the register field is cleared to zero.
RWR	Read/Write reset. All bits are readable and writable. After reset the register field is cleared to zero.
RWS	Read/Write set. All bits are readable and writable. After reset the register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the required function to be immediately executed, then the register field is cleared to zero when the function is complete.
Update	Value written to the register field does not take effect until a soft reset is executed.
WO	Write only. Reads to this type of register field return undefined data.

3.2 Switch Core Registers

Switch Core Registers are of two types:

- Switch Port Registers—are separately configured for each port comprised in the switch. Each port has a unique associated SMI device address and this address is used to access that port's switch register set.
- Switch Global Registers—are configured using a single SMI device address. A global register's setting affects all ports of the switch.

The 88E6208 device contains six ports (MACS). The supported ports are accessible using SMI device addresses 0x08 to 0x0D, or 0x18 to 0x1D depending upon the value of the M_A[3] pin at reset (See the Table: "Reset Configuration," in part 1 of this datasheet).

The 88E6218 device contains seven ports (MACS). The supported ports are accessible using SMI device addresses 0x08 to 0x0E, or 0x18 to 0x1E depending upon the value of the M_A[3] pin at reset (See the Table: "Reset Configuration," in part 1 of the device datasheet).

The switch contains many global registers that are used to control features and functions that are common to all ports in the switch. The global registers are accessible using SMI device address 0x0F or 0x1F depending upon

the value of the M_A[3] pin at reset (See the Table: “Reset Configuration,” in part 1 of the 88E6208/88E6218 datasheet)

Note

See the Table: “Reset Configuration,” in part 1 of the 88E6208/88E6218 datasheet set.

3.2.1 Switch Core Register Map

Table 23: Switch Core Register Map

Description	Offset Hex	Offset Decimal	Page Number
Switch Port Registers (SMI Device Address			
Port Status Register	0x00	0	page 68
Reserved Registers	0x01 - 0x02	1 - 2	page 69
Switch Identifier Register	0x03	3	page 69
Port Control Register	0x04	4	page 70
Reserved Registers	0x05	5	page 71
Port Based VLAN Map	0x06	6	page 72
Default Port VLAN ID & Priority (88E6218 device only)	0x07	7	page 73
Reserved Registers	0x08 - 0x09	8 - 9	page 73
Rate Control (88E6218 device only)	0x0A	10	page 74
Reserved Registers	0x0C - 0x0F	11 - 15	page 75
Rx Counter	0x10	16	page 76
Tx Counter	0x11	17	page 76
Reserved Registers	0x12 - 0x1F	18 - 31	page 76
Switch Global Registers			
Switch Global Status Register	0x00	0	page 77
Switch MAC Address Register Bytes 0 & 1	0x01	1	page 78
Switch MAC Address Register Bytes 2 & 3	0x02	2	page 78
Switch MAC Address Register Bytes 4 & 5	0x03	3	page 78
Switch Global Control Register	0x04	4	page 79
Reserved Registers	0x05 - 0x09	5 - 9	page 79
ATU Control Register	0x0A	10	page 80

Table 23: Switch Core Register Map (Continued)

Description	Offset Hex	Offset Decimal	Page Number
ATU Operation Register	0x0B	11	page 81
ATU Data Register	0x0C	12	page 82
ATU MAC Address Register Bytes 0 & 1	0x0D	13	page 82
ATU Switch MAC Address Register Bytes 2 & 3	0x0E	14	page 82
ATU Switch MAC Address Register Bytes 4 & 5	0x0F	15	page 83
IP-PRI Mapping Register 0 (88E6218 device only)	0x10	16	page 84
IP-PRI Mapping Register 1	0x11	17	page 84
IP-PRI Mapping Register 2	0x12	18	page 85
IP-PRI Mapping Register 3	0x13	19	page 85
IP-PRI Mapping Register 4	0x14	20	page 86
IP-PRI Mapping Register 5	0x15	21	page 86
IP-PRI Mapping Register 6	0x16	22	page 87
IP-PRI Mapping Register 7	0x17	23	page 87
IEEE-PRI Register	0x18	24	page 88
Reserved Registers	0x19 - 0x1F	25 - 31	page 88

3.2.2 Switch Port Registers

Table 24: Port Status Register
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Type	Description
15	LinkPause	RO	Link Partner's Pause bit, returned from the link partner through Auto-Negotiation. This bit is valid for Ports 0 to 4 only and when the Resolved bit is set to a one. 0 = MAC Pause not implemented in the link partner 1 = MAC Pause is implemented in the link partner
14	MyPause	RO	My Pause bit, sent to the link partner during Auto-Negotiation. This bit is valid for Ports 0 to 4 only. It is set high if FD_FLOW_DIS is low during RESETn.(See the Table: "Reset Configuration," in part 1 of the 88E6208/88E6218 datasheet) 0 = MAC Pause not implemented in the link partner 1 = MAC Pause is implemented in the link partner
13	Resolved	RO	Link Mode is resolved. 0 = Link is undergoing Auto-Negotiation or the port is disabled 1 = Link has determined its Speed, Duplex and LinkPause settings
12	Link	RO	Link Status in real time (i.e., it is not latched). 0 = Link is down 1 = Link is up
11	PortMode	RO	Port mode. 0 = SNI mode or MII 200 mode is enabled 1 = MII 10/100 mode is enabled
10	PHYMode	RO	PHY mode. This bit is valid for all ports but it is meaningful for Port 5 and Port 6 only and only when the PortMode (bit 11 above) indicates an MII mode of operation (i.e., PortMode is a one). This bit may be either value for SNI configured ports – but all SNI port configurations are PHY mode. The value of this bit is always zero for Ports 0 to 4 and it comes from Px_MODE2 during configuration and Port 6. Port 5 is always in PHY mode. 0 = Pins are in MII MAC Mode (i.e., INCLK and OUTCLK are inputs) 1 = Pins are in MII PHY Mode (i.e., INCLK and OUTCLK are output) **Note:** Port 6 is available on the 88E6218 only.
9	Duplex	RO	Duplex mode. This bit is valid when the Resolved bit is set to a one. 0 = Half-duplex 1 = Full-duplex
8	Speed	RO	Speed mode. This bit is valid when the Resolved bit, above, is set to a one and the PortMode (bit 11 above) is also a one. If the PortMode bit is a zero then the port's speed is 10 Mbps unless both this bit and the Duplex (bit 9 above) are both ones, then the speed is 200 Mbps. When the port is configured in MII MAC mode, the Speed bit is undefined. 0 = 10 Mbps 1 = 100 Mbps **Note:** 200 Mbps is available on the 88E6218 only.

Table 24: Port Status Register (Continued)
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Type	Description
7:0	Reserved	RES	Reserved for future use.

The PortMode, PHYMode, Duplex, and Speed bits for Port 5 come from the M_A[22:21] pins at reset. For Port 6 they come from the Px_MODE[3:0] pins at Reset. When the PortMode is a one, the PHYMode, Duplex, and Speed bits map the same as the other 10/100 ports that contain PHYs. When the PortMode is a zero the mapping is easier to see by looking at the section: “Reset and initialization” in part 1 of the 88E6208/88E6218 datasheet set.

Note

Registers 0x01 and 0x02 (Hex), or 1 and 2 (Decimal) are reserved.

Table 25: Switch Identifier Register
Offset: 0x03 (Hex), or 3 (Decimal)

Bits	Field	Type	Description
15:4	DeviceID	RO	Device Identifier. The 88E6208 device is identified by the value 0xF91. The 88E6218 device is identified by the value 0xF93.
3:0	RevID	RO	Revision Identifier. The initial version of the 88E6208/88E6218 device has a RevID of 0x0. This RevID field may change at any time. Contact a Marvell FAE for current information on the device revision identifier.

Table 26: Port Control Register
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Type	Description
15	ForceFlow Control	RWR	Force Flow Control. This bit is used to enable full-duplex flow control or half-duplex back pressure on this port depending upon the port's current duplex. This bit can only be changed when the port is Disabled. 0 = Use configuration pin settings for flow control/back pressure 1 = Force flow control/back pressure to be enabled on this port
14	Trailer	RWR	Egress Trailer Mode 0 = Normal mode – frames are transmitted unmodified. 1 = Add a Trailer to all frames transmitted out the port.
13:12	Egress Mode (88E6218 only)	RWR	Egress Mode. 00 = Normal mode – frames are transmitted unmodified 01 = Transmit all frames Untagged – remove the tag from any tagged frame 10 = Transmit all frames Tagged—add a tag to any untagged frame 11 = Always add a Tag (or Egress Double Tag).
11	Header	RWR	Ingress & Egress Header Mode. When this bit is set to a one all frames Egressing out this port are pre-pended with the Marvell 2 byte Egress Header just before the frame's DA field. Also, all frames Ingressing into this port are expected to be pre-pended with the Marvell 2 byte Ingress Header just before the frame's DA field. On Ingress the 1st 2 bytes after the SFD are removed from the frame and the frame's CRC and size is recomputed. If the frame's Ingress Header is non-zero it is used to update the port's VLAN Map register value (Table 27 on page 72).
10	Reserved	RES	Reserved for future use.
9:8	Ingress Mode	RWR	Ingress Mode: 00 = Normal mode—frames are received unmodified 01 = Ingress Trailer mode—frames must be received with a Trailer and the Trailer is checked, potentially used and then removed from the frame. Trailer mode is intended for Ingress data control from a management CPU port so that BPDU frames can be directed. 10 = Remove IEEE 802.3ac tag if one is present (or Ingress Double Tag)—88E6218 device only. 1x = Reserved for future use
7	VLAN Tunnel	RWR	VLAN Tunnel. When this bit is cleared to a zero, the VLANs defined in the VLANTable (Table 27, on page 72) are enforced for ALL frames. When this bit is set to a one, the VLANTable masking is bypassed for any frame entering this port with a DA that is currently 'locked' in the ATU. This includes unicast as well as multicast frames.
6	TagIfBoth (88E6218 only)	RWS	Use IEEE 802.1p tag fields over IP fields. If the current frame is both IEEE 802.3ac tagged and an IPv4 or an IPv6 frame, and UseIP and UseTag bits below are both enabled, then a priority selection between the two needs to be made. 0 = Use IP fields for priority mapping when both field types are present 1 = Use Tag fields for priority mapping when both field types are present

Table 26: Port Control Register (Continued)
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Type	Description
5	UseIP (88E6218 only)	RWS	Use IP for Priority. Use IPv4 TOS and/or DiffServ fields and/or IPv6 Traffic Class fields, if present, for priority mapping. 0 = Ignore IPv4 and IPv6 priority fields 1 = Use IPv4 fields when the frame is IPv4, and use IPv6 fields when the frame is IPv6 for priority mapping.
4	UseTag (88E6218 only)	RWS	Use IEEE Tags. Use IEEE 802.1p Traffic Class field for priority mapping when the frame is an IEEE 802.3ac tagged frame. 0 = Ignore IEEE 802.1p tag fields even it the frame is tagged 1 = Use IEEE 802.1p tag Traffic Class for priority mapping if the frame is tagged
3:2	Reserved	RES	Reserved for future use.
1:0	PortState	RWR Or RWS to 0b11	Port State. These bits are used to manage a port to determine what kind of frames, if any, are allowed to enter or leave. The state of these bits can be changed at any time without disrupting frames currently in transit. The Port States are: 00 = Disabled. The switch port is completely disabled and it will not receive or transmit any frames. 01 = Blocking/Listening. The switch will examine all frames without learning any SA addresses, and discard all but MGMT frames. MGMT (management) frames are the only kind of frame that can be tunneled through Blocked ports. A MGMT frame is any frame whose multicast DA address appears in the ATU Database with the MGMT Entry State. It will allow MGMT frames only to exit the port. This mode is used for BPDU handling for bridge loop detection and Spanning Tree support. 10 = Learning. The switch will examine all frames, learning all SA addresses, and still discard all but MGMT frames. It will allow MGMT frames only to exit the port. 11 = Forwarding. The switch will examine all frames, learning all SA addresses, and receive and transmit all frames like a normal switch. The PortState bits for all ports come up in the Disabled state unless the M_A[0] pins is set to 0, the switch test mode. This mode must only be used for test, not for production.

Note

Register 0x05 (Hex), or 5 (Decimal) is reserved.

Table 27: Port Based VLAN Map
Offset: 0x06 (Hex), or 6 (Decimal)

Bits	Field	Type/ Reset Value	Description
15:12	DBNum	RWR	Port's Default DataBase VLAN Number. This field can be used with to create address databases. This allows the same MAC address to appear multiple times in the address database (at most one time per DBNum) with a different port mapping per entry. This field is should be zero if not being used. It needs to be a unique number for each independent database used. Ports with the same DBNum share the same address database.
11:7	Reserved	RES	Reserved for future use.
6:0	VLANTable	RWS to all ones except for this port's bit	Port based VLAN Table. The bits in this table are used to restrict which output ports this input port can send frames to. To send frames to Port 0, bit 0 of this register must be a one. To send frames to Port 1, bit 1 of this register must be a one, etc. After Reset, all ports are accessible since all the other port number bits are set to a one. This Port's bit will always be zero after Reset. This prevents frames going out the port they came in on. The 88E6208/88E6218 device allows this Port's bit to be set to a one allowing frames to be switched back to the port they came in on. This register is reset to 0x7E for Port 0 (SMI Device Address 0x8), and it resets to 0x7D for Port 1 (Addr 0x9) and to 0x7B for Port 2 (Addr 0xA), to 0x77 for Port3 (Addr 0xB), etc.

Table 28: Default Port VLAN ID & Priority (88E6218 only)
Offset: 0x07 (Hex), or 7 (Decimal)

Bits	Field	Type/ Reset Value	Description
15:14	DefPri	RWR	Default Priority. The bits of this register are used as the default Ingress priority to use when no other priority information is available (either the frame is not IEEE Tagged, nor is it an IPv4 nor an IPv6 frame – or the frame is a priority type that is currently disabled (see UseIP and UseTag in Table 26, on page 70). The Ingress priority determines the Egress Queue the frame is switched into.
13	TagPriLSB	RWR	Tag Priority Least Significant Bit. This bit is used as the lower bit of the IEEE Tagged PRI added during egress to untagged frames that ingressed this port. The upper two bits of the IEEE Tagged PRI added to untagged frames come from the Egress Queue into which the frame was switched.
12	Force Default-VID	RWR	Force to use Default VID. When this bit is set to a one all Ingress frames with IEEE802.ac Tags are treated as if the Tag's VID contains a value of 0x000 (i.e., it is a priority tagged frame). In this case, the frame's VID is ignored and the DefaultVID below is used and replaced into the frame. When this bit is cleared to a zero all IEEE 802.3ac Tagged frames with a non-zero VID use the frame's VID unmodified.
11:0	DefaultVID	RWS to 0x001	VLAN Identifier. The VID field is used as the IEEE Tagged VID added during egress to untagged frames that arrived at this port.

Note

Registers 0x08 and 0x09 (Hex), or 8 and 9 (Decimal) are reserved.

Table 29: Rate Control (88E6218 only)
Offset: 0x0A (Hex), or 10 (Decimal)

Bits	Field	Type	Description
15:14	Limit Mode	RWR	Ingress Limit Mode. These bits determine what kinds of frames are limited and counted against Ingress limiting as follows: 00 = Limit and count all frames 01 = Limit and count Broadcast, Multicast and flooded unicast frames 10 = Limit and count Broadcast and Multicast frames only 11 = Limit and count Broadcast frames only If a frame is not limited by the above setting its size is not counted against the limit for the other frames.
13	Pri3Rate	RWR	Ingress data rate limit for priority-3 frames. Priority 3 frames are discarded after the ingress rate selected below is reached or exceeded: 0 = Use the same rate as Pri2Rate 1 = Use twice the rate as Pri2Rate (i.e., it can be up to 64 Mbps)
12	Pri2Rate	RWR	Ingress data rate limit for priority-2 frames. Priority 2 frames are discarded after the ingress rate selected below is reached or exceeded: 0 = Use the same rate as Pri1Rate 1 = Use twice the rate as Pri1Rate (i.e., it can be up to 32 Mbps)
11	Pri1Rate	RWR	Ingress data rate limit for priority 1 frames. Priority 1 frames are discarded after the ingress rate selected below is reached or exceeded: 0 = Use the same rate as Pri0Rate 1 = Use twice the rate as Pri0Rate (i.e., it can be up to 16 Mbps)
10:8	Pri0Rate	RWR	Ingress data rate limit for priority 0 frames. Priority 0 frames are discarded after the ingress rate selected below is reached or exceeded: 000 = Not Limited = Default 001 = 128 Kbps 010 = 256 Kbps 011 = 512 Kbps 100 = 1 Mbps 101 = 2 Mbps 110 = 4 Mbps 111 = 8 Mbps
7	Reserved	RES	Reserved for future use
6	Limit MGMT	RWR	Limit and count MGMT frame bytes. When this bit is set to a one MGMT frames are included in ingress and egress rate limiting calculations and can be limited. When this bit is cleared to a zero, MGMT bytes are not counted and are not limited
5	Count IFG	RWS	Count IFG bytes. When this bit is set to a one each frame's minimum inter frame gap (IFG) bytes (12 per frame) are included in ingress and egress rate limiting calculations. When this bit is cleared to a zero, IFG bytes are not counted.

Table 29: Rate Control (88E6218 only) (Continued)
Offset: 0x0A (Hex), or 10 (Decimal)

Bits	Field	Type	Description
4	Count Pre	RWS	Count Preamble bytes. When this bit is set to a one each frame's preamble bytes (8 per frame) are included in ingress and egress rate limiting calculations. When this bit is cleared to a zero, preamble bytes are not counted.
3	Reserved	RES	Reserved for future use
2:0	Egress Rate	RWR	Egress data rate limit. The EgressRate bits modify this port's effective transmission rate as follows: 000 = Not Limited = Default 001 = 128 Kbps 010 = 256 Kbps 011 = 512 Kbps 100 = 1 Mbps 101 = 2 Mbps 110 = 4 Mbps 111 = 8 Mbps

Note

Registers 0x0C - 0x0F (Hex), or 12 - 15 (Decimal) are reserved.

Table 30: Rx Counter
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Type/ Reset Value	Description
15:0	RxCtr	RO	Received Counter. When CtrMode is cleared to a zero (Global Control – Table 36, on page 79) this counter increments each time a good frame enters this port. It does not matter if the frame is switched or discarded by the switch. When CtrMode is set to a one this counter increments each time an error frame enters this port. An error frame is one that is 64 bytes or greater with a bad CRC (including alignment errors but not dribbles). Fragments and properly formed frames are not counted. The counter wraps back to zero. The only time this counter does not increment is when this port is Disabled (see PortState, Table 26, on page 70). This register can be cleared by changing the state of the CtrMode bit in the Switch Global Control register (Table 36, on page 79).

Table 31: Tx Counter
Offset: 0x11 (Hex), or 17 (Decimal)

Bits	Field	Type/ Reset Value	Description
15:0	TxCtr	RO	Transmit Counter. When CtrMode is cleared to a zero (see Global Control – Table 36, on page 79) this counter increments each time a frame successfully exits this port. When CtrMode is set to a one this counter increments each time a collision occurs during an attempted transmission. It no longer counts all transmitted frames – but only those transmission attempts that resulted in a collision. The counter wraps back to zero. The only time this counter does not increment is when this port is Disabled (see PortState, Table 26, on page 70). This register can be cleared by changing the state of the CtrMode bit in Global Control (Table 36, on page 79).

Note

Registers 0x12 - 0x1F (Hex), or 18 - 31 (Decimal) are reserved.

3.2.3 Switch Global Registers

Table 32: Switch Global Status Register
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Type	Description
15:12	Reserved	RES	Reserved for future use.
11	ATU Ready	RO	Address Translation Unit Ready. This bit is set to a one when the Address Translation Unit is done with its initialization and it is ready to learn and translate addresses.
10	QC Ready	RO	Queue Controller Ready. This bit is set to a one when the Queue Controller is done with its initialization and it is ready to accept frames.
9:4	Reserved	RES	Reserved for future use.
3	ATUFull	RO, LH, SC	ATU Full Interrupt. This bit is set to a one if the ATU cannot load or learn a new mapping due to all the available locations for an address being locked. It is automatically cleared when read. This bit being high will cause the 88E6208/88E6218 INTn pin to go low if the ATUFullIntEn bit in GlobalControl (Table 36, on page 79) is set to a one.
2	ATUDone	RO, LH, SC	ATU Done Interrupt. This bit is set to a one whenever the ATUBusy bit (Table 38, on page 81) transitions from a one to a zero. It is automatically cleared when read. This bit's being high causes the 88E6208/88E6218 INTn pin to go low if the ATUDoneIntEn bit in Global Control (Table 36, on page 79) is set to a one.
1	PHYInt	RO	PHY Interrupt. This bit is set to a one when the PHYs interrupt logic has at least one active interrupt. This bit being high causes the 88E6208/88E6218 INTn pin to go low if the PHYIntEn bit in Global Control (Table 36, on page 79) is set to a one.
0	EEInt	RO, LH, SC	EEPROM Done Interrupt. This bit is set to a one after the EEPROM is done loading registers, and it is automatically cleared when read. This bit being high causes the 88E6208/88E6218 INTn pin to go low when the EEIntEn bit in Global Control (Table 36, on page 79) is set to a one.

Table 33: Switch MAC Address Register Bytes 0 & 1
Offset: 0x01 (Hex), or 1 (Decimal)

Bits	Field	Type	Description
15:9	MACByte0	RWR	MAC Address Byte 0 (bits 47:41) is used as the switch's source address (SA) in transmitted full-duplex Pause frames. Since bit 0 of byte 0 (bit 40) is the multicast bit (it is the 1st bit down the wire) it is always transmitted as a zero, and its value cannot be changed.
8	DiffAddr	RWR	Different MAC addresses per Port. This bit is used to have all ports transmit the same or different source addresses in full-duplex Pause frames. 0 = All ports transmit the same SA 1 = Each port uses a different SA where bits 47:3 of the MAC address are the same, but bits 2:0 are the port number (Port 0 = 0, Port 1 = 1, and so on.)
7:0	MACByte1	RWR	MAC Address Byte 1 (bits 39:32) is used as the switch's source address (SA) in transmitted full-duplex Pause frames.

Table 34: Switch MAC Address Register Bytes 2 & 3
Offset: 0x02 (Hex), or 2 (Decimal)

Bits	Field	Type	Description
15:8	MACByte2	RWR	MAC Address Byte 2 (bits 31:24) is used as the switch's source address (SA) in transmitted full-duplex Pause frames.
7:0	MACByte3	RWR	MAC Address Byte 3 (bits 23:16) is used as the switch's source address (SA) in transmitted full-duplex Pause frames.

Table 35: Switch MAC Address Register Bytes 4 & 5
Offset: 0x03 (Hex), or 3 (Decimal)

Bits	Field	Type	Description
15:8	MACByte4	RWR	MAC Address Byte 4 (bits 15:8) is used as the switch's source address (SA) in transmitted full-duplex Pause frames.
7:0	MACByte5	RWR	MAC Address Byte 5 (bits 7:0) is used as the switch's source address (SA) in transmitted full-duplex Pause frames. Note: Bits 2:0 of this register are ignored when DiffAddr is set to a one.

Table 36: Switch Global Control Register
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Type	Description
15:12	Reserved	RES	Reserved for future use.
11	Scheduling (88E6218 only)	RWR	Scheduling mode. This bit is used to select the Queue Controller's scheduling mode as follows: 0 = Use an 8, 4, 2, 1 weighted fair queuing scheme 1 = Use a strict priority scheme
10	MaxFrame Size	RWR	Maximum Frame Size allowed. The Ingress block discards all frames that are less than 64 bytes in size. It also discards all frames that are greater than a certain size as follows: 0 = Max size is 1522 if IEEE 802.3ac tagged, or 1518 if not tagged 1 = Max size is 1535
9	ReLoad	SC	Reload the registers using the EEPROM. When this bit is set to a one the contents of the external EEPROM are used to load the registers just as if a reset had occurred. When the reload operation is done, this bit is cleared to a zero automatically, and the EEInt interrupt is set.
8	CtrMode	RWR	Counter Mode. When this bit is set to a one, the Rx counters for all ports (Table 30, on page 76) count Rx errors and the Tx counters for all ports (Table 31, on page 76) count Tx collisions. When this bit is cleared to a zero, the Rx counters for all ports count Rx frames and the Tx counters for all ports count Tx frames. The Rx counters and the Tx counters for all ports are cleared to a zero whenever this bit changes state (i.e., it transitions from a one to a zero or from a zero to a one).
7:4	Reserved	RES	Reserved for future use.
3	ATUFull IntEn	RWR	ATU Full Interrupt Enable. This bit must be set to a one to allow the ATU Full interrupt to drive the 88E6208/88E6218 INTn pin low.
2	ATUDone IntEn	RWR	ATU Done Interrupt Enable. This bit must be set to a one to allow the ATU Done interrupt to drive the 88E6208/88E6218 INTn pin low.
1	PHYIntEn	RWR	PHY Interrupt Enable. This bit must be set to a one to allow active interrupts enabled in PHY registers 0x12 to drive the 88E6208/88E6218 INTn pin low.
0	EEIntEn	RWS	EEPROM Done Interrupt Enable. This bit must be set to a one to allow the EEPROM Done interrupt to drive the 88E6208/88E6218 INTn pin low.

Note

Registers 0x05 - 0x09 (Hex), or 5 - 9 (Decimal) are reserved.

Table 37: ATU Control Register
Offset: 0x0A (Hex), or 10 (Decimal)

Bits	Field	Type	Description
15	SWReset	SC	Switch Software Reset. Writing a one to this bit causes the QC and the MAC state machines in the switch to be reset. Register values are not modified, except for the PortState bits (Table 26 on page 70) and the EEPROM is not re-read. The PHYs and ATU are not affected by this bit. When the reset operation is done, this bit is cleared to a zero automatically. The reset occurs immediately. To prevent transmission of CRC frames, use the PortState bits to set each port to the Disabled state and wait for 2 ms (i.e., the time for a maximum frame to be transmitted at 10 Mbps) before setting the SWReset bit to a one.
14	LearnDis	RWR	ATU Learn Disable. 0 = Normal operation, learning is determined by the PortState (Table 26, on page 70) 1 = Automatic learning is disabled on all ports – CPU ATU loads still work
13:12	ATUSize	RWS to 0x1	Address Translation Unit Table Size. The initial size of the ATU database is 1024 entries. The size of the ATU database can be modified at any time, but an ATU reset and a Switch Software Reset (bit 15 above) occurs automatically if the new ATUSize is different from the old ATUSize. 00 = 512 Entry Address Database 01 = 1024 Entry Address Database - default 10 = 2048 Entry Address Database (88E6218 device only) 11 = Reserved
11:4	AgeTime	RWS to 0x13	ATU Age Time. These bits determine the time that each ATU Entry remains valid in the database, since its last access as a Source Address, before being purged. The value in this register times 16 is the age time in seconds. For example: The default value of 0x13 is 19 decimal. 19 x 16 = 304 seconds or just over 5 minutes. The minimum age time is 0x1 or 16 seconds. The maximum age time is 0xFF or 4080 seconds or 68 minutes. When the AgeTime is set to 0x0 the Aging function is disabled, and all learned addresses will remain in the database for ever.
3:0	Reserved	RES	Reserved for future use.

Table 38: ATU Operation Register
Offset: 0x0B (Hex), or 11 (Decimal)

Bits	Field	Type/ Reset Value	Description
15	ATUBusy	SC	Address Translation Unit Busy. This bit must be set to a one to start an ATU operation (see ATUOp below). Since only one ATU operation can be executing at one time, this bit must be zero before setting it to a one. When the requested ATU operation completes, this bit is automatically cleared to a zero. The transition of this bit from a one to a zero can be used to generate an interrupt (Table 36, on page 79).
14:12	ATUOp	RWR	Address Translation Unit Table Opcode. The 88E6208/88E6218 device supports the following ATU operations. All of these operations can be executed while frames are transiting through the switch: 000 = No Operation 001 = Flush All Entries - All frames will flood until new addresses are learned. 010 = Flush all Unlocked Entries - An Unlocked entry is any unicast address with an EntryState less than 0xF. All unicast frames will flood until new addresses are learned. 011 = Load or Purge an Entry in a particular DBNum Database - An Entry is Loaded if the EntryState (Table 39, on page 82) is non-zero. An Entry is Purged if it exists and if the EntryState is zero. 100 = Get Next - A Get Next operation finds the next higher MAC address currently in a the ATU's database. The ATUByte[5:0] values (Table 40, on page 82) are used as the address to start from. To find the lowest MAC address set ATU[5:0] to zero. When the operation is done ATUByte[5:0] contains the next higher MAC address. To find the next address simply issue the Get Next opcode again. If ATUByte[5:0] is returned set to all one's, no higher MAC address was found. To Search for a particular address, perform a Get Next operation using a MAC address with a value one less than the one being searched for. 101 = Reserved 111 = Reserved
11:4	Reserved	RES	Reserved for future use.
3:0	ATU DBNum	RWR	ATU Database Number for CPU accesses. If separate address databases (DBNums - Table 27 on page 72) are not being used these bits must remain zero. If DBNums are being used these bits are used to set the DBNum value on Load or Purge operations. If the same MAC address is stored in multiple address databases (DBNums - Table 27 on page 72) the Get Next function will find only one instance of the MAC address.

Table 39: ATU Data Register
Offset: 0x0C (Hex), or 12 (Decimal)

Bits	Field	Type	Description
15:14	EntryPri (88E6218 only)	RWR	ATU Entry Priority Data. These bits are used as the input Entry Priority data for ATU load operation. It is the resulting Entry Priority from the ATU Get Next operation.
13:11	Reserved	RES	Reserved for future use.
10:4	PortVec (9:4 in 88E6208)	RWR	Port Vector. These bits are used as the input Port Vector for ATU load operation. It is the resulting Port Vector from the ATU Get Next operation. Bit 10 is reserved in case of the 88E6208 device.
3:0	Entry_State	RWR	ATU Entry State. These bits are used as the input Entry State for ATU Load or purge operations. It is the resulting Entry State from the ATU Get Next operation.

Table 40: ATU Switch MAC Address Register Bytes 0 & 1
Offset: 0x0D (Hex), or 13 (Decimal)

Bits	Field	Type	Description
15:8	ATUByte0	RWR	ATU MAC Address Byte 0 (bits 47:40) is used as the input MAC address for ATU load, purge, or Get Next operations. It is the resulting MAC address from ATU Get Next operation. Bit 0 of byte 0 (bit 40) is the multicast bit (it is the 1st bit down the wire). Any MAC address with the multicast bit set to a one is considered locked by the ATU.
7:0	ATUByte1	RWR	ATU MAC Address Byte 1 (bits 39:32) is used as the input MAC address for ATU load, purge, or Get Next operations. It is the resulting MAC address from the ATU Get Next operation.

Table 41: ATU Switch MAC Address Register Bytes 2 & 3
Offset: 0x0E (Hex), or 14 (Decimal)

Bits	Field	Type	Description
15:8	ATUByte2	RWR	ATU MAC Address Byte 2 (bits 31:24) is used as the input MAC address for ATU load, purge or Get Next operations. It is the resulting MAC address from ATU Get Next operations.
7:0	ATUByte3	RWR	ATU MAC Address Byte 3 (bits 23:16) that are used as the input MAC address for ATU load, purge or Get Next operations. It is the resulting MAC address from ATU Get Next operations.

Table 42: ATU Switch MAC Address Register Bytes 4 & 5
Offset: 0x0F (Hex), or 15 (Decimal)

Bits	Field	Type	Description
15:8	ATUByte4	RWR	ATU MAC Address Byte 4 (bits 15:8) is used as the input MAC address for ATU load, purge or Get Next operations. It is the resulting MAC address from ATU Get Next operations.
7:0	ATUByte5	RWR	ATU MAC Address Byte 5 (bits 7:0) is used as the input MAC address for ATU load, purge or Get Next operations. It is the resulting MAC address from ATU Get Next operations.

Table 43: IP-PRI Mapping Register 0 (88E6218 only)
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Type	Description
15:14	IP_0x1C	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x1C.
13:12	IP_0x18	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x18.
11:10	IP_0x14	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x14.
9:8	IP_0x10	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x10.
7:6	IP_0x0C	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x0C.
5:4	IP_0x08	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x08.
3:2	IP_0x04	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x04.
1:0	IP_0x00	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x00.

Table 44: IP-PRI Mapping Register 1 (88E6218 only)
Offset: 0x11 (Hex), or 17 (Decimal)

Bits	Field	Type	Description
15:14	IP_0x3C	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x3C.
13:12	IP_0x38	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x38.
11:10	IP_0x34	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x34.
9:8	IP_0x30	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x30.
7:6	IP_0x2C	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x2C.
5:4	IP_0x28	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x28.
3:2	IP_0x24	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x24.
1:0	IP_0x20	RWR	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x20.

Table 45: IP-PRI Mapping Register 2 (88E6218 only)
Offset: 0x12 (Hex), or 18 (Decimal)

Bits	Field	Type	Description
15:14	IP_0x5C	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x5C.
13:12	IP_0x58	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x58.
11:10	IP_0x54	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x54.
9:8	IP_0x50	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x50.
7:6	IP_0x4C	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x4C.
5:4	IP_0x48	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x48.
3:2	IP_0x44	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x44.
1:0	IP_0x40	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x40.

Table 46: IP-PRI Mapping Register 3 (88E6218 only)
Offset: 0x13 (Hex), or 19 (Decimal)

Bits	Field	Type	Description
15:14	IP_0x7C	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x7C.
13:12	IP_0x78	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x78.
11:10	IP_0x74	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x74.
9:8	IP_0x70	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x70.
7:6	IP_0x6C	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x6C.
5:4	IP_0x68	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x68.
3:2	IP_0x64	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x64.
1:0	IP_0x60	RWS to 0x1	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x60.

Table 47: IP-PRI Mapping Register 4 (88E6218 only)
Offset: 0x14 (Hex), or 20 (Decimal)

Bits	Field	Type	Description
15:14	IP_0x9C	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x9C.
13:12	IP_0x98	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x98.
11:10	IP_0x94	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x94.
9:8	IP_0x90	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x90.
7:6	IP_0x8C	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x8C.
5:4	IP_0x88	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x88.
3:2	IP_0x84	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x84.
1:0	IP_0x80	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0x80.

Table 48: IP-PRI Mapping Register 5 (88E6218 only)
Offset: 0x15 (Hex), or 21 (Decimal)

Bits	Field	Type	Description
15:14	IP_0xBC	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xBC.
13:12	IP_0xB8	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xB8.
11:10	IP_0xB4	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xB4.
9:8	IP_0xB0	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xB0.
7:6	IP_0xAC	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xAC.
5:4	IP_0xA8	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xA8.
3:2	IP_0xA4	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xA4.
1:0	IP_0xA0	RWS to 0x2	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xA0.

Table 49: IP-PRI Mapping Register 6 (88E6218 only)
Offset: 0x16 (Hex), or 22 (Decimal)

Bits	Field	Type	Description
15:14	IP_0xDC	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xDC.
13:12	IP_0xD8	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xD8.
11:10	IP_0xD4	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xD4.
9:8	IP_0xD0	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xD0.
7:6	IP_0xCC	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xCC.
5:4	IP_0xC8	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xC8.
3:2	IP_0xC4	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xC4.
1:0	IP_0xC0	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xC0.

Table 50: IP-PRI Mapping Register 7 (88E6218 only)
Offset: 0x17 (Hex), or 23 (Decimal)

Bits	Field	Type	Description
15:14	IP_0xFC	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xFC.
13:12	IP_0xF8	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xF8.
11:10	IP_0xF4	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xF4.
9:8	IP_0xF0	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xF0.
7:6	IP_0xEC	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xEC.
5:4	IP_0xE8	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xE8.
3:2	IP_0xE4	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xE4.
1:0	IP_0xE0	RWS to 0x3	IPv4 and IPv6 mapping. The value in this field is used as the frame's priority when bits (7:2) of its IP TOS/DiffServ/Traffic Class value are 0xE0.

Table 51: IEEE-PRI Register (88E6218 only)
Offset: 0x18 (Hex), or 24 (Decimal)

Bits	Field	Type	Description
15:14	Tag_0x7	RWS to 0x3	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 7.
13:12	Tag_0x6	RWS to 0x3	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 6.
11:10	Tag_0x5	RWS to 0x2	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 5.
9:8	Tag_0x4	RWS to 0x2	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 4.
7:6	Tag_0x3	RWS to 0x1	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 3.
5:4	Tag_0x2	RWR	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 2.
3:2	Tag_0x1	RWR	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 1.
1:0	Tag_0x0	RWS to 0x1	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0.

Note

Registers 0x19 - 0x1F (Hex), or 25 - 31 (Decimal) are reserved.

3.3 PHY Registers

The 88E6208/88E6218 device contains five physical layer devices (PHYs). These devices are accessible using SMI device addresses 0x00 to 0x04 (or 0x10 to 0x14) depending upon the value of the M_A[3] pin at reset (see the table: “Reset Configuration” in part 1 of the 88E6318 datasheet). The PHYs are fully IEEE 802.3 compliant including their register interface.

The PHYs in the 88E6208/88E6218 device are identical to those in the Marvell® 88E3082 Octal Transceiver except that there are five transceivers (transceivers 5 to 7 do not exist and are not accessible).

3.3.1 PHY Register Map

Description	Offset Hex	Offset Decimal	Page Number
PHY Control Register	0x00	0	page 91
PHY Status Register	0x01	1	page 92
PHY Identifier	0x02	2	page 94
PHY Identifier	0x03	3	page 94
Auto-Negotiation Advertisement Register	0x04	4	page 95
Link Partner Ability Register (Base Page)	0x05	5	page 97
Link Partner Ability Register (Next Page)	0x05	5	page 97
Auto-Negotiation Expansion Register	0x06	6	page 98
Next Page Transmit Register	0x07	7	page 99
Link Partner Next Page Register	0x08	8	page 99
Reserved Registers	0x09-0x0F	9 - 15	page 100
PHY Specific Control Register I	0x10	16	page 100
PHY Specific Status Register	0x11	17	page 103
PHY Interrupt Enable	0x12	18	page 105
PHY Interrupt Status	0x13	19	page 106
PHY Interrupt Port Summary (Common register to all ports)	0x14	20	page 107
PHY Receive Error Counter	0x15	21	page 108
LED Parallel Select Register	0x16	22	page 108
Reserved Register	0x17	23	page 109
PHY LED Control Register	0x18	24	page 110
PHY Manual LED Override Register	0x19	25	page 110
VCT™ Control Register	0x1A	26	page 111
VCT™ Status Register	0x1B	27	page 112
PHY Specific Control Register II	0x1C	28	page 113
Reserved Registers	0x1D to 0x1F	29 - 31	page 113

Table 52 defines the register types used in the register map.

Table 52: Register Types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only.
ROC	Read only clear. After read, register field is cleared.
R/W	Read and write with initial value indicated.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, register field is cleared to zero.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field doesn't take effect until soft reset is executed.
Retain	Value written to the register field doesn't take effect without a software reset.
WO	Write only. Reads to this type of register field return undefined data.

3.3.2 PHY Registers

Table 53: PHY Control Register
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SWReset	R/W, SC	0x0	Self Clear	PHY Software Reset Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0	Enable Loopback Mode When loopback mode is activated, the transmitter data presented on TXD is looped back to RXD internally. The PHY has to be in forced 10 or 100 Mbps mode. Auto-Negotiation must be disabled. 1 = Enable loopback 0 = Disable loopback
13	SpeedLSB	R/W	ANEG [2:0]	Update	Speed Selection (LSB) When a speed change occurs, the PHY drops link and tries to determine speed when Auto-Negotiation is on. Speed, Auto-Negotiation enable, and duplex enable take on the values set by ANEG[2:0] on hardware reset. A write to these registers has no effect unless any one of the following also occurs: Software reset is asserted (bit 15) or Power down (bit 11) transitions from power down to normal operation. 1 = 100 Mbps 0 = 10 Mbps
12	AnegEn	R/W	ANEG [2:0]	Update	Auto-Negotiation Enable Speed, Auto-Negotiation enable, and duplex enable take on the values set by ANEG[2:0] on hardware reset. A write to these registers has no effect unless any one of the following also occurs: Software reset is asserted (bit 15, above), Power down (bit 11, below), or transitions from power down to normal operation. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	PwrDwn	R/W	0x0	0x0	Power Down Mode When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (bit 15, above) and Restart Auto-Negotiation (bit 9, below) are not set by the user. 1 = Power down 0 = Normal operation

Table 53: PHY Control Register (Continued)
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Isolate	RO	Always 0	Always 0	Isolate Mode Will always be 0. The Isolate function is not available, since full MII is not implemented. 0 = Normal operation
9	RestartAneg	R/W, SC	0x0	Self Clear	Restart Auto-Negotiation Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex	R/W	ANEG [2:0]	Update	Duplex Mode Selection Speed, Auto-Negotiation enable, and duplex enable take on the values set by ANEG[2:0] on hardware reset. A write to these registers has no effect unless any one of the following also occurs: Software reset is asserted (bit 15), Power down (bit 11), or transitions from power down to normal operation. 1 = Full-duplex 0 = Half-duplex
7	ColTest	RO	Always 0	Always 0	Collision Test Mode Will always be 0. The Collision test is not available, since full MII is not implemented. 0 = Disable COL signal test
6	SpeedMSB	RO	Always 0	Always 0	Speed Selection Mode (MSB) Will always be 0. 0 = 100 Mbps or 10 Mbps
5:0	Reserved	RO	Always 0	Always 0	Will always be 0.

Table 54: PHY Status Register
Offset: 0x01 (Hex), or 1 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100T4	RO	Always 0	Always 0	100BASE-T4 This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100FDX	RO	Always 1	Always 1	100BASE-T and 100BASE-X full-duplex 1 = PHY able to perform full-duplex
13	100HDX	RO	Always 1	Always 1	100BASE-T and 100BASE-X half-duplex 1 = PHY able to perform half-duplex

Table 54: PHY Status Register (Continued)
Offset: 0x01 (Hex), or 1 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
12	10FDX	RO	Always 1	Always 1	10BASE-T full-duplex 1 = PHY able to perform full-duplex
11	10HPX	RO	Always 1	Always 1	10BASE-T half-duplex 1 = PHY able to perform half-duplex
10	100T2FDX	RO	Always 0	Always 0	100BASE-T2 full-duplex. This protocol is not available. 0 = PHY not able to perform full-duplex
9	100T2HDX	RO	Always 0	Always 0	100BASE-T2 half-duplex This protocol is not available. 0 = PHY not able to perform half-duplex
8	ExtdStatus	RO	Always 0	Always 0	Extended Status 0 = No extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Must always be 0.
6	MFPreSup	RO	Always 1	Always 1	MF Preamble Suppression Mode Must be always 1. 1 = PHY accepts management frames with preamble suppressed
5	AnegDone	RO	0x0	0	Auto-Negotiation Complete 1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed
4	RemoteFault	RO, LH	0x0	0	Remote Fault Mode 1 = Remote fault condition detected 0 = Remote fault condition not detected
3	AnegAble	RO	Always 1	Always 1	Auto-Negotiation Ability Mode 1 = PHY able to perform Auto-Negotiation
2	Link	RO, LL	0x0	0	Link Status Mode This register indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read RTLink in Table 64 on page 103. 1 = Link is up 0 = Link is down
1	JabberDet	RO, LH	0x0	0	Jabber Detect 1 = Jabber condition detected 0 = Jabber condition not detected
0	ExtdReg	RO	Always 1	Always 1	Extended capability mode. 1 = Extended register capabilities

Table 55: PHY Identifier
Offset: 0x02 (Hex), or 2 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	OUI MSb	RO	0x0141	0x0141	Organizationally Unique Identifier bits 3:18 0000000101000001 Marvell® OUI is 0x005043

Table 56: PHY Identifier
Offset: 0x03 (Hex), or 3 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	Always 000011	Organizationally Unique Identifier bits19:24
9:4	ModelNum	RO	Varies	Varies	Model Number = 001000
3:0	RevNum	RO	Varies	Varies	Revision Number Contact Marvell® FAEs for information on the device revision number.

Table 57: Auto-Negotiation Advertisement Register
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	AnegAd NxtPage	R/W	0x0	Retain	Next Page 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 53 on page 91) or link goes down.
14	Ack	RO	Always 0	Always 0	Must be 0.
13	AnegAd ReFault	R/W	0x0	Retain	Remote Fault Mode 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 53 on page 91) or link goes down.
12:11	Reserved	R/W	0x0	Retain	Must be 00. Reserved bits are R/W to allow for forward compatibility with future IEEE standards. Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 53 on page 91) or link goes down.
10	AnegAd Pause	R/W	0x0	Retain	Pause Mode 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 53 on page 91) or link goes down.
9	AnegAd 100T4	RO	Always 0	Always 0	100BASE-T4 mode 0 = Not capable of 100BASE-T4
8	AnegAd 100FDX	R/W	0x1	Retain	100BASE-TX full-duplex Mode 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 53 on page 91) or link goes down.

Table 57: Auto-Negotiation Advertisement Register (Continued)
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
7	AnegAd 100HDX	R/W	0X1	Retain	100BASE-TX half-duplex Mode 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 53 on page 91) or link goes down.
6	AnegAd 10FDX	R/W	0X1	Retain	10BASE-TX full-duplex Mode 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 53 on page 91) or link goes down.
5	AnegAd 10HDX	R/W	0X1	Retain	10BASE-TX half-duplex Mode 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 53 on page 91) or link goes down.
4:0	AnegAd Selector	RO	Always 0x01	Always 0x01	Selector Field Mode 00001 = 802.3

Table 58: Link Partner Ability Register (Base Page)
Offset: 0x05 (Hex), or 5 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LPNxt Page	RO	0x0	0	Next Page Mode Base page will be overwritten if next page is received and if Reg8NxtPg (Table 63 on page 100) is disabled. When Reg8NxtPg (Table 63 on page 100) is enabled, then next page is stored in the Link Partner Next Page register (Table 62 on page 99), and the Link Partner Ability Register (Table 58 on page 97) holds the base page. Received Code Word Bit 15
14	LPAck	RO	0x0	0	Acknowledge Received Code Word Bit 14
13	LPRemote Fault	RO	0x0	0	Remote Fault Received Code Word Bit 13
12:5	LPTechAble	RO	0x00	0x00	Technology Ability Field Received Code Word Bit 12:5
4:0	LPSelector	RO	00000	00000	Selector Field Received Code Word Bit 4:0

Table 59: Link Partner Ability Register (Next Page)
Offset: 0x05 (Hex), or 5 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LPNxtPage	RO	--	--	Next Page Mode Base page will be overwritten if next page is received and if Reg8NxtPg (Table 63 on page 100) is disabled. When Reg8NxtPg (Table 63 on page 100) is enabled, then next page is stored in the Link Partner Next Page register (Table 62 on page 99), and Link Partner Ability Register (Table 58 on page 97) holds the base page. Received Code Word Bit 15
14	LPAck	RO	--	--	Acknowledge Received Code Word Bit 14
13	LPMessage	RO	--	--	Message Page Received Code Word Bit 13
12	LPack2	RO	--	--	Acknowledge 2 Received Code Word Bit 12
11	LPToggle	RO	--	--	Toggle Received Code Word Bit 11
10:0	LPData	RO	--	--	Message/Unformatted Field Received Code Word Bit 10:0

Table 60: Auto-Negotiation Expansion Register
Offset: 0x06 (Hex), or 6 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	Always 0x000	Always 0x000	Reserved. Must be 00000000000. The Auto-Negotiation Expansion Register is not valid until the AnegDone (Table 54 on page 92) indicates completed.
4	ParFaultDet	RO	0x0	0x0	Parallel Detection Level 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function
3	LPNxtPg Able	RO	0x0	0x0	Link Partner Next Page Able 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	LocalNxtPg Able	RO	Always 0x1	Always 0x1	Local Next Page Able This bit is equivalent to AnegAble (Table 54 on page 92). 1 = Local Device is Next Page able
1	RxNewPage	RO/LH	0x0	0x0	Page Received 1 = A New Page has been received 0 = A New Page has not been received
0	LPAnegAble	RO	0x0	0x0	Link Partner Auto-Negotiation Able 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 61: Next Page Transmit Register
Offset: 0x07 (Hex), or 7 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TxNxtPage	R/W	0x0	0x0	Next Page A write to the Next Page Transmit Register implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Reserved Transmit Code Word Bit 14
13	TxMessage	R/W	0x1	0x1	Message Page Mode Transmit Code Word Bit 13
12	TxAck2	R/W	0x0	0x0	Acknowledge2 Transmit Code Word Bit 12
11	TxToggle	RO	0x0	0x0	Toggle Transmit Code Word Bit 11
10:0	TxData	R/W	0x001	0x001	Message/Unformatted Field Transmit Code Word Bit 10:0

Table 62: Link Partner Next Page Register
Offset: 0x08 (Hex), or 8 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	RxNxtPage	RO	0x0	0x0	Next Page If Reg8NxtPg (Table 63 on page 100) is enabled, then next page is stored in the Link Partner Next Page register (Table 62 on page 99); otherwise, theLink Partner Next Page register (Table 62 on page 99) is cleared to all 0's. Received Code Word Bit 15
14	RxAck	RO	0x0	0x0	Acknowledge Received Code Word Bit 14
13	RxMessage	RO	0x0	0x0	Message Page Received Code Word Bit 13
12	RxAck2	RO	0x0	0x0	Acknowledge 2 Received Code Word Bit 12
11	RxToggle	RO	0x0	0x0	Toggle Received Code Word Bit 11
10:0	RxData	RO	0x001	0x000	Message/Unformatted Field Received Code Word Bit 10:0

Note

Registers 0x09 through 0x0F (hexadecimal (9 through 15 decimal) are reserved. Do not read or write to these registers.

Table 63: PHY Specific Control Register
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RES	--	--	Reserved.
14	EDet	R/W	ENA_EDET	Retain	Energy Detect 1 = Enable with sense and pulse 0 = Disable Enable with sense only is not supported Enable Energy Detect takes on the appropriate value defined by the CONFIG9 pin at hardware reset.
13	DisNLP Check	R/W	0x0	0x0	Disable Normal Linkpulse Check Linkpulse check and generation disable have no effect, if Auto-Negotiation is enabled locally. 1 = Disable linkpulse check 0 = Enable linkpulse check
12	Reg8NxtPg	R/W	0x0	0x0	Enable the Link Partner Next Page register (Table 59 on page 97) to store Next Page. If set to store next page in the Link Partner Next Page register (Table 59 on page 97), then 802.3u is violated to emulate 802.3ab. 1 = Store next page in the Link Partner Next Page register (Table 59 on page 97) 0 = Store next page in the Link Partner Ability Register (Base Page) register (Table 58 on page 97).
11	DisNLPGen	R/W	0x0	0x0	Disable Linkpulse Generation. Linkpulse check and generation disable have no effect, when Auto-Negotiation is enabled locally. 1 = Disable linkpulse generation 0 = Enable linkpulse generation
10	ForceLink	R/W	0x0	0x0	Force Link Good When link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation
9	DisScrambler	R/W	ANEG [2:0]	Retain	Disable Scrambler If fiber mode is selected then the scrambler is disabled at hardware reset. 1 = Disable scrambler 0 = Enable scrambler

Table 63: PHY Specific Control Register (Continued)
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
8	DisFEFI	R/W	DIS_FEFI ANEG [2:0]	Retain	Disable FEFI In 100BASE-FX mode, Disable FEFI takes on the appropriate value defined by the CONFIG8 pin at hardware reset. FEFI is automatically disabled regardless of the state of this bit if copper mode is selected. 1 = Disable FEFI 0 = Enable FEFI For the 88E3083 device, this bit applies to Port 7 only.
7	ExtdDistance	R/W	0x0	0x0	Enable Extended Distance When using cable exceeding 100 meters, the 10BASE-T receive threshold must be lowered in order to detect incoming signals. 1 = Lower 10BASE-T receive threshold 0 = Normal 10BASE-T receive threshold
6	TPSelect	R/W	ANEG [2:0]	Update	(Un)Shielded Twisted Pair This setting can be changed by writing to this bit followed by software reset. 1 = Shielded Twisted Pair 0 = Unshielded Twisted Pair - default
5:4	AutoMDI[X]	R/W	ENA_XC,1	Update	MDI/MDIX Crossover This setting can be changed by writing to these bits followed by software reset. If ENA_XC is 1 at hardware reset then bits 5:4 = 11 00 = Manual MDIX Configuration (Transmit on pins TXP/TXN, Receive on pins RXP/RXN) 01 = Manual MDI Configuration (Transmit on pins RXP/RXN, Receive on pins TXP/TXN) 1x = Enable Automatic Crossover
3:2	RxFIFO Depth	R/W	0x0	0x0	Receive FIFO Depth 00 = 4 Bytes 01 = 6 Bytes 10 = 8 Bytes 11 = Reserved
1	AutoPol	R/W	0x0	00	Polarity Reversal If polarity is disabled, then the polarity is forced to be normal in 10BASE-T mode. Polarity reversal has no effect in 100BASE-TX mode. 1 = Disable automatic polarity reversal 0 = Enable automatic polarity reversal

Table 63: PHY Specific Control Register (Continued)
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
0	DisJabber	R/W	0x0	00	Disable Jabber Jabber has no effect in full-duplex or in 100BASE-X mode. 1 = Disable jabber function 0 = Enable jabber function

Table 64: PHY Specific Status Register
Offset: 0x11 (Hex), or 17 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RES	--	--	Reserved
14	ResSpeed	RO	ANEG [2:0]	Retain	Resolved Speed Speed and duplex takes on the values set by ANEG[2:0] pins on hardware reset only. The values are updated after the completion of Auto-Negotiation. The registers retain their values during software reset. 1 = 100 Mbps 0 = 10 Mbps
13	ResDuplex	RO	ANEG [2:0]	Retain	Resolved Duplex Mode Speed and duplex takes on the values set by ANEG[2:0] pins on hardware reset only. The values are updated after the completion of Auto-Negotiation. The registers retain their values during software reset. This bit is valid only after the resolved bit 11 is set. 1 = Full-duplex 0 = Half-duplex
12	RcvPage	RO, LH	0x0	0x0	Page Receive Mode 1 = Page received 0 = Page not received
11	Resolved	RO	0x0	0x0	Speed and Duplex Resolved. Speed and duplex bits (14 and 13) are valid only after the Resolved bit is set. The Resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Resolved 0 = Not resolved
10	RTLink	RO	0x0	0x0	Link (real time) 1 = Link up 0 = Link down
9:7	Reserved	RES	0x0	0x0	Must be 000.
6	MDI/MDIX	RO	0x1	0x1	MDI/MDIX Crossover Status 1 = MDIX - Transmit on pins RXP/RXN, Receive on pins TXP/TXN 0 = MDI - Transmit on pins TXP/TXN, Receive on pins RXP/RXN
5	Reserved	RES	0x4	0x4	Must be 0.
4	Sleep	RO	0	0x0	Energy Detect Status 1 = Chip is in sleep mode (No wire activity) 0 = Chip is not in sleep mode (Active)
3:2	Reserved	RES	0x0	0x0	Must be 00.

Table 64: PHY Specific Status Register (Continued)
Offset: 0x11 (Hex), or 17 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
1	RTPolarity	RO	0x0	0x0	Polarity (real time) 1 = Reversed 0 = Normal
0	RTJabber	RO	Retain	0x0	Jabber (real time) 1 = Jabber 0 = No Jabber

Table 65: PHY Interrupt Enable
Offset: 0x12 (Hex), or 18 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RES	--	--	Reserved
14	SpeedIntEn	R/W	0x0	Retain	Speed Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
13	DuplexIntEn	R/W	0x0	Retain	Duplex Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
12	RcvPageIntEn	R/W	0x0	Retain	Page Received Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
11	AnegDone IntEn	R/W	0x0	Retain	Auto-Negotiation Completed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
10	LinkIntEn	R/W	0x0	Retain	Link Status Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
9	SymErrIntEn	R/W	0x0	Retain	Symbol Error Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
8	FlsCrsIntEn	R/W	0x0	Retain	False Carrier Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
7	FIFOErrInt	R/W	0x0	Retain	FIFO Over/Underflow Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
6	MDI[x]IntEn	R/W	0x0	0x0	MDI/MDIX Crossover Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
5	Reserved	RES	0x0	Retain	Must be 0.
4	EDetIntEn	R/W	0x0	Retain	Energy Detect Interrupt Enable 1 = Enable 0 = Disable
3:2	Reserved	RES	0x0	Retain	Must be 00.
1	PolarityIntEn	R/W	0x0	Retain	Polarity Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable

Table 65: PHY Interrupt Enable (Continued)
Offset: 0x12 (Hex), or 18 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
0	JabberIntEn	R/W	0x0	Retain	Jabber Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable

Table 66: PHY Interrupt Status
Offset: 0x13 (Hex), or 19 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RES	--		Reserved
14	SpeedInt	RO, LH	0x0	0x0	Speed Changed 1 = Speed changed 0 = Speed not changed
13	DuplexInt	RO, LH	0x0	0x0	Duplex Changed 1 = Duplex changed 0 = Duplex not changed
12	RxPageInt	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	AnegDoneInt	RO, LH	0x0	0x0	Auto-Negotiation Completed 1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	LinkInt	RO, LH	0x0	0x0	Link Status Changed 1 = Link status changed 0 = Link status not changed
9	SymErrInt	RO, LH	0x0	0x0	Symbol Error 1 = Symbol error 0 = No symbol error
8	FlsCrsInt	RO, LH	0x0	0x0	False Carrier 1 = False carrier 0 = No false carrier
7	FIFOErrInt	RO, LH	0x0	0x0	FIFO Over /Underflow Error 1 = Over/underflow error 0 = No over/underflow error
6	MDIMDIXInt	RO, LH	0x0	0x0	MDI/MDIX Crossover Changed 1 = MDI/MDIX crossover changed 0 = MDI/MDIX crossover not changed
5	Reserved	RO	Always 0	Always 0	Must be 0

Table 66: PHY Interrupt Status (Continued)
Offset: 0x13 (Hex), or 19 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
4	EDetChg	RO, LH	0x0	0x0	Energy Detect Changed 1 = Changed 0 = No Change
3:2	Reserved	RO	0x0	0x0	Must be 00
1	PolarityInt	RO	0x0	0x0	Polarity Changed 1 = Polarity changed 0 = Polarity not changed
0	JabberInt	RO, LH	0x0	0x0	Jabber Mode 1 = Jabber 0 = No Jabber

Table 67: PHY Interrupt Port Summary
Offset: 0x14 (Hex), or 20 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x0	0x0	Must be 00000000000.
4	Port4Int Active	RO	0x0	0x0	Port 4 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt
3	Port3Int Active	RO	0x0	0x0	Port 3 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt
2	Port2Int Active	RO	0x0	0x0	Port 2 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt
1	Port1Int Active	RO	0x0	0x0	Port 1 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt

Table 67: PHY Interrupt Port Summary (Continued)
Offset: 0x14 (Hex), or 20 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
0	Port0Int Active	RO	0x0	0x0	Port 0 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt

Table 68: Receive Error Counter
Offset: 0x15 (Hex), or 21 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RxErrCnt	RO	0x0000	0x0000	Receive Error Count This register counts receive errors on the media interface. When the maximum receive error count reaches 0xFFFF, the counter will not roll over.

Table 69: LED Parallel Select Register (Global)[1]
Offset: 0x16 (Hex), or 22 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RES	0000	Retain	Must be 0000
11:8	LED2	R/W	LED[1:0] 00 = LINK 01 = LINK 10 = LINK/RX 11= LINK ACT	Retain	LED2 Control The parallel LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 0000 = COLX, 0001 = ERROR, 0010 = DUPLEX, 0011 = DUPLEX/COLX, 0100 = SPEED, 0101 = LINK, 0110 = TX, 0111 = RX, 1000 = ACT, 1001 = LINK/RX, 1010 = LINK/ACT, 1011 to 1111 = Force to 1

Table 69: LED Parallel Select Register (Global)[1] (Continued)
Offset: 0x16 (Hex), or 22 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
7:4	LED1	R/W	LED[1:0] 00 = RX 01 = ACT 10 = TX 11= DUPLEX /COLX	Retain	LED1 Control The parallel LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 0000 = COLX, 0001 = ERROR, 0010 = DUPLEX, 0011 = DUPLEX/COLX, 0100 = SPEED, 0101 = LINK, 0110 = TX, 0111 = RX, 1000 = ACT, 1001 = LINK/RX, 1011 to 1111 = Force to 1
3:0	LED0	R/W	LED[1:0] 00 = TX 01 = SPEED 10 = SPEED 11= SPEED	Retain	LED0 Control The parallel LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 0000 = COLX, 0001 = ERROR, 0010 = DUPLEX, 0011 = DUPLEX/COLX, 0100 = SPEED, 0101 = LINK, 0110 = TX, 0111 = RX, 1000 = ACT, 1001 = LINK/RX, 1011 to 1111 = Force to 1

1. See Table 19 on page 61 and Table 20 on page 62 for parallel LED display modes that can be selected by hardware pin configuration at reset.

Note

Register 0x17 hexadecimal (23 decimal) is reserved. Do not read or write to this register.

Table 70: PHY LED Control Register (Global)
Offset: 0X18 (Hex), 0r 24 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Must be 0.
14:12	PulseStretch	R/W	0x4	Retain	Pulse stretch duration. Default Value = 100. 000 = No pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11:9	BlinkRate	R/W	0x1	Retain	Blink Rate. This is a global setting. Default Value = 001 000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
8:6	Reserved	RES	0x2	Retain	Reserved
5:0	Reserved	RES	0x0	0x0	Reserved

Table 71: PHY Manual LED Override
Offset: 0x19 (Hex), or 25 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	R/W	0x0	Retain	0000000000
5:4	LED2	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On
3:2	LED1	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On

Table 71: PHY Manual LED Override (Continued)
Offset: 0x19 (Hex), or 25 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
1:0	LED0	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On

Table 72: VCT™ Register for TXP/N Pins
Offset: 0x1A[1] (Hex), or 26 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	EnVCT	R/W, SC	0x0	0x0	Enable VCT The 88E3082/88E3083 device must be in forced 100 Mbps mode before enabling this bit. 1 = Run VCT 0 = VCT completed After running VCT once, bit 15 = 0 indicates VCT completed. The cable status is reported in the VCTTst bits in registers 26 and 27. Refer to the “Virtual Cable Tester™” feature in section 2.4.
14:13	VCTTst	RO	0x0	Retain	VCT Test Status These VCT test status bits are valid after completion of VCT. 11 = Test fail 00 = valid test, normal cable (no short or open in cable) 10 = valid test, open in cable (Impedance > 333 ohm) 01 = valid test, short in cable (Impedance < 33 ohm)
12:8	AmpRfln	RO	0x0	Retain	Amplitude of Reflection The amplitude of reflection is stored in these register bits. These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x13 = Zero amplitude 0x07 = Maximum negative amplitude These bits are valid after completion of VCT (bit 15) and if the VCT test status bits (bits 14:13) have not indicated test failure.
7:0	DistRfln	RO	0x0	Retain	Distance of Reflection These bits refer to the approximate distance (+/- 1m) to the open/short location, measured at nominal conditions (room temperature and typical VDDs) These bits are valid after completion of VCT (bit 15) and if the VCT test status bits (bit 14:13) have not indicated test failure.

1. The results stored in this register apply to the TX_Pair.

Table 73: VCT™ Register for RXP/N pins
Offset: 0x1B[1] (Hex), or 27 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Reserved
14:13	VCTTst	RO	0	Retain	VCT Test Status The VCT test status bits are valid after completion of VCT. 11 = Test fail 00 = valid test, normal cable (no short or open in cable) 10 = valid test, open in cable (Impedance > 333 ohm) 01 = valid test, short in cable (Impedance < 33 ohm)
12:8	AmpRfln	RO	0	Retain	Amplitude of Reflection The amplitude of reflection is stored in these register bits. These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x13 = Zero amplitude 0x07 = Maximum negative amplitude These bits are valid after completion of VCT (bit 15) and if VCT test status bits (bit 14:13) have not indicated test failure.
7:0	DistRfln	RO	0	Retain	Distance of Reflection These bits refer to the approximate distance (+/- 1m) to the open/short location, measured at nominal conditions (room temperature and typical VDDs) These bits are valid after completion of VCT (bit 15) and if VCT test status bits (bits 14:13) have not indicated test failure.

1. The results stored in this register apply to the RX_Pair.

Figure 27: Cable Fault Distance Trend Line

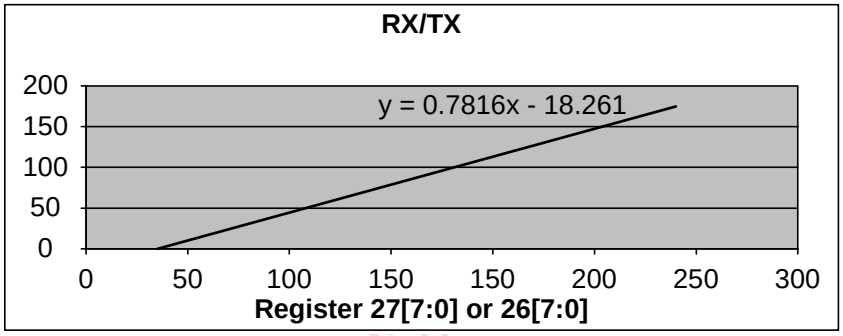


Table 74: PHY Specific Control Register II
Offset: 0x1C (Hex), or 28 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x0	0x0	Must be 000000000000000
0	SelClsA	R/W	SEL_ CLASS A	Update	1 = Select BackPlane driver (Class A) 0 = Select class CAT 5 driver (Class B)

Note

Registers 0x1D through 0x1F (hexadecimal (29 through 31 decimal) are reserved. Do not read or write to these registers.

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