GATEWAYS

Link Street™ 88E6208/88E6218 Datasheet

SOHO Gateway SOC with
ARM9E CPU, 10/100 Switch and PHYs

Part 1 of 3: Overview, Pinout, & Electrical Specifications

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Document Status	
Advanced Information	This document contains design specifications for initial product development. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
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Final Information	This document contains specifications on a product that is in final release. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
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Overview

The Marvell® Link Street™ 88E6208/88E6218 devices are single-chip gateway routers, enabling the design of highly integrated gateways for multiple PCs to share a common broadband Internet connection with DSL or cable modem. Each Link Street device contains an ARM9E CPU, 8 kB data cache, 8 kB instruction cache, SDRAM/Flash memory controller, multi-port 10/100 Fast Ethernet switch and PHY transceivers. The Link Street 88E6218 also contains support for Quality of Service for prioritizing voice, video, and data traffic.

Two pin compatible devices exist in the product family:

The 88E6208 is targeted at the low cost but high performance market. Its pinout has been optimized to support a complete router on a 2 layer PCB using a single SDRAM and Flash.

The 88E6218 has a higher CPU clock speed to enhance the performance of software security functions for Virtual Private Networks; an additional MII port for connecting to other networking devices such as an external switch for port expansion; and features like QoS, Rate Limiting, and additional memory interface options.

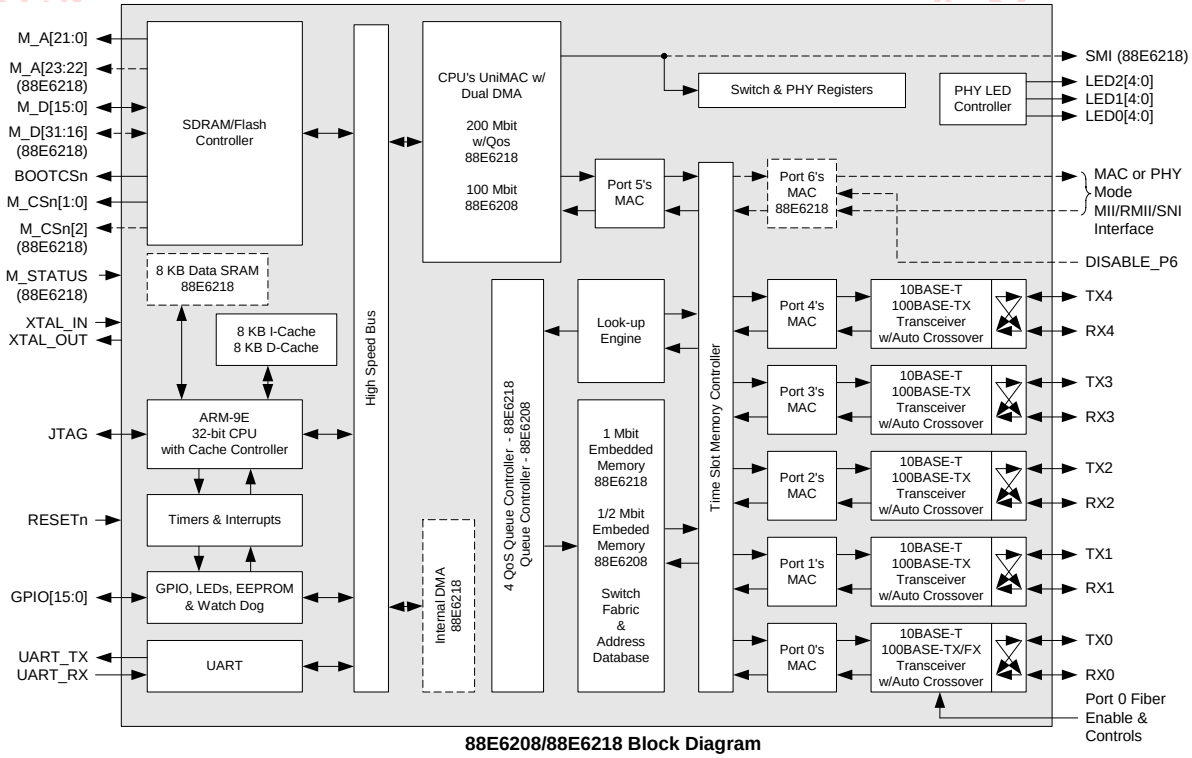
Features

- **Single-chip SOHO Gateway/Router CPU and Fast Ethernet QoS Switch with Patented Uni-MAC™ Architecture**

Router/CPU Features

- ARM9E 32-bit RISC CPU with DSP Instruction Extensions, @ 133MHz/150MHz, including on-chip 8 kB Instruction Cache plus 8 kB Data Cache and 8 kB Data RAM (88E6218 only)
- Integrated SDRAM and Flash Memory Controller including support for memory-mapped peripherals including DSP
- SDRAM interface can be 16- or 32-bits (88E6218 only) wide, addressing up to 64 MB in 32-bit and 32 MB in 16-bit memory
- FLASH interface can be 8-, 16- or 32-bits (88E6218 only) wide, addressing up to 64 MB memory
- External Chip Select pins are supported (three in 88E6208, four in 88E6218)
- Internal IEEE 802.3 MAC, 200 Mbps full-duplex (100 Mbps in 88E6208), with optional address filtering and priority queueing under DMA control

(Features continued on next page)



88E6208/88E6218 Block Diagram

- MDC/MDIO master controller for Switch (external device register access available in 88E6218 only)
- Internal DMA controller (88E6218 only)
- Watchdog timer
- UART Serial Port Interface for PC or POTS Modem & system debug
- JTAG interface for in-circuit testing and real-time in-circuit emulation, including setting breakpoints & watchpoints

ETHERNET SWITCH FEATURES

- 7-Port QoS Fast Ethernet Switch with wirespeed non-blocking QoS switch core (6-Port non-QoS switch in 88E6208)
- 5 PHY Ports: Can be used as:
  - 1 WAN Port: Copper TX or Fiber FX
  - 4 LAN Copper TX Ports
- 1 RMII/MII/SNI Port with up to 200 Mbps full-duplex operation, directly connects at full-speed to another network, such as another switch or Wireless LAN (88E6218 only)
- 1 internal UniMAC™ double-speed MII port, connects the switch to the CPU's MAC at 200 Mbps full-duplex (in 88E6218, 100 Mbps in 88E6208)
- Integrated Voice/Video/Data networking: full IEEE 802.1p, IPv4 DiffServ and IPv6 Traffic Class support with four (4) QoS priority queues per port, typically supporting Management, Voice, Video, and Data streams (88E6218 only)
- Port-Based VLANs, configurable in any combination
- Per port Ingress Rate Limiting and Egress Rate Shaping (88E6218 only)
- On-chip packet buffer SRAM
- Supports up to 2K MAC addresses in multiple address databases
- Spanning Tree support: prevents bridge loops for complete plug-and-play
- Marvell PHYAdvantage™ DSP-based PHYs provide automatic MDI/MDIX detection and interface, enabling end-user connection of either Straight or Crossover RJ-45 cables
- Four MIB statistics counters per port for remote-office network management: TX Frame Count, RX Frame Count, # Collisions, # CRC Errors
- Low-power CMOS IC
- 216-Pin LQFP

The following table summarizes the feature differences between the pin compatible 88E6208 and 88E6218 devices.

Feature	88E6208	88E6218
CPU		
Maximum CPU Speed	133 MHz	150 MHz
8K Data Tightly-Coupled Memory SRAM	No	Yes
Internal DMA	No	Yes
External Memory Width	16-bits	32-bits
Maximum Flash Size	8 MB	64 MB
External Chip Selects	3 - BootCSn, M_CSn[1:0]	4 - BootCSn, M_CSn[2:0]
M_STATUS pin for Flash Memory	No[1]	Yes
Address Bus pins	M_A[21:0]	M_A[23:0]
UniMAC™ QoS	No	Yes - 4 Queues
UniMAC DA Filter	No	Yes
SWITCH		
# of Switch Ports	6	7
External MII	No	Yes
Switch QoS	No	Yes - 4 Queues
Ingress Rate Limiting	No	Yes
Egress Rate Shaping	No	Yes
Max. UniMAC Speed	100 Mbps FD	200 Mbps FD
Embedded Memory	0.5 Mb	1 Mb

1. A GPIO pin can be used instead.

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Preface

About this Document

Part 1: Overview, Pinout, and Electrical Specifications provides a features list and overview describing the features in the 88E6208/88E6218. It also provides the pin description, pin map, and the electrical specifications. This volume is part of a three-volume set that describes the hardware features, the ARM9E CPU and peripheral interfaces and the switch core and PHYs of the 88E6208/88E6218.

The other two manuals in this set are:

- *Part 2: CPU & Peripherals* which provides a description of the CPU and each of the peripheral interfaces of the 88E6208/88E6218 and includes the related register tables.
- *Part 3 Switch Core and PHYs* which provides a description of the switch core and PHYs of the 88E6208/88E6218 and includes the related register tables.

In addition, Part 1 provides an overview to the complete three-volume set.

Related Documentation

The following 88E6208/88E6218 documents relate to this manual.

- 88E6208/88E6218 Part 2: CPU Core and Peripherals, Document Number MV-S101300-02
- 88E6208/88E6218 Part 3: Switch Core and PHYs, Document Number MV-S101300-03

Document Conventions

Table 1: Document Conventions

Document Conventions The following name and usage conventions are used in this document:	
Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_Addr[12:0]
Active Low Signals n	A lower-case n symbol at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated in courier blue font. Example: `RegInit` OR Example: Global_Control<DevEn>, Where Global Control represents the register name, and <DevEn> represents the register field name. Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use.

Section 1. Signal Description

Figure 1: 88E6208 216-Pin LQFP Package

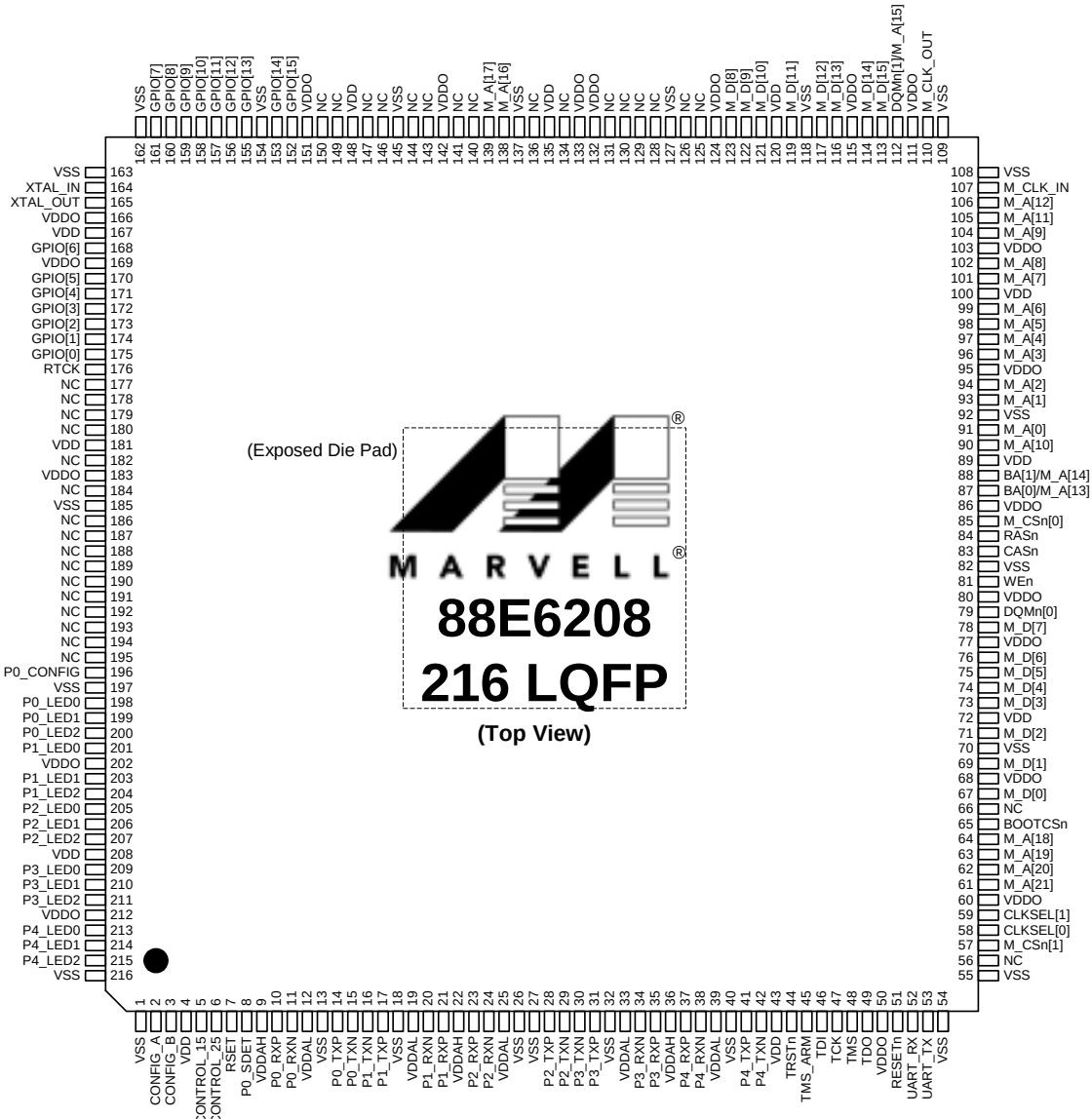
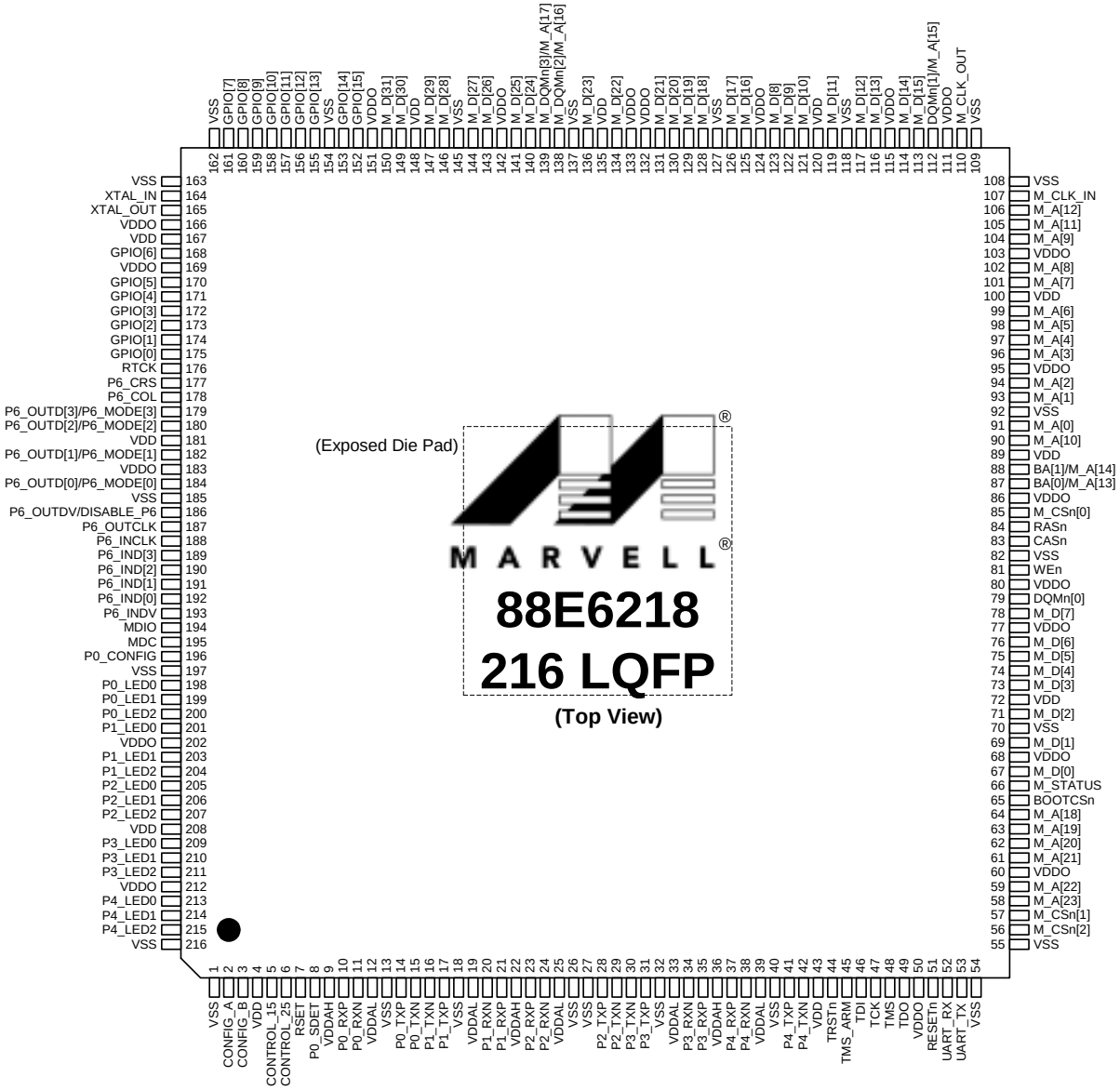


Figure 2: 88E6218 216-Pin LQFP Package



1.1 Pin Description

1.1.1 Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

Table 2: Switch Network Interface

216-LQFP Package Pin #	Pin Name	Pin Type	Description
37 35 23 21 10	P[4:0]_RXP	Typically Input	Receiver input – Positive. P[4:0]_RXP connects directly to the receiver magnetics. If the port is configured for 100BASE-FX mode (Port 0 only), RXP connects directly to the fiber-optic receiver's positive output. For lowest power, all unused port RXP pins should be tied to VSS. These pins can become outputs if Auto MDI/MDIX is enabled (See Part 3 of the 3 part 88E6208/88E6218 datasheet for details).
38 34 24 20 11	P[4:0]_RXN	Typically Input	Receiver input – Negative. P[4:0]_RXN connects directly to the receiver magnetics. If the port is configured for 100BASE-FX mode (Port 0 only), RXN connects directly to the fiber-optic receiver's negative output. For lowest power, all unused port RXN pins should be tied to VSS. These pins can become outputs if Auto MDI/MDIX is enabled (See Part 3 of the 3 part 88E6208/88E6218 datasheet for details).
41 31 28 17 14	P[4:0]_TXP	Typically Output	Transmitter output – Positive. P[4:0]_TXP connects directly to the transmitter magnetics. If the port is configured for 100BASE-FX mode (Port 0 only), P0_TXP connects directly to the fiber-optic transmitter's positive input. For lowest power, all unused port TXP pins should be tied to VSS. These pins can become inputs if Auto MDI/MDIX is enabled (See Part 3 of the 3 part 88E6208/88E6218 datasheet for details).
42 30 29 16 15	P[4:0]_TXN	Typically Output	Transmitter output – Negative. P[4:0]_TXN connects directly to the transmitter magnetics. If the port is configured for 100BASE-FX mode (Port 0 only) P0_TXN connects directly to the fiber-optic transmitter's negative input. For lowest power, all unused port TXN pins should be tied to VSS. These pins can become inputs if Auto MDI/MDIX is enabled (See Part 3 of the 3 part 88E6208/88E6218 datasheet for details).
8	P0_SDET	Input	Signal Detect input. If Port 0 is configured for 100BASE-FX mode, P0_SDET indicates whether a signal is detected by the fiber-optic transceiver. A positive level indicates that a signal is detected. If Port 0 is configured for 10/100BASE-T mode, P0_SDET is not used but it cannot be left floating since this pin does not contain internal resistors. An unused P0_SDET pin can be tied to VSS.

Table 3: Switch PHY Configuration

216-LQFP Package Pin #	Pin Name	Pin Type	Description
196	P0_CONFIG	Input	Port 0 Configuration. The P0_CONFIG pin is used to set the default configuration for Port 0 by connecting the pin to other device pins as defined in Table 15, "PHY Configuration Pins," on page 44. Ports 1, 2, 3 and 4 default configuration is Auto-Negotiation enabled. Any port's default configuration can be modified by accessing the PHY registers by a CPU. Fiber mode vs. copper mode cannot be configured in this way, however. Fiber vs. copper must be selected at Reset by using the P0_CONFIG pins. The P0_CONFIG pin is configured after Reset and contains an internal pull down resistor so it can be left floating to select Auto-Negotiation.
2	CONFIG_A	Input	Global Configuration A. This global configuration pin is used to set the default LED mode and Far End Fault Indication (FEFI) mode by connecting these pins to other device pins as defined in Table 15, "PHY Configuration Pins," on page 44. The LED modes are defined in Part 3 of the 3 part 88E6208/88E6218 datasheet. The CONFIG_A pin is configured after Reset. It contains an internal pull-up resistor so it can be left floating to select the VDDO options.
3	CONFIG_B	Input	Global Configuration B. This global configuration pin is used to set the default mode for Auto-Crossover, the PHY driver type and Energy Detect by connecting these pins to other device pins as defined in Table 15, "PHY Configuration Pins," on page 44. Auto crossover and Energy Detect are defined in Part 3 of the 3 part 88E6208/88E6218 datasheet. The CONFIG_B pin is configured after Reset. It contains an internal pull-up resistor so it can be left floating to select the VDDO options.

Table 4: Switch PHY Status LEDs

216-LQFP Package Pin #	Pin Name	Pin Type	Description
215 211 207 204 200	P[4:0]_LED2	Output	Parallel LED outputs – one for each port. This active low LED pin directly drives an LED in Parallel LED mode. It can be configured to display many options. P[1:0]_LED2 can be used to configure certain parameters in the PHY. P[4:0]_LED2 are driven active low whenever RESETn is active low. See Part 3 of the 3 part 88E6208/88E6218 datasheet for LED display and configuration options.
214 210 206 203 199	P[4:0]_LED1	Output	Parallel LED outputs – one for each port. This active low LED pin directly drives an LED in Parallel LED mode. It can be configured to display many options. P[1:0]_LED1 can be used to configure certain parameters in the PHY. P[4:0]_LED1 are driven active low whenever RESETn is active low. See Part 3 of the 3 part 88E6208/88E6218 datasheet for LED display and configuration options.
213 209 205 201 198	P[4:0]_LED0	Output	Parallel LED outputs – one for each port. This active low LED pin directly drives an LED in Parallel LED mode. It can be configured to display many options. P[1:0]_LED0 can be used to configure certain parameters in the PHY. P[4:0]_LED0 are driven active low whenever RESETn is active low. See Part 3 of the 3 part 88E6208/88E6218 datasheet for LED display and configuration options.

Table 5: Regulator, Reference & Clock

216-LQFP Package Pin #	Pin Name	Pin Type	Description
7	RSET	Analog	Resistor reference. A 2.0 kΩ 1% resistor is placed between the RSET and VSS. This resistor is used to set an internal bias reference current.
5	CONTROL_15	Analog	Voltage control to external 1.5V regulator. This signal controls an external PNP transistor to generate the 1.5V power supply for the VDD and VDDAL pins.
6	CONTROL_25	Analog	Voltage control to external 2.5V regulator. This signal controls an external PNP transistor to generate the 2.5V power supply for the VDDO and VDDAH pins.
164	XTAL_IN	Input	25 MHz system reference clock input provided from the board. The clock source can come from an external crystal or an external oscillator. This is the only clock required as it is used for the Switch, the PHYs, and the CPU. Refer to section 4.6.3 for XTAL_IN timing requirements.
165	XTAL_OUT	Output	System reference clock output provided to the board. This output can only be used to drive an external crystal. It cannot be used to drive external logic. If an external oscillator is used this pin should be left unconnected.
51	RESETn	Input	Hardware reset. Active low. The 88E6208/88E6218 is configured during reset. When RESETn is low all configuration pins become inputs and the value seen on these pins is latched on the rising edge of RESETn or some time after. Refer to section 4.6.2 of the AC Electrical Specifications for Reset and Configuration Timing details.
59 58	CLKSEL[1:0] (88E6208 only)	Typically Output Input Only During RESETn	CPU clock speed selection (for Rev. A and Rev. B of the 88E6208 only). During normal operation these pins are outputs driving undefined data. During reset these pins become inputs and the value seen on these pins is latched on the rising edge of RESETn or some time after. See Table 13, “Switch/CPU Interface Configuration Pins,” on page 42 for configuration information. These pins become no connect (NC) on future revisions of the 88E6208, and the CPU clock speed selection will move to M_A[17:16]. To maintain compatibility of the 88E6208, board designs should support CPU clock speed selection on both the CLKSEL[1:0] and M_A[17:16] pins.

Table 6: General Purpose I/O – JTAG & Debug

216-LQFP Package Pin #	Pin Name	Pin Type	Description
152 153 155 156 157 158 159 160 161 168 170 171 172 173 174 175	GPIO[15:0]	I/O	General Purpose I/O. These pins can be programmed to perform many functions besides I/O pins under software control. These include Serial EEPROM interface, Software controlled LEDs, LEDs for switch Port 5, Interrupt inputs to the CPU, and Watch Dog Reset output. Not all functions can be supported at one time. Refer to "Section 5 GPIO Interface", in Part 2 of the 3 part 88E6208/88E6218 datasheet for more information on which GPIO pins can perform a particular function. GPIO[15:0] are tri-stated during RESETn and are internally pulled high so they can be left unconnected if not used.
52	UART_RX	Input	UART Receive Input. This is the input to the device's general purpose UART. UART_RX is internally pulled high so it can be left unconnected if not used.
53	UART_TX	Output	UART Transmit Output. This is the output from the device's general purpose UART.
47	TCK	Input	JTAG test clock. TCK is internally pulled high so it can be left unconnected if not used.
46	TDI	Input	JTAG test data input. TDI is internally pulled high so it can be left unconnected if not used.
49	TDO	Output	JTAG test data output.
48	TMS	Input	JTAG test mode select for the device's pins and for the PHY. TMS is internally pulled high so it can be left unconnected if not used.
45	TMS_ARM	Input	JTAG test mode select for the ARM Event Trace Manager. TMS_ARM is internally pulled high so it can be left unconnected if not used.

Table 6: General Purpose I/O – JTAG & Debug (Continued)

216-LQFP Package Pin #	Pin Name	Pin Type	Description
44	TRSTn	Input	Active low JTAG Test Interface and ARM Event Trace Manager reset. TRSTn is internally pulled high. If the JTAG Test Interface is not being used, TRSTn must be low: - If the JTAG Test Interface will never be used, TRSTn can be tied to VSS. - If the JTAG Test Interface will be used periodically (like for manufacturing testing or software debug), TRSTn can be pulled low to VSS using a 10 kΩ resistor.
176	RTCK	Output	Return Clock. When using the ARM's JTAG controller (for the ARM's Event Trace Manager), this output provides the return clock synchronization signal for off-chip debug device (for example Multi-ICE). The debug device issues a TCK signal that cannot not progress to next TCK until RTCK is received.

Table 7: SDRAM, FLASH & Device Interface

216-LQFP Package Pin #	Pin Name	Pin Type	Description
110	M_CLK_OUT	Output	Memory clock output. Connect this pin to the CLK (clock) pin on SDRAM memories and to the M_CLK_IN pin described below. The frequency of this pin is the frequency of the CPU core and they run synchronously.
107	M_CLK_IN	Input	Memory clock input. Connect this pin to the M_CLK_OUT pin described above. It is used to adjust the read timing when reading the data from the SDRAM memories.
65	BOOTCSn	Output	Boot chip select (typically FLASH), active low. Connect this pin to the boot FLASH memory CEn (chip enabled) pin.
56	M_CSn[2] (88E6218 only)	Output	SDRAM or device chip select, active low. Each chip select can be programmed by software to be an SDRAM type using multiplexed addresses or a non-multiplexed device like FLASH or some other device. Each chip select has its own address space and can have independent timing.
57 85	M_CSn[1:0]	Output	
66	M_STATUS (88E6218 only)	Input	Memory Status. This pin accepts Ready/Busy# status indication for FLASH memory devices so software can determine when the FLASH device is ready for the next write operation. The value on this pin is readable in the memory controller's Control and Status register. 88E6208 does not support the M_STATUS pin. A GPIO pin can be used instead. M_STATUS contains a internal pull-up resistor so the pin can be left unconnected if not used.
84	RASn/ OEn	Output	Row address strobe, active low. Connect this pin to RASn (row address strobe) on SDRAM memories and to OEn (output enable) on device (FLASH) memories.
83	CASn/ WPn	Output	Column address strobe, active low. Connect this pin to CASn (column address strobe) on SDRAM memories and to WPn (write protect) on device (FLASH) memories.
81	WEn	Output	Write enable, active low. Connect this pin to WEn (write enable) on SDRAM and device (FLASH) memories.

Table 7: SDRAM, FLASH & Device Interface (Continued)

216-LQFP Package Pin #	Pin Name	Pin Type	Description
106 105 90 104 102 101 99 98 97 96 94 93 91	M_A[12:0]	Typically Output Input only during RESETn	Memory Address. Connect these pin to the multiplexed address pins on SDRAM memories and to address 12:0 on device (FLASH) memories. M_A[12:0] contain internal resistors (most are internal pull-ups, but some are internal pull-downs) that are used to configure the 88E6208/88E6218 during a hardware reset. When RESETn is asserted, these pins become inputs and the desired configuration value is latched at the rising edge of RESETn. See Table 12, “CPU Configuration Pins,” on page 41 and Table 14, “Switch Configuration Pins,” on page 42 for configuration information.
88 87	BA[1:0]/ M_A[14:13]	Typically Output Input only during RESETn	Bank Select. Connect these pin to the bank select pins on SDRAM memories and to address 14:13 on device (FLASH) memories. BA[1:0] contain internal resistors that are used to configure the 88E6208/88E6218 during a hardware reset. When RESETn is asserted, these pins become inputs and the desired configuration value is latched at the rising edge of RESETn. See Table 14, “Switch Configuration Pins,” on page 42 for configuration information.
139 138	DQMn[3:2]/ M_A[17:16], (DQMn[3:2] 88E6218 only)	Typically Output Input only during RESETn	Date byte enables, active low. Connect these pins to DQMn[3:2] (byte enables) on SDRAM memories and to address 17:16 on device (FLASH) memories. For 88E6208, DQMn[3] becomes M_A[17], and DQMn[2] becomes M_A[16]. See Table 12, “CPU Configuration Pins,” on page 41 for M_A[17] and M_A[16] details.
112 79	DQMn[1:0]/ M_A[15], BYTEn	Typically Output	Date byte enables, active low. Connect these pins to DQMn[1:0] (byte enables) on SDRAM memories and to address 15 on device (FLASH) memories. For 88E6208/88E6218, DQMn[1] becomes M_A[15]. DQMn[0] becomes BYTEn which can be used to configure the (FLASH) device to word or byte mode.

Table 7: SDRAM, FLASH & Device Interface (Continued)

216-LQFP Package Pin #	Pin Name	Pin Type	Description
58 59	M_A[23:22] (88E6218 only)	Typically Output Input only during RESETn	Memory address bits 23:22. For 88E6218, connect M_A[23:22] to address 23:22 on device (FLASH) memories (these pins are not used for SDRAMs). M_A[23:22] contain internal resistors that are used to configure the 88E6218 during a hardware reset. When RESETn is asserted, these pins become inputs and the desired configuration value is latched at the rising edge of RESETn. See Table 12, “CPU Configuration Pins,” on page 41 for configuration information.
61 62 63 64	M_A[21:18]	Typically Output Input only during RESETn	Memory address bits 21:18. For 88E6208/88E6218, connect M_A[21:18] to address 21:18 on device (FLASH) memories (these pins are not used for SDRAMs). M_A[21:18] contain internal resistors that are used to configure the 88E6208/88E6218 during a hardware reset. When RESETn is asserted, these pins become inputs and the desired configuration value is latched at the rising edge of RESETn. See Table 13, “Switch/CPU Interface Configuration Pins,” on page 42 for configuration information.
150 149 147 146 144 143 141 140 136 134 131 130 129 128 126 125	M_D[31:16] (88E6218 only)	I/O	Memory data. For the 88E6218, these pins form the upper 16-bits of a 32-bit wide memory data bus used to connect the ARM CPU to external SDRAM, FLASH and/or other devices. M_D[31:0] is used for 32-bit wide SDRAM or devices. Make sure the device width used is correctly configured in the memory controller’s registers.

Table 7: SDRAM, FLASH & Device Interface (Continued)

216-LQFP Package Pin #	Pin Name	Pin Type	Description
113 114 116 117 119 121 122 123 78 76 75 74 73 71 69 67	M_D[15:0]	I/O	Memory data. For the 88E6218, these pins form the lower 16 bits of a 32-bit wide memory data bus used to connect the ARM CPU to external SDRAM, FLASH and/or other devices. For the 88E6208, these pins form the complete 16-bit wide memory data bus used to connect the ARM CPU to external SDRAM, FLASH and/or other devices. If the device (FLASH or other device) is 8-bits wide, connect it to M_D[7:0]. If the SDRAM or device is 16-bits wide, connect it to M_D[15:0].

Table 8: Switch Port 6's Input MII - 88E6218 Only

216-LQFP Package Pin #	Pin Name	Pin Type	Description
188	P6_INCLK	I/O	Input Clock. P6_INCLK is a reference for P6_INDV and P6_IND[3:0]. The direction and speed of P6_INCLK is determined by P6_MODE[3:0] at the end of RESETn. If the port is in PHY Mode, P6_INCLK is an output. In this mode the frequency of the clock will be 25 MHz if the port is in 100BASE-X mode, and 2.5 MHz if the port is in 10BASE-T mode and 50 MHz for 200BASE mode. P6_INCLK is not used in RMII mode. If the port is in MAC Mode, P6_INCLK is an input. In this mode the frequency of the clock can be anywhere from DC to 25 MHz or 50 MHz although it should be 25 MHz for 100BASE-X mode and 2.5 MHz for 10BASE-T mode. 50 MHz is needed for 200BASE mode. P6_INCLK is not used in RMII mode. P6_INCLK is tri-stated during RESETn and it is internally pulled high so the pin can be left unconnected if not used.
189 190 191 192	P6_IND[3:0]	Input	Input Data. P6_IND[3:0] receives the data nibble to be transmitted into the switch in 100BASE-X and 10BASE-T modes. P6_IND[3:0] is synchronous to P6_INCLK (or P6_OUTCLK in RMII mode). These pins are inputs regardless of the port's mode (i.e., PHY mode or MAC mode). Only P6_IND0 is used when SNI mode is selected. P6_IND[1:0] are used when RMII mode is selected. P6_IND[3:0] are internally pulled high via resistor so the pins can be left unconnected when they are not used.
193	P6_INDV	Input	Input Data Valid. When P6_INDV is asserted high, data on P6_IND[3:0] is encoded and transmitted into the switch. P6_INDV must be synchronous to P6_INCLK (or P6_OUTCLK in RMII mode). P6_INDV is internally pulled low via resistor so the pin can be left unconnected when it is not used.

Table 9: Switch Port 6's Output MII - 88E6218 Only

216-LQFP Package Pin #	Pin Name	Pin Type	Description
187	P6_OUTCLK	I/O	Output Clock. P6_OUTCLK is a reference for P6_OUTDV, P6_OUTD[3:0], and P6_INDV and P6_IND[1:0] in RMII mode. The direction and speed of P6_OUTCLK is determined by P6_MODE[3:0] at the end of RESETn. If the port is in PHY Mode, P6_OUTCLK is an output. In this mode the frequency of the clock will be 25 MHz if the port is in 100BASE-X mode, and 2.5 MHz if the port is in 10BASE-T mode and 50 MHz for 200BASE mode and RMII mode. If the port is in MAC Mode, P6_OUTCLK is an input. In this mode the frequency of the clock can be anywhere from DC to 25MHz or 50 MHz although it should be 25 MHz for 100BASE-X mode and 2.5 MHz for 10BASE-T mode and 50 MHz for 200BASE mode. MAC mode RMII mode is not supported. P6_OUTCLK is tri-stated during RESETn and it is internally pulled high so the pin can be left unconnected if not used.
179 180 182 184	P6_OUTD[3:0]/ P6_MODE[3:0]	Normally Output Input only when RESETn is low	Output Data. Data transmitted from the switch is decoded and presented on P6_OUTD[3:0] pins synchronous to P6_OUTCLK. These pins are outputs regardless of the port's mode (i.e., PHY or MAC mode). Only P6_OUTD0 contains meaningful data when SNI mode is selected. P6_OUTD[1:0] are used when RMII mode is selected. During RESETn these internally pulled high pins are tri-stated and used to latch in the desired operating mode for the port as described in Table 14.
186	P6_OUTDV/ DISABLE_P6	Output	Output Data Valid. When P6_OUTDV is asserted high, data transmitted from the switch is decoded and presented on P6_OUTD[3:0]. P6_OUTDV is synchronous to P6_OUTCLK. During RESETn this internally pulled high pin is tri-stated and used to latch in the enable value for switch Port 6. If this pin is high or left unconnected during RESETn Port 6 will be disabled. Use a 4.7 kΩ resistor to VSS to enable Port 6.

Table 9: Switch Port 6's Output MII - 88E6218 Only (Continued)

216-LQFP Package Pin #	Pin Name	Pin Type	Description
177	P6_CRS	I/O	Carrier Sense. After RESETn, P6_CRS becomes an output if PHY Mode is selected for this port. It remains an input if MAC Mode is selected. P6_CRS asserts (or is expected to be asserted) when the receive data path is non-idle. In half-duplex mode P6_CRS is also asserted (or is expected to be asserted) during transmission. P6_CRS is asynchronous to P6_OUTCLK and P6_INCLK. P6_CRS is tri-stated during RESETn and it is internally pulled low so the pin can be left unconnected if not used.
178	P6_COL	I/O	Collision. After RESETn, P6_COL becomes an output if PHY Mode is selected for this port. It remains an input if MAC Mode is selected. P6_COL asserts (or is expected to be asserted) only in half-duplex mode when both the transmit and receive paths are non-idle. In full-duplex mode, P6_COL is always low (or it is ignored). P6_COL is asynchronous to P6_OUTCLK and P6_INCLK. P6_COL is tri-stated during RESETn and it is internally pulled low so the pin can be left unconnected if not used.

Table 10: External SMI Register Access Interface - 88E6218 Only

216-LQFP Package Pin #	Pin Name	Pin Type	Description
195	MDC	Output	MDC is the management data clock reference for the serial management interface (SMI). A continuous clock stream is not generated. MDC occurs only when an SMI operation is taking place. MDC's frequency is the CPU's core clock frequency divided by 64 (2.08 MHz @ 133 MHz CPU speed). The SMI is used to access the registers in external devices like PHYs that could be connected to Port 6's MII. MDC is internally pulled high via a resistor so it can be left floating when unused.
194	MDIO	I/O	MDIO is the management data. MDIO is used to transfer management data in and out of the device synchronously to MDC. This pin requires an external pull-up resistor in the range of 1.5 kΩ to 10 kΩ. The 88E6218 internal switch uses 16 of the 32 possible SMI port addresses. The 16 that are used are selectable using the M_A[3] configuration pin (see Table 14 for details). MDIO is internally pulled high via a resistor so it can be left floating when unused.

Table 11: Power & Ground

216-LQFP Package Pin #	Pin Name	Pin Type	Description
50 60 68 77 80 86 95 103 111 115 124 132 133 142 151 166 169 183 202 212	VDDO	Power	3.3 volt Power to digital I/O.
9 22 36	VDDAH	Power	2.5 volt Power to analog core.
12 19 25 33 39	VDDAL	Power	1.5 volt Power to analog core.
4 43 72 89 100 120 135 148 167 181 208	VDD	Power	1.5 volt Power to digital core.

Table 11: Power & Ground (Continued)

216-LQFP Package Pin #	Pin Name	Pin Type	Description
1 13 18 26 27 32 40 54 55 70 82 92 108 109 118 127 137 145 154 162 163 185 197 216	VSS	Ground	Ground to digital I/O and core.
Exposed Die Pad	VSS	Ground	Solder the exposed die pad to the PCB for best thermal and electrical performance. Contact Marvell FAEs for information on PCB layout recommendations.

Table 11: Power & Ground (Continued)

216-LQFP Package Pin #	Pin Name	Pin Type	Description
56 58 59 66 125 126 128 129 130 131 134 136 140 141 143 144 146 147 149 150 177 178 179 180 182 184 186 187 188 189 190 191 192 193 194 195	NC	No Connect	88E6208 Only. Do not connect these pins to anything. These pins are not to be connected.

1.1.2 88E6208 216-Pin LQFP Pin Assignment List - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
87	BA[0]/M_A[13]	97	M_A[4]
88	BA[1]/M_A[14]	98	M_A[5]
65	BOOTCSn	99	M_A[6]
83	CASn/WPn	101	M_A[7]
58	CLKSEL[0]	102	M_A[8]
59	CLKSEL[1]	104	M_A[9]
2	CONFIG_A	90	M_A[10]
3	CONFIG_B	105	M_A[11]
5	CONTROL_15	106	M_A[12]
6	CONTROL_25	138	M_A[16]
79	DQMn[0]/BYTEn	139	M_A[17]
112	DQMn[1]/M_A[15]	64	M_A[18]
--	Exposed Die Pad	63	M_A[19]
175	GPIO[0]	62	M_A[20]
174	GPIO[1]	61	M_A[21]
173	GPIO[2]	107	M_CLK_IN
172	GPIO[3]	110	M_CLK_OUT
171	GPIO[4]	85	M_CSn[0]
170	GPIO[5]	57	M_CSn[1]
168	GPIO[6]	67	M_D[0]
161	GPIO[7]	69	M_D[1]
160	GPIO[8]	71	M_D[2]
159	GPIO[9]	73	M_D[3]
158	GPIO[10]	74	M_D[4]
157	GPIO[11]	75	M_D[5]
156	GPIO[12]	76	M_D[6]
155	GPIO[13]	78	M_D[7]
153	GPIO[14]	123	M_D[8]
152	GPIO[15]	122	M_D[9]
91	M_A[0]	121	M_D[10]
93	M_A[1]	119	M_D[11]
94	M_A[2]	117	M_D[12]
96	M_A[3]	116	M_D[13]

Pin #	Pin Name	Pin #	Pin Name
114	M_D[14]	194	NC
113	M_D[15]	195	NC
56	NC	198	P0_LED0
66	NC	199	P0_LED1
125	NC	200	P0_LED2
126	NC	11	P0_RXN
128	NC	10	P0_RXP
129	NC	15	P0_TXN
130	NC	14	P0_TXP
131	NC	201	P1_LED0
134	NC	203	P1_LED1
136	NC	204	P1_LED2
140	NC	20	P1_RXN
141	NC	21	P1_RXP
143	NC	16	P1_TXN
144	NC	17	P1_TXP
146	NC	205	P2_LED0
147	NC	206	P2_LED1
149	NC	207	P2_LED2
150	NC	24	P2_RXN
177	NC	23	P2_RXP
178	NC	29	P2_TXN
179	NC	28	P2_TXP
180	NC	209	P3_LED0
182	NC	210	P3_LED1
184	NC	211	P3_LED2
186	NC	34	P3_RXN
187	NC	35	P3_RXP
188	NC	30	P3_TXN
189	NC	31	P3_TXP
190	NC	213	P4_LED0
191	NC	214	P4_LED1
192	NC	215	P4_LED2
193	NC	38	P4_RXN

Pin #	Pin Name	Pin #	Pin Name
37	P4_RXP	19	VDDAL
42	P4_TXN	25	VDDAL
41	P4_TXP	33	VDDAL
196	P0_CONFIG	39	VDDAL
8	P0_SDET	50	VDDO
84	RASn/OEn	60	VDDO
51	RESETn	68	VDDO
7	RSET	77	VDDO
176	RTCK	80	VDDO
47	TCK	86	VDDO
46	TDI	95	VDDO
49	TDO	103	VDDO
48	TMS	111	VDDO
45	TMS_ARM	115	VDDO
44	TRSTn	124	VDDO
52	UART_RX	132	VDDO
53	UART_TX	133	VDDO
4	VDD	142	VDDO
43	VDD	151	VDDO
72	VDD	166	VDDO
89	VDD	169	VDDO
100	VDD	183	VDDO
120	VDD	202	VDDO
135	VDD	212	VDDO
148	VDD	1	VSS
167	VDD	13	VSS
181	VDD	18	VSS
208	VDD	26	VSS
9	VDDAH	27	VSS
22	VDDAH	32	VSS
36	VDDAH	40	VSS

Pin #	Pin Name	Pin #	Pin Name
54	VSS	154	VSS
55	VSS	162	VSS
70	VSS	163	VSS
82	VSS	185	VSS
92	VSS	197	VSS
109	VSS	216	VSS
118	VSS	81	WEn
127	VSS	164	XTAL_IN
137	VSS	165	XTAL_OUT
145	VSS	--	--

1.1.3 88E6218 216-Pin LQFP Pin Assignment List - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
87	BA[0]/M_A[13]	97	M_A[4]
88	BA[1]/M_A[14]	98	M_A[5]
65	BOOTCSn	99	M_A[6]
83	CASn/WPn	101	M_A[7]
2	CONFIG_A	102	M_A[8]
3	CONFIG_B	104	M_A[9]
5	CONTROL_15	90	M_A[10]
6	CONTROL_25	105	M_A[11]
79	DQMn[0]/BYTEn	106	M_A[12]
112	DQMn[1]/M_A[15]	64	M_A[18]
138	DQMn[2]/M_A[16]	63	M_A[19]
139	DQMn[3]/M_A[17]	62	M_A[20]
--	Exposed Die Pad	61	M_A[21]
175	GPIO[0]	59	M_A[22]
174	GPIO[1]	58	M_A[23]
173	GPIO[2]	107	M_CLK_IN
172	GPIO[3]	110	M_CLK_OUT
171	GPIO[4]	85	M_CSn[0]
170	GPIO[5]	57	M_CSn[1]
168	GPIO[6]	56	M_CSn[2]
161	GPIO[7]	67	M_D[0]
160	GPIO[8]	69	M_D[1]
159	GPIO[9]	71	M_D[2]
158	GPIO[10]	73	M_D[3]
157	GPIO[11]	74	M_D[4]
156	GPIO[12]	75	M_D[5]
155	GPIO[13]	76	M_D[6]
153	GPIO[14]	78	M_D[7]
152	GPIO[15]	123	M_D[8]
91	M_A[0]	122	M_D[9]
93	M_A[1]	121	M_D[10]
94	M_A[2]	119	M_D[11]
96	M_A[3]	117	M_D[12]

Pin #	Pin Name	Pin #	Pin Name
116	M_D[13]	20	P1_RXN
114	M_D[14]	21	P1_RXP
113	M_D[15]	16	P1_TXN
125	M_D[16]	17	P1_TXP
126	M_D[17]	205	P2_LED0
128	M_D[18]	206	P2_LED1
129	M_D[19]	207	P2_LED2
130	M_D[20]	24	P2_RXN
131	M_D[21]	23	P2_RXP
134	M_D[22]	29	P2_TXN
136	M_D[23]	28	P2_TXP
140	M_D[24]	209	P3_LED0
141	M_D[25]	210	P3_LED1
143	M_D[26]	211	P3_LED2
144	M_D[27]	34	P3_RXN
146	M_D[28]	35	P3_RXP
147	M_D[29]	30	P3_TXN
149	M_D[30]	31	P3_TXP
150	M_D[31]	213	P4_LED0
66	M_STATUS	214	P4_LED1
195	MDC	215	P4_LED2
194	MDIO	38	P4_RXN
198	P0_LED0	37	P4_RXP
199	P0_LED1	42	P4_TXN
200	P0_LED2	41	P4_TXP
11	P0_RXN	196	P0_CONFIG
10	P0_RXP	8	P0_SDET
15	P0_TXN	178	P6_COL
14	P0_TXP	177	P6_CRS
201	P1_LED0	188	P6_INCLK
203	P1_LED1	192	P6_IND[0]
204	P1_LED2	191	P6_IND[1]

Pin #	Pin Name	Pin #	Pin Name
190	P6_IND[2]	9	VDDAH
189	P6_IND[3]	22	VDDAH
193	P6_INDV	36	VDDAH
187	P6_OUTCLK	12	VDDAL
184	P6_OUTD[0]/P6_MODE[0]	19	VDDAL
182	P6_OUTD[1]/P6_MODE[1]	25	VDDAL
180	P6_OUTD[2]/P6_MODE[2]	33	VDDAL
179	P6_OUTD[3]/P6_MODE[3]	39	VDDAL
186	P6_OUTDV/DISABLE_P6	50	VDDO
84	RASn/OEn	60	VDDO
51	RESETn	68	VDDO
7	RSET	77	VDDO
176	RTCK	80	VDDO
47	TCK	86	VDDO
46	TDI	95	VDDO
49	TDO	103	VDDO
48	TMS	111	VDDO
45	TMS_ARM	115	VDDO
44	TRSTn	124	VDDO
52	UART_RX	132	VDDO
53	UART_TX	133	VDDO
4	VDD	142	VDDO
43	VDD	151	VDDO
72	VDD	166	VDDO
89	VDD	169	VDDO
100	VDD	183	VDDO
120	VDD	202	VDDO
135	VDD	212	VDDO
148	VDD	1	VSS
167	VDD	13	VSS
181	VDD	18	VSS
208	VDD	27	VSS

Pin #	Pin Name	Pin #	Pin Name
26	VSS	137	VSS
32	VSS	145	VSS
40	VSS	154	VSS
54	VSS	162	VSS
55	VSS	163	VSS
70	VSS	185	VSS
82	VSS	197	VSS
92	VSS	216	VSS
108	VSS	81	WEn
109	VSS	164	XTAL_IN
118	VSS	165	XTAL_OUT
127	VSS	--	--

Section 2. Reset and Initialization

The 88E6208/88E6218 uses certain pins as configuration inputs to set parameters following a reset. The definition of these configuration pins changes after reset to their normal function. The following tables list and define the pins that affect the CPU, Switch/CPU interface, Switch, and PHY configuration. These pins require a 4.7 kΩ connection to VSS or VDDO to override the internal resistor's default.

Table 12: CPU Configuration Pins

Pin	Configuration Function
M_A[18]	Flash Boot Device Width
	1 = 8-bit boot device (default) 0 = 16-bit boot device **NOTE:** Internally pulled high to 1.
{M_A[10],M_A[22], M_A[23]}	Core Frequency Selector (88E6218 only)
	000 = Reserved for Internal Use only. 001 = 143 MHz (only if part is speed marked accordingly) 010 = 83 MHz 011 = 100 MHz 100 = 125 MHz 101 = 133 MHz (default) 110 = 150 MHz (only if part is speed marked accordingly) 111 = Reserved for internal use only **NOTE:** Internally pulled to 3'b101.
{M_A[10],M_A[16], M_A[17]} (In future revisions) or {M_A[10], CLKSEL[1], CLKSEL[0]} (In Rev A and Rev B)	Core Frequency Selector (88E6208 only)
	000 = Reserved for internal use only 001 = Reserved for internal use only 010 = 83 MHz 011 = 100 MHz 100 = 125 MHz 101 = 133 MHz (default) 110 = Reserved for internal use only 111 = Reserved for internal use only **NOTE:** Internally pulled to 3'b101. **NOTE:** In 88E6208 Rev A and Rev B, M_A[17:16] do not perform this function. Instead, this function is performed by the CLKSEL[1:0] pins. Future versions of the 88E6208 will not have the CLKSEL[1:0] pins. The M_A[17:16] pins will be used instead. Clock selection options should be done on both the CLKSEL[1:0] and the M_A[17:16] pins (at least as PCB stuffing options) to maintain compatibility with future revisions of the 88E6208.
M_A[7:6]	PCB Options
	User definable configuration bits that are readable as defined in Part 2 of the 3 part 88E6208/ 88E6218 datasheet. **NOTE:** Internally pulled high to 1.

Table 13: Switch/CPU Interface Configuration Pins

Pin	Configuration Function
M_A[20]	Port 5 runs at 2.5 MHz MII
	1 = Switch Port 5 runs at the rate determined by M_A[21] (default) 0 = Switch Port 5 runs at 2.5 MHz MII 10 Mbps PHY Mode, driving clocks to CPU's UniMAC **NOTE:** Internally pulled high 1.
M_A[21]	Port 5 200BASE Mode (88E6218 only)
	0 = Switch Port 5 runs in 25 MHz MII 100 Mbps PHY Mode, driving clocks to CPU's UniMAC (default) 1 = Switch Port 5 runs in 50 MHz MII 200 Mbps PHY Mode, driving clocks to CPU's UniMAC (88E6218 only) **NOTE:** Internally pulled low to 0.

Table 14: Switch Configuration Pins

Pin	Configuration Function
M_A[0]	Switch Test Mode
	1 = Switch ports come up in the disabled port state - Software must enable the switch ports only after software is done configuring the switch (like defining the port based VLANs for fire-wall protection). 0 = Switch ports come up in the forwarding port state (for test purposes only) **NOTE:** Internally pulled high to 1.
M_A[3]	SMI Address
	1 = Internal switch uses SMI Device addresses 0x10 to 0x1F (default) 0 = Internal switch uses SMI Device addresses 0x00 to 0x0F **NOTE:** Internally pulled high to 1.
BA[1]/M_A[14]	Full-Duplex Flow Control Disable
	1 = Disable full-duplex flow control as defined in the switch - This mode can be overridden on a port-by-port basis by using the port's Force Flow Control bit. 0 = Enable full-duplex flow control on all full-duplex ports as defined in the switch **NOTE:** Internally pulled high to 1.
BA[0]/M_A[13]	Half-Duplex Flow Control Disable
	1 = Disable half-duplex flow control on all half-duplex ports as defined in the switch - This mode can be overridden on a port-by-port basis by using the port's Force Flow Control bit. 0 = Enable half-duplex flow control on all half-duplex ports as defined in the switch **NOTE:** Internally pulled high to 1.

Table 14: Switch Configuration Pins (Continued)

Pin	Configuration Function
P6_OUTD[3:0]	Port 6 Configuration (88E6218 only)
	0000 = PHY half-duplex SNI 10 Mbps Rising edge clock with collision active low 0001 = PHY half-duplex SNI 10 Mbps Rising edge clock with collision active high 0010 = PHY full-duplex SNI 10 Mbps Rising edge clock (collision is don't care) 0011 = MAC full-duplex MII 200 Mbps 50 MHz MII input clock mode 0100 = PHY half-duplex SNI 10 Mbps Falling edge clock with collision active low 0101 = PHY half-duplex SNI 10 Mbps Falling edge clock with collision active high 0110 = PHY full-duplex SNI 10 Mbps Falling edge clock (collision is don't care) 0111 = PHY full-duplex MII 200 Mbps 50 MHz MII output clock mode 1000 = MAC half-duplex MII 0 -100 Mbps DC to 25 MHz MII input clock mode 1001 = PHY half-duplex RMII 100 Mbps 50 MHz Reduced MII output clock mode 1010 = MAC full-duplex MII 0 -100 Mbps DC to 25 MHz MII input clock mode 1011 = PHY full-duplex RMII 100 Mbps 50 MHz Reduced MII output clock mode 1100 = PHY half-duplex MII 10 Mbps 2.5 MHz MII output clock mode 1101 = PHY half-duplex MII 100 Mbps 25 MHz MII output clock mode 1110 = PHY full-duplex MII 10 Mbps 2.5 MHz MII output clock mode 1111 = PHY full-duplex MII 100 Mbps 25 MHz MII output clock mode (default) **NOTE:** Internally pulled high to 1.
P6_OUTDV	Port 6 Disable (88E6218 only)
	1 = Disabled 0 = Enabled **NOTE:** Internally pulled high to 1.

Table 15: PHY Configuration Pins

Pin	Configuration Function
CONFIG_A	Global Configuration A
	This global configuration pin is used to set the default LED mode and Far-End Fault Indication (FEFI) mode by connecting these pins to other device pins as follows: VSS = LED Mode 0, FEFI disabled P0_LED0 = LED Mode 0, FEFI enabled P0_LED1 = LED Mode 1, FEFI disabled P0_LED2 = LED Mode 1, FEFI enabled P1_LED0 = LED Mode 2, FEFI disabled P1_LED1 = LED Mode 2, FEFI enabled P1_LED2 = LED Mode 3, FEFI disabled VDDO = LED Mode 3, FEFI enabled (default) The FEFI and the LED modes are explained in Part 3 of the 3 part 88E6208/88E6218 datasheet. **NOTE:** Internally pulled high to 1.
CONFIG_B	Global Configuration B
	This global configuration pin is used to set the default mode for Auto-Crossover, the PHY driver type and Energy Detect by connecting these pins to other device pins as follows: VSS = No Crossover, Backplane drivers, Energy Detect disabled P0_LED0 = No Crossover, CAT 5 drivers, Energy Detect enabled P0_LED1 = No Crossover, Backplane drivers, Energy Detect disabled P0_LED2 = No Crossover, CAT 5 drivers, Energy Detect enabled P1_LED0 = Auto Crossover, Backplane drivers, Energy Detect disabled P1_LED1 = Auto Crossover, CAT 5 drivers, Energy Detect enabled P1_LED2 = Auto Crossover, Backplane drivers, Energy Detect disabled VDDO = Auto Crossover, CAT 5 drivers, Energy Detect enabled (default) Auto crossover, Back Plane vs. CAT 5 drivers, and Energy Detect are covered in Part 3 of the 3 part 88E6208/88E6218 datasheet. **NOTE:** Internally pulled high to 1.
P0_CONFIG	Port 0 Configuration
	The P0_CONFIG pin is used to set the default configuration for Port 0 by connecting these pins to other device pins as follows: VSS = Auto-Negotiation enabled (default) P0_LED1 = Forced 10BASE-T half-duplex P0_LED2 = Forced 10BASE-T full-duplex P1_LED0 = Forced 100BASE-TX half-duplex P1_LED1 = Forced 100BASE-TX full-duplex P1_LED2 = Forced 100BASE-FX half-duplex VDDO = Forced 100BASE-FX full-duplex Ports 1, 2, 3 and 4's default configuration is Auto-Negotiation enabled. Any port's default configuration can be modified by accessing the PHY registers by a CPU. However, fiber mode vs. copper mode cannot be configured in this way. Fiber vs. copper must be selected at Reset by using the P[0]_CONFIG pin. **NOTE:** Internally pulled low to 0.

Section 3. Functional Description

The datasheet for the 88E6208/88E6218 has been separated along major functional block lines. This portion of the datasheet (Part 1) contains the common information about the part; its pinout, pinlist, electrical data, etc. The CPU along with its peripherals, including the CPU's Unified Media Access Controller (UniMAC™), is covered in Part 2 of this datasheet. The Switch along with its PHYs and it's MAC to the CPU is covered in Part 3.

The 88E6208/88E6218 devices contain two major functional blocks, the CPU and the Switch. These two blocks are connected internally via a standard IEEE Ethernet MII with Ethernet MACs on both sides of the interface. This implementation is identical to previous 'multiple-chip' solutions, so the software architecture and programmer's interface are the same as earlier products, making the job of porting previous software easier.

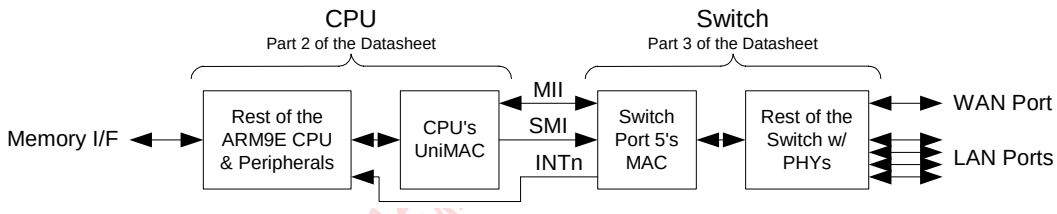
The I/O registers in the Switch and in the PHYs are accessed in the same way as before. The CPU's UniMAC contains a SMI (Serial Management Interface) master block connected to the Switch and PHYs. The 88E6218 device supports an external 10/100/200 Mbps MII connected to Switch Port 6. In this device, the CPU's SMI master block not only connects to the internal Switch and PHYs, it also exits the 88E6218 device through the device's MDC/MDIO pins. An external SMI slave device can be connected to the 88E6218 device's MDC/MDIO pins as long as it uses unique SMI device addresses from the internal Switch and PHYs. The Switch and PHY's addresses can be configured by a pin at reset (see Section Section 2. "Reset and Initialization" on page 41).

The Switch's interrupt (which combines interrupts generated from the Switch and PHYs) is sent to the CPU's interrupt register. The IRQ interrupt sources are described in Part 2 of the 3 part 88E6208/88E6218 datasheet.

The UniMAC architecture provides an efficient networking interface between the ARM9E CPU and the 88E6208/88E6218 multi-port Ethernet switch fabric. The purpose of the UniMAC architecture is to enhance networking performance in the SOHO gateway/router application.

The UniMAC is an Ethernet MAC compatible with the IEEE 802.3 standard and contains a superset of features including extra speed and functionality. In the 88E6218, the UniMAC can operate up to double the standard clock rate, so the UniMAC runs up to 200 Mbps full-duplex (that is, 200 Mbps in both transmit and receive directions simultaneously providing a total bandwidth of 400 Mbps). In addition, the UniMAC contains multiple receive queues and multiple transmit queues (88E6218 only), which provides a higher level of routing performance by providing packet pre-queuing based upon its source and/or destination. In addition, the UniMAC accelerates Internet Protocol routing by aligning the incoming Internet Protocol data packet along a 32-bit boundary, which enables the CPU to handle packets more quickly and increases routing performance.

Figure 3: CPU & Switch Interconnect



3.1 UniMAC Interface Options

The UniMAC or MII between the CPU and the Switch works as any standard MII, but it also contains some optional improvements that can be used to accelerate routing performance.

3.1.1 UniMAC Speeds

The UniMAC interface can run at 10/100 Mbps or 200 Mbps (88E6218 only) full-duplex. The interface's speed and mode is set by Port 5's configuration pins (see Table 13, "Switch/CPU Interface Configuration Pins," on page 42).

3.1.2 Marvell Header Mode

Switch Port 5 can be set to prepend 2 bytes of data in front of each frame sent to the CPU and to remove these 2 bytes of data coming back from the CPU. This Marvell Header Mode is optional, but it can increase CPU routing performance greatly by aligning the IP data portion of the frames in the CPU's memory on 32-bit boundaries. On ingress to the CPU the Marvell Header contains information the CPU needs, like the switch's source port of the frame, its priority (88E6218 only), etc. On egress from the CPU, the CPU uses the Header to indicate the port based VLAN information of the frame so that frames sent to the LAN ports only go out the LAN ports and not out the WAN port (the header information is directly written to switch Port 5's Port Based VLAN Map register - Part 3). The Marvell Header supports the following features:

- Higher routing performance due to 32-bit IP data alignment
- The WAN port can be any port on the switch
- More than one WAN port can be used either as a hot backup or for link aggregation
- Any switch port can be a DMZ port or other port type

Refer to Part 3 of the 3 part 88E6208/88E6218 datasheet for more information on the format of the Marvell Header to and from the CPU.

The CPU's UniMAC can independently be set to process the Marvell Header or ignore it. If Switch Port 5 does not generate/use the Marvell Header then the CPU must not try to process it. If Switch Port 5 generates/uses Marvell Headers, the CPU's UniMAC can process it or ignore it.

Table 16 shows the valid options of the Switch and/or the CPU when in Marvell Header mode. Refer to Part 2 of the 3 part 88E6208/88E6218 datasheet for more information on the Marvell UniMAC settings.

Table 16: Marvell UniMAC Header Options

Switch Port 5's Header Insertion/ Removal (See Part 3)	CPU's UniMAC Receive Queue Steering Header Mode (See Part 2)	Result
Off	Disabled	• Classic MAC interface. • Frame IP data is not 32-bit aligned in CPU memory. • DA filtering supported (88E6218 only). • CPU Receive Queue QoS steering determined by CPU's MAC processing (88E6218 only). • Switch's Marvell Trailer mode must be used to determine source port of the frame and I/O register writes to Port 5's Port Based VLAN Map register is required when switching from WAN to LAN traffic.
Off	Any Mode Enabled	• Do not use this option. Undefined results will occur.
On	Disabled	• Frame IP data becomes 32-bit aligned in CPU memory. • DA filtering not supported. • CPU Receive Queue QoS steering cannot be used. • CPU can use the Marvell Header to determine source port of the frame and also use it to update Port 5's Port Based VLAN Map register on the fly without the need of I/O register writes.
On	Any Mode Enabled	• Frame IP data becomes 32-bit aligned in the CPU memory. • DA filtering is supported (88E6218 only). • CPU Receive Queue QoS steering determined by various bits in the Marvell Header. • Which Header bits utilized are selectable by registers in the CPU's UniMAC. • CPU can use the Marvell Header to determine source port of the frame and also use it to update Port 5's Port Based VLAN Map register on the fly without the need of I/O register writes.

Section 4. Electrical Specifications

4.1 Absolute Maximum Ratings

Table 17: Absolute Maximum Ratings

NOTE: Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD(3.3)}$	Power Supply Voltage on V_{DDO} with respect to V_{SS}	-0.5	3.3	+3.6	V
$V_{DD(2.5)}$	Power Supply Voltage on V_{DDAH} with respect to V_{SS}	-0.5	2.5	+3.6 or $V_{DD(3.3)}$ +0.5[1] whichever is less	V
$V_{DD(1.5)}$	Power Supply Voltage on V_{DD}, or V_{DDAL} with respect to V_{SS}	-0.5	1.5	+3.6 or $V_{DD(2.5)}$ +0.5[2] whichever is less	V
V_{PIN}	Voltage applied to any input pin with respect to V_{SS}	-0.5		+3.6 or V_{DDO} +0.5[3] whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[4]	°C

1. $V_{DD(2.5)}$ must never be more than 0.5V greater than $V_{DD(3.3)}$ or damage will result. This implies that power must be applied to $V_{DD(3.3)}$ before or at the same time as $V_{DD(2.5)}$.
2. $V_{DD(1.5)}$ must never be more than 0.5V greater than $V_{DD(2.5)}$ or damage will result. This implies that power must be applied to $V_{DD(2.5)}$ before or at the same time as $V_{DD(1.5)}$.
3. V_{PIN} must never be more than 0.5V greater than VDDO or damage will result.
4. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

4.2 Recommended Operating Conditions

Table 18: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	3.3V power supply	For pins V_{DDO}	3.135	3.3	3.465	V
$V_{DD(2.5)}$	2.5V power supply	For pins V_{DDAH}	2.375	2.5	2.625	V
$V_{DD(1.5)}$	1.5V power supply	For pins V_{DD}, V_{DDAL}	1.425	1.5	1.575	V
T_A	Ambient operating temperature		0		70	°C
T_J	Maximum junction temperature				125[1]	°C
RSET	Internal bias reference	Resistor value placed between RSET- and RSET+ pins	1980	2000	2020	Ω

1. Refer to the white paper on TJ Thermal Calculations for more Information.

4.3 Notes on Powering Up and Powering Down

When turning on power, turn on the voltage power in the following sequence: The highest voltage power VDDO must be turned on first; then, turn on the next higher voltage power for the 88E6208/88E6218, etc.

This power-up sequence must be used due to a protection diode between the two power rails. These diodes leak current if the tie-high terminal becomes tie low by an improper turn-on sequence.

When powering down, first turn off the lowest voltage and then turn off the higher voltage.

4.4 Package Thermal Data

4.4.1 Thermal Conditions for 216-pin LQFP Package

Table 19: Thermal Conditions for 216-pin LQFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient of the 216-Pin LQFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		20.5		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		17.6		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		16.6		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		16.1		°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 216-Pin LQFP package $\psi_{JT} = (T_J - T_{TOP})/P$. Ttop = Temperature on the top center of the package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.39		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		--		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		--		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		--		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 216-Pin LQFP package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		7.8		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 216-Pin LQFP package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		12.7		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

4.5 DC Electrical Characteristics

4.5.1 DC Power Characteristics

Table 20: DC Power Characteristics
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
$I_{DD(3.3)}$	3.3 volt Power to outputs	V_{DDO}	CPU @ 133 MHz		180		mA
			CPU @ 150 MHz		185		mA
$I_{DD(2.5)}$	2.5 volt[2] Power to analog core	V_{DDAH}	No link on any port		135		mA
			All ports 10 Mbps linked but idle		135		mA
			All ports 10 Mbps and active		425		mA
			All ports 100 Mbps		220		mA
$I_{DD(1.5)}$	1.5 volt Power to analog core	V_{DDAL}	No link on any port		0		mA
			All ports 10 Mbps		0		mA
			All ports 100 Mbps		30		mA
	1.5 volt Power to digital core w/CPU @ 133 MHz Add 15 mA w/CPU @ 150 MHz	V_{DD}	No link on any port		100		mA
			All ports 10 Mbps linked but idle		190		mA
			All ports 10 Mbps and active		195		mA
			All ports 100 Mbps linked but idle		240		mA
			All ports 100 Mbps and active		260		mA

1. The values listed are typical values with LED mode 3, 3 LEDs per port, and Auto-Negotiation on.
2. The 2.5V power source must supply an additional 100 mA (Typical) current from the center tap on the magnetics. (This number is not included in this table.)

4.5.2 Digital Operating Conditions

Table 21: Digital Operating Conditions
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	All pins		2.0		V_{DDO} +0.5	V
		XTAL_IN		1.4			V
V_{IL}	Low level input voltage	All pins		-0.5		0.8	V
		XTAL_IN				0.6	
V_{OH}	High level output voltage	LED pins[1]	I_{OH} = -8 mA V_{DDO} = Min	2.4			V
		XTAL_OUT	I_{OH} = -1 mA		$V_{IH(XTAL\_IN)}$ +0.2		V
		All others	I_{OH} = -4 mA V_{DDO} = Min	2.4			V
V_{OL}	Low level output voltage	LED pins[1]	I_{OL}= 8 mA			0.4	V
		XTAL_OUT	I_{OL} = 1 mA		$V_{IL(XTAL\_IN)}$ -0.2		V
		All others	I_{OL}= 4 mA			0.4	V
I_{ILK}	Input leakage current	With pull-up resistor	$0<V_{IN}<V_{DD}$			+ 10 - 50	µA
		With pull-down resistor	$0<V_{IN}<V_{DD}$			+ 50 - 10	µA
		All others	$0<V_{IN}<V_{DD}$			±10v	µA
C_{IN}	Input capacitance	All pins				5	pF

1. The LED pins are as follows: P4_LED2[2:0], P3_LED1[2:0], P2_LED2[2:0], P1_LED1[2:0], P0_LED1[2:0]

Table 22: Internal Resistor Description

Pin #	Pin Name	Resistor	Pin #	Pin Name	Resistor
2	CONFIG_A	Internal pull-up	66	M_STATUS	Internal pull-up
3	CONFIG_B	Internal pull-up	88, 87	BA[1:0]/ M_A[14:13]	Internal pull-up
44	TRSTn	Internal pull-up	106, 105, 90, 104, 102, 101, 99, 98, 97, 96, 94, 93, 91	M_A[12:0]	Internal pull-up
45	TMS_ARM	Internal pull-up	139, 138, 112, 79	DQMn[3:0]/ M_A[17:15], BYTEn	Internal pull-up[1]
46	TDI	Internal pull-up	152, 153, 155, 156, 157, 158, 159, 160, 161, 168, 170, 171, 172, 173, 174, 175	GPIO[15:0]	Internal pull-up
47	TCK	Internal pull-up	177	P6_CRS	Internal pull-down
48	TMS	Internal pull-up	178	P6_COL	Internal pull-down
49	TDO	None	179, 180, 182, 184	P6_OUTD[3:0]/ P6_MODE[3:0]	Internal pull-up
51	RESETn	None	186	P6_OUTDV/ DISABLE_P6	Internal pull-up
52	UART_RX	Internal pull-up	187	P6_OUTCLK	Internal pull-up
53	UART_TX	None	188	P6_INCLK	Internal pull-up
58 (88E6218)	M_A[23]	Internal pull-up	189, 190,191, 192	P6_IND[3:0]	Internal pull-up
58 (88E6208)	CLKSEL[0]	Internal pull-up	193	P6_INDV	Internal pull-down
59 (88E6218)	M_A[22]	Internal pull-down	194	MDIO	Internal pull-up
59 (88E6208)	CLKSEL[1]	Internal pull-down	195	MDC	Internal pull-up
61	M_A[21]	Internal pull-down	196	P0_CONFIG	Internal pull-down
62, 63, 64	M_A[20:18]	Internal pull-up			

1. In future revisions, MA_[16] will have an internal pull-down. See Table 12, “CPU Configuration Pins,” on page 41 for M_A[16] details.

4.5.3 IEEE DC Transceiver Parameters

Table 23: IEEE DC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14
-100BASE-TX ANSI X3.263-1995
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	TXP/N[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		TXP/N[1:0]	10BASE-T cable model	585[1]			mV
		TXP/N[0]	100BASE-FX mode	0.4	0.8	1.2	V
		TXP/N[1:0]	100BASE-TX mode	0.950	1.0	1.05	V
	Overshoot[2]	TXP/N[4:0]	100BASE-TX mode	0		5%	V
	Amplitude Symmetry (positive/ negative)	TXP/N[1:0]	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage accept level	RXP/N[1:0]	10BASE-T mode	585[3]			mV
		RXP/N[0] P[1:0]_SDET P/N	100BASE-FX mode	200			mV
	Signal Detect Assertion	RXP/N[1:0]	100BASE-TX mode	1000	460[4]		mV peak-peak
	Signal Detect De-assertion	RXP/N[1:0]	100BASE-TX mode	200	360[5]		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. ANSI X3.263-1995 Figure 9-1.
3. The input test is actually a template test. IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The 88E6208/88E6218 will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should be de-assert signal detect (internal signal in 100BASE-TX mode). The 88E6208/88E6218 will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

4.6 AC Electrical Specifications

4.6.1 Asynchronous Signals

The following are asynchronous signals:

- UART interface pins
- GPIO interface pins

4.6.2 Reset and Configuration Timing

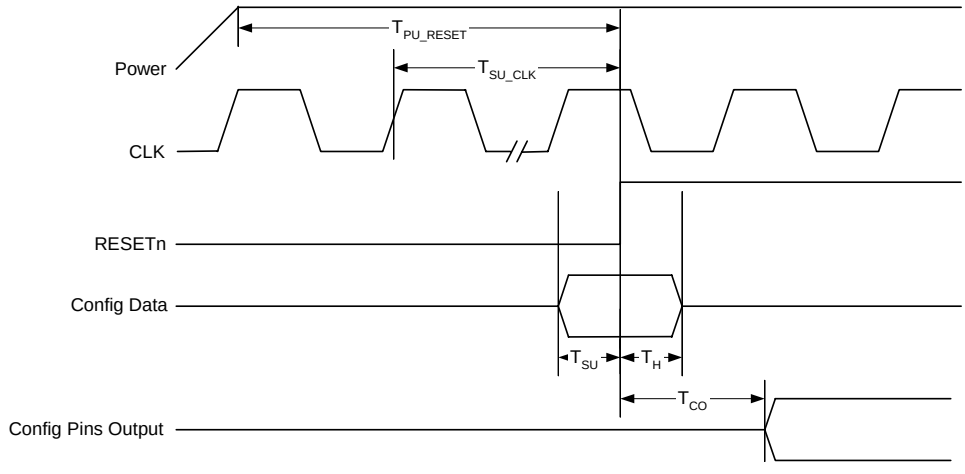
Table 24: Reset and Configuration Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{PU_RESET}	Valid power to RESETn de-asserted		10			ms	
T_{SU_CLK}	Number of valid clock cycles prior to RESETn de-asserted		10			Clks	
T_{SU}	Configuration data valid prior to RESETn de-asserted		200			ns	1
T_{HD}	Configuration data valid after RESETn de-asserted		0			ns	
T_{CO}	Configuration output driven after RESETn de-asserted		40			ns	2

1. When RESETn is low all configuration pins become inputs, and the value seen on these pins is latched on the rising edge of RESETn.
2. P6_OUTD[3:0]/P6_MODE[3:0], and P6_OUTDV are normally outputs that are also used to configure the 88E6208/88E6218 during hardware reset. When reset is asserted, these pins become inputs and the desired device configuration is latched at the rising edge of RESETn.

Figure 4: Reset and Configuration Timing



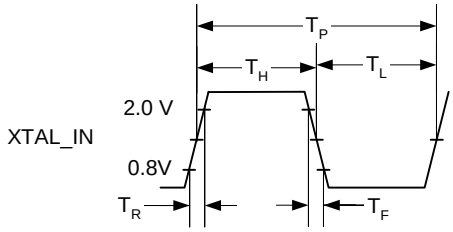
4.6.3 Clock Timing when using a 25 MHz Oscillator

Table 25: Clock Timing when using a 25 MHz Oscillator

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	XTAL_IN period		40 -50 ppm	40	40 +50 ppm	ns	25 MHz
T_H	XTAL_IN high time		16			ns	
T_L	XTAL_IN low time		16			ns	
T_R	XTAL_IN rise				3	ns	
T_F	XTAL_IN fall				3	ns	

Figure 5: Oscillator Clock Timing



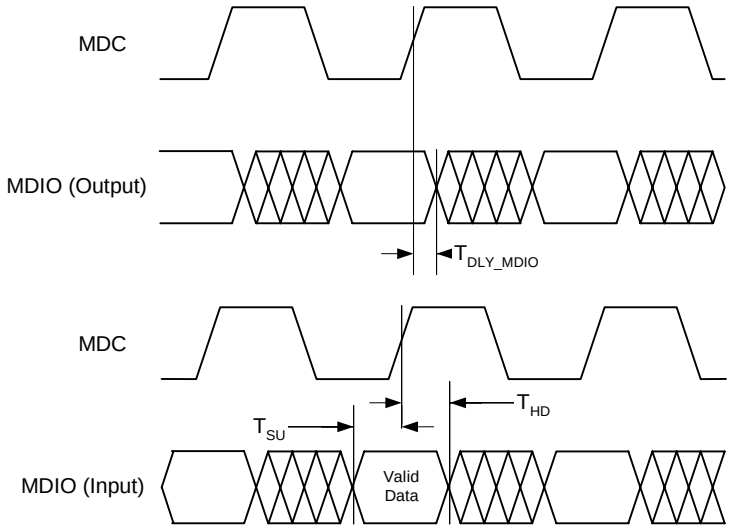
4.6.4 Serial Management Interface Timing

Table 26: Serial Management Interface Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		20	ns	
T_{SU}	MDIO (Input) to MDC setup time		10			ns	
T_{HD}	MDIO (Input) to MDC hold time		10			ns	

Figure 6: Serial Management Interface Timing



4.6.5 SDRAM/Device Interface Timing

Note

Proper design of the memory controller interface to SDRAM and Flash is required for high frequencies. Please contact Marvell® for design and layout guidelines.

Table 27: SDRAM/Device Interface Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{CYC}	M_SDCLK_OUT	SDRAM clock output	6.7			ns	
T_{CYC}	M_SDCLK_IN	SDRAM clock input	6.7			ns	
T_{VAL}	All SDRAM outputs	All SDRAM outputs time to Signal valid delay.	2		5.4 - X	ns	1,2
T_{SU}	All SDRAM inputs	All SDRAM inputs – input setup time.	0.5			ns	3
T_H	All SDRAM inputs	All SDRAM inputs – input hold time.	1			ns	4

1. Relative to M_SDCLK_OUT
2. X = 0.5*(7.5 - T_{CYC})
3. Relative to M_SDCLK_IN
4. Relative to M_ SDCLK_IN

Note

All timings assume internal M_SDCLK_OUT delay line programmed to 2 (refer to 88E6208/88E6218 RevB0 Release Notes).

Figure 7: Flash/ROM Read Access

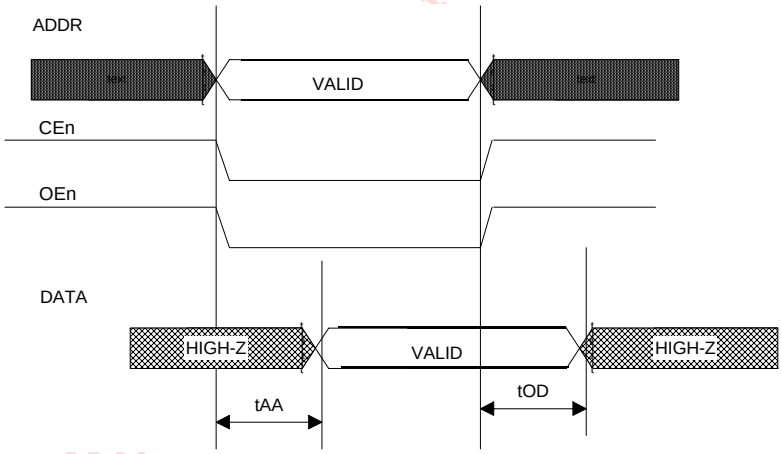
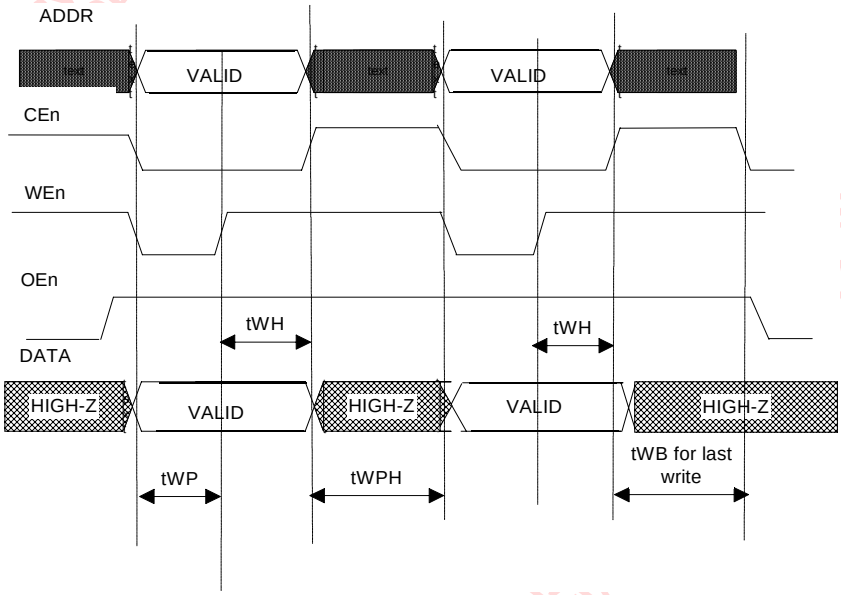


Figure 8: Flash/ROM Write Access



4.6.6 GPIO Timing

Table 28: GPIO Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{OH}	Switching current high	VCC - 0.4	10			mA	1, 2
I_{OL}	Switching current low	0.4	16			mA	
T_{SLEW_RISE}	Output rise slew	0.3VCC-0.6VCC	1.5			V/ns	
T_{SLEW_FALL}	Output fall slew rate	0.6VCC-0.3VCC	1.0			V/ns	
TPLH	Output mode low to high delay	50%~50%. 10 pF load	1.0		3.0	ns	
TPHL	Output mode high to low delay	50%~50%. 10 pF load	1.0		3.0	ns	

1. GPIO are operating in fast slew rate mode.
2. The rise/fall time of the input signal is 0.5 ns.

4.6.7 Switch Port 6 MII Rx Timing (PHY Mode) - 88E6218 Only

Table 29: Switch Port 6 MII Receive Timing (PHY Mode) - 88E6218 Only

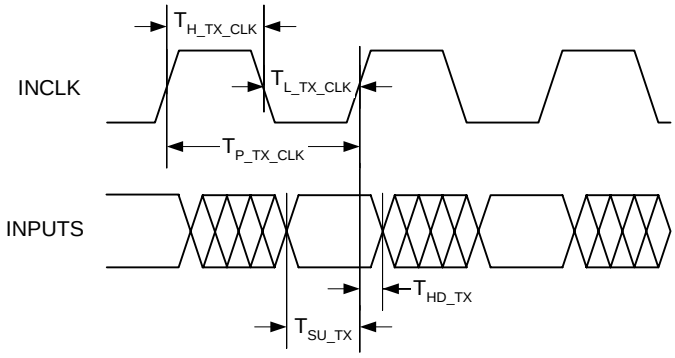
In PHY mode, the P6_INCLK pins are outputs.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_TX\_CLK}$	P6_INCLK period	10BASE mode		400		ns	1
		100BASE mode		40		ns	1
$T_{H\_TX\_CLK}$	P6_INCLK high	10BASE mode	160	200	240	ns	
		100BASE mode	16	20	24	ns	
$T_{L\_TX\_CLK}$	P6_INCLK low	10BASE mode	160	200	240	ns	
		100BASE mode	16	20	24	ns	
T_{SU_TX}	MII inputs (P6_IND[3:0], P6_INDV) valid prior to P6_INCLK going high.		15			ns	
T_{HD_TX}	MII inputs (P6_IND[3:0], P6_INDV) valid after P6_INCLK going high.		0			ns	

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 9: PHY Mode MII Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an output in this mode.

4.6.8 Switch Port 6 MII Tx Timing (PHY Mode) - 88E6218 Only

Table 30: Switch Port 6 MII Transmit Timing (PHY Mode) - 88E6218 Only

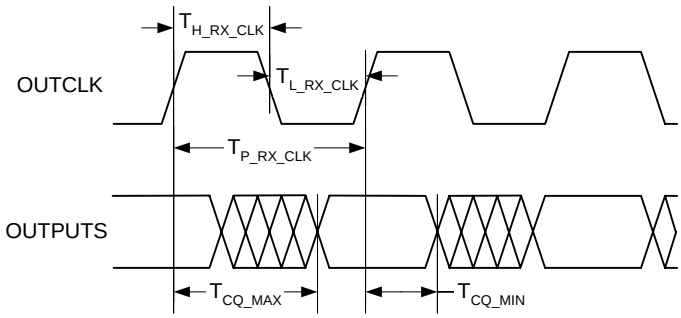
In PHY mode, the P6_OUTCLK pin is an output.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_RX\_CLK}$	P6_OUTCLK period	10BASE mode		400		ns	1
		100BASE mode		40		ns	1
$T_{H\_RX\_CLK}$	P6_OUTCLK high	10BASE mode	160	200	240	ns	
		100BASE mode	16	20	24	ns	
$T_{L\_RX\_CLK}$	P6_OUTCLK low	10BASE mode	160	200	240	ns	
		100BASE mode	16	20	24	ns	
T_{CQ_MAX}	P6_OUTCLK to outputs (P6_OUTD[3:0], P6_OUTDV) valid				25	ns	
T_{CQ_MIN}	P6_OUTCLK to outputs P6_OUTD[3:0], P6_OUTDV) invalid		10			ns	

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 10: PHY Mode MII Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

4.6.9 Switch Port 6 Clock Timing (MAC Mode) - 88E6218 Only

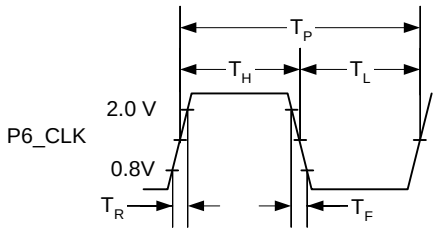
Table 31: Switch Port 6 Clock Timing (MAC Mode) - 88E6218 Only

In MAC mode, INCLK and OUTCLK are inputs.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	P6_INCLK period		0	4 or 40	40 +50 ppm	ns	DC to 25 MHz
T_H	P6_INCLKhigh time		16			ns	
T_L	P6_INCLK low time		16			ns	
T_R	P6_INCLK rise				3	ns	
T_F	P6_INCLK fall				3	ns	

Figure 11: MAC Clock Timing



4.6.10 Switch Port 6 MII Rx Timing (MAC Mode) - 88E6218 Only

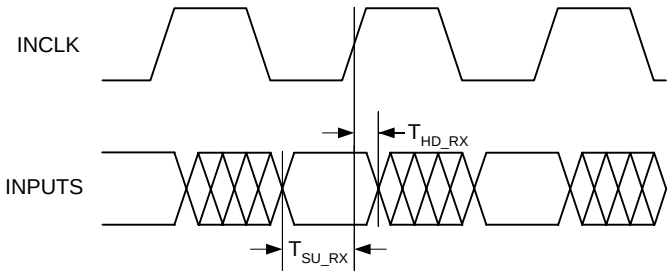
Table 32: Switch Port 6 MII Receive Timing (MAC Mode) - 88E6218 Only

In MAC mode, the P6_INCLK pin is an input.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{SU_RX}	MII inputs (P6_IND[3:0], P6_INDV) valid prior to P6_INCLK going high	With 10 pF load	10			ns	
T_{HD_RX}	MII inputs (P6_IND[3:0], P6_INDV) valid after P6_INCLK going high	With 10 pF load	10			ns	

Figure 12: MAC Mode MII Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an input in this mode.

4.6.11 Switch Port 6 MII Tx Timing (MAC Mode) - 88E6218 Only

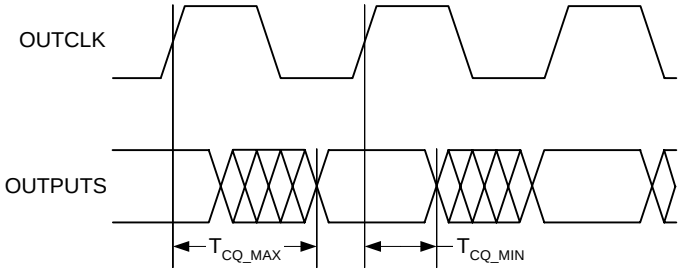
Table 33: Switch Port 6 MII Transmit Timing (MAC Mode) - 88E6218 Only

In MAC mode, the P6_OUTCLK pin is an input.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{CQ_MAX}	P6_OUTCLK to outputs (P6_OUTD[3:0], P6_OUTDV) valid	With 10 pF load			25	ns	
T_{CQ_MIN}	P6_OUTCLK to outputs (P6_OUTD[3:0], P6_OUTDV) invalid	With 1 0pF load	0			ns	

Figure 13: MAC Mode MII Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an input in this mode.

4.6.12 Switch Port 6 Clock Timing - 200 Mbps (MAC Mode) - 88E6218 Only

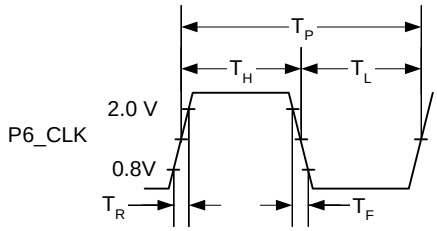
Table 34: Switch Port 6 Clock Timing - 200 Mbps (MAC Mode) - 88E6218 Only

In MAC mode, INCLK and OUTCLK are inputs.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	P6_INCLK period		20 -50ppm	20	20 +50 ppm	ns	DC to 25 MHz
T_H	P6_INCLK high time		8			ns	
T_L	P6_INCLK low time		8			ns	
T_R	P6_INCLK rise				3	ns	
T_F	P6_INCLK fall				3	ns	

Figure 14: MAC Clock Timing - 200 Mbps



4.6.13 Switch Port 6 MII Rx Timing (PHY Mode) - 200 Mbps - 88E6218 Only

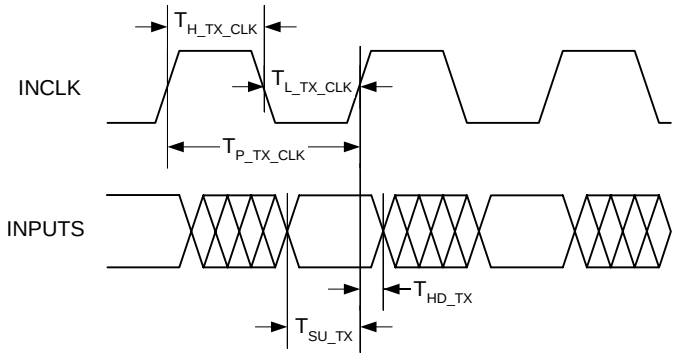
Table 35: Switch Port 6 MII Receive Timing (PHY Mode) - 200 Mbps - 88E6218 Only

In PHY mode, the P6_INCLK pin is output.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_TX\_CLK}$	P6_INCLK period	200BASE mode		20		ns	
$T_{H\_TX\_CLK}$	P6_INCLK high	200BASE mode	8	10	12	ns	
$T_{L\_TX\_CLK}$	P6_INCLK low	200BASE mode	8	10	12	ns	
T_{SU_TX}	MII inputs (P6_IND[3:0], P6_INDV) valid prior to P6_INCLK going high.		13			ns	
T_{HD_TX}	MII inputs (P6_IND[3:0], P6_INDV) valid after P6_INCLK going high.		0			ns	

Figure 15: PHY Mode MII Receive Timing - 200 Mbps



NOTE: INCLK is the clock used to clock the input data.
It is an output in this mode.

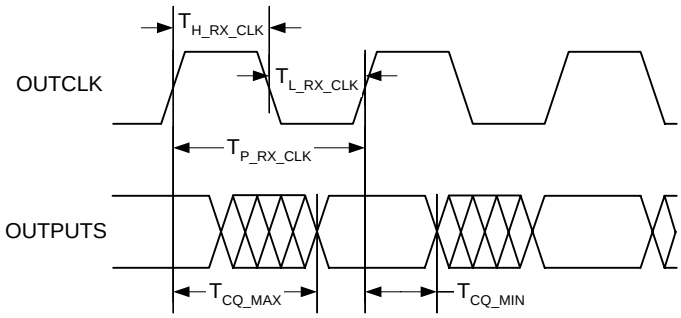
4.6.14 Switch Port 6 MII Tx Timing (PHY Mode) - 200 Mbps - 88E6218 Only

Table 36: Switch Port 6 MII Transmit Timing (PHY Mode) - 200 Mbps - 88E6218 Only

In PHY mode, the P6P[x]_OUTCLK pin is are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_RX\_CLK}$	P6_OUTCLK period	200BASE mode		20		ns	
$T_{H\_RX\_CLK}$	P6_OUTCLK high	200BASE mode	8	10	12	ns	
$T_{L\_RX\_CLK}$	P6_OUTCLK low	200BASE mode	8	10	12	ns	
T_{CQ_MAX}	P6_OUTCLK to outputs (P6_OUTD[3:0], P6_OUTDV) valid				15	ns	
T_{CQ_MIN}	P6_OUTCLK to outputs P6_OUTD[3:0], P6_OUTDV) invalid		3			ns	

Figure 16: PHY Mode MII Transmit Timing - 200 Mbps



NOTE: OUTCLK is the clock used to clock the output data.
It is an output in this mode.

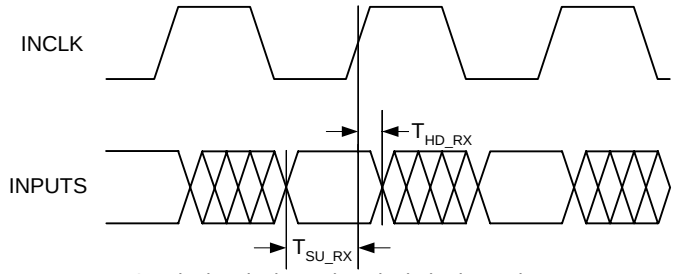
4.6.15 Switch Port 6 MII Rx Timing (MAC Mode) - 200 Mbps - 88E6218 Only

Table 37: Switch Port 6 MII Receive Timing (MAC Mode) - 200 Mbps - 88E6218 Only

In MAC mode, the P6P[x]_INCLK pin is are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{SU_RX}	MII inputs (P6_IND[3:0], P6_INDV) valid prior to P6_INCLK going high	With 10 pF load	5			ns	
T_{HD_RX}	MII inputs (P6_IND[3:0], P6_INDV) valid after P6_INCLK going high	With 10 pF load	3			ns	

Figure 17: MAC Mode MII Receive Timing - 200 Mbps



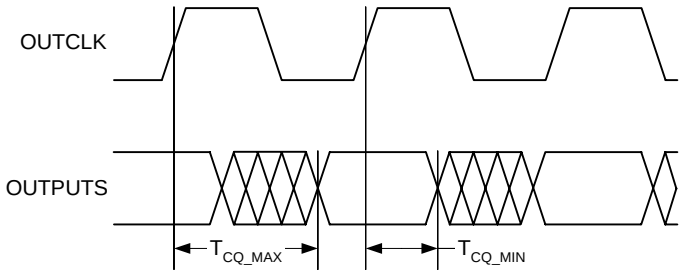
NOTE: INCLK is the clock used to clock the input data.
It is an input in this mode.

4.6.16 Switch Port 6 MII Tx Timing (MAC Mode) - 200 Mbps - 88E6218 Only

Table 38: Switch Port 6 MII Transmit Timing (MAC Mode) - 200 Mbps - 88E6218 Only
In MAC mode, the P6_OUTCLK pin is an input.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{CQ_MAX}	P6_OUTCLK to outputs (P6_OUTD[3:0], P6_OUTDV valid	With 10 pF load			7	ns	
T_{CQ_MIN}	P6_OUTCLK to outputs (P6_OUTD[3:0], P6_OUTDV invalid	With 10pF load	0			ns	

Figure 18: MAC Mode MII Transmit Timing - 200 Mbps



NOTE: OUTCLK is the clock used to clock the output data. It is an input in this mode.

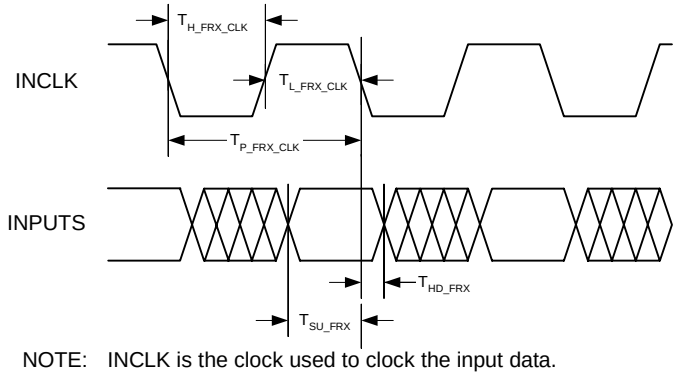
4.6.17 Switch Port 6 SNI Falling Edge Rx Timing - 88E6218 Only

Table 39: Switch Port 6 SNI Falling Edge Receive Timing - 88E6218 Only

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_FRX\_CLK}$	SNI falling edge INCLK period	10BASE-T Mode		100		ns	
$T_{H\_FRX\_CLK}$	SNI falling edge INCLK high		35	50	65	ns	
$T_{L\_FRX\_CLK}$	SNI falling edge INCLK low		35	50	65	ns	
T_{SU_FRX}	SNI receive data valid prior to INCLK going low		20			ns	
T_{HD_FRX}	SNI receive data valid after INCLK going low		10			ns	

Figure 19: SNI Falling Edge Receive Timing



NOTE: INCLK is the clock used to clock the input data. It is an output in this mode.

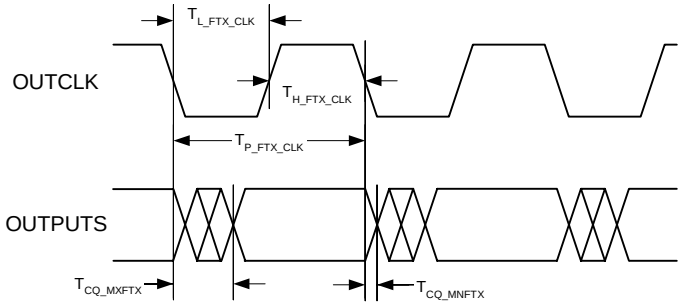
4.6.18 Switch Port 6 SNI Falling Edge Tx Timing - 88E6218 Only

Table 40: Switch Port 6 SNI Falling Edge Transmit Timing - 88E6218 Only

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_FTX\_CLK}$	SNI falling edge OUTCLK period	10BASE-T Mode		100		ns	
$T_{H\_FTX\_CLK}$	SNI falling edge OUTCLK high		35	50	65	ns	
$T_{L\_FTX\_CLK}$	SNI falling edge OUTCLK low		35	50	65	ns	
T_{CQ_MXFTX}	SNI falling edge OUTCLK to output valid				20	ns	
T_{CQ_MNFTX}	SNI falling edge OUTCLK to output invalid		10			ns	

Figure 20: SNI Falling Edge Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

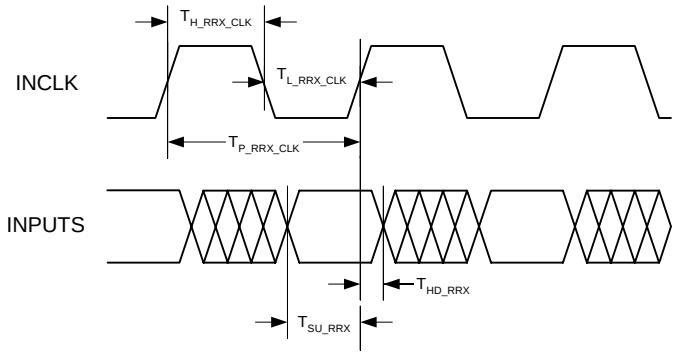
4.6.19 Switch Port 6 SNI Rising Edge Rx Timing - 88E6218 Only

Table 41: Switch Port 6 SNI Rising Edge Receive Timing - 88E6218 Only

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_RRX\_CLK}$	SNI rising edge INCLK period	10BASE-T Mode		100		ns	
$T_{H\_RRX\_CLK}$	SNI rising edge INCLK high		35	50	65	ns	
$T_{L\_RRX\_CLK}$	SNI rising edge INCLK low		35	50	65	ns	
T_{SU_RRX}	SNI receive data valid prior to INCLK going high		20			ns	
T_{HD_RRX}	SNI receive data valid after INCLK going high		10			ns	

Figure 21: SNI Rising Edge Receive Timing



NOTE: INCLK is the clock used to clock the input data. It is an output in this mode.

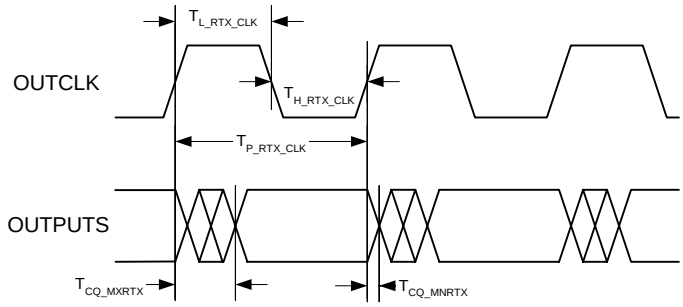
4.6.20 Switch Port 6 SNI Rising Edge Tx Timing - 88E6218 Only

Table 42: Switch Port 6 SNI Rising Edge Transmit Timing - 88E6218 Only

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_RTX\_CLK}$	SNI rising edge OUTCLK period	10BASE-T Mode		100		ns	
$T_{H\_RTX\_CLK}$	SNI rising edge OUTCLK high		35	50	65	ns	
$T_{L\_RTX\_CLK}$	SNI rising edge OUTCLK low		35	50	65	ns	
T_{CQ_MXRTX}	OUTCLK to output valid				20	ns	
T_{CQ_MNRTX}	OUTCLK to output invalid		10			ns	

Figure 22: SNI Rising Edge Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

4.6.21 Switch Port 6 RMII Rx Timing - 88E6218 Only

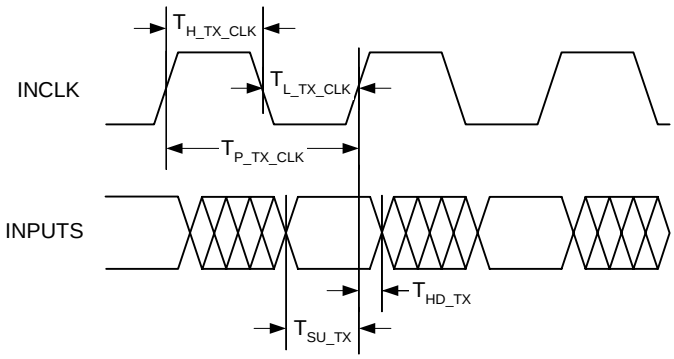
Table 43: Switch Port 6 RMII Receive Timing - 88E6218 Only

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_TX\_CLK}$	P[x]_INCLK period	10BASE mode				ns	1
		100BASE mode		20		ns	1
$T_{H\_TX\_CLK}$	P[x]_INCLK high	10BASE mode				ns	
		100BASE mode	8	10	12	ns	
$T_{L\_TX\_CLK}$	P[x]_INCLK low	10BASE mode				ns	
		100BASE mode	8	10	12	ns	
T_{SU_TX}	MII inputs (P6_IND[1:0], P6_INDV) valid prior to P6_INCLK going high.		7.5			ns	
T_{HD_TX}	MII inputs (P6_IND[1:0], P6_INDV) valid after P6_INCLK going high.		0			ns	

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 23: PHY Mode RMII Receive Timing



NOTE: INCLK is the clock used to clock the input data. It is an output in this mode.

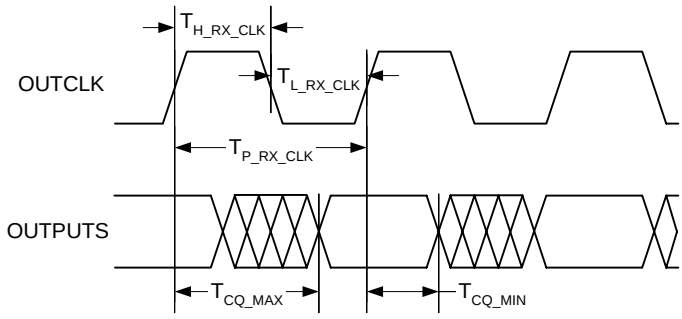
4.6.22 Switch Port 6 RMII Tx Timing - 88E6218 Only

Table 44: Switch Port 6 RMII Transmit Timing - 88E6218 Only
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_RX\_CLK}$	P[x]_OUTCLK period	10BASE mode				ns	1
		100BASE mode		20		ns	1
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	10BASE mode				ns	
		100BASE mode	8	10	12	ns	
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	10BASE mode				ns	
		100BASE mode	8	10	12	ns	
T_{CQ_MAX}	P6_OUTCLK to outputs (P6_OUTD[1:0], P6_OUTDV) valid				12.5	ns	
T_{CQ_MIN}	P6_OUTCLK to outputs P6_OUTD[1:0], P6_OUTDV) invalid		0			ns	

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 24: PHY Mode RMII Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an output in this mode.

4.6.23 Two-Wire Serial Interface (TWSI) Timing

Table 45: Two-Wire Serial Interface (TWSI) Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

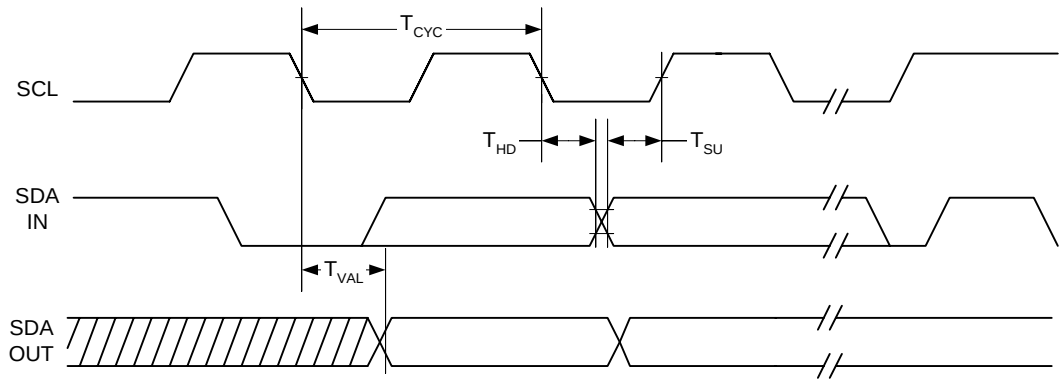
SDA setup, hold, and output delay times are referenced to SCL rising edge.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{FREQ}	SCL - TWSI Clock	Frequency			400	kHz
T_{CYC}	SCL - TWSI Clock	Clock Cycle	2.5			µs
T_{SU}	SDA - TWSI Data	Setup	10			ns
T_{H}	SDA - TWSI Data	Hold	5			ns
T_{VAL}	SDA - TWSI Data	Output Delay	1		15	ns

Note

The Two-Wire Serial Interface features a programmable clock. The driver (or SW application) must set the clock speed for 100/400 kHz.

Figure 25: Two-Wire Serial Interface Timing



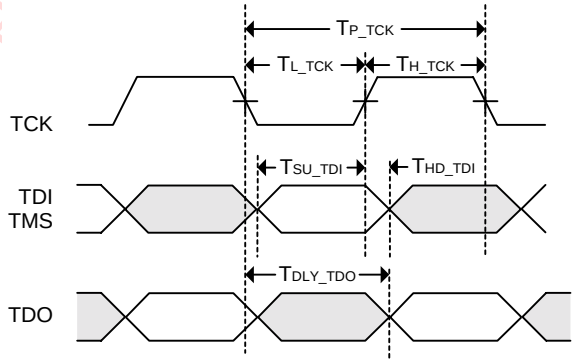
4.6.24 JTAG Timing

Table 46: JTAG Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period		100			ns
T_{H_TCK}	TCK High		40			ns
T_{L_TCK}	TCK Low		40			ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time		5			ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time		20			ns
T_{DLY_TDO}	TCK to TDO Delay		1		15	ns

Figure 26: JTAG Timing



4.7 IEEE AC Parameters

Table 47: IEEE AC Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14-2000
-100BASE-TX ANSI X3.263-1995
-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

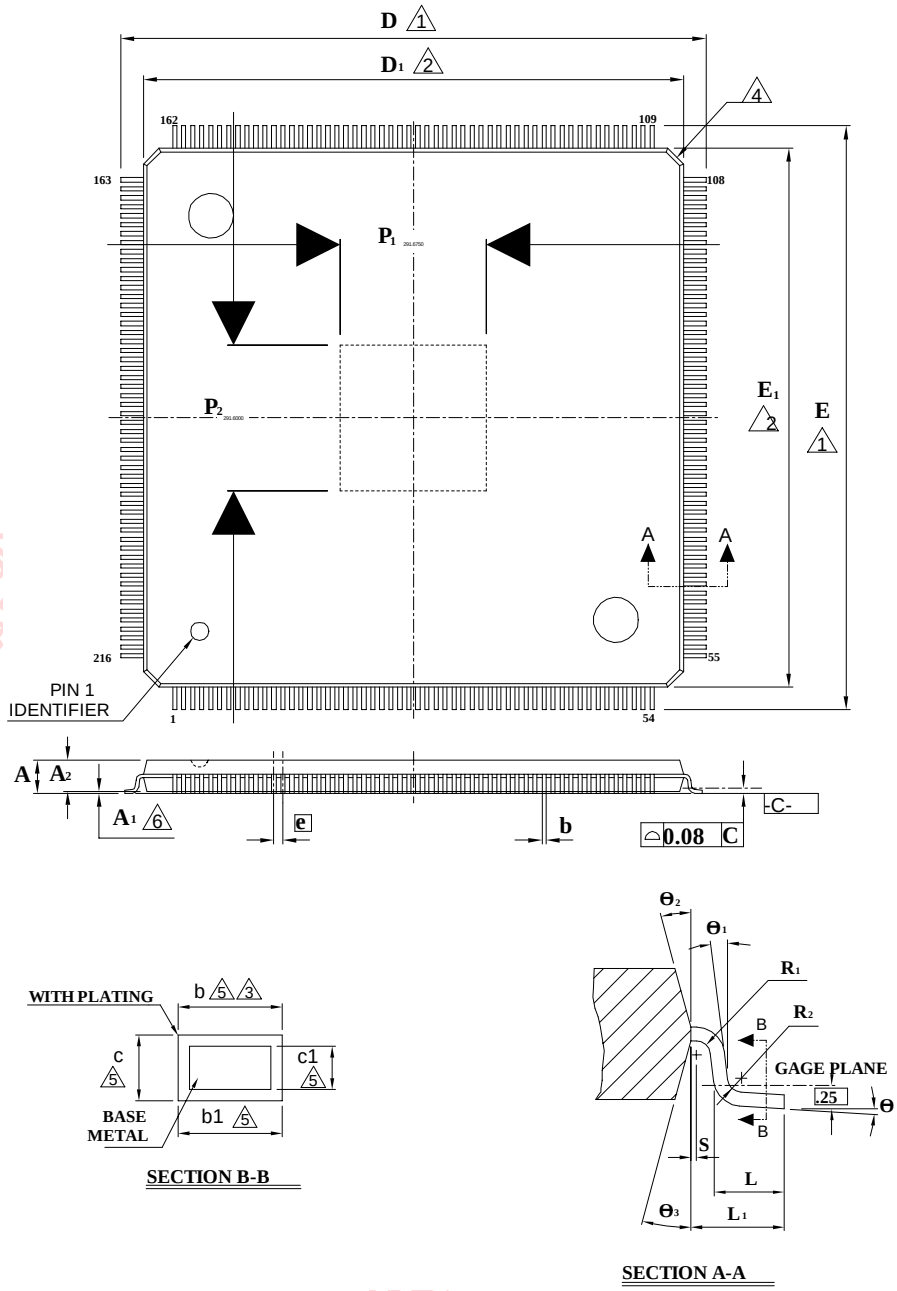
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	TXP/N[4:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall time	TXP/N[4:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{RISE}/ T_{FALL} Symmetry		TXP/N[4:0]	100BASE-TX	0		0.5	ns
DCD	Duty cycle distortion	TXP/N[4:0]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		TXP/N[4:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3.

Section 5. Package Mechanical Dimensions

Figure 27: Link Street™ 88E6208/88E6218 216-pin LQFP Package with Exposed Die Pad



Symbol	Dimension in mm		
	Min	Nom	Max
A	--	--	1.60
A_1	0.05	--	0.15
A_2	1.35	1.40	1.45
b	0.13	0.18	0.23
b_1	0.13	0.16	0.19
c	0.09	0.14	0.20
c_1	0.09	0.12	0.16
D	25.60	26.00	26.40
D_1	--	24.00	--
E	25.60	26.00	26.40
E_1	--	24.00	--
e	0.40 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	--	--
R_2	0.08	--	--
S	0.20	--	--
P_1	8.64 BSC		
P_2	8.64 BSC		
θ	0°	3.5°	7°
θ_1	0°	--	--
θ_2	11°	12°	13°
θ_3	11°	12°	13°

Note

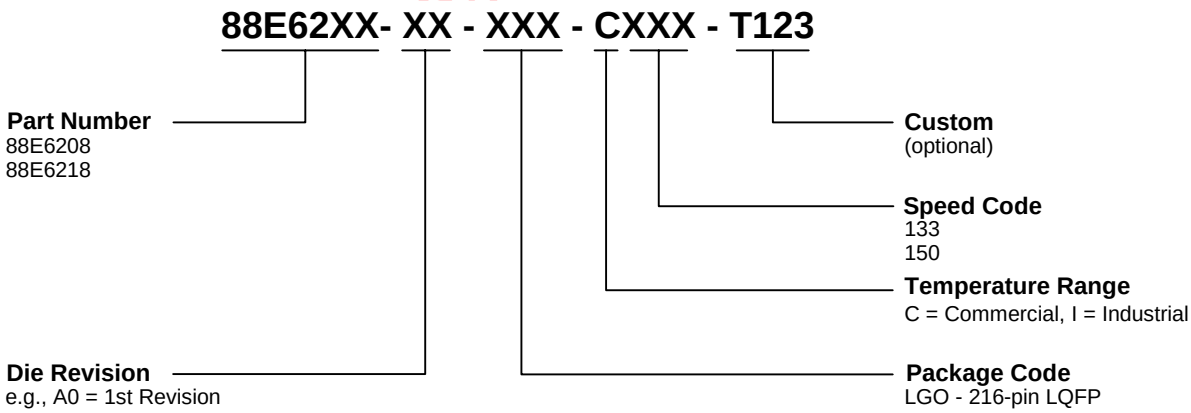
1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION: MILLIMETER.

Section 6. Order Information

6.1 Ordering Part Numbers and Package Markings

Figure 28 shows the ordering part numbering scheme for the 88E6208/88E6218 devices. Contact Marvell FAEs or sales representatives for complete ordering information.

Figure 28: Sample Ordering Part Number

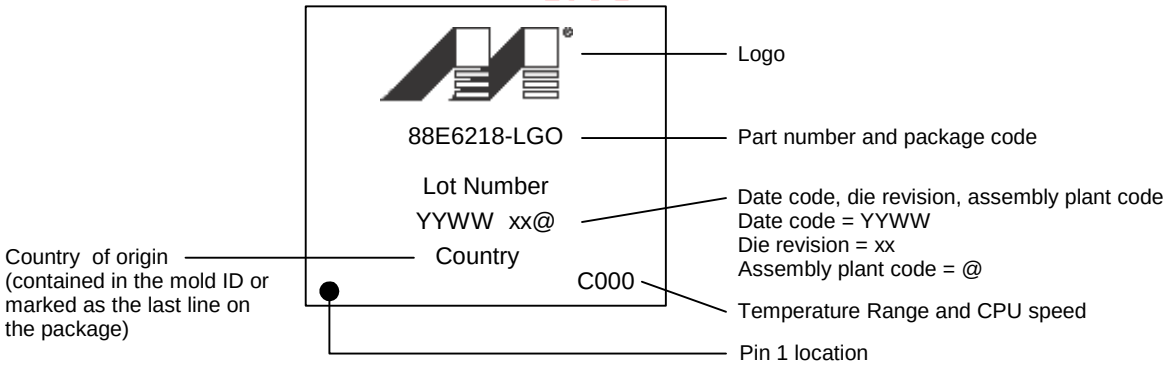


The standard ordering part numbers for the respective solutions are as follows:

- 88E6208-XX-LGO-C133
- 88E6218-XX-LGO-C133
- 88E6218-XX-LGO-C150

Figure 29 shows a typical package marking and pin 1 location for the 88E6218 part. Markings for the other variants are similar.

Figure 29: 88E6218 Package Marking and Pin 1 Location



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