Ronald Macmaster and Parth Adhia

EID: Rpm953 and Pda375

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EE 445L – Lab 2 (Prep): Performance Debugging

a) What is the purpose of all the DCW statements?

DCW declares a 16 bit half word global variable in memory. These specific DCW statements define GPIO port addresses for PORT F access (system control, digital enable, data base, and directional).

b) The main program toggles PF1. Neglecting interrupts for this part, estimate how fast PF1 will toggle.

It takes 6 instructions to toggle the LED, and each instruction takes about 25 ns to execute.
Thus, it takes about 6 * 25ns = 150ns to toggle the LED. The LED toggles at 6.7 MHz.

c) What is in R0 after the first LDR is executed? What is in R0 after the second LDR is executed?

After the first LDR, R0 contains the base address of GPIO Port F.
After the second LDR, R0 contains the current data value of PF1.

d) How would you have written the compiler to remove an instruction?

Instead of overwriting the Port F address (in R0) with the data value, load the data value of PF1 into R1 instead. Then, you can avoid reloading the Port F address into R1 (instruction 4).

e) 100-Hz ADC sampling occurs in the Timer0 ISR. The ISR toggles PF2 three times. Toggling three times in the ISR allows you to measure both the time to execute the ISR and the time between interrupts. See Figure 2.1. Do these two read-modify write sequences to Port F create a critical section? If yes, describe how to remove the critical section? If no, justify your answer?

No, these read-modify write sequences **do not** create a critical section.
PF2 is accessed through bit-specific addressing, and the ISR does not share PF2 with any other program threads. The value read into PF1 and modified in the main thread will always be accurate because it is unaffected by updates to PF2 in the ISR.

PMF Plot (Step 6)