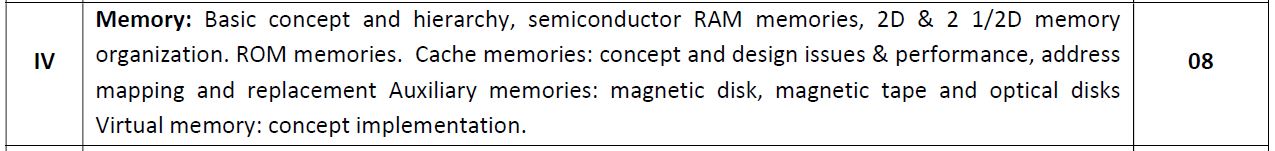
***ABES ENGINEERING COLLEGE,GHAZIABAD***

***Unit No-04 Question Bank***

***Paper Code:BCS302***

***Paper Name: Computer Organization and Architecture***

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| No. | Questions | CO | KL |
| 1. | Consider a machine with a byte addressable main memory of bytes and block size of 8 bytes. Assume that a direct mapped cache cosnsiting of 32 lines used with this machine. How many bits will be there in Tag line, word field of format of main memory addresses ?  *UGC-NET-2020*  *C:\Users\Asus\OneDrive\Desktop\WhatsApp Image 2024-01-17 at 11.44.05 AM.jpeg* |  |  |
| 2. | Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generate 32-bit address. The number of bits required for cache indexing and Tag bit respectively.  *GATE 2005*  *C:\Users\Asus\OneDrive\Desktop\Capture.JPG* |  |  |
| 3. | Write a short note on Magnetic Tape, Magnetic disk and Optical disk. |  |  |
| 4. | Explain the following terms with example.  a) Locality of reference  b) Cache write back  c) Cache write through  d) Simultaneous Access |  |  |
| 5. | Consider a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order:- 4,3,25,,8,19,6,25,8,16,35,45,22,8,3,16,25,7.  If LRU(Least Recent Unit) replacement policy is used. Which cache block will have memory block 7 ?Also calcu;ate the hit ratio and miss ratio. *GATE 2004*  *C:\Users\Asus\OneDrive\Desktop\Capture2.JPG* |  |  |
| 6. | What are the differences between SRAM & DRAM?   |  |  |  | | --- | --- | --- | | No. | SRAM | DRAM | | 1. | Made of flip-flops | Made up of capacitors (storage in the form of electric charges) | | 2. | No refresh required | Periodic refresh is required to keep the content | | 3. | Faster Read/write | Slower Read/write | | 4. | Expensive | Less expensive | | 5. | Used for cache memory implementation | Used for main memory implementation | | 6. | Low idle power consuption | High idle power consumption | | 7. | High operational power consumption | Low operational power consumption | | CO4 |  |
| 7. | Discuss the Concept of Cache Memory with an example. |  |  |
| 8. | The logical address space in a computer system consisting 8 pages and 1024 words each, mapped into a physical memory of 32 frames. How many bits are there in the physical address and logical address respectively? |  |  |
| 9. | Consider a cache consisting of 256 block of 16 words each for a total of 4096 words and assume that the main memory is addressable by a 16 bit addresses and it consist of 4K blocks.How many bits are there in TAG,SET, WORD field for 2-way set associative technique ?  *AKTU 2020-21*  *C:\Users\Asus\OneDrive\Desktop\Capture1.JPG* |  |  |
| 10. | A virtual memory has a page size of 1k words. There are 8 pages and 4 blocks. The associative memory page contains the following entries.   |  |  | | --- | --- | | PAGE | BLOCK | | 0 | 3 | | 2 | 1 | | 5 | 2 | | 7 | 0 |   Make a list of virtual addresses (in decimal) that will cause page fault if used by CPU. | CO4 | K3 |
| 11. | A Digital computer has a memory unit of 64 K\*16 and a cache memory of 1K words.The Cache uses direct mapping with a block size of 4 words.  Calculate:   * 1. How many bits are there in the tag, index, block and word fields of the address format.   2. How many bits are there in each word of cache   3. how many blocks can cache accommodate.   AKTU 2021-22  C:\Users\Asus\OneDrive\Desktop\Capture.JPG | CO4 | K3 |
| 12. | Discuss 2D RAM and 2.5D RAM with suitable diagram. | CO4 |  |
| 13. | Calculate the page fault for a given string with the help of LRU & FIFO page replacement algorithm , Size of frames =4 and string 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6  *AKTU 2020-21*  *C:\Users\Asus\OneDrive\Desktop\Capture1.JPG* | CO4 |  |
| 14. | What do you mean by Virtual memory? Discuss how Paging helps in implementing Virtual memory? | CO4 | 𝐾2 |
| 15. | Discuss the memory hierarchy in computer system in the context of speed,size and cost. *AKTU 2020-21*  **Memory Hierarchy** : The Computer memory hierarchy looks like a pyramid structure which is used to describe the differences among [**memory types**](https://www.tutorialspoint.com/computer_fundamentals/computer_memory.htm). It separates the computer storage based on hierarchy.  Memory hierarchy is arranging different kinds of storage present on a computing device based on speed of access. At the very top, the highest performing storage is CPU registers which are the fastest to read and write to. Next is cache memory followed by conventional DRAM memory, followed by disk storage with different levels of performance including SSD, optical and magnetic disk drives.      Single memory unit can not accommodate all the programs and data.The memory unit that directly communicates with the CPU is called main memory e.g. RAM & ROM.  Devices that provide backup storage are called auxiliary memory e.g. magnetic disks & tapes.  A special and very high speed memory called a cache is used to provide program and data available to CPU at rapid rate  Memory hierarchy consists of all storage devices from smaller and faster cache memory to high capacity and slow auxiliary memory. | CO4 | K1 |
| 16. | Discuss the following:  a) RAM Vs ROM  b) HIT Ratio and MISS Ratio  c) FIFO Vs LRU | CO4 | K1 |
| 17. | Discuss the different mapping techniques used in cache memories and their relative merits and demerits. | CO4 | K1 |
| 18. | A computer uses RAM chips of 1024 \* 1 capacity.  (a.) How many chips are needed & how should their address line be connected to provide a memory capacity of 1024 \* 8 ?  (b.) How many chips are needed to provide a memory capacity of 16 KB ? *AKTU 2020-21*  C:\Users\Asus\OneDrive\Desktop\Capture.JPG |  |  |
| 19. | An eight way set associative cache consists of a total of 256 blocks. The main memory contain 8192 blocks ,each consisting of 128 words.  (a.) How many bits are there in the main memory address?  (b)How many bits are there in TAG, SET and WORD fields ?  *AKTU 2022-23*  *UGC-NET 2012*  *C:\Users\Asus\OneDrive\Desktop\Capture1.JPG* | CO4 | K3 |
| 20. | What is the average memory access time time for a machine with a cache hit rate of 80 % and cache access time of 5 ns and main memory access time of 100 ns when  (a.) Simultaneously access memory organizations is used  (b.) Hierachical memory organizations is used.  C:\Users\Asus\OneDrive\Desktop\Capture.JPG | CO4 | K3 |
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