

COBIFIVE Datasheet

Five core quantum-inspired Ising solver chip

Version: 2024.11.19

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1. Overview

COBIFIVE Ising Solver Chip

AXI Interface

- >50MHz AXI clock frequency
- Asynchronous read-write
- 16-bit write data bus
- 1-bit read data
- *_LAST signals included in the AXI interface

Input/Output Pads

- 25 input/output digital pins
 - Input pin configuration: Schmitt trigger
 - Output pin configuration: Hysteresis and pull-down, 12mA drive current per pin

Features

- Manufactured in 28nm
- 0.9V core voltage, 1.8V IO voltage
- Input data: 52 x 51 hex numbers = $52 \times 51 \times 4 = 10,608$ bits
- Output data: 69 bits
 - 15b (best_ham) + 46b (best_spin) + 4b (core id) + 4b (problem_id)
 - First output: best_ham
 - Last output: problem_id
- Programmable on-chip clock frequency ranging from 150MHz to 2GHz

2. Pin Configuration

Fig. 2.1 illustrates the bonding diagram of COBIFIVE which is using QP-QFN48-6MM-.4MM package type as shown in Fig. 2.2.

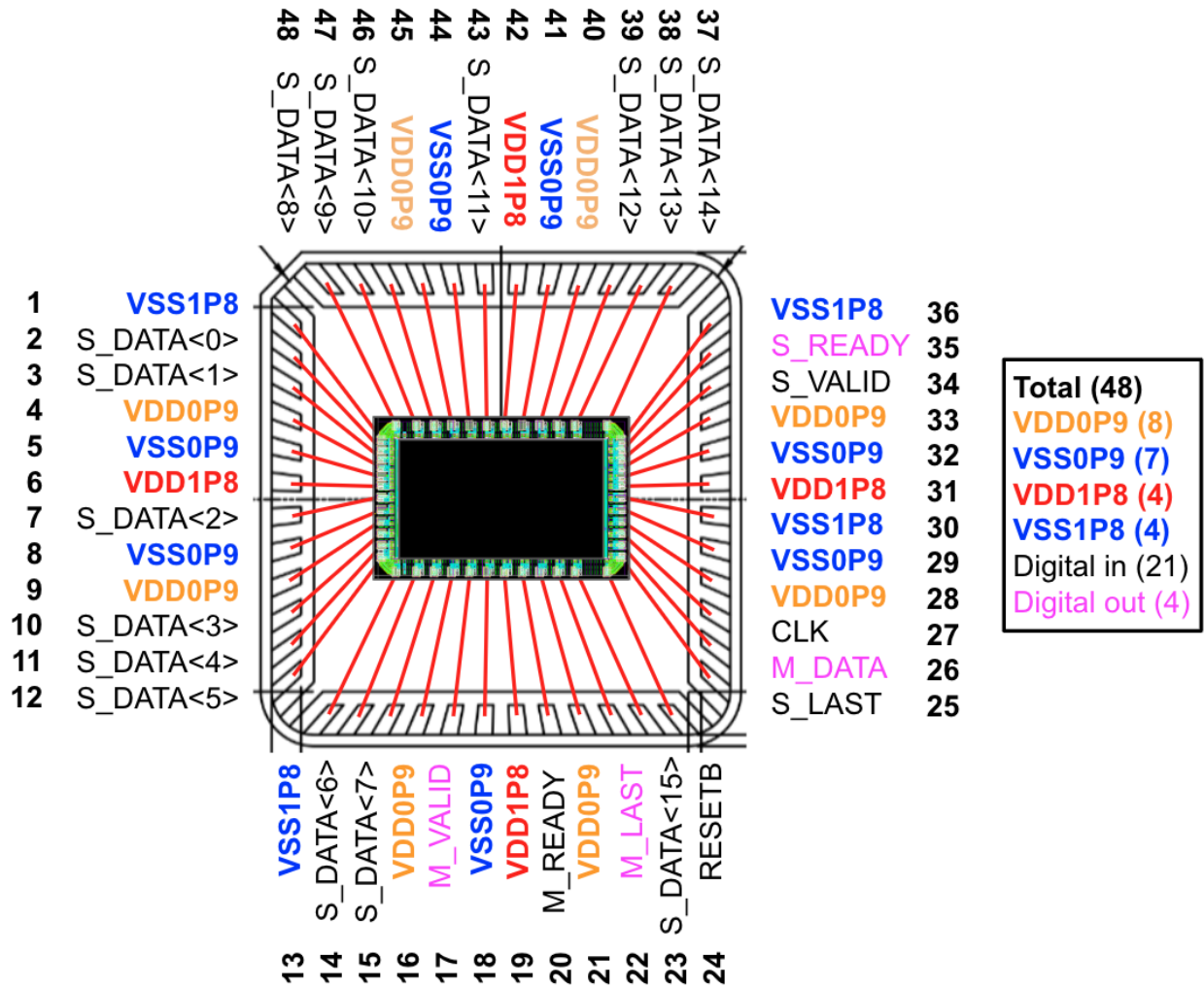


Fig. 2.1. COBIFIVE chip bonding diagram

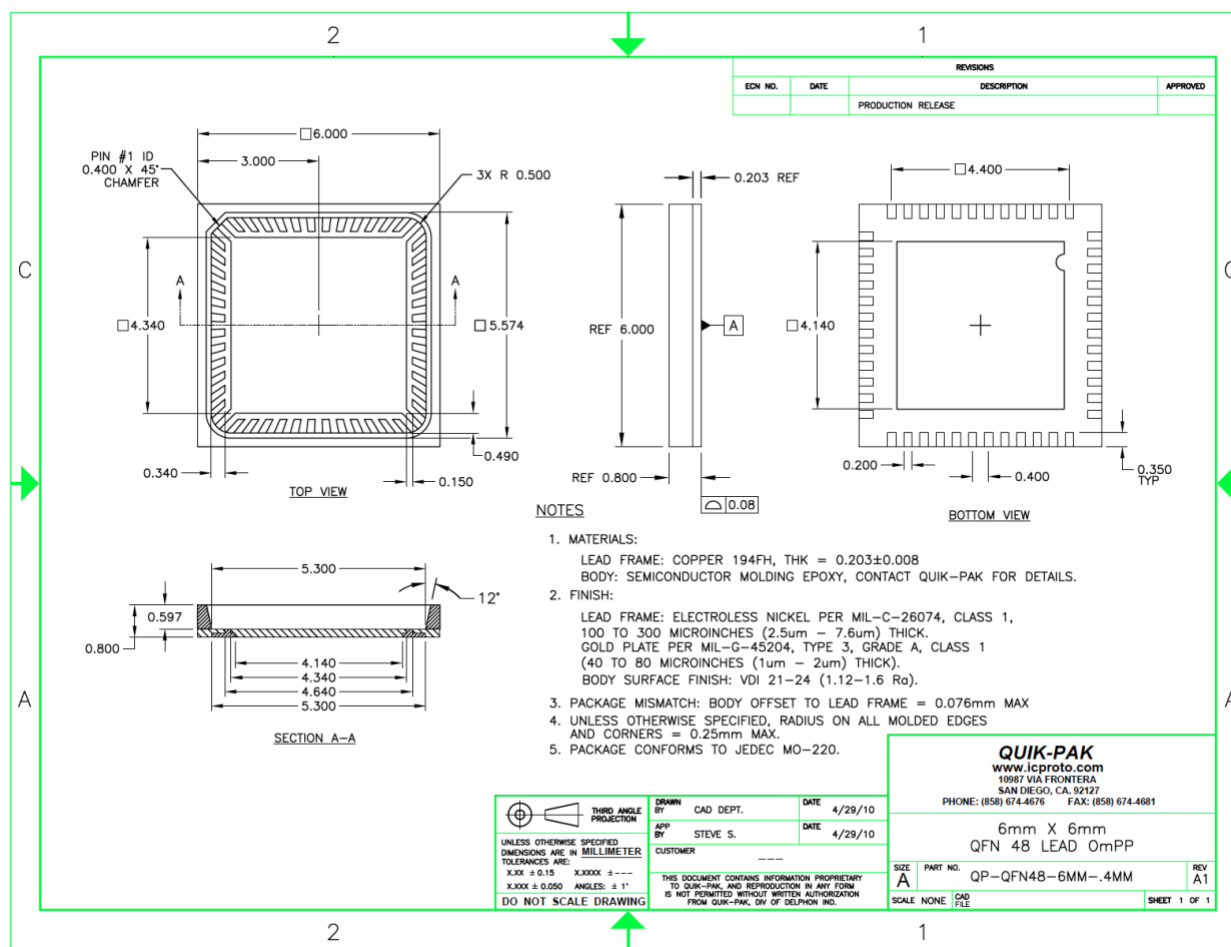


Fig. 2.2. COBIFIVE chip package diagram (QFN 48, 6mm x 6mm, 0.4mm pitch)

3. Pin Function

Table 3.1 describes the Pin Functions of COBIFIVE

Pin		I/O	Description	Activation Type
Name	Number			
Power/ Ground				
VDD1P8	6,19,31,42	PWR	I/O power supply 1.8V	NA
VSS1P8	1,13,30,36	PWR	I/O power supply 0V	NA
VDD0P9	4,9,16,21, 28,33,40,4 5	PWR	Core power supply 0.9V	NA
VSS0P9	5,8,18,29, 32,41,44	PWR	Core power supply 0V	NA
CLK, Reset				
CLK	27	Input	AXI clock used for both asynchronous read and write	Active High
RESETB	24	Input	Active low reset for entire chip	Active Low
AXI Data Transmission Interface				

S_DATA<0:15>	2,3,7,10,11,12,14,15,23,37,38,39,43,46,47,48	Input	Write Data, S_DATA<15> is MSB	Active High
S_VALID	34	Input	Indicates S_DATA input is valid	Active High
S_LAST	25	Input	Toggled active for 1 CLK cycle on the last S_DATA stream in	Active High
S_READY	35	Output	When active, COBIFIVE is ready to receive write data	Active High
M_DATA	26	Output	Read Data	Active High
M_VALID	17	Output	COBIFIVE indicating M_DATA is valid	Active High
M_LAST	22	Output	Toggled active for 1 CLK cycle on last M_DATA stream out	Active High
M_READY	20	Input	When active, chip will load read data	Active High

Table 3.1 Pin functions

4. Supply Voltage and Current

Table 4.1 shows absolute maximum ratings over operating free-air temperature range (unless otherwise noted).

Rating	Value	Unit
VDD1P8 Voltage	1.8	V
VSS1P8 Voltage	0	V
VDD1P8 Current	20 (max)	mA
VSS1P8 Current	20 (max)	mA
VDD0P9 Voltage	0.9	V
VSS0P9 Voltage	0	V
VDD0P9 Current	140 (max)	mA
VSS0P9 Current	140 (max)	mA
Digital I/O Voltage	1.8	V
Digital I/O Current per pin	12 (max)	mA

Table 4.1 Supply voltage and current consumption

5. Chip Block Diagram

Fig. 5.1 depicts the high level block diagram of the chip.

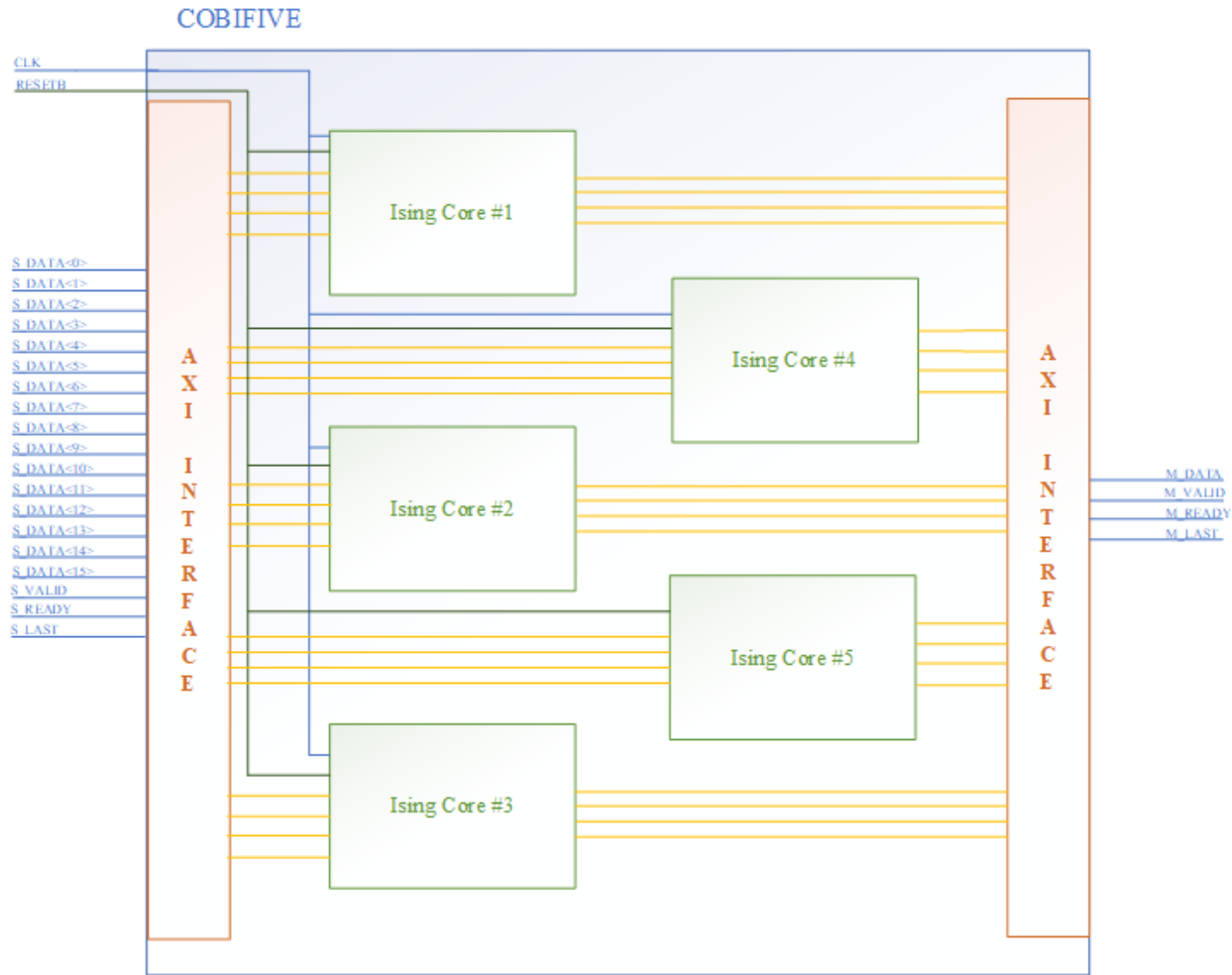


Fig. 5.1 COBIFIVE Block Diagram

6. Input format

There are four types of functional bits shown in Fig. 6.1, including calibration bits (red), SHIL (blue), control bits (yellow), dummy bits (green), short bits (gray) and data (white). The chip is configured and operates under various conditions by assigning different values to the above functional bits. In order to comply with the 16-bit AXI transaction requirements, two additional random data elements are inserted at the beginning of each line. For the actual input data, it is recommended to replace these random values with zeros.

[illegible]

Fig. 6.1 Input Graph Format

Control bits	Width	Description	Range Values	Suggested default
sample_time	16b	Parameter in controller, time duration between two sample signal, would better if greater than 8C which is used for pre-silicon verification	0x0000 ~ 0xFFFF	0x00FD

weight_time	16b	Parameter in controller, time duration between two weight_enb (weight enable) signals, usually the same as shil_time	0x0000 ~ 0xFFFF	0x0003
shil_time	16b	Parameter in controller, time duration between two shil_enb (shil enable) signal, usually the same as weight_time_off	0x0000 ~ 0xFFFF	0x000F
rosc_time	16b	Not used	0x0000 ~ 0xFFFF	0x0003
max_fails	16b	Parameter in accelerator, a static sampling parameter, should be no less than 1	0x0000 ~ 0xFFFF	0x001F
sample_delay	16b	Parameter in accelerator, delay parameter from Ising core to accelerator	0x0000 ~ 0xFFFF	0x00FF
dco_freq	4b	Frequency setting for dco, used for configuring different dco frequency a. Chip will only function correctly when dco_freq = 0x0000 or it will result in intermittent stalls	0x0000 ~ 0x000F	0x0000 (USE THIS VALUE ONLY)
problem_id	16b	The id of problems, special meaning for the highest bit a. problem_id[15] = 1'b1 -> bypass gradient search (use 0 as default)	0x0000 ~ 0xFFFF	0x0000 ~ 0x00FF

Table 6.1 Last row control bits explanation

Write Text File Conversion (Hexadecimal to Binary)

Here is an example of how the 4-Character Hexadecimal data is written to the chip through the AXI stream bus protocol:

4-Character Hexadecimal data = 000A

S_DATA<15:0> = 0000 0000 0000 1010

0 0 0 A

OR

S_DATA <15> = 0

S_DATA <14> = 0

S_DATA <13> = 0

S_DATA <12> = 0

S_DATA <11> = 0

S_DATA <10> = 0

S_DATA <9> = 0

S_DATA <8> = 0

S_DATA <7> = 0

S_DATA <6> = 0

S_DATA <5> = 0


```
S_DATA <4> = 0
S_DATA <3> = 1
S_DATA <2> = 0
S_DATA <1> = 1
S_DATA <0> = 0
```

The following example graph demonstrates how hexadecimal bits are grouped to form 16-bit segments and transmitted via the AXI interface. Consider the last three rows from Fig. 6.1 Input Graph as an example. These rows correspond to data, calibration, short, and control bits, respectively. In reality, the input data will transfer from the first row to the 51st row.

[illegible]

Fig. 6.2 Last two rows' data from Fig. 6.1 Input Graph Format

Figure 6.3 demonstrates how the input graph data is transferred to COBIFIVE through the AXI interface. The transfer always begins from right to left for each row, as illustrated in Figure 6.4.

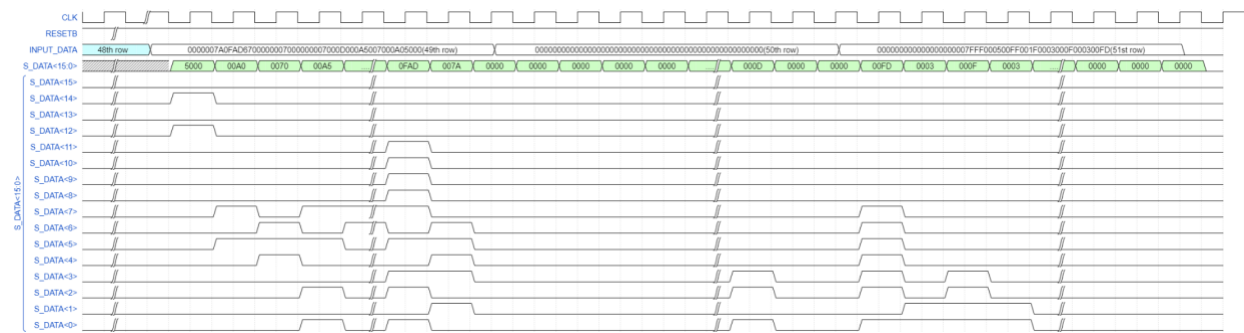


Fig. 6.3 Hex Bits Transition Via 16-bit AXI

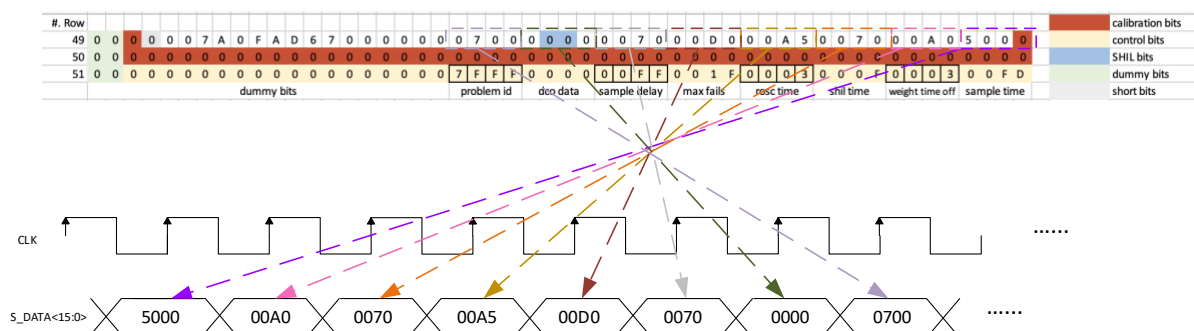


Fig. 6.4 Sequential Data Transfer Across Rows with Bit Mapping

Data and signals to the COBIFIVE are to be switched on negative CLK edges to prevent setup and hold time violations.

Writing to the chip occurs asynchronously of reading. Writing can occur during reading.

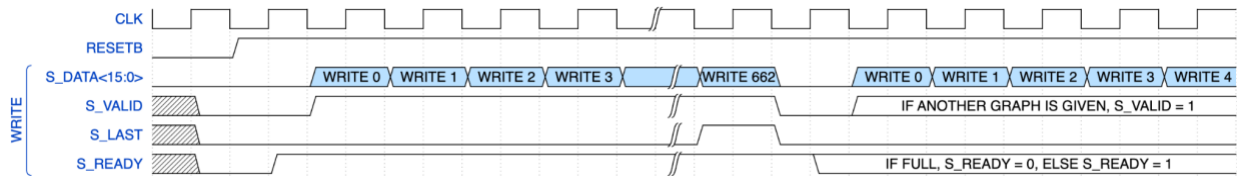


Fig. 9.1.1 Writing Directly After Reset

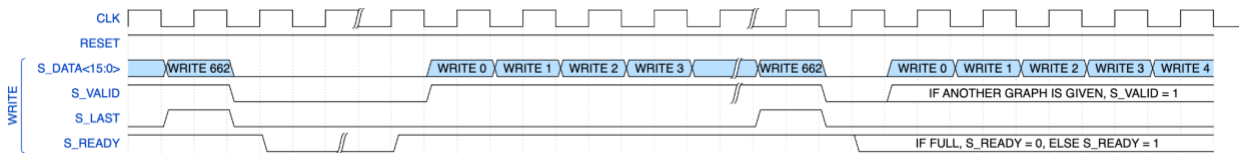


Fig. 9.1.2 Write After Waiting for S_READY High

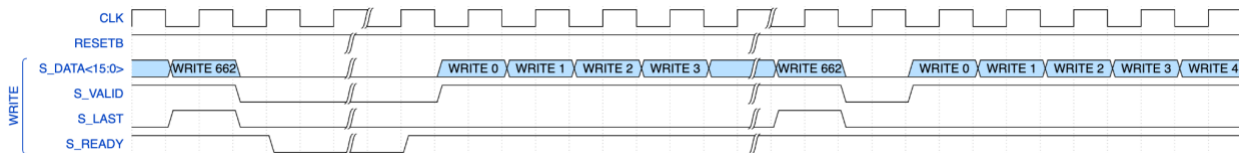


Fig. 9.1.3 Write Directly If both S_READY and S_VALID Stays High

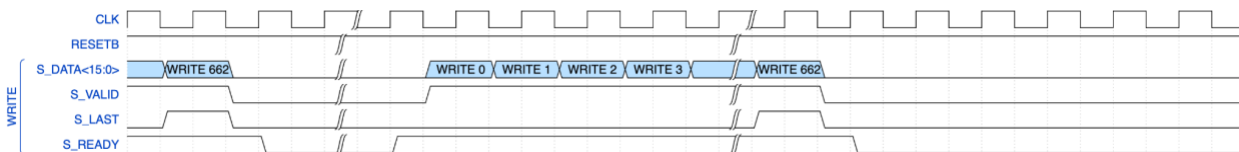


Fig. 9.1.4 No Write If S_READY Goes Low

NOTE: After S_LAST is toggled, the COBIFIVE may or may not be able to accept more data. If both S_VALID and S_READY stays **HIGH**, continue to the next write pattern. Otherwise, if S_READY goes **LOW** after S_LAST is toggled, wait until S_READY goes **HIGH** again. Both scenarios are shown in “Writing Directly After Reset” and “Write After Waiting for S_READY High”. “Write Directly If both S_READY and S_VALID Stays High” shows the continuous write mode. “No Write If S_READY Goes Low” shows the stop writing mode.

9.2 Read Timing and Control

A read pattern within the COBIFIVE consists of 69 writes of 1 bit (M_DATA is 1 bits). At the 69th write, M_LAST will be toggled high. Read 0 is the first line of the text file. The last line is Read 68.

Data and signals from the COBIFIVE are to be recorded on negative CLK edges to ensure data stability.

Reading from the chip occurs asynchronously of writing. Reading can occur during writing.

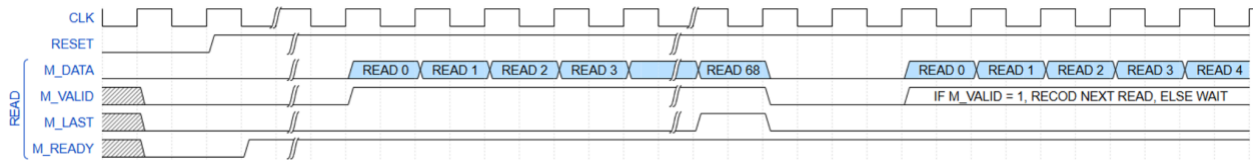


Fig. 9.2.1 Read After Reset

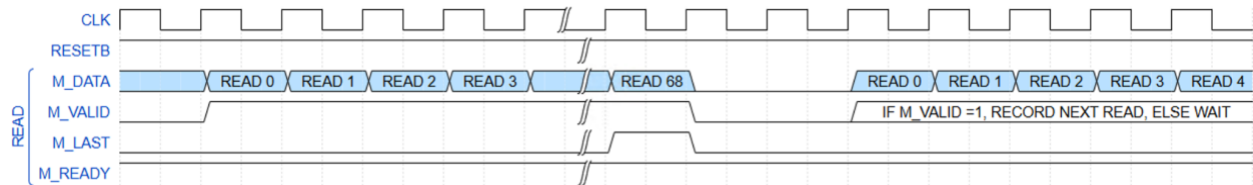


Fig. 9.2.2 Read After Waiting for M_VALID

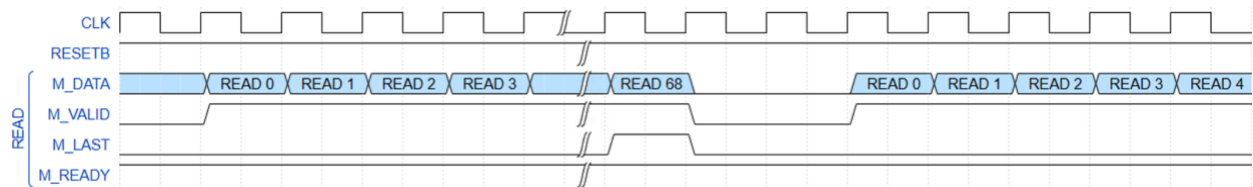


Fig. 9.2.3 Read If M_VALID Stays HIGH

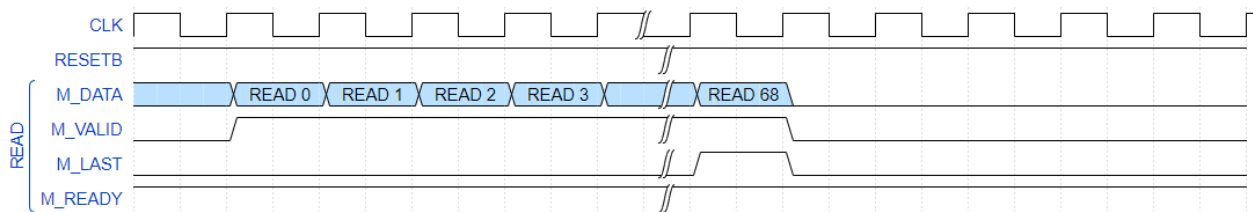


Fig. 9.2.4 Read If M_VALID Goes Low

NOTE: After M_LAST is toggled, the COBIFIVE may or may not be able to read more data. If both M_VALID stays **HIGH**, continue to the next read-out pattern. Otherwise, if M_VALID goes **LOW** after M_LAST is toggled, wait until M_VALID goes **HIGH** again. Both scenarios are shown in “**Read After Reset**” and “**Read After Waiting for M_VALID**”. “**Read If M_VALID Stays HIGH**” shows the continuous write mode. “**Read If M_VALID Goes Low**” shows the stop writing mode.

Multiple boards, multiple chips, and multiple core operation example

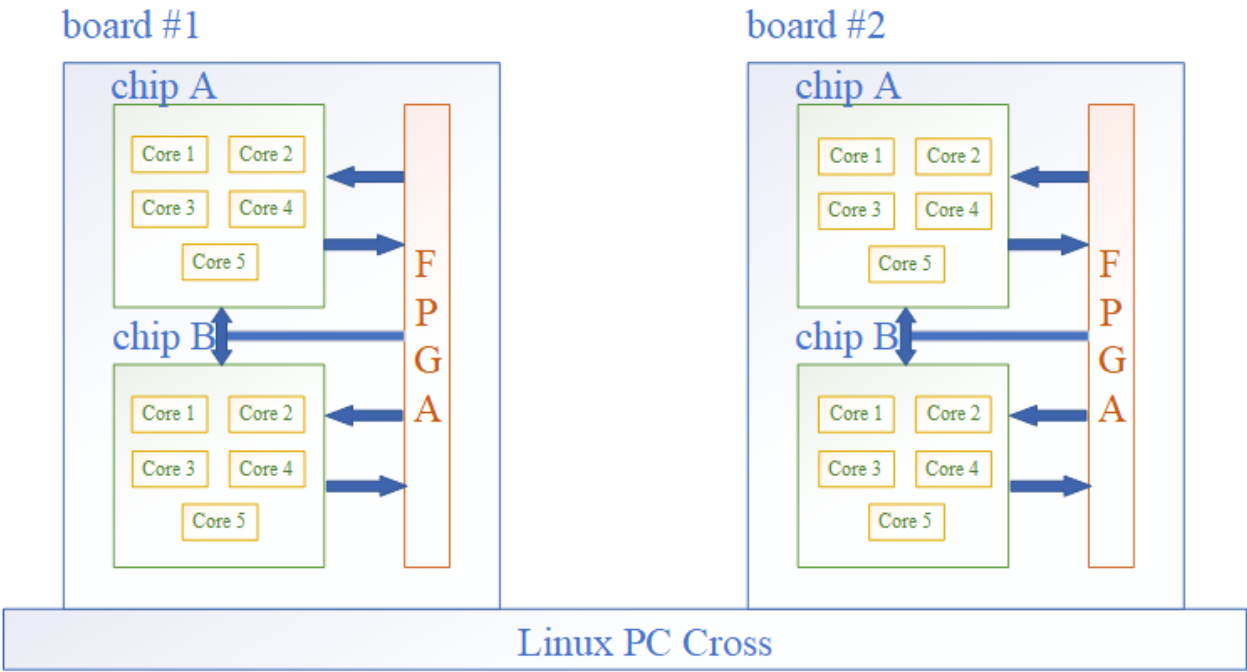
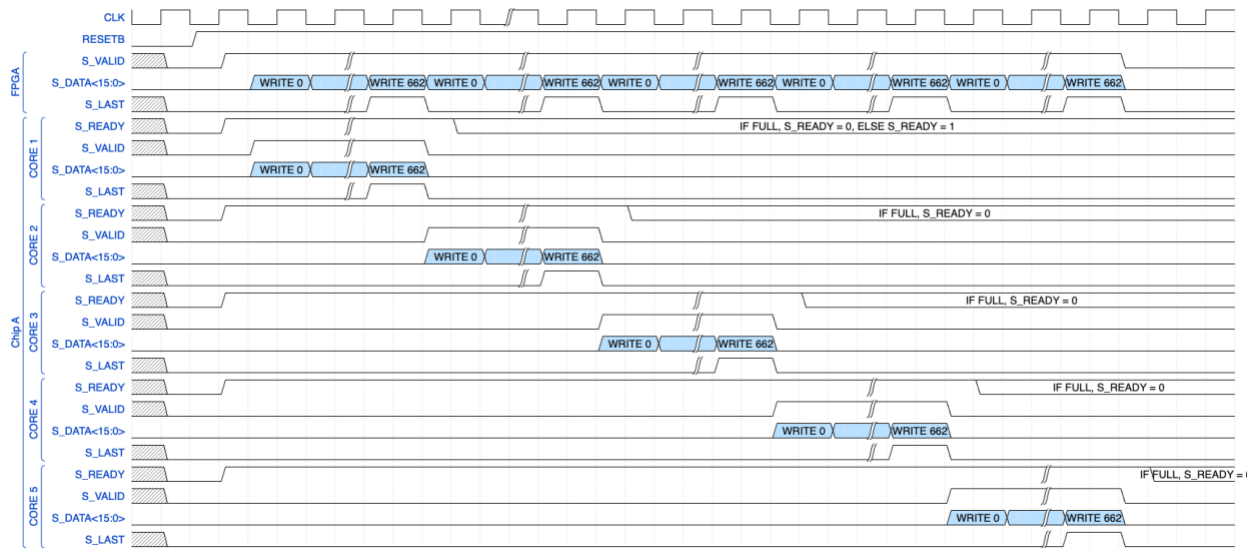


Fig. 9.4 Multiple Chips controlled by FPGA



Appendix A

Input data (52 columns x 51 rows x 4b)

All 0 weight graph example

[illegible]

All +7 weight graph example

[illegible]

Random weight graph example

[illegible]

Expected output from chip (69 bits)

Best_Ham[14:0], Best_Spins[45:0], Core_ID[3:0], Problem_ID[3:0]

All 0 weight graph example

Take core 0 as an example when `problem_id[15] = 1'b0`

[illegible]

Best_Spins[45:0] should look like random 0's and 1's

All + 7 weight graph example

Take core 0 as an example when `problem_id[15] = 1'b0`

[illegible]

Best Spins[45:0] should be all 0's

Random weight graph example

(energy might be differ but similar to -650 as max_fails is set to tb 2 for boosting the simulation speed)

Take core 0 as an example when `problem_id[15] = 1'b0`

[illegible]

(around -650) Best_Spins[45:0] will be random since it is an analog circuit

Appendix B

Input data examples (52 columns x 51 rows x 4b) including random, all +3, all +2, and all +1 graphs, for additional testing and verification.

All +3 weight graph example

[illegible]

Random weight graph 1 example

[illegible]

Random weight graph 2 example

[illegible]

Random weight graph 3 example

000
00005508080000000000D00000940000B300000000000000000000000
000A05EBE0000000000000000000000000000060C90000007000
0000000F90000D000044300000090000A00044000080E00000B0
000000000D00000F000000000E0EA0A000000000F02000000
0000D0500000000000000D000000000200000000E00009000
0000000005000073C000F0F00055020000700B0000000F00D0
0000B000044000E00F00000000000680000004460000050
00006600000000000000000000000990000F00500000000
000007402F000000300000C000F0EC900F000C000009700
000050900000000000000060000000000000000000000005
0000000000500000000F0EF00000400002A00008800000000
00000000000B000000E0F3000009008C0000000000F08000
0000000000000000A00300000C0000E0000000000000000
000E0000200000000DB0020000000005070002700035000
000D000000000000004C0000000000000000000000000070
0000E0000DE00000060A6000000000000A3000000000000
0000B0000000000000F0000000000000000000000E0800000
00004000C000000000000000025000000E00000000F00
0000B0005000000005000000070000E6000000000000040
000000000000000200000000070000320000000D0A07B00
00000000000030F000000000400000008D00B000000000
000080000000000000000000000000000000E0500000D7B0
000000050400000000000040000020000000F40000A5000
000000900009000000060000000A700000000006007400
000
00
0003000000004A0060A00000000000000200A03F0FA0A0000
0002600000000000F00000000000F00C00000300000000000
0000000040F0000004000F00003000E00000000000000E00
00000006900680000000004000000080000000300007800
0000D00007080F0000E90000700005000000044600000
00000A8000D00E0000300000006000000B0E0A00000CB0000
00030000C006000000000C0006004008008000A000480000
000000000B000700000000800F0A0B80000F060B8000200
0000FB0000000000000D0D6000000000008007000000D0
008000D0000000000E000000DC0F00007000000000200900
000AA500000000020707000900800040000000005C0080
0000000003000000B080000000000000B00300000006000
0000000000000000000590000000700090000000003000
00000000000000090000000000000083000070A000000000
0002060090000000C009F0000000000090D0000000000A20
000D000A00000A000C0200000000000070070000000000
0009000004000C0090000000000000000A00000000005E0
0000B004000000000720700E0008B000000E700C00000
000BF0000E0C0040B0000350000800000066000AB00005000
00000000000000000390000B0000507600000065000000
0000000006400084002D00000E080006000A0500080000
0000000090030400AE02500000000B00000D00200900500
000
00AAAAAAAAAAAAAAAAAAAAA01100000FF001F00300F00300F

Random weight graph 4 example

```
000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000000000000000
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000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000000000000000
00090000F0900000D0030000008BC00000000000000000000000
000000B4040000000703000009000A0E00000000000000000000
0000000C00000700000000000000000020000000000000000000
00000000B000000000000000000000000000002D000000000000
00007000E00000C0000800000000063000C000000000000000000
000000000000800000000000000C000000C00000E3000000000000
0004008F08000005000F00000000000000000000000000000000
00000000F000A0A0D500C0000FF0F0400000000000000000000
000004000000000E000000000000000B000D0000000000000000
0000F000004000000E0005000000B0300404000000000000000
0000000000C0000080099000005000809B00000000000000000
00200000600B0000000B60000000080000000000000000000000
0000000000002D04000000450000000000000E0000000000000
000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000000000000000
0000870000000000300000000000A0A30CEFF0000000000000000
0000B0000000020000600C00000800E000BE7000000000000000
0000000007000D6000006000000000093030000000000000000
000000000A0000000000000000000000000000A0000000000000
0000000000F0600800FE2000F0A9000000000000000000000000
00030000C000000000000007000005E00004000000000000000
0000000A0A0000000000000000000000000000000000000000000
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0000040770B00000300009000FF000470090000000000000000
00000B00000000000000B5D0000000000000000000000000000
000000000000000000000000000000000000000000000000000
00AAAAAAAAAAAAAAAAAAAAAA011100000FF001F0003000F000300F
```

Random weight graph 5 example

[illegible]

Random weight graph 6 example

[illegible]

