COBIFIVE Datasheet

Five core quantum-inspired Ising solver chip

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# 1. Overview

**COBIFIVE Ising Solver Chip**

**AXI Interface**

* >50MHz AXI clock frequency
* Asynchronous read-write
* 16-bit write data bus
* 1-bit read data
* \*\_LAST signals included in the AXI interface

**Input/Output Pads**

* 25 input/output digital pins
  + Input pin configuration: Schmitt trigger
  + Output pin configuration: Hysteresis and pull-down, 12mA drive current per pin

**Features**

* Manufactured in 28nm
* 0.9V core voltage, 1.8V IO voltage
* Input data: 52 x 51 hex numbers = 52 x 51 x 4 = 10,608 bits
* Output data: 69 bits
  + 15b (best\_ham) + 46b (best\_spin) + 4b (core id) + 4b (problem\_id)
  + First output: best\_ham
  + Last output: problem\_id
* Programmable on-chip clock frequency ranging from 150MHz to 2GHz

# 2. Pin Configuration

Fig. 2.1 illustrates the bonding diagram of COBIFIVE which is using QP-QFN48-6MM-.4MM package type as shown in Fig. 2.2.

A computer chip with many numbers and a black square

Description automatically generated with medium confidence

Fig. 2.1. COBIFIVE chip bonding diagram

A blueprint of a computer chip

Description automatically generated

Fig. 2.2. COBIFIVE chip package diagram (QFN 48, 6mm x 6mm, 0.4mm pitch)

# 3. Pin Function

Table 3.1 describes the Pin Functions of COBIFIVE

| Pin | | I/O | Description | Activation Type |
| --- | --- | --- | --- | --- |
| Name | Number |
| **Power/ Ground** | | | | |
| VDD1P8 | 6,19,31,42 | PWR | I/O power supply 1.8V | NA |
| VSS1P8 | 1,13,30,36 | PWR | I/O power supply 0V | NA |
| VDD0P9 | 4,9,16,21,28,33,40,45 | PWR | Core power supply 0.9V | NA |
| VSS0P9 | 5,8,18,29,32,41,44 | PWR | Core power supply 0V | NA |
| **CLK, Reset** | | | | |
| CLK | 27 | Input | AXI clock used for both asynchronous read and write | Active High |
| RESETB | 24 | Input | Active low reset for entire chip | Active Low |
| **AXI Data Transmission Interface** | | | | |
| S\_DATA<0:15> | 2,3,7,10,11,12,14,15,23,37,38,39,43,46,47,48 | Input | Write Data, S\_DATA<15> is MSB | Active High |
| S\_VALID | 34 | Input | Indicates S\_DATA input is valid | Active High |
| S\_LAST | 25 | Input | Toggled active for 1 CLK cycle on the last S\_DATA stream in | Active High |
| S\_READY | 35 | Output | When active, COBIFIVE is ready to receive write data | Active High |
| M\_DATA | 26 | Output | Read Data | Active High |
| M\_VALID | 17 | Output | COBIFIVE indicating M\_DATA is valid | Active High |
| M\_LAST | 22 | Output | Toggled active for 1 CLK cycle on last M\_DATA stream out | Active High |
| M\_READY | 20 | Input | When active, chip will load read data | Active High |

Table 3.1 Pin functions

# 4. Supply Voltage and Current

Table 4.1 shows absolute maximum ratings over operating free-air temperature range (unless otherwise noted).

| Rating | Value | Unit |
| --- | --- | --- |
| VDD1P8 Voltage | 1.8 | V |
| VSS1P8 Voltage | 0 | V |
| VDD1P8 Current | 20 (max) | mA |
| VSS1P8 Current | 20 (max) | mA |
| **VDD0P9 Voltage** | **0.9** | **V** |
| **VSS0P9 Voltage** | **0** | **V** |
| **VDD0P9 Current** | **140 (max)** | **mA** |
| **VSS0P9 Current** | **140 (max)** | **mA** |
| Digital I/O Voltage | 1.8 | V |
| Digital I/O Current per pin | 12 (max) | mA |

Table 4.1 Supply voltage and current consumption

# 5. Chip Block Diagram

Fig. 5.1 depicts the high level block diagram of the chip.

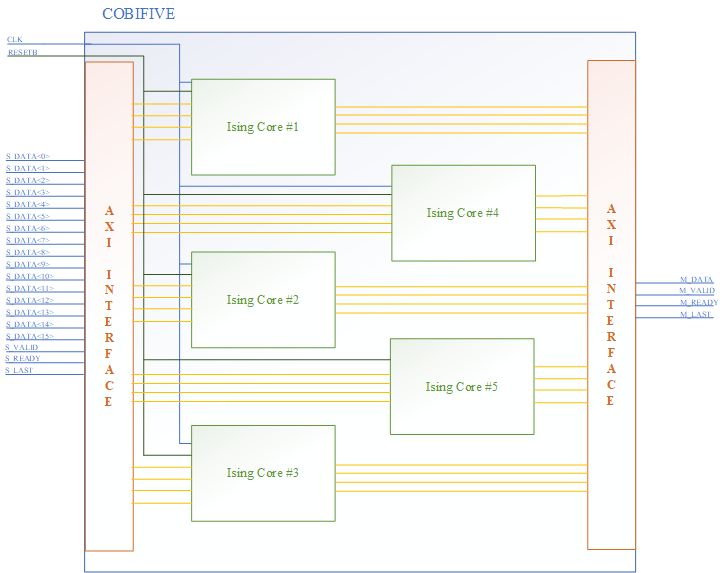


Fig. 5.1 COBIFIVE Block Diagram

# 6. Input format

There are four types of functional bits shown in Fig. 6.1, including calibration bits (red), SHIL (blue), control bits (yellow), dummy bits (green), short bits (gray) and data (white). The chip is configured and operates under various conditions by assigning different values to the above functional bits. In order to comply with the 16-bit AXI transaction requirements, two additional random data elements are inserted at the beginning of each line. For the actual input data, it is recommended to replace these random values with zeros.



Fig. 6.1 Input Graph Format

| Control bits | Width | Description | Range Values | Suggested default |
| --- | --- | --- | --- | --- |
| sample\_time | 16b | Parameter in controller, time duration between two sample signal, would better if greater than 8C which is used for pre-silicon verification | 0x0000 ~ 0xFFFF | 0x00FD |
| weight\_time | 16b | Parameter in controller, time duration between two weight\_enb (weight enable) signals, usually the same as shil\_time | 0x0000 ~ 0xFFFF | 0x0003 |
| shil\_time | 16b | Parameter in controller, time duration between two shil\_enb (shil enable) signal, usually the same as weight\_time\_off | 0x0000 ~ 0xFFFF | 0x000F |
| rosc\_time | 16b | Not used | 0x0000 ~ 0xFFFF | 0x0003 |
| max\_fails | 16b | Parameter in accelerator, a static sampling parameter, should be no less than 1 | 0x0000 ~ 0xFFFF | 0x001F |
| sample\_delay | 16b | Parameter in accelerator, delay parameter from Ising core to accelerator | 0x0000 ~ 0xFFFF | 0x00FF |
| dco\_freq | 4b | Frequency setting for dco, used for configuring different dco frequency   1. Chip will only function correctly when **dco\_freq = 0x0000** or it will result in intermittent stalls | 0x0000 ~ 0x000F | **0x0000**  **(USE THIS VALUE ONLY)** |
| problem\_id | 16b | The id of problems, special meaning for the highest bit   1. problem\_id[15] = 1’b1 -> bypass gradient search (use 0 as default) | 0x0000 ~ 0xFFFF | 0x0000 ~ 0x00FF |

Table 6.1 Last row control bits explanation

**Write Text File Conversion (Hexadecimal to Binary)**

Here is an example of how the 4-Character Hexadecimal data is written to the chip through the AXI stream bus protocol:

4-Character Hexadecimal data = 000A

S\_DATA<15:0> = 0000 0000 0000 1010

0 0 0 A

**OR**

S\_DATA <15> = 0

S\_DATA <14> = 0

S\_DATA <13> = 0

S\_DATA <12> = 0

S\_DATA <11> = 0

S\_DATA <10> = 0

S\_DATA <9> = 0

S\_DATA <8> = 0

S\_DATA <7> = 0

S\_DATA <6> = 0

S\_DATA <5> = 0

S\_DATA <4> = 0

S\_DATA <3> = 1

S\_DATA <2> = 0

S\_DATA <1> = 1

S\_DATA <0> = 0

The following example graph demonstrates how hexadecimal bits are grouped to form 16-bit segments and transmitted via the AXI interface. Consider the last three rows from Fig. 6.1 Input Graph as an example. These rows correspond to data, calibration, short, and control bits, respectively. In reality, the input data will transfer from the first row to the 51st row.



Fig. 6.2 Last two rows’ data from *Fig. 6.1* *Input Graph Format*

Figure 6.3 demonstrates how the input graph data is transferred to COBIFIVE through the AXI interface. The transfer always begins from right to left for each row, as illustrated in Figure 6.4.

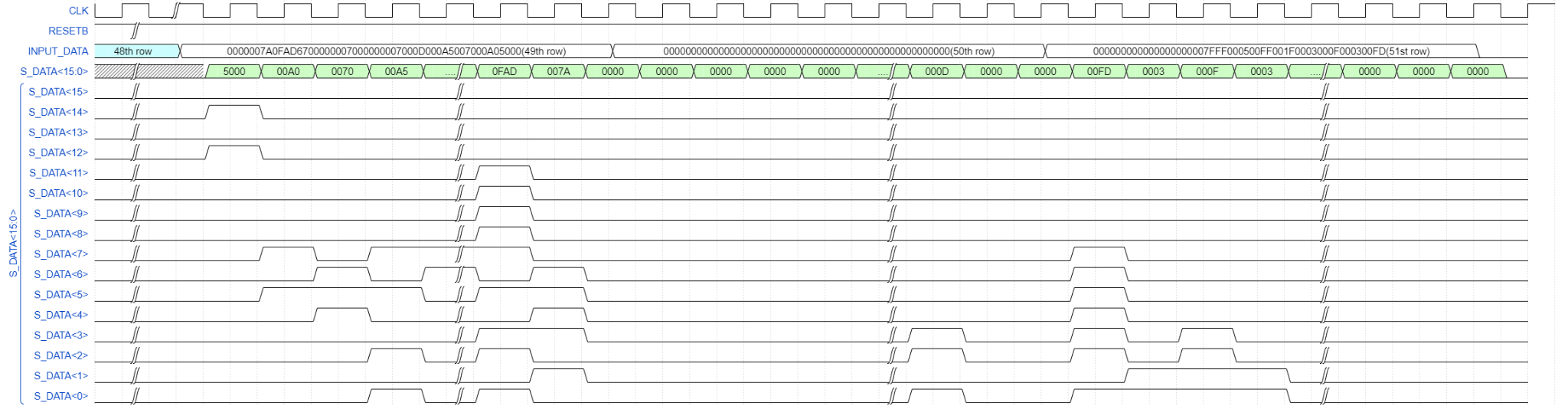


Fig. 6.3 Hex Bits Transition Via 16-bit AXI



Fig. 6.4 Sequential Data Transfer Across Rows with Bit Mapping

# 7. Output Format

COBIFIVE outputs 69 bits when each core completes the computation. The breakdown of the output bits from left to right is:

Best\_Ham[14:0], Best\_Spins[45:0], Core\_ID[3:0], Problem\_ID[3:0] (only last hex digit)

Here’s an example output bit stream.

000000000000000RRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRR10001000

R: random 1’s and 0’s, changes every time

# 8 Reset Timing and Control

Table 8.1 provides the definition, typical values and maximum clock frequency.

| Pin | Description | Symbol | Min | Typ | Max | Unit |
| --- | --- | --- | --- | --- | --- | --- |
| CLK | AXI Write and Read Clock Frequency (tcyc = 1/fBus) | fBus | dc | 125 | 200 | MHz |

Table 8.1 AXI clock frequency

RESETB will be activated low to initialize COBIFIVE at the beginning, and then set to high while waiting for the next rising edge of CLK.



Fig. 8.1 COBIFIVE Startup/Reset

# 9. Application Information

## 9.1 Write Timing and Control

A write pattern within the COBIFIVE consists of 663 writes of 16 bits (S\_DATA is 16 bits). At the last write cycle, S\_LAST will be toggled high. A text file similar to Fig. 6.1, consisting of 663 lines of data with each line containing 16 bits in hexadecimal, represents the written pattern.

Data and signals to the COBIFIVE are to be switched on negative CLK edges to prevent setup and hold time violations.

Writing to the chip occurs asynchronously of reading. Writing can occur during reading.

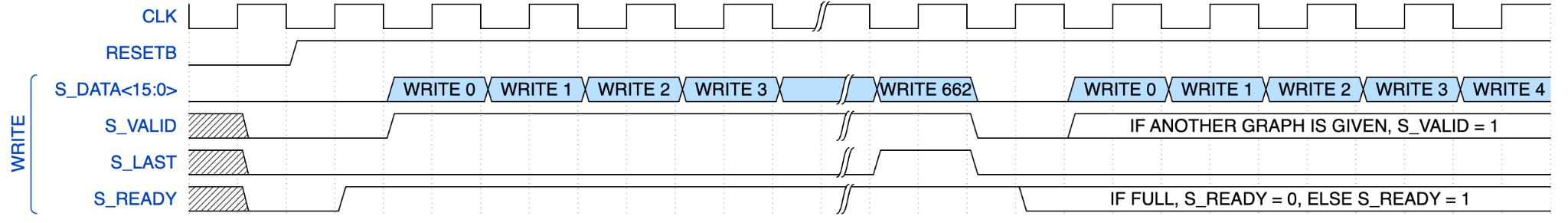
****

Fig. 9.1.1 Writing Directly After Reset

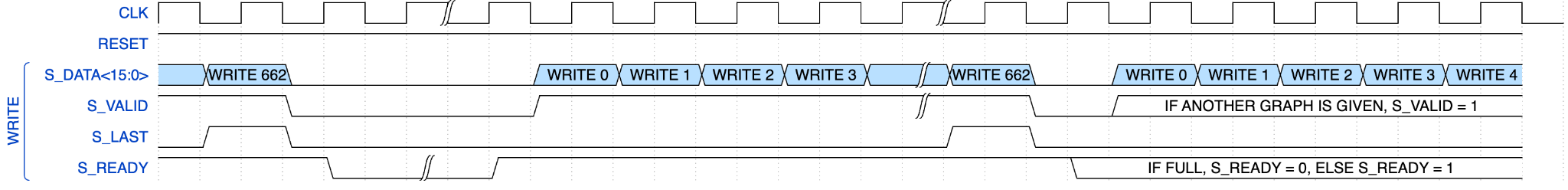
****

Fig. 9.1.2 Write After Waiting for S\_READY High

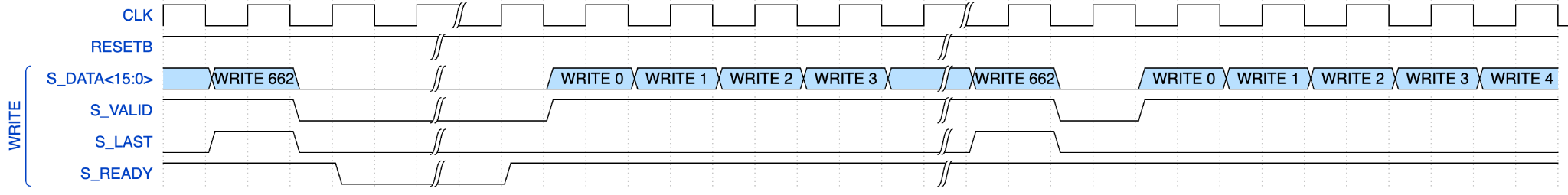
****

Fig. 9.1.3 Write Directly If both S\_READY and S\_VALID Stays High

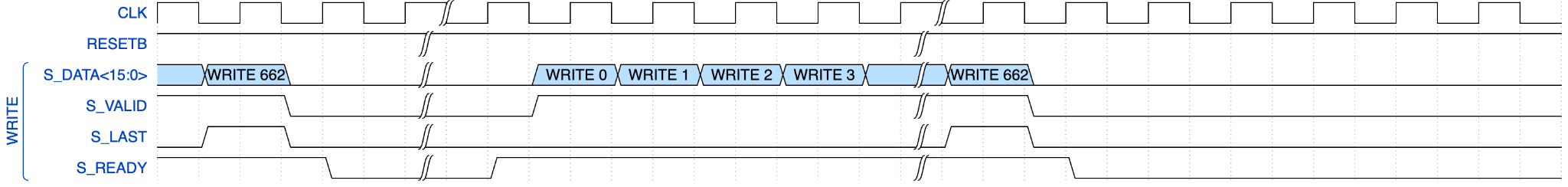
****

Fig. 9.1.4 No Write If S\_READY Goes Low

NOTE: After S\_LAST is toggled, the COBIFIVE may or may not be able to accept more data. If both S\_VALID and S\_READY stays **HIGH**, continue to the next write pattern. Otherwise, if S\_READY goes **LOW** after S\_LAST is toggled, wait until S\_READY goes **HIGH** again. Both scenarios are shown in “**Writing Directly After Reset”** and “**Write After Waiting for S\_READY High**”. “**Write Directly If both S\_READY and S\_VALID Stays High”** shows the continuous write mode. “**No Write If S\_READY Goes Low”** shows the stop writing mode.

## 9.2 Read Timing and Control

A read pattern within the COBIFIVE consists of 69 writes of 1 bit (M\_DATA is 1 bits). At the 69th write, M\_LAST will be toggled high. Read 0 is the first line of the text file. The last line is Read 68.

Data and signals from the COBIFIVE are to be recorded on negative CLK edges to ensure data stability.

Reading from the chip occurs asynchronously of writing. Reading can occur during writing.

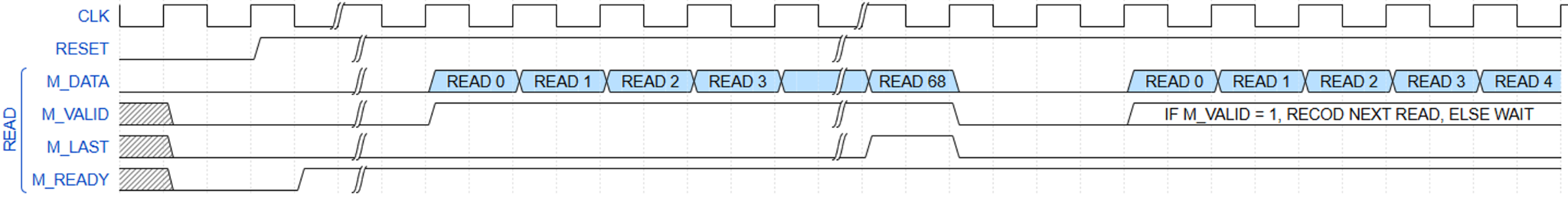


Fig. 9.2.1 Read After Reset

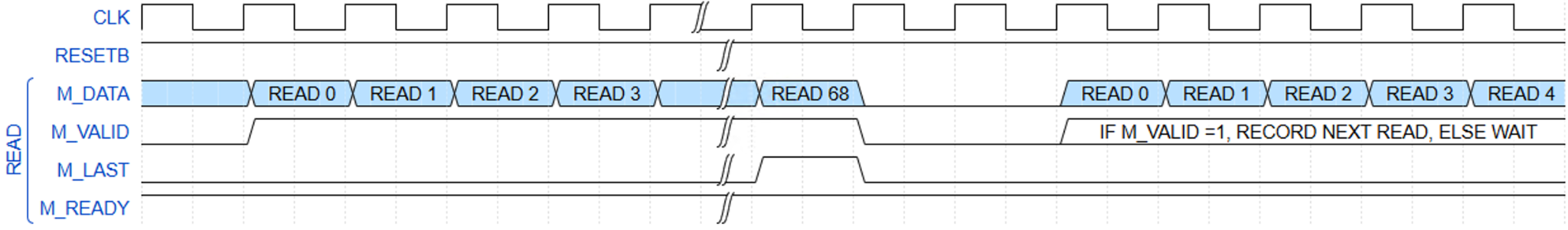


Fig. 9.2.2 Read After Waiting for M\_VALID

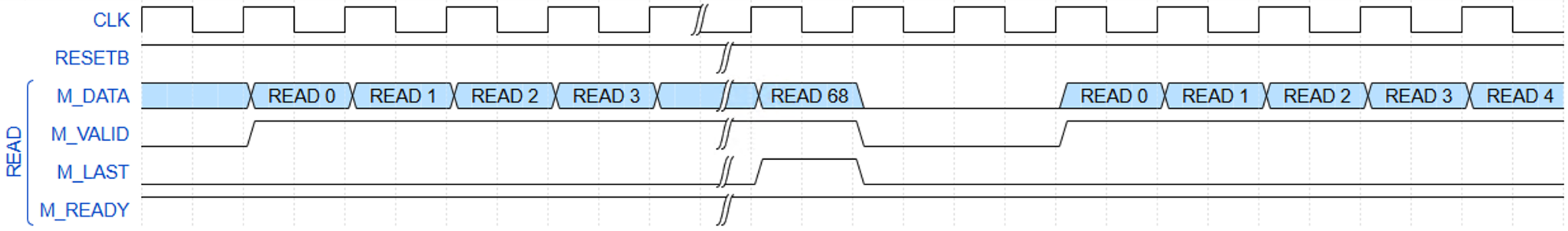


Fig. 9.2.3 Read If M\_VALID Stays HIGH

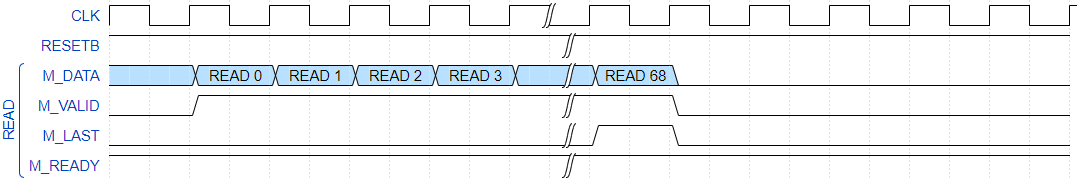


Fig. 9.2.4 Read If M\_VALID Goes Low

NOTE: After M\_LAST is toggled, the COBIFIVE may or may not be able to read more data. If both M\_VALID stays **HIGH**, continue to the next read-out pattern. Otherwise, if M\_VALID goes **LOW** after M\_LAST is toggled, wait until M\_VALID goes **HIGH** again. Both scenarios are shown in “**Read After Reset”** and “**Read After Waiting for M\_VALID**”. “**Read If M\_VALID Stays HIGH”** shows the continuous write mode. “**Read If M\_VALID Goes Low”** shows the stop writing mode.

## Multiple boards, multiple chips, and multiple core operation example

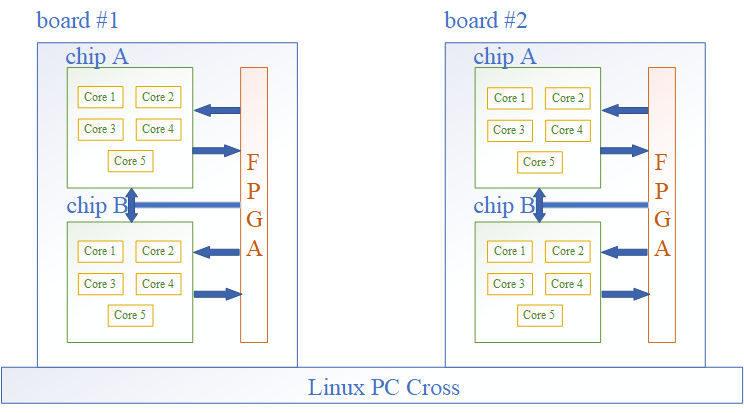
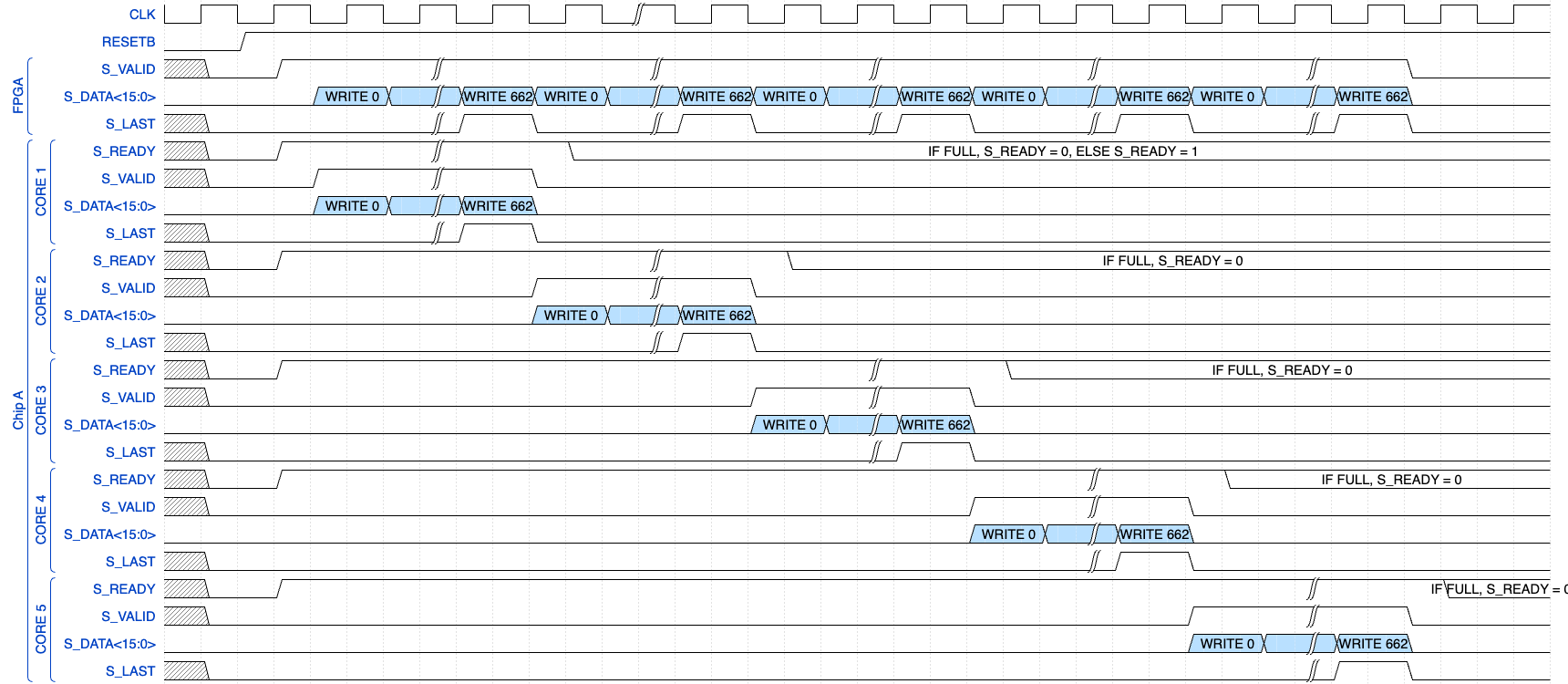


Fig. 9.4 Multiple Chips controlled by FPGA



# Appendix A

## Input data (52 columns x 51 rows x 4b)

All 0 weight graph example All +7 weight graph example 



Random weight graph example

## Expected output from chip (69 bits)

Best\_Ham[14:0], Best\_Spins[45:0], Core\_ID[3:0], Problem\_ID[3:0]

All 0 weight graph example

Take core 0 as an example when problem\_id[15] = 1’b0

000000000000000 1111111111111111111111111111111111111111111111 0000 0001

Best\_Spins[45:0] should look like random 0’s and 1’s

All + 7 weight graph example

Take core 0 as an example when problem\_id[15] = 1’b0

100011101100110 0000000000000000000000000000000000000000000000 0000 0001

Best\_Spins[45:0] should be all 0’s

Random weight graph example

(energy might be differ but similar to -650 as max\_fails is set to tb 2 for boosting the simulation speed)

Take core 0 as an example when problem\_id[15] = 1’b0

111110101110110 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx 0000 0001

(around -650) Best\_Spins[45:0] will be random since it is an analog circuit

# Appendix B

## Input data examples (52 columns x 51 rows x 4b) including random, all +3, all +2, and all +1 graphs, for additional testing and verification.

All +3 weight graph example

All +2 weight graph example All +1 weight graph example



Random weight graph 1 example Random weight graph 2 example



Random weight graph 3 example Random weight graph 4 example



Random weight graph 5 example Random weight graph 6 example



Random weight graph 7 example Random weight graph 8 example 

