EECS 215: Introduction to Electronic Circuits FA24
Homework Set 5

Issued: 10/4/24

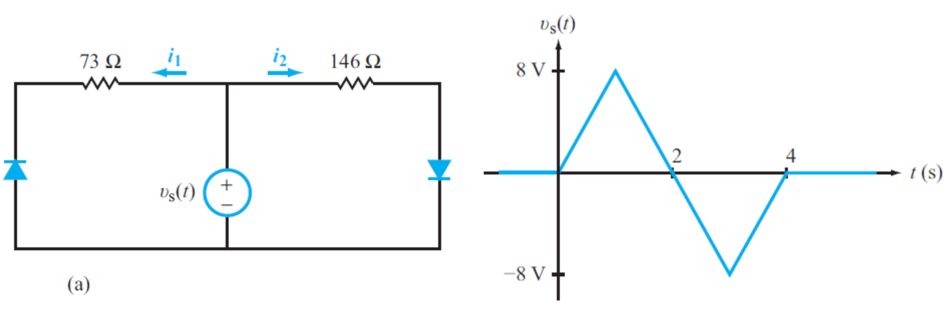
Due: 10/11/24, 5;00 PM submitted electronically on Gradescope.

Contents

Problem 1. UMF P2.71 with additions.

a. Use Matlab to generate the plots. Assume 0.7V for the voltage drop of a forward-biased diode.
b. Simulate using LTSpice (see the diode example from HW03) and compare the results to part a.

2.71 If the voltage source in the circuit of Fig. P2.70(a) generates the single triangular waveform shown in Fig. P2.70(c), generate plots for $i_1(t)$ and $i_2(t)$.



(c) Triangular wave

Problem 2. UMF P.3.93 with modifications.

a. Draw the linear circuit model for this circuit.

b. Obtain an expression for V_{out} vs. V_{in} for the circuit below. Assume $V_{BE} = 0.7V$ when the transistor is on and that we are interested in the regime $V_{in} \geq 0.7V$

c. What is the small signal gain of this circuit $G = \frac{\partial V_{out}}{\partial V_{in}}$

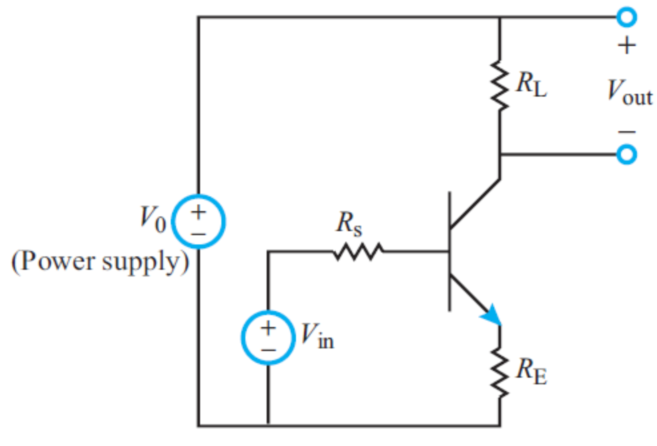


Figure P3.93: Circuit for Problem 3.93.

Problem 3. UMF with additions/changes

a. Do the problem as stated in the text but with the device transconductances changed to $g_1 = g_2 = 20\Omega^{-1}$. If needed, assume the MOSFET threshold voltage is 0.

b. Find the Thevenin equivalent for this circuit as seen at the output.

*4.60 Determine $v_{out}(t)$ as a function of $v_s(t)$ for the circuit in Fig. P4.60. Assume $V_{DD} = 2.5$ V.

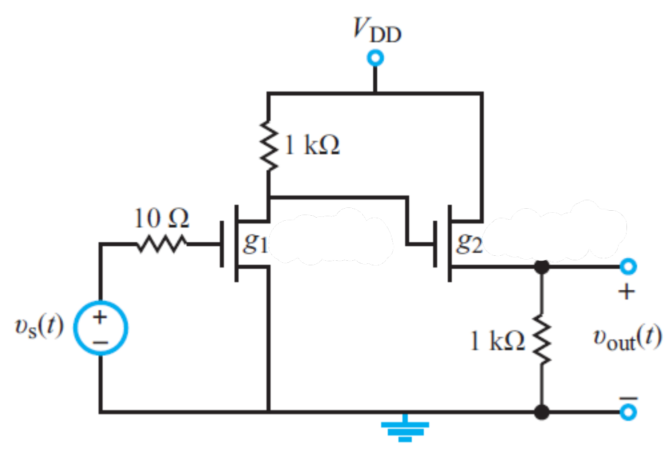


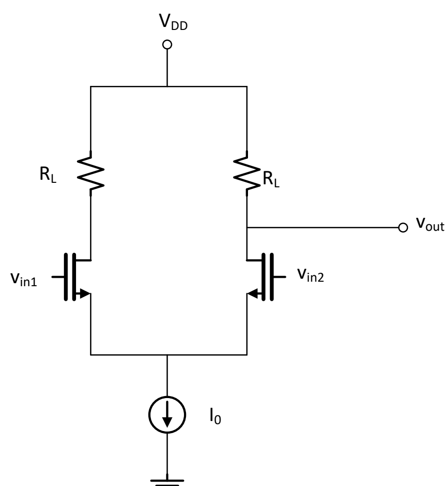
Figure P4.60: Two-MOSFET circuit for Problem 4.60.

Problem 4. MOSFET Differential Amplifier

Suppose we have the circuit shown below built with the idealized MOSFET covered in the text and class (UMF section 4-11). The two MOSFETs in the circuit are identical.

a. Redraw the circuit using the linear equivalent circuit model for the idealized MOSFET.

b. Using this picture, use nodal analysis to find a function relating v_{out} measure to ground vs. v_{in1}, v_{in2} and the MOSFET transconductance (g) and the other circuit constants.



Problem 5. UMF P3.83

a. Do the problem as stated in the text.

b. Use LTSpice to simulate for V_{oc}, I_{SC} and the circuit node voltages when the correct R_L is attached. Take the ground to be the negative terminal of the 15V voltage source.

*3.83 Determine the maximum power that can be extracted by the load resistor from the circuit in Fig. P3.83.

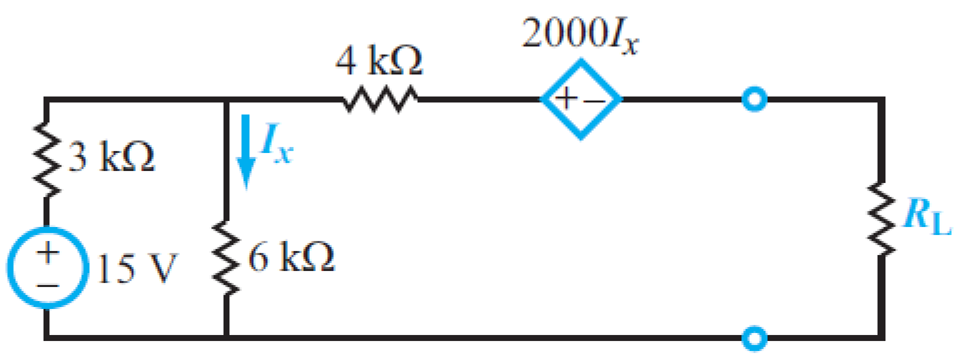


Figure P3.83: Circuit for Problem 3.83.

Problem 6. UMF P4.24 (with additions)

a. Do the problem as stated.

b. Find the limits on the linear range of v_S assuming we must have $-15V \le v_o \le 15V$ due to the power supply limitations.

4.24 For the circuit in Fig. P4.24, obtain an expression for voltage gain $G = \upsilon_o/\upsilon_s$.

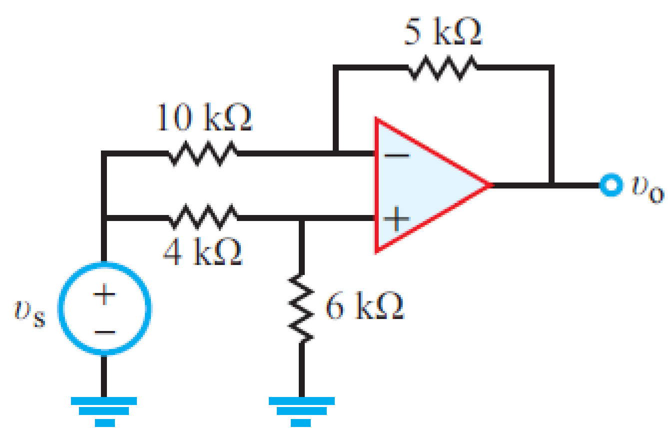


Figure P4.24 Circuit for Problem 4.24.

Problem 7. UMF 4.36

4.36 Find the value of v_o in the circuit in **Fig. P4.36**.

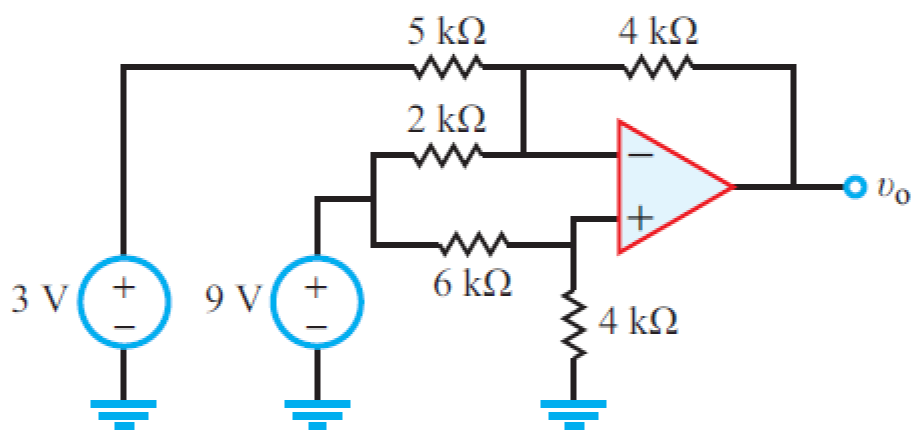


Figure P4.36 Circuit for Problem 4.36.

Problem 8. UMF 4.50

*4.50 Relate the output voltage υ_o in **Fig. P4.50** to υ_s.

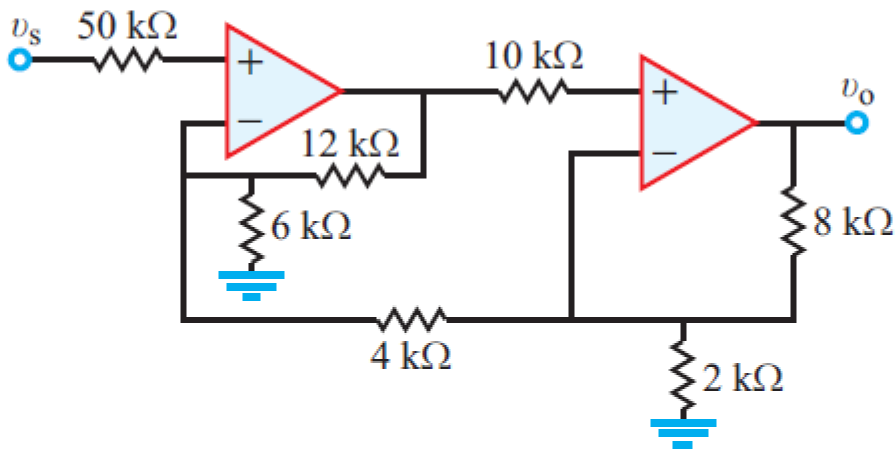


Figure P4.50 Circuit for Problem 4.50.