KEY

ECE 273 Final Exam

04.29.02

Version B

Name:

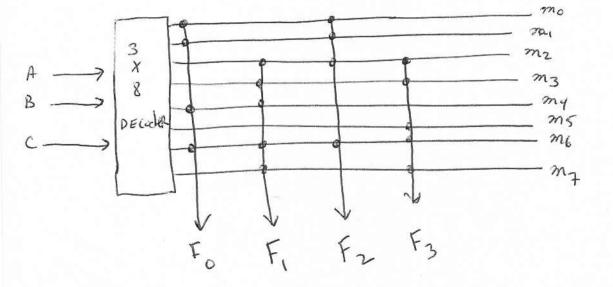
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## Instructions:

- As discussed in class, there are 5 problem categories resulting in 6 problems:
  - o (15%) Complete state machine design (problem 5)
  - o (19%) State assignment, minimization, and realization (problem 6)
  - o (18%) Multiple-input / Multiple-output devices. (problem 1)
  - o (25%) Various short minimization problems (problem 2)
  - o (23%) Short problems for misc. topics (problem 3 and problem 4)
- Work the problems in the space provided. Do not use a bluebook. If you need additional paper, put your name on it and attach it to the exam.
- Make sure the location of your answers is clear (circle them if necessary).
- Each problem has a set number of points assigned to it, designated by a number in square brackets. Problems with subparts have the point value for each subpart similarly marked.
- If you're not sure about something, *ask*. I will be happy to clarify, reword, or explain the intent of a question to you and the class. Someone else is probably wondering the same thing.
- · Don't panic.

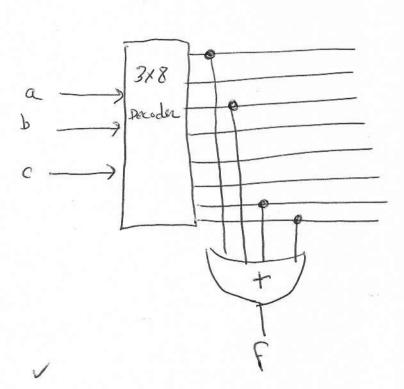
[18] 1. Complete the following problems dealing with multiple-input / multiple-output devices [10] (a) Show how to implement the following logic table using a ROM.

	I	npu	t	Output				
	A	В	C	F <sub>0</sub>	$F_1$	F <sub>2</sub>	F <sub>3</sub>	
9	0	0	0	1	0	1	0	
Į.	0	0	1	1	0	1	0	
_	0	1	0	0	1	1	1	
3	0	1	1	0	1	0	1	
1	1	0	0	1	1	0	0	
•	1	0	1	0	0	0	1	
	1	1	0	1	1	1	1	
1	1	1	1	0	1	0	1	





[4] (b) Show how to use a 3-8 Line Decoder to implement f(a,b,c) = ab + a'c'



= 
$$abc + abc'$$
  
+  $abc' + a'b'c'$   
=  $gamma m(0, 2, 6, 7)$ 

[4] (c) Show how to implement f(a,b,c) = ab + a'c' using a 4x1 multiplexer.

$$\begin{array}{c} (I_{o})C' \longrightarrow \\ (I_{o})C' \longrightarrow \\ (I_{o})C' \longrightarrow \\ (I_{o})C \longrightarrow \\ (I_{o})C$$

[25] 2. Simplify each of the following as directed [2.5 points each]. Write your answers next to the question and use the following pages for your work.

Simplify to minimum sum of products form.

(a) 
$$(A+B+C)(A'+B'+D')(A'+B'+C')(A+B+D)$$

(b) 
$$(A'+B+D)(A+C)(A+B'+D)(A'+C'+D')(A'+B)$$

(c) 
$$f(a,b,c,d) = \sum m(1,3,5,7,9,12)$$

(d) 
$$f(a,b,c,d) = \prod M(0,2,4,6,8,10,11)$$

Write in product of sums form (doesn't need to be minimum POS form)

(e) 
$$ab + a'c' + a'bc$$

(f) 
$$a'b'c'+abd+a'c+a'cd'+ac'd+ab'c'$$

Write in *minterm* form (i.e. write as  $f = \sum m(...)$ )

(g) 
$$f(a,b,c,d) = (abc'd + abcd + a'b'c'd' + abcd' + ab'c'd + ab'c'd' + a'bcd + a'b'cd)'$$

(h) 
$$f(a,b,c,d) = ab + c'd$$

Write in maxterm form (i.e. write as  $f = \prod M(...)$ )

(i) 
$$f(a,b,c,d) = [(a+b+c+d)(a'+b'+c+d')(a+b'+c'+d)(a+b+c'+d)(a'+b+c'+d)]'$$

(i) 
$$f(a,b,c,a) = ((a+b+c+a)($$

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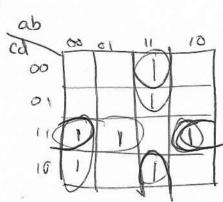
(a'c + ab + bc) (ac'+ad' + a'b' + b'c' + b'd' + a'd + c'd)

= (a'b'c + a'b'cd' + a'b'cd' + a'cd +

abc' + abd' + abe'd +

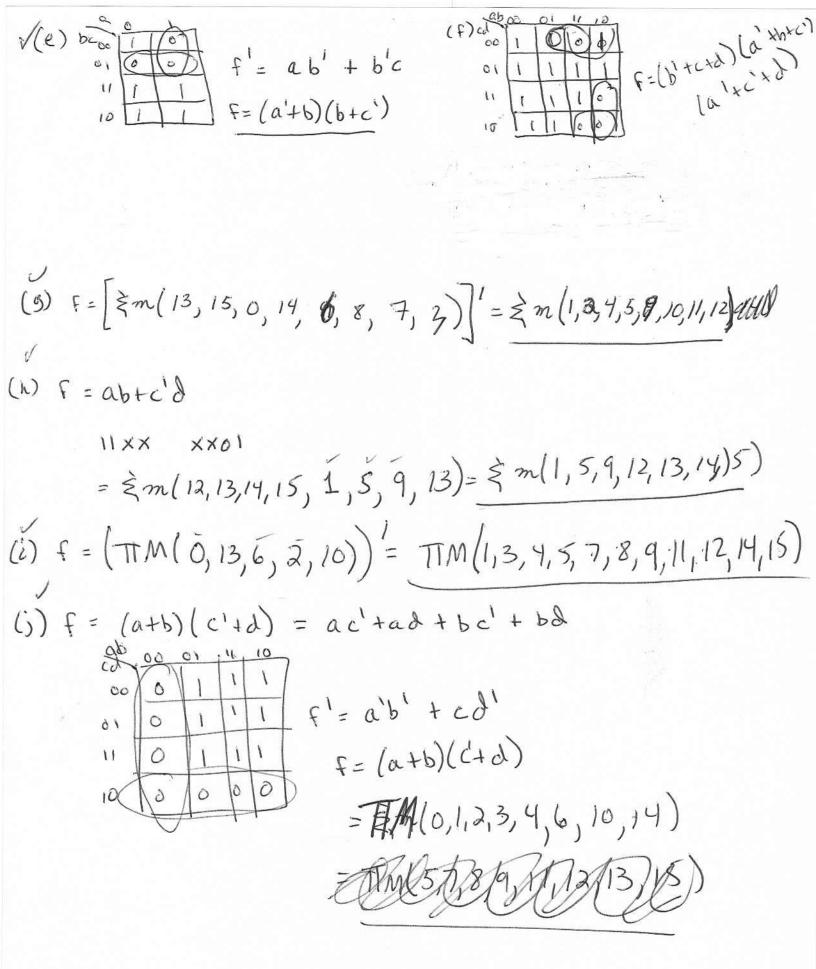
abcd' + a'bcd)

ab



= abc' + a'cd + a'b'c + abod' + abod' + abcd' + abcd' + abcd' + abcd' + abcd' + abcd' = ab + c'd + a'd = a'd + abc'd + abc'd' + abc'd + a'd

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## [15] 3. Work the following short problems

[3] (a) Draw a circuit diagram for f = a + bc' + b'cd using only NAND gates.



[3] (c) Given  $f(a,b,c) = \sum m(0,1,2,3,6,7)$ , find the minimum SOP form using the QM method.

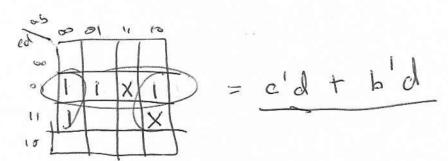
[3] (c) Given 
$$f(a,b,c) = \sum m(0,1,2,3,6,7)$$
, find the minimum SOP is

Lead I level II

Level II

 $0 000 \sqrt{(0,1)} 00 - (0,1,2,3) 0 - (0,1,2,3) 0 - (0,1,2,3) 0 - (0,1,2,3) 0 - (0,2,1,3) 0 - (0,2,2,2,1,3) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,2,2,2,2) 0 - (0,2,$ 

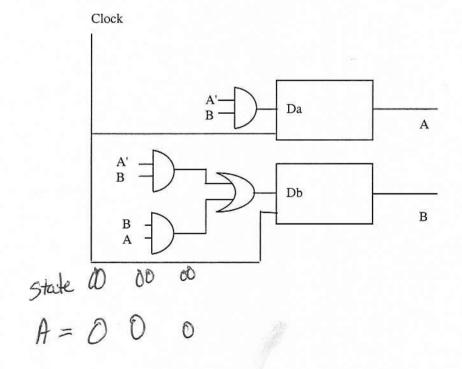
[3] (d) Find a minimum SOP for  $f(a,b,c,d) = \sum m(1,3,5,9) + \sum d(11,13)$ 



[3] (e) Draw  $f(a,b,c,d) = \sum m(1,5,6,10,13,14)$  using 3 OR gates and 2 AND gates by factoring. = a'c'd' + bc' + ac'd' + bc'd' + bc'd' + ac'd' + ac'

(Clock)

[3] (f) Given the input sequence X=011 and the initial state AB=00, write the output sequence Z for the circuit below.



[8] 4. Answer True of False [2 points each]. Write your answers next to the question; use the bottom of this page for your work.

T

(a) An 8-1 MUX can implement any function of 3 variables.

F

(b) abc + ab'c' + b'cd + bc'd + ad = abc + ab'c' + b'cd + bc'd

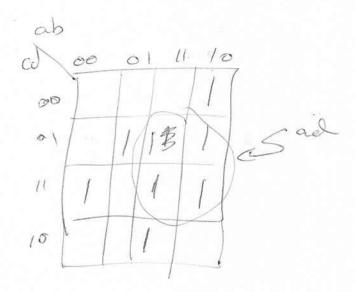
F

(c) (x+y)(y+z)(x+z) = (x'+y')(y'+z')(x'+z')

F

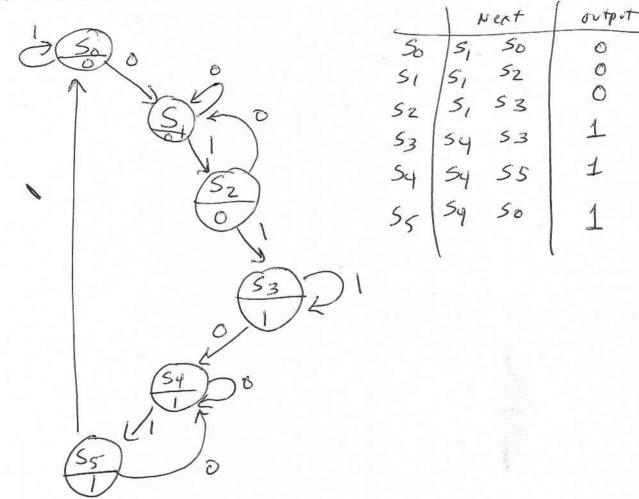
 $\sqrt{\text{d}}$  If  $f_1(a,b,c,d) = \sum m(1,3,5,7)$  and  $f_2(a,b,c) = \sum m(1,3,5,7)$  then  $f_1 = f_2$ 



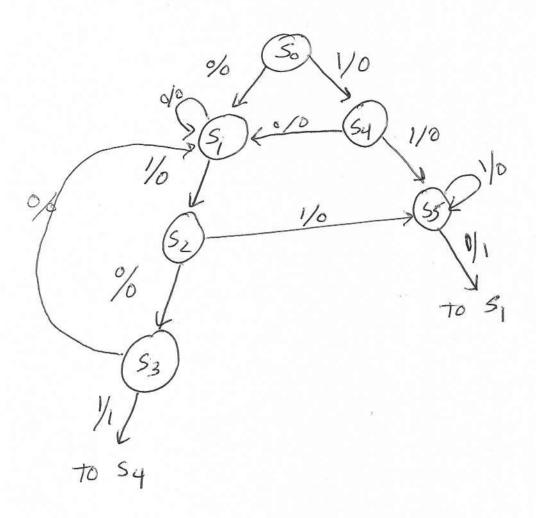


[15] 5. Design the following state machines. You need only draw a state graph and state table that meets the description.

[7] (a) Design a Moore machine that has one output bit (Z) and one input bit (X). When the input sequence 011 occurs, the output becomes 1 and remains 1 until 011 occurs again; at which time the output returns to 0. The output remains 0 until 011 is detected again, etc. You should be able to design this with 6 states.



[8] (b) Design a Mealy machine that detects the sequences 0101 and 110 simultaneously.

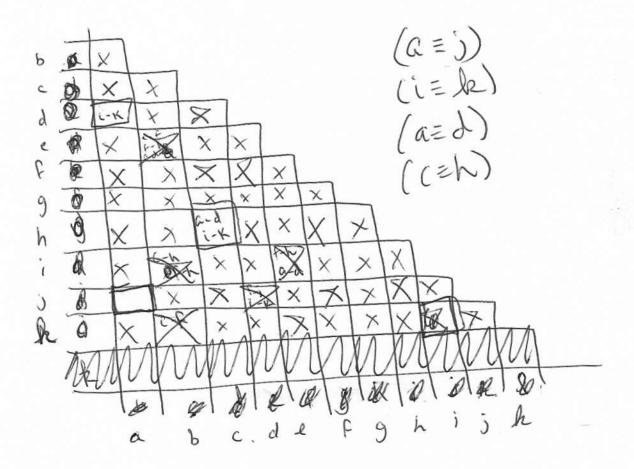


50 50 51 51 52 53 52 53 55 53 51 54	output	0.	tys		
		0	5 <sub>2</sub> 5 <sub>5</sub>	50 51 53	5 <sub>1</sub>
5 <sub>5</sub> 5 <sub>1</sub> 5 <sub>5</sub>		0	55	5, 5,	54

[19] 6. Given the state table

Present	Next State				Output			
State	X=00	X=01	X=10	X=11	X=00	X=01	X=10	X=11
a	a	a	g	*i	1	0	0	0
b	С	f	g	,eta	0	0	0	0
С	g	С	a	i	1	0	0	0
_d_	a_	<u>-d</u>	g	_i_	1	0	0	0
e	f	おこ	g	a	0.	0	0	0
f	eta	С	da	Κì	1	. 0	0	- 0
g	С	Ø.	g	e	0	1	0	0
h	g	h	da	Jr i	1	0	0	0
i	Jr.c.	drc	g	da	0-	0	0	0
_ <del>j</del>	j	-j-	g	k	1	-0-	0	0
k	c	-е-	g	d	0	_0_	-0-	-0-

[9] (a) Find the minimum number of states and write the minimal state table.



[6] (b) Find a 'good' assignment of flip-flop outputs to states and explain your work.

[4] (c) Draw the circuit resulting from this assignment.