

## 4-2 Negative Feedback

► **Feedback** refers to taking a part of the output signal and feeding it back into the input. It is called **positive feedback** if it increases the intensity of the input signal, and it is called **negative feedback** if it decreases it. In negative feedback, the output terminal is connected to the  $v_n$  terminal, either directly or through a resistor. ◀

Positive feedback causes the op amp to saturate, thereby forcing its output voltage  $v_o$  to become equal to its supply voltage  $V_{cc}$ . This behavior is used to advantage in certain types of applications but they are outside the scope of this book. Negative feedback, on the other hand, is an essential ingredient of all of the op-amp circuits covered in this and forthcoming chapters.

Why do some op-amp circuits need feedback and why negative feedback specifically? It seems counter-intuitive to want to decrease the input signal when the intent is to amplify it! We will answer this question by examining the circuit of Example 4-1 in some detail. To facilitate the discussion we have reproduced the circuit diagram (into a smaller version) and inserted it in **Fig. 4-8(a)**.

When we say an op amp has a supply voltage  $V_{cc}$  of 10 V, we actually mean that a positive (10 V) dc voltage source is connected to pin 7 of its package and another, negative (-10 V) source is connected to its pin 4 (**Fig. 4-2(b)**). The op-amp circuit cannot generate an output voltage  $v_o$  that exceeds its supply voltage. Hence,  $v_o$  is bounded to  $\pm V_{cc}$  which means

$$|v_o| \leq V_{cc},$$

or equivalently,

$$-V_{cc} \leq v_o \leq V_{cc}. \quad (4.11)$$

Thus, the **linear dynamic range** of  $v_o$  extends from  $-V_{cc}$  to  $+V_{cc}$ .

According to Example 4-1,  $v_o$  is related to the signal voltage  $v_s$  by

$$v_o = Gv_s, \quad (4.12)$$

with

$$G \approx \frac{R_1 + R_2}{R_2}. \quad (4.13)$$

Inserting Eq. (4.12) into Eq. (4.11) gives

$$|Gv_s| \leq V_{cc}, \quad (4.14)$$

or

$$\frac{-V_{cc}}{G} \leq v_s \leq \frac{V_{cc}}{G}, \quad (4.15)$$

which states that the linear dynamic range of  $v_s$  is inversely proportional to the circuit gain  $G$ .

**(a) Unity Gain:** If  $R_2 = \infty$  (open circuit between node  $b$  and ground in the circuit of **Fig. 4-8(a)**), Eq. (4.13) gives  $G \approx 1$ . The corresponding dynamic range of  $v_s$  extends from  $-V_{cc}$  to  $+V_{cc}$ , the same as the output. The input-output transfer plot relating  $v_o$  to  $v_s$  is displayed in green in **Fig. 4-8(b)**.

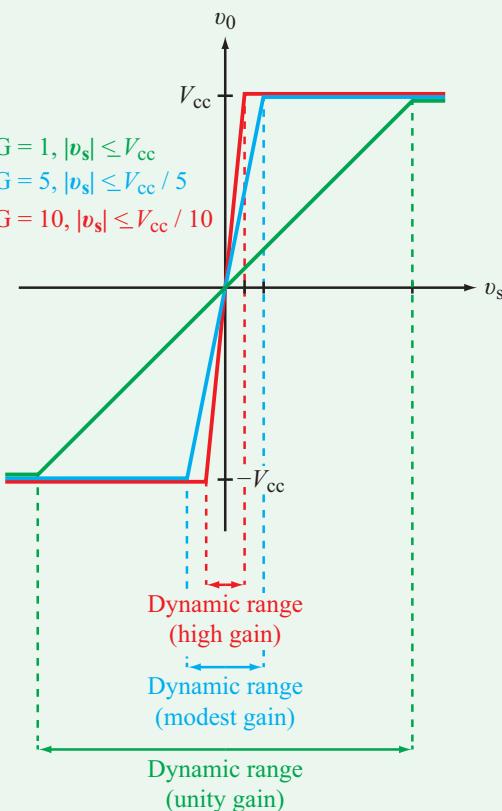
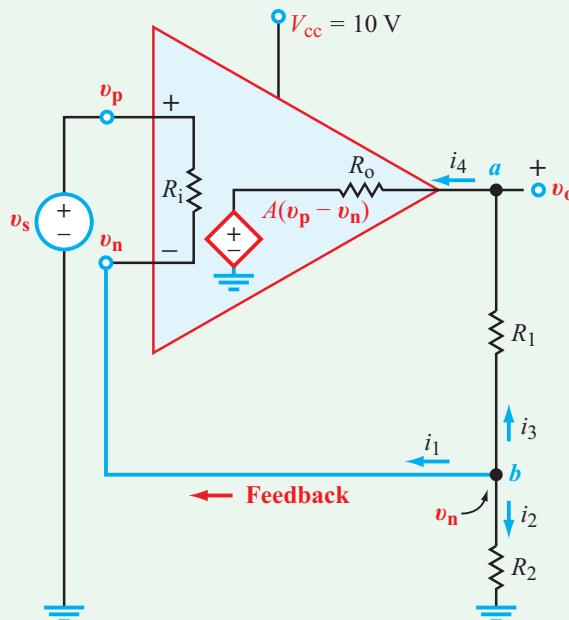
**(b) Modest Gain:** If we choose  $R_1/R_2 = 4$ , Eq. (4.13) gives  $G = 5$ , and the dynamic range of  $v_s$  now extends from  $-(10/5) = -2$  V to  $+2$  V. Thus, the gain is higher than the unity-gain case by a factor of 5, but the dynamic range of  $v_s$  is narrower by the same factor.

**(c) Maximum Gain:** If  $R_1$  is removed (replaced with an open circuit between nodes  $a$  and  $b$ ) and  $R_2$  is set equal to zero (short circuit), no feedback will take place in the circuit of **Fig. 4-8(a)**. Use of the exact expression for  $G$  given by Eq. (4.8) leads to  $G = A$ . Since  $A = 10^6$ , the absence of feedback provides a huge gain, but operationally  $v_s$  becomes limited to a very narrow range extending from  $-10 \mu\text{V}$  to  $+10 \mu\text{V}$ .

► Application of negative feedback offers a trade-off between circuit gain and dynamic range for the input voltage. ◀

**Concept Question 4-5:** Why is negative feedback used in op-amp circuits? (See **CAD**)

**Concept Question 4-6:** How large is the circuit gain  $G$  in the absence of feedback? How large is it with 100 percent feedback (equivalent to setting  $R_1 = 0$  in the circuit of **Fig. 4-8(a)**)? (See **CAD**)



**Figure 4-8:** Trade-off between gain and dynamic range.

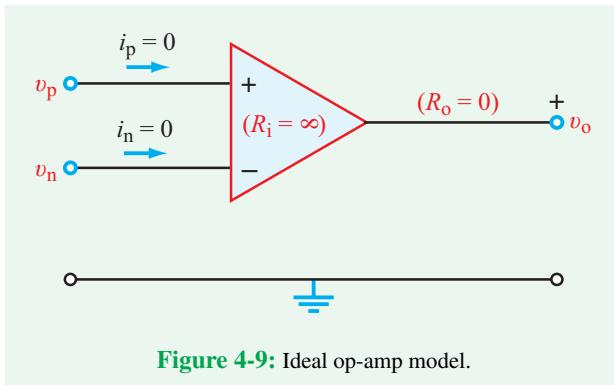
**Exercise 4-2:** To evaluate the trade-off between the circuit gain  $G$  and the linear dynamic range of  $v_s$ , apply Eq. (4.8) to find the magnitude of  $G$  and then determine the corresponding dynamic range of  $v_s$  for each of the following values of  $R_2$ : 0 (no feedback), 800  $\Omega$ , 8.8 k $\Omega$ , 40 k $\Omega$ , 80 k $\Omega$ , and 1 M $\Omega$ . Except for  $R_2$ , all other quantities remain unchanged.

Answer:	$R_2$	$G$	$v_s$ Range
	0	$10^6$	-10 $\mu$ V to +10 $\mu$ V
	800 $\Omega$	101	-99 mV to +99 mV
	8.8 k $\Omega$	10.1	-0.99 V to +0.99 V
	40 k $\Omega$	3	-3.3 V to +3.3 V
	80 k $\Omega$	2	-5 V to +5 V
	1 M $\Omega$	1.08	-9.26 V to +9.26 V

(See )

### 4-3 Ideal Op-Amp Model

We noted in Section 4-1 that the op amp has a very large input resistance  $R_i$  on the order of  $10^7 \Omega$ , a relatively small output resistance  $R_o$  on the order of 1–100  $\Omega$ , and an open-loop gain  $A \approx 10^6$ . Usually, the series resistances of the input circuit connected to terminals  $v_p$  and  $v_n$  are several orders of magnitude smaller than  $R_i$ . Consequently, not only will very little current flow through the input circuit, but also the voltage drop across the input-circuit resistors will be negligibly small in comparison with the voltage drop across  $R_i$ . These considerations allow us to simplify the equivalent circuit of the op amp by replacing it with the ideal op-amp circuit model shown in Fig. 4-9, in which  $R_i$  has been replaced with an open circuit between terminals  $v_p$  and  $v_n$  implies



the following **ideal op-amp current constraint**:

$$i_p = i_n = 0 \quad (\text{ideal op-amp model}). \quad (4.16)$$

In reality,  $i_p$  and  $i_n$  are very small but not identically zero; for if they were, there would be no amplification through the op amp. Nevertheless, the current condition given by Eq. (4.16) will prove quite useful.

Similarly, at the output side, *if the load resistor connected in series with  $R_o$  is several orders of magnitude larger than  $R_o$ , then  $R_o$  can be ignored by setting it equal to zero*. Finally, in the ideal op-amp model, the large open-loop gain  $A$  is made infinite—the consequence of which is that

$$v_p - v_n = \frac{v_o}{A} \rightarrow 0 \quad \text{as } A \rightarrow \infty.$$

Hence, we obtain the **ideal op-amp voltage constraint**

$$v_p = v_n \quad (\text{ideal op-amp model}). \quad (4.17)$$

In reality  $v_p$  and  $v_n$  are not exactly equal, but very close to being equal, and only when negative feedback is in use. Nevertheless, setting  $v_p = v_n$  leads to highly accurate results when relating the output to the input. In summary:

- The ideal op-amp model characterizes the op amp in terms of an equivalent circuit in which  $R_i = \infty$ ,  $R_o = 0$ , and  $A = \infty$ . ◀

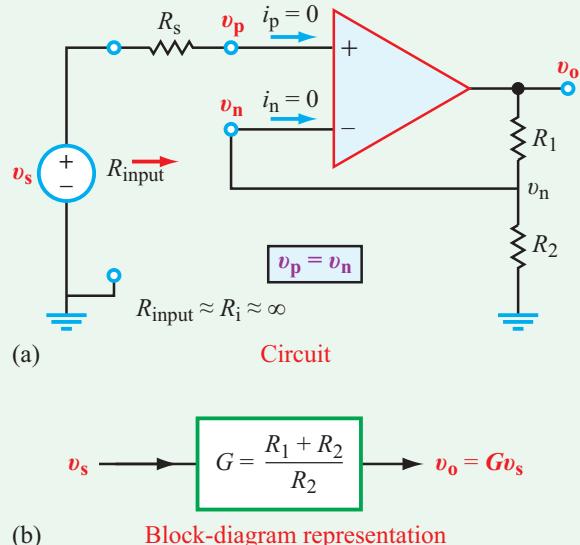
The operative consequences are given by Eqs. (4.16) and (4.17) and in **Table 4-2**.

**Table 4-2: Characteristics of the ideal op-amp model.**

### Ideal Op Amp

- Current constraint  $i_p = i_n = 0$
- Voltage constraint  $v_p = v_n$
- $A = \infty \quad R_i = \infty \quad R_o = 0$

### Noninverting Amplifier



**Figure 4-10:** Noninverting amplifier circuit: (a) using ideal op-amp model and (b) equivalent block-diagram representation.

To illustrate the utility of the ideal op-amp model, let us re-examine the circuit we analyzed earlier in Example 4-1, but we will do so this time using the ideal model. The new circuit, as shown in **Fig. 4-10**, includes a source resistance  $R_s$ , but because the op amp draws no current ( $i_p = 0$ ), there is no voltage drop across  $R_s$ . Hence,

$$v_p = v_s, \quad (4.18)$$

and on the output side,  $v_o$  and  $v_n$  are related through voltage division by

$$v_o = \left( \frac{R_1 + R_2}{R_2} \right) v_n. \quad (4.19)$$

Using these two equations, in conjunction with  $v_p = v_n$  (from Eq. (4.17)), we end up with the following result for the circuit

gain  $G$ :

$$G = \frac{v_o}{v_s} = \left( \frac{R_1 + R_2}{R_2} \right), \quad (4.20)$$

which is identical to Eq. (4.10).

► The **input resistance** of the noninverting amplifier circuit shown in Fig. 4-10 is the Thévenin resistance of the op-amp circuit as seen by the input source  $v_s$ . Because  $i_p = 0$ , it is easy to show that  $R_{\text{input}} = R_i \approx \infty$ , where  $R_i$  is the input resistance of the op amp (typically on the order of  $10^9 \Omega$ ). ◀

► From here on forward, we use the ideal op-amp model exclusively. ◀

**Concept Question 4-7:** What are the current and voltage constraints of the ideal op amp? (See CAD)

**Concept Question 4-8:** What are the values of the input and output resistances of the ideal op amp? (See CAD)

**Concept Question 4-9:** In the ideal op-amp model,  $R_o$  is set equal to zero. To satisfy such an approximation, does the load resistance need to be much larger or much smaller than  $R_o$ ? Explain. (See CAD)

**Exercise 4-3:** Consider the noninverting amplifier circuit of Fig. 4-10(a) under the conditions of the ideal op-amp model. Assume  $V_{cc} = 10$  V. Determine the value of  $G$  and the corresponding dynamic range of  $v_s$  for each of the following values of  $R_1/R_2$ : 0, 1, 9, 99,  $10^3$ ,  $10^6$ .

**Answer:**

$R_1/R_2$	$G$	$v_s$ Range
0	1	-10 V to +10 V
1	2	-5 V to +5 V
9	10	-1 V to +1 V
99	100	-0.1 V to +0.1 V
$10^3$	$\sim 1000$	-10 mV to +10 mV (approx.)
$10^6$	$\sim 10^6$	-10 $\mu$ V to +10 $\mu$ V (approx.)

(See CAD)

## 4-4 Inverting Amplifier

► In an **inverting amplifier** op-amp circuit, the input source is connected to terminal  $v_n$  (instead of to terminal  $v_p$ ) through an **input source resistance**  $R_s$ , and terminal  $v_p$  is connected to ground. ◀

Feedback from the output continues to be applied at  $v_n$  (through a **feedback resistance**  $R_f$ ), as shown in Fig. 4-11. It is called an **inverting amplifier** because (as we will see shortly) the circuit gain  $G$  is negative.

To relate the output voltage  $v_o$  to the input signal voltage  $v_s$ , we start by writing down the node-voltage equation at terminal  $v_n$  as

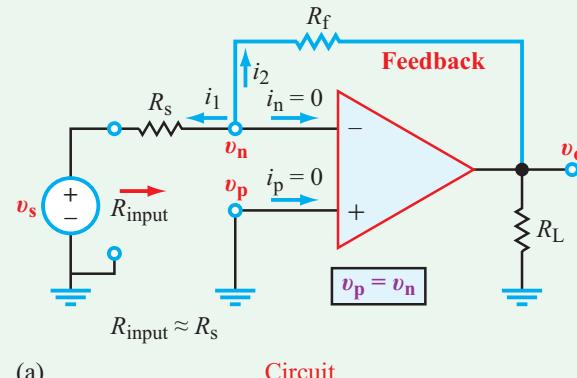
$$i_1 + i_2 + i_n = 0 \quad (4.21)$$

or

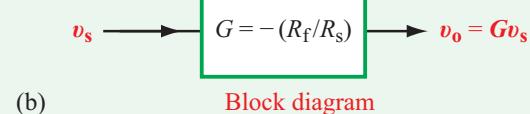
$$\frac{v_n - v_s}{R_s} + \frac{v_n - v_o}{R_f} + i_n = 0. \quad (4.22)$$

Upon invoking the op-amp current constraint given by Eq. (4.16), namely  $i_n = 0$ , and the voltage constraint  $v_n = v_p$ ,

### Inverting Amplifier



(a) Circuit



**Figure 4-11:** Inverting amplifier circuit and its block-diagram equivalent.

as well as recognizing that  $v_p = 0$  (because terminal  $v_p$  is connected to ground), we obtain the relationship

$$v_o = -\left(\frac{R_f}{R_s}\right)v_s. \quad (4.23)$$

The circuit voltage gain of the inverting amplifier therefore is given by

$$G = \frac{v_o}{v_s} = -\left(\frac{R_f}{R_s}\right). \quad (4.24)$$

► In addition to amplifying  $v_s$  by the ratio  $(R_f/R_s)$ , the inverting amplifier also reverses the polarity of  $v_s$ . ◀

►  $v_o$  is independent of the magnitude of the load resistance  $R_L$ , so long as  $R_L$  is much larger than the op-amp output resistance  $R_o$  (which is an implicit assumption of the ideal op-amp model). ◀

Because  $v_n = 0$ , a Thévenin analysis of the circuit in Fig. 4-11(a) would reveal that the **input resistance** of the inverting amplifier circuit (as seen by source  $v_s$ ) is  $R_{\text{input}} = R_{\text{Th}} = R_s$ .

► **Caution:** Under the ideal op-amp model, it is not possible to compute  $i_o$ , the current that flows into the op amp from output terminal  $v_o$ . Hence, it is inappropriate to apply KCL at that terminal because additional current can be delivered by the supply voltage sources  $V_{cc}$  and  $-V_{cc}$ . ◀

#### Example 4-2: Amplifier with Input Current Source

For the circuit shown in Fig. 4-12(a): (a) obtain an expression for the input-output transfer function  $K_t = v_o/i_s$  and evaluate it for  $R_1 = 1 \text{ k}\Omega$ ,  $R_2 = 2 \text{ k}\Omega$ ,  $R_f = 30 \text{ k}\Omega$ , and  $R_L = 10 \text{ k}\Omega$ ; and (b) determine the linear dynamic range of  $i_s$  if  $V_{cc} = 20 \text{ V}$ .

**Solution:** (a) Application of the source transformation method converts the combination of  $i_s$  and  $R_2$  into a voltage source  $v_s = i_s R_2$ , in series with a resistance  $R_2$ . Upon combining  $R_2$  in series with  $R_1$ , we obtain the new circuit shown in Fig. 4-12(b), which is identical in form to the inverting amplifier circuit of Fig. 4-11, except that now the source

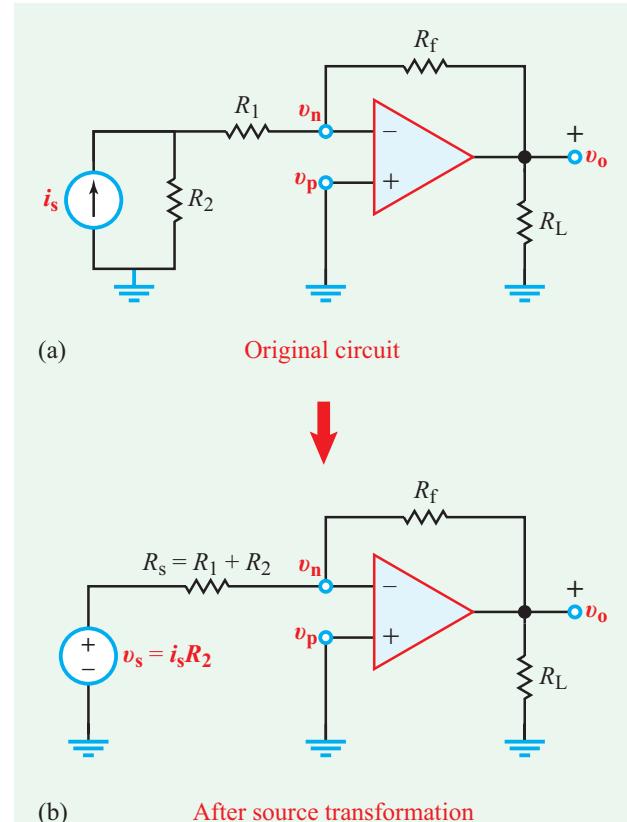


Figure 4-12: Inverting amplifier circuit of Example 4-2.

resistance is  $R_s = (R_1 + R_2)$ . Hence, application of Eq. (4.23) gives

$$v_o = -\left(\frac{R_f}{R_1 + R_2}\right)v_s = -\left(\frac{R_f}{R_1 + R_2}\right)R_2 i_s, \quad (4.25)$$

from which we obtain the transfer function

$$K_t = \frac{v_o}{i_s} = -\frac{R_f R_2}{R_1 + R_2}. \quad (4.26)$$

For  $R_1 = 1 \text{ k}\Omega$ ,  $R_2 = 2 \text{ k}\Omega$ , and  $R_f = 30 \text{ k}\Omega$ ,

$$K_t = \frac{v_o}{i_s} = -2 \times 10^4 \quad (\text{V/A}).$$

(b) From the expression for  $K_t$ ,

$$i_s = -\frac{v_o}{2 \times 10^4},$$

and since  $|v_o|$  is bounded by  $V_{cc} = 20$  V, the linear range for  $i_s$  is bounded by

$$|i_s| = \left| \frac{V_{cc}}{2 \times 10^4} \right| = \left| \frac{20}{2 \times 10^4} \right| = 1 \text{ mA.}$$

Thus, the linear range of  $i_s$  extends from  $-1$  mA to  $+1$  mA.

**Concept Question 4-10:** How does feedback control the gain of the inverting-amplifier circuit? (See CAD)

**Concept Question 4-11:** The expression given by Eq. (4.24) states that the gain of the inverting amplifier is independent of the magnitude of  $R_L$ . Would the expression remain valid if  $R_L = 0$ ? Explain. (See CAD)

**Exercise 4-4:** The input to an inverting-amplifier circuit consists of  $v_s = 0.2$  V and  $R_s = 10 \Omega$ . If  $V_{cc} = 12$  V, what is the maximum value that  $R_f$  can assume before saturating the op amp?

**Answer:**  $G_{\max} = -60$ ,  $R_f = 600 \Omega$ . (See CAD)

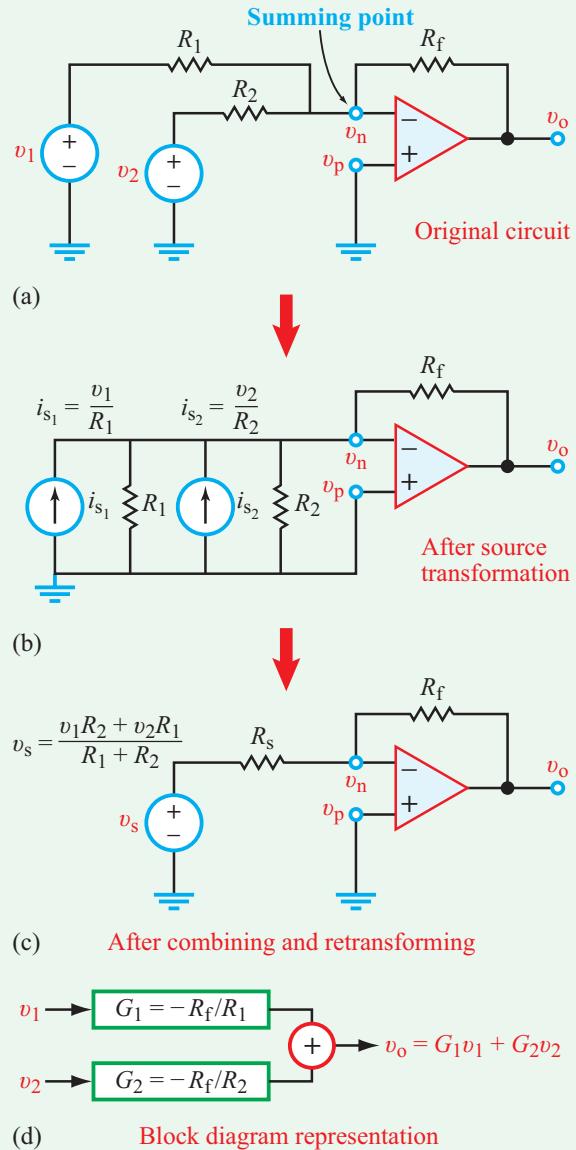
## 4-5 Inverting Summing Amplifier

By connecting multiple sources in parallel at terminal  $v_n$  of the inverting amplifier, the circuit becomes an **adder** (or more precisely a **scaled inverting adder**), as depicted by the block diagram of Fig. 4-13(d). After we demonstrate how such a circuit (usually called an **inverting summing amplifier**) works for two input voltages  $v_1$  and  $v_2$ , we will extend it to multiple sources. There are many applications where we may want to scale and add multiple voltages together, such as combining or averaging results from several sensors.

For the circuit shown in Fig. 4-13(a), our goal is to relate the output voltage  $v_o$  to  $v_1$  and  $v_2$ . To do so, we apply the source-transformation technique so as to cast the input circuit in the form of a single voltage source  $v_s$  in series with a source resistance  $R_s$ . The steps involved in the transformation are illustrated in Fig. 4-13(b) and (c). Voltage to current transformation gives  $i_{s1} = v_1/R_1$  and  $i_{s2} = v_2/R_2$ , which can be combined together into a single current source as

$$i_s = i_{s1} + i_{s2} = \frac{v_1}{R_1} + \frac{v_2}{R_2} = \frac{v_1 R_2 + v_2 R_1}{R_1 R_2}. \quad (4.27)$$

### Inverting Summing Amplifier



**Figure 4-13:** Inverting summing amplifier.

Similarly, the two parallel resistors add up to

$$R_s = \frac{R_1 R_2}{R_1 + R_2}. \quad (4.28)$$

If we transform  $(i_s, R_s)$  into a voltage source  $(v_s, R_s)$ , we get

$$v_s = i_s R_s = \left( \frac{v_1 R_2 + v_2 R_1}{R_1 R_2} \right) \frac{R_1 R_2}{R_1 + R_2} = \frac{v_1 R_2 + v_2 R_1}{R_1 + R_2}. \quad (4.29)$$

The circuit in **Fig. 4-13(c)** is identical in form to that of the inverting amplifier of **Fig. 4-11**. Hence, by applying the input-output voltage relationship given by Eq. (4.23), we have

$$\begin{aligned} v_o &= -\left(\frac{R_f}{R_s}\right)v_s = -\frac{R_f}{\left(\frac{R_1 R_2}{R_1 + R_2}\right)} \left(\frac{v_1 R_2 + v_2 R_1}{R_1 + R_2}\right) \\ &= -\left(\frac{R_f}{R_1}\right)v_1 - \left(\frac{R_f}{R_2}\right)v_2. \end{aligned} \quad (4.30)$$

This expression for  $v_o$  can be written in the form

$$v_o = G_1 v_1 + G_2 v_2, \quad (4.31)$$

where  $G_1 = -(R_f/R_1)$  is the (negative) gain applied to source voltage  $v_1$ , and  $G_2 = -(R_f/R_2)$  is the gain applied to  $v_2$ . Thus:

- The summing amplifier scales  $v_1$  by negative gain  $G_1$  and  $v_2$  by negative gain  $G_2$  and adds them together. ◀

### 4-5.1 Special Cases

For the special case where  $R_1 = R_2 = R$ ,

$$v_o = -\left(\frac{R_f}{R}\right)(v_1 + v_2) \quad \left( \begin{array}{l} \text{equal gain} \\ R_1 = R_2 = R \end{array} \right), \quad (4.32)$$

and if additionally  $R_f = R_1 = R_2$ , then  $G_1 = G_2 = -1$ . In this case, the summing amplifier becomes an inverted adder with

$$v_o = -(v_1 + v_2) \quad \left( \begin{array}{l} \text{inverted adder} \\ R_1 = R_2 = R_f \end{array} \right). \quad (4.33)$$

Generalizing to the case where the input consists of  $n$  input voltage sources  $v_1$  to  $v_n$  (and associated source resistances  $R_1$  to  $R_n$ , respectively), all connected in parallel at the same summing point (terminal  $v_n$ ), the output voltage becomes

$$v_o = \left(-\frac{R_f}{R_1}\right)v_1 + \left(-\frac{R_f}{R_2}\right)v_2 + \cdots + \left(-\frac{R_f}{R_n}\right)v_n. \quad (4.34)$$

### Example 4-3: Summing Circuit

Use inverting amplifiers to design a circuit that performs the operation

$$v_o = 4v_1 + 7v_2.$$

**Solution:** The desired circuit has to amplify  $v_1$  by a factor of 4, amplify  $v_2$  by a factor of 7, and add the two together. A summing amplifier can do that, but it also inverts the sum. Hence, we will need to use a two-stage cascaded circuit with the first stage providing the desired operation within a “-” sign and then follow it up with an inverting amplifier with a gain of  $(-1)$ . The two-stage circuit is shown in **Fig. 4-14**.

For the first stage, we need to select values for  $R_1$ ,  $R_2$ , and  $R_{f1}$  such that

$$\frac{R_{f1}}{R_1} = 4 \quad \text{and} \quad \frac{R_{f1}}{R_2} = 7.$$

Since we have only two constraints, we can satisfy the specified ratios with an infinite number of combinations. Arbitrarily, we choose  $R_{f1} = 56 \text{ k}\Omega$ , which then specifies the other resistors as

$$R_1 = 14 \text{ k}\Omega \quad \text{and} \quad R_2 = 8 \text{ k}\Omega.$$

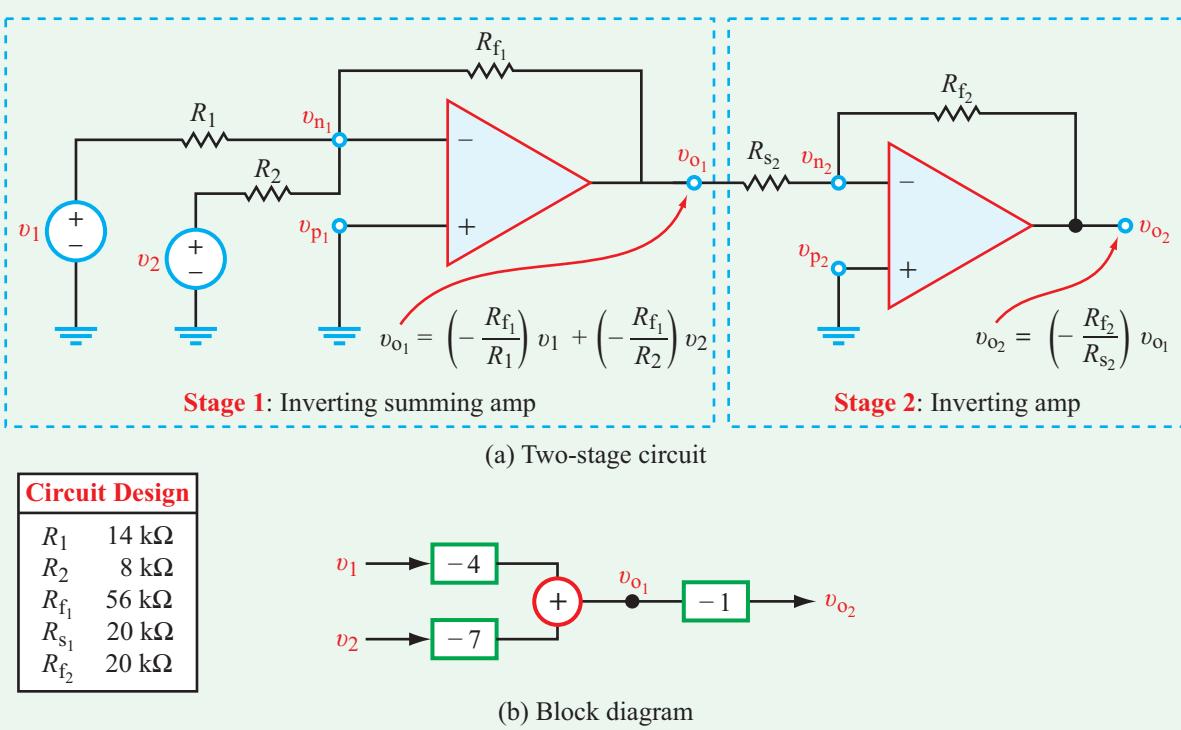
For the second stage, a gain of  $(-1)$  requires that

$$\frac{R_{f2}}{R_{s2}} = 1.$$

Arbitrarily, we choose  $R_{f2} = R_{s2} = 20 \text{ k}\Omega$ .

### 4-5.2 Noninverting Summer

To perform the summing operation, the solution offered in Example 4-3 employed two inverting amplifier circuits—one



**Figure 4-14:** Two-stage circuit realization of  $v_o = 4v_1 + 7v_2$ .

to perform an inverted sum, and a second one to provide multiplication by  $(-1)$ . Alternatively, the same result can be achieved by using a single op amp in a noninverting amplifier circuit, as shown in **Fig. 4-15**.

From our analysis in Section 4-3, we established that the output voltage  $v_o$  of the noninverting amplifier circuit is related to  $v_p$  by

$$\frac{v_o}{v_p} = G = \frac{R_1 + R_2}{R_2}. \quad (4.35)$$

For the circuit in **Fig. 4-15**, in view of the ideal op-amp constraint that the op amp draws no current ( $i_p = 0$ ), it is a straightforward task to show that

$$v_p = \frac{v_1 R_{s_2} + v_2 R_{s_1}}{R_{s_1} + R_{s_2}}. \quad (4.36)$$

Combining Eqs. (4.35) and (4.36) leads to

$$v_o = G \left[ \left( \frac{R_{s_2}}{R_{s_1} + R_{s_2}} \right) v_1 + \left( \frac{R_{s_1}}{R_{s_1} + R_{s_2}} \right) v_2 \right]. \quad (4.37)$$

To realize a coefficient of 4 for  $v_1$  and a coefficient of 7 for  $v_2$ , it is necessary that

$$\frac{GR_{s_2}}{R_{s_1} + R_{s_2}} = 4$$

and

$$\frac{GR_{s_1}}{R_{s_1} + R_{s_2}} = 7.$$

A possible solution that satisfies these two constraints is  $R_{s_1} = 7\text{k}\Omega$ ,  $R_{s_2} = 4\text{k}\Omega$ , and  $G = 11$ . Furthermore, the specified value of  $G$  can be satisfied by choosing  $R_1 = 50\text{k}\Omega$  and  $R_2 = 5\text{k}\Omega$ .

#### 4-5.3 Multiple Ways of Building a System

There are often several different choices for how to implement a linear equation such as  $v_o = 4v_1 + 7v_2$  (Example 4-3) with op-amp circuits. Here are a few options:

- (a)  $v_o = (4v_1) + (7v_2)$ : Multiply  $v_1$  by 4 (noninverting amplifier with a gain of 4) and  $v_2$  by 7 (noninverting amplifier with a gain of 7), and then add them together (noninverting summer with a gain of 1).

## Technology Brief 10

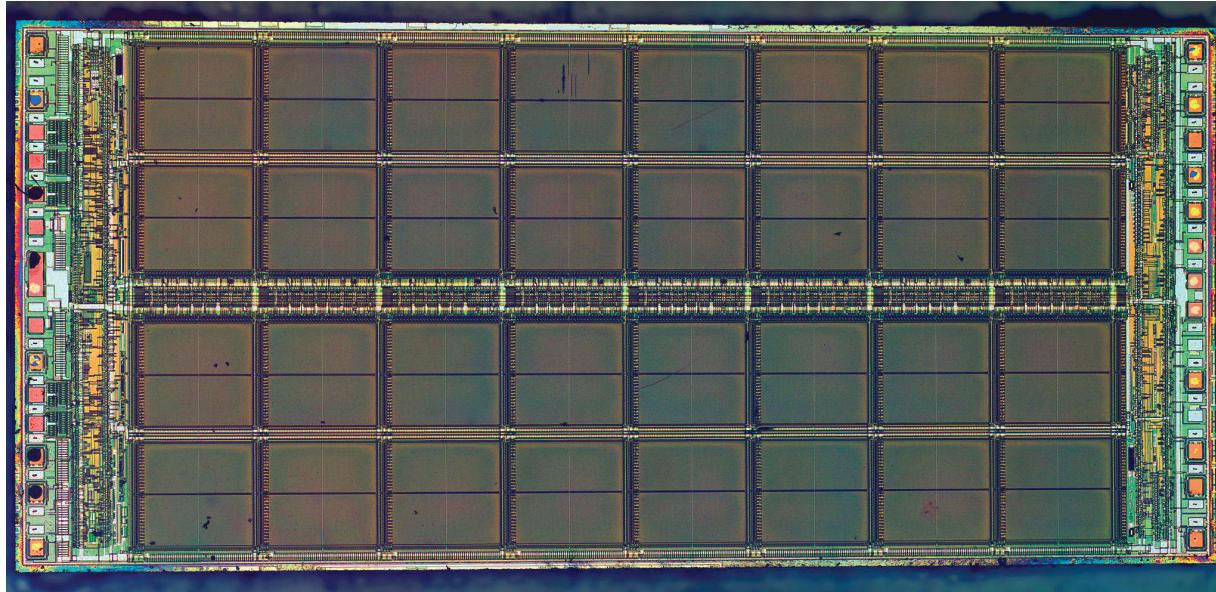
### Computer Memory Circuits

The storage of information in electronically addressable devices is one of the hallmarks of all modern computer systems. Among these devices are a class of storage media, collectively called **solid-state** or **semiconductor memories**, which store information by changing the state of an electronic circuit. The state of the circuit usually has two possibilities (0 or 1) and is termed a **bit** (see Technology Brief 8). Values in memories are represented by a string of **binary** bits; a 5-bit sequence  $[V_1 V_2 V_3 V_4 V_5]$ , for example, can be used to represent any integer decimal value between 0 and 31. How do computers store these bits? Many types of technologies have emerged over the last 40 years, so in this Brief, we will highlight some of the principal technologies in use today or under development. It is worth noting that memory devices usually store these values in arrays. For example, a small memory might store sixteen different 16-bit numbers; this memory usually would be referred to as a  $16 \times 16$  block or a 256-bit memory. Of course, modern multi-gigabyte computer memories use thousands of much larger blocks to store very large numbers of bits (Fig. TF10-1).

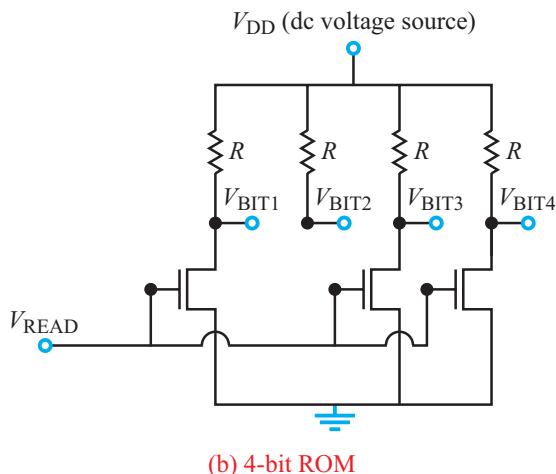
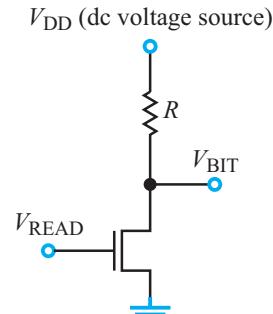
### Read-Only Memories (ROMs)

One of the oldest, still-employed, memory architectures is the **read-only memory** (ROM). The ROM is so termed because it can only be “written” once, and after that it can only be read. ROMs usually are used to store information that will not need to be changed (such as certain startup information on your computer or a short bit of code always used by an integrated circuit in your camera). Each bit in the ROM is held by a single MOSFET transistor.

Consider the circuit in Fig. TF10-2(a), which operates much like the circuit in Fig. 4-25. The MOSFET has three voltages, all referenced to ground. For convenience, the input voltage is labeled  $V_{\text{READ}}$  and the output voltage is labeled  $V_{\text{BIT}}$ . The third voltage,  $V_{\text{DD}}$ , is the voltage of the dc power supply connected to the drain terminal via a resistor  $R$ . If  $V_{\text{READ}} \ll V_{\text{DD}}$ , then the output registers a voltage  $V_{\text{BIT}} = V_{\text{DD}}$  denoting the binary state “1,” but if  $V_{\text{READ}} \geq V_{\text{DD}}$ , then the output terminal shorts to ground, generating  $V_{\text{BIT}} = 0$  denoting the binary state “0.” But how does this translate into a permanent memory on a chip? Let us examine the 4-bit ROM diagrammed in Fig. TF10-2(b). In this case, some bits simply do not have transistors;  $V_{\text{BIT}2}$ , for example, is permanently connected to  $V_{\text{DD}}$  via a resistor. This may seem trivial,



**Figure TF10-1:** Integrated circuit die photo of a Micron MT4C1024  $2^{20}$ -bit DRAM chip. Die size is 8.662 mm  $\times$  3.969 mm. (Courtesy of ZeptoBars.)



**Figure TF10-2:** (a) 1-bit ROM that uses a MOSFET transistor, and (b) 4-bit ROM configured to store the sequence [0100], whose decimal value is 4.

but this specific 4-bit memory configuration always stores the value [0100]. In this same way, thousands of such components can be strung together in rows and columns in  $N \times N$  arrays. As long as a power supply of voltage  $V_{DD}$  is connected to the circuit, the memory will report its contents to an external circuit as [0100]. Importantly, even if you remove power altogether, the values are not lost; as soon as you add power back to the chip, the same values appear again (i.e., you would have to break the chip to make it forget what it is storing!). Because of the permanency of this data, these memories also often are called **nonvolatile memories** (NVM).

### Random-Access Memories (RAMs)

RAMs are a class of memories that can be read to and written from constantly. RAMs generally fall into two

categories: **static RAMs** and **dynamic RAMs** (DRAMs). Because RAMs lose the state of their bits if the power is removed, they are termed **volatile memories**. Static RAMs not only can be read from and written to, but also do not forget their state as long as power is supplied. These circuits also are composed of transistors, but each single bit in a modern static RAM consists of four transistors wired up in a bi-stable circuit (the explanation of which we will leave to your intermediate digital components classes!). Dynamic RAMs, on the other hand, are illustrated more easily. Dynamic RAMs usually hold more bits per area than static RAMs, but they need to be refreshed constantly (even when power is supplied continuously to the chip).

**Figure TF10-3** shows a simple one-transistor dynamic RAM. Again, we will treat the transistor as we did in

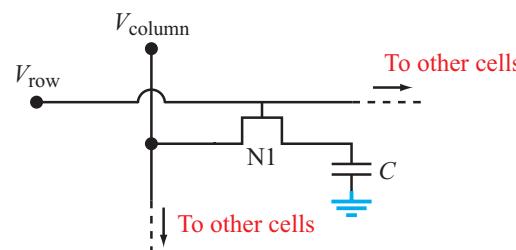


Figure TF10-3: 1-bit DRAM cell.

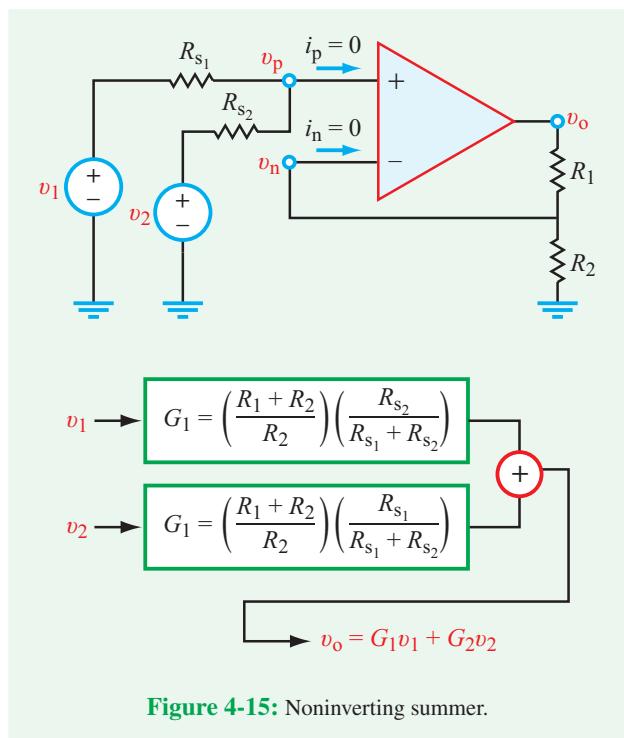
Section 4-11. Note that if we make  $V_{\text{ROW}} > V_{\text{DD}}$ , then the transistor will conduct and the capacitor  $C$  will start charging to whatever value we select for  $V_{\text{COLUMN}}$ . When writing a bit,  $V_{\text{COLUMN}}$  usually is set at either 0 (GND) or 1 ( $V_{\text{DD}}$ ). We can calculate how long this charging-up process will require, because we know the value of  $C$  and the transistor's current gain  $g$  (see Section 5-7). When the capacitor is charged to  $V_{\text{DD}}$ , a value of 1 is stored in the DRAM. Had we applied instead a value of zero volts to  $V_{\text{COLUMN}}$ , the transistor would have discharged to ground (instead of charged to  $V_{\text{DD}}$ ) and the bit would have a value of 0. However, note that unlike the ROM, the state of the bit is not “hardwired.” That is, if even tiny leakage currents were to flow through the transistor when it is not on (that is, when  $V_{\text{ROW}} < V_{\text{DD}}$ ), then charge will constantly leak away and the voltage of the transistor will drop slowly with time. After a short time (on the order of a few milliseconds in the dynamic RAM in your computer), the capacitor will have irrecoverably lost its value. How is that mitigated? Well, it turns out that a modern memory will read and then re-write every one of its (several billion) bits every 64 milliseconds to keep them refreshed! Because each bit is so simple (one transistor and one capacitor), it is possible to manufacture DRAMs with very high memory densities (which is why 1-Gbit DRAMs are now available in packages of reasonable size). Other variations of DRAMs also exist whose architectures deviate slightly from the previous model—at either the transistor or system level. **Synchronous Graphics RAM** (SGRAM), for example, is a DRAM modified for use with graphics adaptors; **Double Data Rate 4 RAM** (DDR4RAM) is a fourth-generation enhancement over DRAM which allows for faster clock speeds and lower operating voltages.

## Advanced Memories

Several substantially different technologies are emerging that likely will change the market landscape—just as Flash memories revolutionized portable memory (like your USB memory stick). Apart from the drive to increase storage density and access speed, one of the principal drivers in today’s memory research is the development of non-volatile memories that do not degrade over time (unlike Flash).

The **Ferroelectric RAM** (FeRAM) is the first of these technologies to enter mainstream production; FeRAM replaces the capacitor in DRAM (Fig. TF10-3) with a ferroelectric capacitor that can hold the binary state even with power removed. While FeRAM can be faster than Flash memories, FeRAM densities are still much smaller than modern Flash (and Flash densities continue to increase rapidly). FeRAM currently is used in niche applications where the increased speed is important.

**Magnetoresistive RAM** (MRAM) is another emerging technology, currently commercialized by Everspin Technologies (spun out from Freescale Semiconductor), which relies on magnetic plates to store bits of data. In MRAM, each cell is composed of two ferromagnetic plates separated by an insulator. The storage and retrieval of bits occurs by manipulation of the magnetic polarization of the plates with associated circuits. Like FeRAM, MRAM currently is overshadowed by Flash memories, but improvements in density, speed, and fabrication methods may make it a viable alternative in the mainstream consumer market in the future. Even more speculative is the idea of using single carbon nanotubes to store binary bits by changing their configuration electronically; this technology is currently known as **Nano RAM** (NRAM).

**Figure 4-15:** Noninverting summer.

- (b)  $v_o = (-4v_1 - 7v_2)(-1)$ : Multiply  $v_1$  by  $-4$  and  $v_2$  by  $-7$  and add them together (inverting summing amplifier with gains of  $-4$  and  $-7$ ), and then multiply the result by  $-1$  (inverting amplifier with a gain of  $-1$ ).
- (c)  $v_o = (4v_1 + 7v_2)$ : Multiply  $v_1$  by  $4$  and  $v_2$  by  $7$  and add them together (noninverting summing amplifier with gains of  $4$  and  $7$ ).
- (d)  $v_o = [(2v_1) + (3.5v_2)] \times 2$ : Multiply  $v_1$  by  $2$  (noninverting amplifier with a gain of  $2$ ) and  $v_2$  by  $3.5$  (noninverting amplifier with a gain of  $3.5$ ), and then add them (noninverting summer with a gain of  $2$ ).

Why might you choose one of these systems over another? There are several reasons:

- To minimize the number of op amps (option c)
- To meet gain limitations. An inverting amplifier can have a gain of less than  $1$ , but a noninverting amplifier cannot.
- To avoid saturation. The output voltage of any individual stage is limited by its  $V_{cc}$ . The order in which multiplica-

tion/summation is done must keep each individual stage from exceeding  $+/- V_{cc}$ .

- Sensitivity when adding large and small values. Care is typically taken to add values that are similar in magnitude, so amplification is typically done prior to summation if two values have significantly different magnitudes.
- Other considerations ...

**Concept Question 4-12:** What type of op-amp circuits (inverting, noninverting, and others) might one use to perform the operation  $v_o = G_1v_1 + G_2v_2$  with  $G_1$  and  $G_2$  both positive? (See [CAD](#))

**Concept Question 4-13:** What is an inverting adder? (See [CAD](#))

**Exercise 4-5:** The circuit shown in [Fig. 4-14\(a\)](#) is to be used to perform the operation

$$v_o = 3v_1 + 6v_2.$$

If  $R_1 = 1.2 \text{ k}\Omega$ ,  $R_{s_2} = 2 \text{ k}\Omega$ , and  $R_{f_2} = 4 \text{ k}\Omega$ , select values for  $R_2$  and  $R_{f_1}$  so as to realize the desired result.

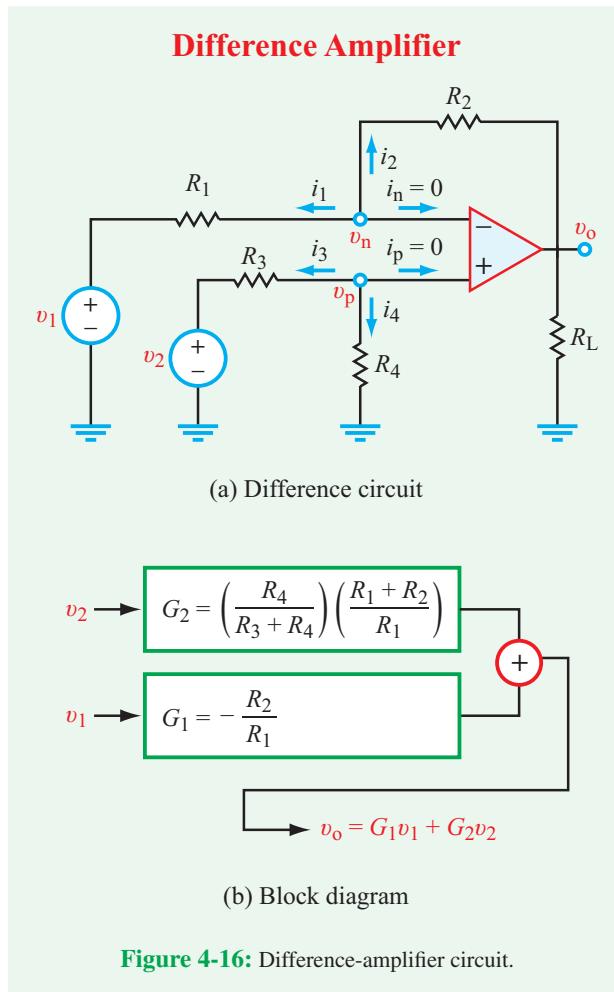
**Answer:**  $R_{f_1} = 1.8 \text{ k}\Omega$ ,  $R_2 = 600 \Omega$ . (See [CAD](#))

## 4-6 Difference Amplifier

When an input signal  $v_2$  is connected to terminal  $v_p$  of a noninverting amplifier circuit, the output is a scaled version of  $v_2$ . A similar outcome is generated by an inverting amplifier circuit when an input voltage  $v_1$  is connected to the op amp's  $v_n$  terminal, except that in addition to scaling  $v_1$  its polarity is reversed as well. The **difference amplifier** circuit combines these two functions to perform **subtraction**.

In the difference-amplifier circuit of [Fig. 4-16\(a\)](#), the input signals are  $v_1$  and  $v_2$ ,  $R_2$  is the feedback resistance,  $R_1$  is the source resistance of  $v_1$ , and resistances  $R_3$  and  $R_4$  serve to control the scaling factor (gain) of  $v_2$ . To obtain an expression that relates the output voltage  $v_o$  to the inputs  $v_1$  and  $v_2$ , we apply KCL at nodes  $v_n$  and  $v_p$ . At  $v_n$ ,  $i_1 + i_2 + i_n = 0$ , which is equivalent to

$$\frac{v_n - v_1}{R_1} + \frac{v_n - v_o}{R_2} + i_n = 0 \quad (\text{node } v_n). \quad (4.38)$$

**Figure 4-16:** Difference-amplifier circuit.

At  $v_p$ ,  $i_3 + i_4 + i_p = 0$ , or

$$\frac{v_p - v_2}{R_3} + \frac{v_p}{R_4} + i_p = 0 \quad (\text{node } v_p). \quad (4.39)$$

Upon imposing the ideal op-amp constraints  $i_p = i_n = 0$  and  $v_p = v_n$ , we end up with

$$v_o = \left[ \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_1} \right) \right] v_2 - \left( \frac{R_2}{R_1} \right) v_1, \quad (4.40)$$

which can be cast in the form

$$v_o = G_2 v_2 + G_1 v_1, \quad (4.41)$$

where the scale factors (gains) are given by

$$G_2 = \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_1} \right) \quad (4.42a)$$

and

$$G_1 = -\left( \frac{R_2}{R_1} \right). \quad (4.42b)$$

According to **Fig. 4-16(b)** which is a block-diagram representation of the difference amplifier circuit:

► The difference amplifier scales  $v_2$  by positive gain  $G_2$ ,  $v_1$  by negative gain  $G_1$  and adds them together. ◀

For the difference amplifier to function as a subtraction circuit with equal gain, its resistors have to be interrelated by

$$R_2 R_3 = R_1 R_4, \quad (4.43)$$

in which case Eq. (4.41) reduces to

$$v_o = \left( \frac{R_2}{R_1} \right) (v_2 - v_1) \quad (\text{equal gain}). \quad (4.44)$$

Exact subtraction with no scaling requires that  $R_1 = R_2$ .

**Exercise 4-6:** The difference-amplifier circuit of **Fig. 4-16** is used to realize the operation

$$v_o = (6v_2 - 2) \text{ V.}$$

Given that  $R_3 = 5 \text{ k}\Omega$ ,  $R_4 = 6 \text{ k}\Omega$ , and  $R_2 = 20 \text{ k}\Omega$ , specify values for  $v_1$  and  $R_1$ .

**Answer:**  $v_1 = 0.2 \text{ V}$ ,  $R_1 = 2 \text{ k}\Omega$ . (See **CAD**)

## 4-7 Voltage Follower/Buffer

### 4-7.1 No Buffer

In electronic circuits, we often need to incorporate the functionality of a relatively simple (but important) circuit that serves to isolate the input source from variations in the load resistance  $R_L$ . Such a circuit is called a **voltage follower**, **buffer**, or **unity gain amplifier**. To appreciate the utility of the voltage follower, let us first examine the circuit shown in **Fig. 4-17(a)**. A source input circuit represented by its Thévenin equivalent ( $v_s$ ,  $R_s$ ), is connected to a load  $R_L$ . The output voltage is

$$v_o = \frac{v_s R_L}{R_s + R_L} \quad (\text{without voltage follower}), \quad (4.45)$$

which obviously is dependent on both  $R_s$  and  $R_L$ , so if the load resistance  $R_L$  changes, so will the output voltage  $v_o$ .

### 4-7.2 With Op-Amp Buffer

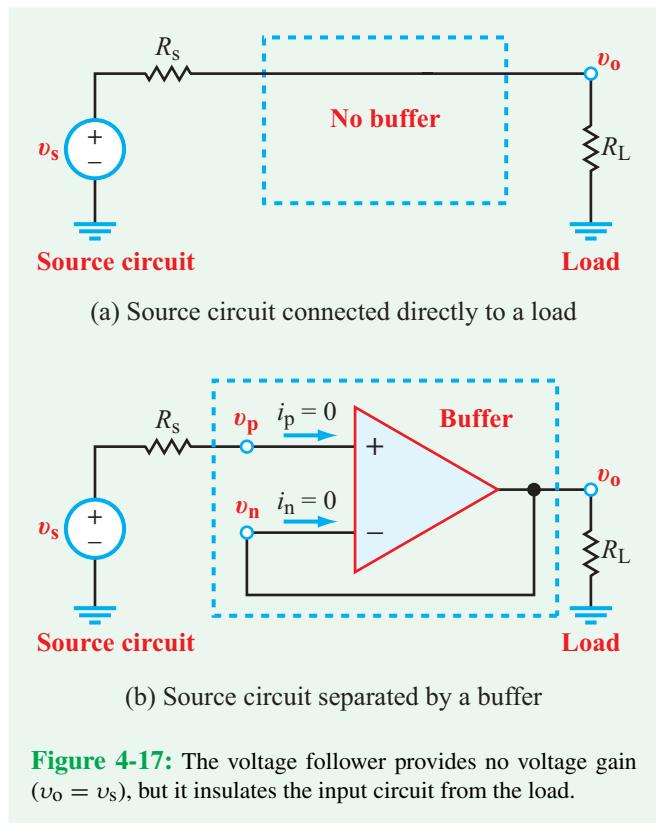
In contrast, when the op-amp voltage follower circuit shown in **Fig. 4-17(b)** is inserted in between the source circuit and the load, the output voltage becomes completely independent of both  $R_s$  and  $R_L$ . Because  $i_p = 0$ , it follows that  $v_p = v_s$ . Furthermore, in view of the op-amp constraint  $v_p = v_n$  and because the output node is connected directly to  $v_n$ , it follows that

$$v_o = v_p = v_s \quad (\text{with voltage follower}), \quad (4.46)$$

and this is true regardless of the values of  $R_s$  and  $R_L$  (excluding  $R_s = \text{open circuit}$  and/or  $R_L = \text{short circuit}$ , either of which would invalidate the entire circuit). Thus:

- The output of the voltage follower **follows** the input signal while remaining immune to changes in  $R_L$  because it has a high input resistance and low output resistance. ◀

A circuit that offers this type of protection is often called a **buffer**.



**Figure 4-17:** The voltage follower provides no voltage gain ( $v_o = v_s$ ), but it insulates the input circuit from the load.

- When designing and building a multistage circuit, designers usually insert buffers between adjacent stages, which allows them to design each stage separately and then cascade them all together with buffers in between them. ◀

### 4-7.3 Input-Output Resistance

When is a buffer needed? Consider again the circuit in **Fig. 4-17(a)**. Let us examine  $v_o$  for various values of  $R_s$  and  $R_L$ .

$R_s$ (kΩ)	$R_L$ (kΩ)	$v_o$ (V)	% change	Buffer needed?
1	0.1	0.09	91%	Yes
1	1	0.5	50%	Yes
1	10	0.91	9%	Probably
1	100	0.99	1%	No

If  $R_s < R_L$ , or even if  $R_s \approx R_L$ , there is a substantial difference between  $v_o$  and  $v_s$ . This is **overloading** the circuit, which we

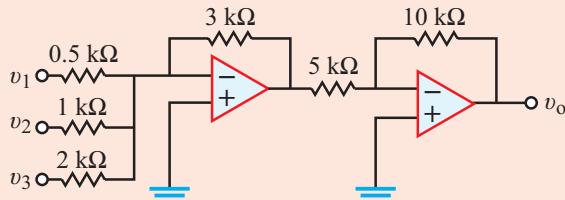
typically just call ***loading***. Substantial current is drawn from the source, and the voltage is decreased as a result. To prevent this, a buffer is needed. But if  $R_s \ll R_L$ , the change is minimal, and the circuit does not require a buffer.

An additional interesting aspect of buffering has to do with where the current is coming from and where it is going to in the circuit. In **Fig. 4-17(a)**, the current is coming from the source and going to the load. Excess current is being drawn, and the circuit is (over)loaded, thus reducing the output voltage  $v_o$ . In **Fig. 4-17(b)**, the current is *not* coming from the source, but it is going to the load. Where is it coming from? The answer is that it is coming from the output of the buffer, extracted from the power supply voltage  $V_{cc}$  that powers the op amp in the buffer.

**Concept Question 4-14:** What is the function of a voltage follower, and why is it called a “buffer”? (See [CAD](#))

**Concept Question 4-15:** How much voltage gain is provided by the voltage follower? (See [CAD](#))

**Exercise 4-7:** Express  $v_o$  in terms of  $v_1$ ,  $v_2$ , and  $v_3$  for the circuit in **Fig. E4.7**.



**Figure E4.7**

**Answer:**  $v_o = 12v_1 + 6v_2 + 3v_3$ . (See [CAD](#))

These circuits can be used in various combinations to realize specific signal-processing operations. We note that the input-output transfer functions are independent of the load resistance  $R_L$  that may be connected between the output terminal  $v_o$  and ground. In the case of the noninverting amplifier, the transfer function is also independent of the source resistance  $R_s$ .

- ▶ When cascading multiple stages of op-amp circuits in series, care must be exercised to ensure that none of the op amps is driven into saturation by the cumulative gain of the multiple stages. ◀

When analyzing circuits that involve op amps, whether in configurations similar to or different from those we encountered so far in this chapter, the basic rules to remember are as follows:

### Basic Rules of Op-Amp Circuits

- (1) KCL and KVL always apply everywhere in the circuit, but KCL is inapplicable at the output node when applying the ideal op-amp model. All other circuit-analysis tools can be applied to op-amp circuits.
- (2) The op amp will operate in the linear range so long as  $|v_o| < |V_{cc}|$ .
- (3) The ideal op-amp model assumes that the source resistance  $R_s$  (connected to terminals  $v_p$  or  $v_n$ ) is much smaller than the op-amp input resistance  $R_i$  (which usually is no less than  $10 M\Omega$ ), and the load resistance  $R_L$  is much larger than the op-amp output resistance  $R_o$  (which is on the order of tens of ohms).
- (4) The ideal op-amp constraints are  $i_p = i_n = 0$  and  $v_p = v_n$ .

### Example 4-4: Block-Diagram Representation

Generate a block-diagram representation for the circuit shown in **Fig. 4-18(a)**.

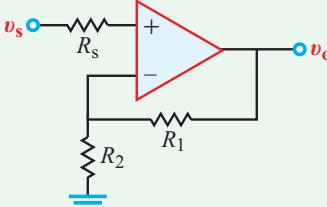
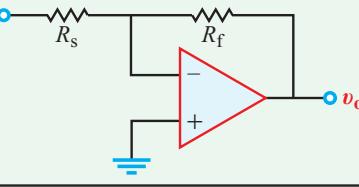
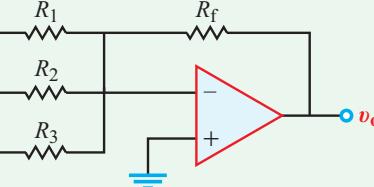
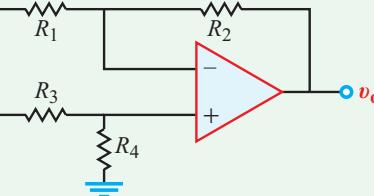
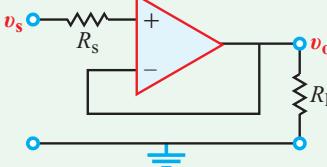
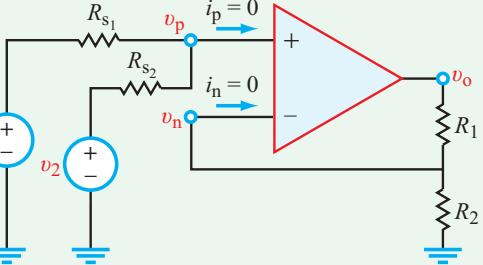
**Solution:** The first op amp is an inverting amplifier (**Table 4-3(b)**) with a dc input voltage  $v_1 = 0.42$  V. Its circuit gain  $G_i$  (with the subscript added to denote “inverting amp”) is

$$G_i = -\frac{30K}{10K} = -3,$$

## 4-8 Op-Amp Signal-Processing Circuits

**Table 4-3** provides a summary of the op-amp circuits we have considered thus far, together with their functional characteristics in the form of block-diagram representations.

**Table 4-3:** Summary of op-amp circuits.

Op-Amp Circuit	Block Diagram
 <p><b>Noninverting Amp</b> <math>(v_o \text{ independent of } R_s)</math></p>	$v_s \rightarrow \boxed{G = \frac{R_1 + R_2}{R_2}} \rightarrow v_o = Gv_s$
 <p><b>Inverting Amp</b></p>	$v_s \rightarrow \boxed{G = -\frac{R_f}{R_s}} \rightarrow v_o = Gv_s$
 <p><b>Inverting Summing Amp</b></p>	$v_1 \rightarrow \boxed{G_1 = -R_f/R_1}$ $v_2 \rightarrow \boxed{G_2 = -R_f/R_2}$ $v_3 \rightarrow \boxed{G_3 = -R_f/R_3}$ $v_o = G_1v_1 + G_2v_2 + G_3v_3$
 <p><b>Subtracting Amp</b></p>	$v_1 \rightarrow \boxed{G_1 = -\frac{R_2}{R_1}}$ $v_2 \rightarrow \boxed{G_2 = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right)}$ $v_o = G_1v_1 + G_2v_2$
 <p><b>Voltage Follower / Buffer</b> <math>(v_o \text{ independent of } R_s \text{ and } R_L)</math></p>	$v_s \rightarrow \boxed{G = 1} \rightarrow v_o = v_s$
 <p><b>Noninverting Summing Amp</b></p>	$v_1 \rightarrow \boxed{G_1 = \left(\frac{R_1 + R_2}{R_2}\right)\left(\frac{R_{s_2}}{R_{s_1} + R_{s_2}}\right)}$ $v_2 \rightarrow \boxed{G_2 = \left(\frac{R_1 + R_2}{R_2}\right)\left(\frac{R_{s_1}}{R_{s_1} + R_{s_2}}\right)}$ $v_o = G_1v_1 + G_2v_2$

and its output is

$$v_{o_1} = G_1 v_1 = -3(0.42) = -1.26 \text{ V.}$$

The second op amp is a difference amplifier. Using **Table 4-3(d)**, the gains of its positive and negative channels are

$$\begin{aligned} G_2 &= \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_1} \right) \\ &= \left( \frac{2K}{1K + 2K} \right) \left( \frac{10K + 20K}{10K} \right) = 2 \end{aligned}$$

and

$$G_1 = -\frac{R_2}{R_1} = -\frac{20K}{10K} = -2.$$

Hence,

$$v_o = G_2 v_2 + G_1 v_{o_1} = 2v_2 - 2(-1.26) = (2v_2 + 2.52) \text{ V.}$$

#### Example 4-5: Elevation Sensor

A hand-held elevation sensor uses a pair of capacitors separated by a flexible metallic membrane (**Fig. 4-19(a)**) to measure the height  $h$  above sea level. The lower chamber in **Fig. 4-19(a)** is sealed, and its pressure is  $P_0$ , which is the standard atmospheric pressure at sea level. The pressure in the upper chamber, which

is open to the outside air, is  $P$ . When at sea level,  $P = P_0$ , so the membrane assumes a flat shape and the two capacitances are equal. Since atmospheric pressure decreases with elevation, a rise in altitude results in a change in the pressure  $P$  in the upper chamber, causing the membrane to bend upwards (**Fig. 4-19(b)**), thereby changing the capacitances of the two capacitors. The sensor measures a voltage  $v_s$  that is proportional to the change in capacitance.

Based on measurements of  $v_s$  as a function of  $h$ , the data was found to exhibit an approximately linear variation given by

$$v_s = 2 + 0.2h \quad (\text{V}), \quad (4.47)$$

where  $h$  is in km. The sensor is designed to operate over the range  $0 \leq h \leq 10$  km. Design a circuit whose output voltage  $v_o$  (in volts) is an exact indicator of the height  $h$  (in km).

**Solution:** Based on the given information, the sensor voltage  $v_s$  will serve as the input to the circuit we are asked to design, and the output  $v_o$  will represent the height elevation  $h$ . We therefore need a circuit that can perform the operation

$$v_o = h = \frac{1}{0.2} v_s - \frac{2}{0.2} = 5v_s - 10, \quad (4.48)$$

where we have inverted Eq. (4.47) to solve for  $h$  in terms of  $v_s$ . The functional form of Eq. (4.48) indicates that we have

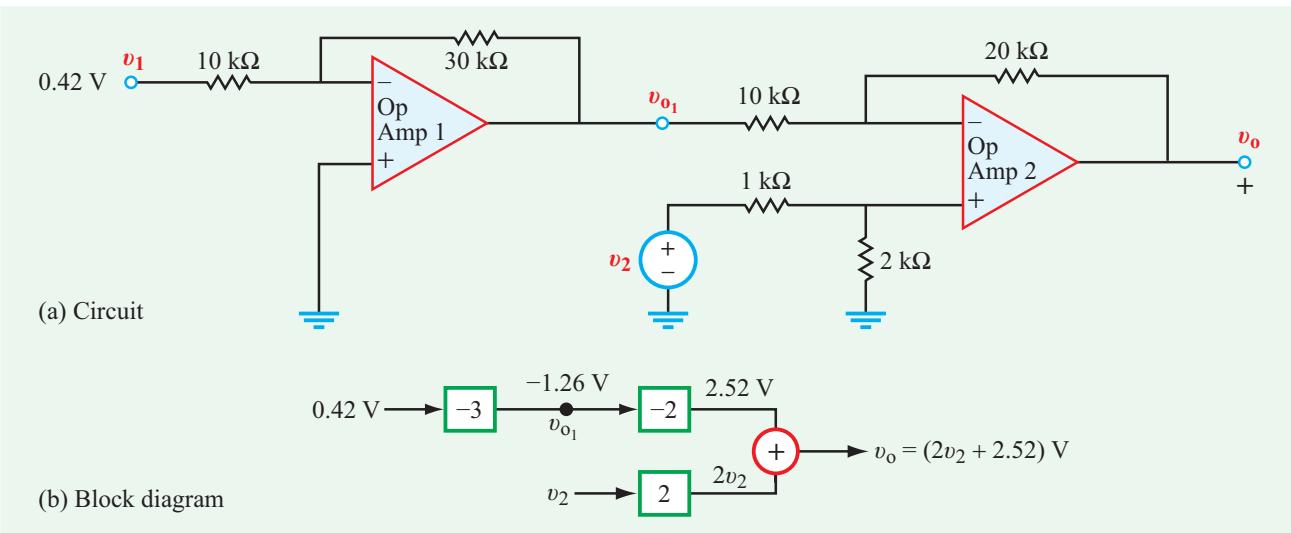
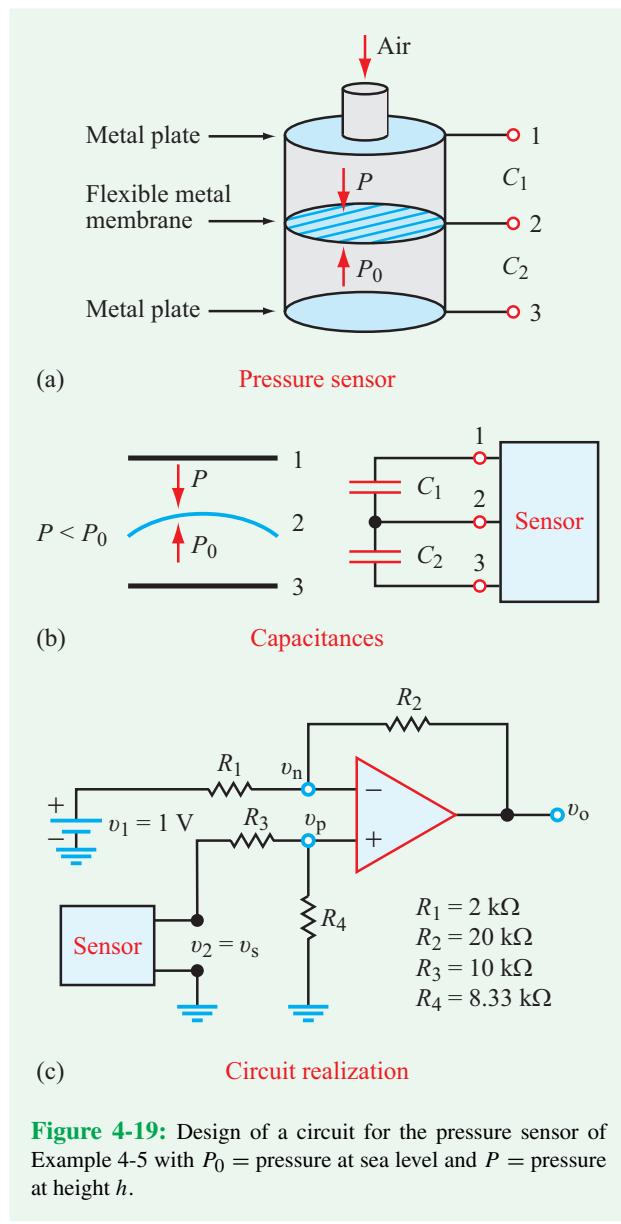


Figure 4-18: Block-diagram representation (Example 4-4).



**Figure 4-19:** Design of a circuit for the pressure sensor of Example 4-5 with  $P_0$  = pressure at sea level and  $P$  = pressure at height  $h$ .

only one active (variable) input, namely  $v_s$ , which we need to amplify by a factor of 5, but we also need to subtract 10 V from it. There are multiple circuit configurations that can achieve the desired operation, including the subtractor circuit shown in **Table 4-3(d)** and in **Fig. 4-19(c)**. According to Eq. (4.40), the output of the difference amplifier is given by

$$v_o = \left[ \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_1} \right) \right] v_2 - \left( \frac{R_2}{R_1} \right) v_1. \quad (4.49)$$

Equation (4.49) can be made to implement Eq. (4.48) if we select the following

- (a)  $v_s = v_2$
- (b)  $v_1$  as a dc voltage source such that  $(R_2/R_1)v_1 = 10$  V, which can be satisfied by arbitrarily selecting  $v_1 = 1$  V and  $(R_2/R_1) = 10$
- (c) values for  $R_1$  through  $R_4$  that simultaneously satisfy the conditions

$$\frac{R_2}{R_1} = 10 \quad \text{and} \quad \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_1} \right) = 5.$$

A possible set of values that meets these conditions is

$$R_1 = 2 \text{ k}\Omega, \quad R_2 = 20 \text{ k}\Omega, \\ R_3 = 10 \text{ k}\Omega, \quad R_4 = 8.33 \text{ k}\Omega.$$

Before we conclude the design, we should check to make sure that the op amp will operate in its linear range over the full range of operation of the sensor. According to Eq. (4.47), as  $h$  varies from zero to 10 km,  $v_s$  varies from 2 V to 4 V. The corresponding range of variation of  $v_o$ , from Eq. (4.48), is from zero to 10 V. Hence, we should choose an op amp designed to function with a dc supply voltage  $V_{cc}$  that exceeds 10 V.

#### Example 4-6: Circuit with Multiple Op Amps

Relate the output voltage  $v_o$  to the input voltages  $v_1$  and  $v_2$  of the circuit in **Fig. 4-20**.

**Solution:** By comparing the circuit connections surrounding the four op amps with those given in **Table 4-3**, we recognize op amps 1 and 2 as noninverting amplifiers (sources  $v_1$  and  $v_2$  are connected to + input terminals), op amp 3 as an inverting amplifier with a gain of  $-1$  (equal input and feedback resistors  $R_4$ ), and op amp 4 as an inverting summing amplifier (**Table 4-3(b)**) with equal gain (same input resistances  $R_6$  at summing point).

We start by examining the pair of input op amps. Because they are not among the standard configurations in **Table 4-3**, we will use KVL/KCL to evaluate them. For op amp 1,  $v_{p1} = v_1$  and  $v_{n1} = v_{p1}$  (op-amp voltage constraint). Hence,

$$v_a = v_{n1} = v_1.$$

Similarly, for op amp 2,

$$v_b = v_{n2} = v_2.$$

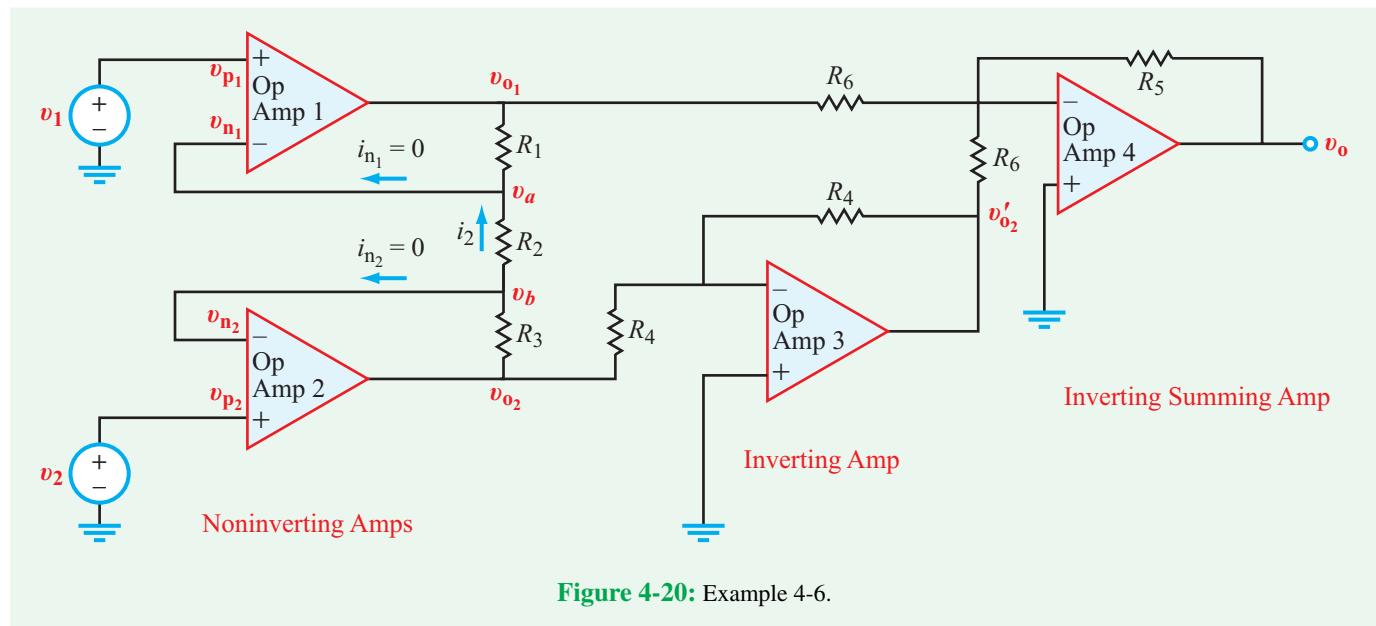


Figure 4-20: Example 4-6.

Since  $i_{n1} = i_{n2} = 0$  (op-amp current constraint),

$$i_2 = \frac{v_b - v_a}{R_2} = \frac{v_2 - v_1}{R_2},$$

and

$$\begin{aligned} v_{o_2} - v_{o_1} &= i_2(R_1 + R_2 + R_3) \\ &= \left( \frac{R_1 + R_2 + R_3}{R_2} \right) (v_2 - v_1). \end{aligned} \quad (4.50)$$

Op amp 3 is a standard inverting amplifier, so we can use **Table 4-3(c)** to obtain

$$v'_{o_2} = -\left(\frac{R_4}{R_2}\right)v_{o_2} = -v_{o_2}.$$

Op amp 4 is an inverting summing amplifier (**Table 4-3(c)**) with output

$$\begin{aligned} v_o &= -\frac{R_5}{R_6}(v_{o_1} + v'_{o_2}) \\ &= -\frac{R_5}{R_6}(v_{o_1} - v_{o_2}) \\ &= \frac{R_5}{R_6}(v_{o_2} - v_{o_1}) = R_5 \left( \frac{R_1 + R_2 + R_3}{R_6 R_2} \right) (v_2 - v_1). \end{aligned} \quad (4.51)$$

### Example 4-7: Interesting Op-Amp Circuit

Generate a plot for  $i_L$  at the output side of the circuit shown in **Fig. 4-21(a)** versus  $v_s$ , covering the full linear range of  $v_s$ .

**Solution:** This circuit is not one of the standard op-amp configurations in **Table 4-3**, so we need to analyze it using KVL/KCL. At node  $v_n$ , KCL gives

$$\frac{v_n}{2k} + \frac{v_n - v_o}{6k} = 0,$$

which leads to

$$v_o = 4v_n.$$

At node  $v_p$ , KCL gives

$$\frac{v_p - (v_s + 0.5)}{2k} = 0,$$

which leads to

$$v_p = v_s + 0.5.$$

By imposing the op-amp constraint  $v_p = v_n$ , we have

$$v_o = 4v_n = 4(v_s + 0.5) = 4v_s + 2.$$

At the output side,

$$i_L = \frac{v_o - 4}{1k} = \frac{4v_s + 2 - 4}{1k} = (4v_s - 2) \text{ mA.}$$

For  $v_o = V_{cc} = 10 \text{ V}$ ,

$$10 = 4v_s + 2, \quad \text{or } v_s = 2 \text{ V},$$

and for  $v_o = -V_{cc} = -10 \text{ V}$ ,

$$-10 = 4v_s + 2, \quad \text{or } v_s = -3 \text{ V.}$$

Hence, linear range of  $v_s$  is

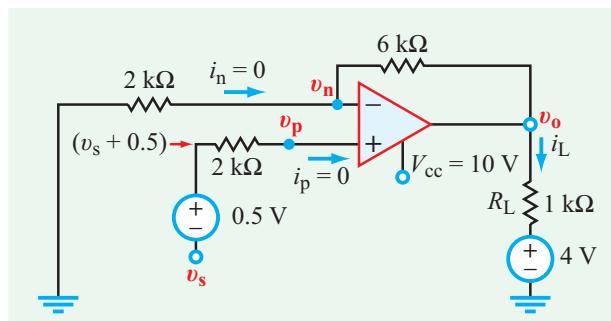
$$-3 \text{ V} \leq v_s \leq 2 \text{ V} \quad (\text{linear range}).$$

**Figure 4-21(b)** displays a plot of  $i_L$  versus  $v_s$  over the latter's linear range. Note that the linear range is not symmetrical.

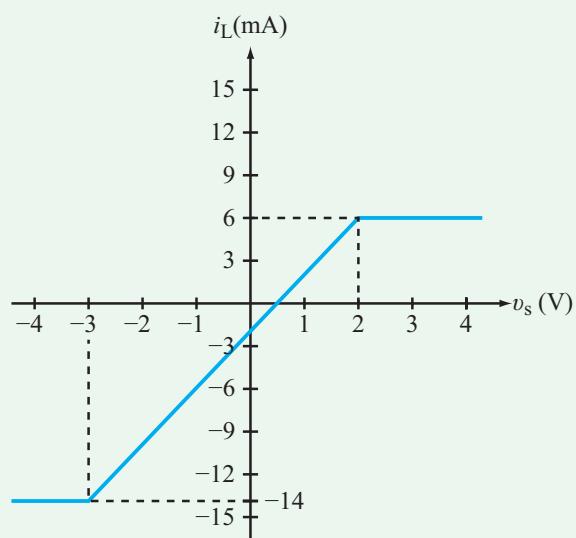
## 4-9 Instrumentation Amplifier

► An electric **sensor** is a circuit used to measure a physical quantity, such as distance, motion, temperature, pressure, or humidity. *In some applications, the intent is not to measure the magnitude of a certain quantity, but rather to sense small deviations from a nominal value.* ◀

For example, if the temperature in a room is to be maintained at  $20^\circ\text{C}$ , the functional goal of the temperature sensor is to measure the difference between the room temperature  $T$  and the reference temperature  $T_0 = 20^\circ\text{C}$  and then to activate an air conditioning or heating unit if the deviation exceeds a certain prespecified threshold. Let us assume the threshold is  $0.1^\circ\text{C}$ . Instead of requiring the sensor to be able to measure  $T$  with an absolute accuracy of no less than  $0.1^\circ\text{C}$ , an alternative approach would be to design the sensor to measure  $\Delta v = v_2 - v_1$ , where  $v_2$  is the voltage output of a thermocouple circuit responding to the room temperature  $T$  and  $v_1$  is the voltage corresponding to what a calibrated thermocouple would measure when  $T_0 = 20^\circ\text{C}$ . Thus, the sensor is designed to measure the deviation of  $T$  from  $T_0$ , rather than  $T$  itself, with an absolute accuracy of no less than  $0.1^\circ\text{C}$ . The advantage of such an approach is that the signal is now  $\Delta v$ , which is more than two orders of magnitude smaller than  $v_2$ . A circuit with a precision of 10 percent is not good enough for measuring  $v_2$ , but it is plenty good for measuring  $\Delta v$ .



(a) Circuit



(b)  $i_L - v_s$  transfer plot

**Figure 4-21:** Circuit for Example 4-7.

To appreciate the advantage of the differential measurement approach over the direct measurement approach, consider the two system configurations represented in **Fig. 4-22**.

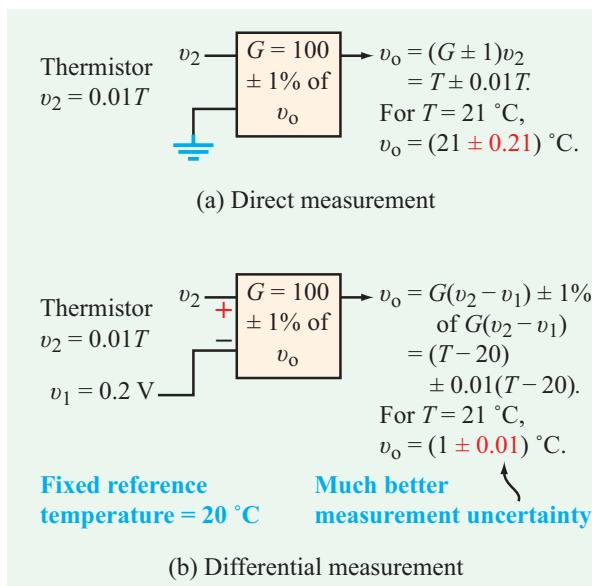
### (a) Direct Measurement Approach

In the configuration depicted in **Fig. 4-22(a)**, input voltage  $v_2$  represents the voltage across a thermistor used to measure the temperature  $T$  in a house. The voltage is related to  $T$  by

$$v_2 = 0.01T,$$

with  $T$  in  $^\circ\text{C}$ . The application circuit has a gain of 100 and a measurement precision of  $\pm 1\%$  of the amplified output. Thus,

$$v_o = (100 \pm 1)v_2 = (100 \pm 1) \times 0.01T = T \pm 0.01T.$$



**Figure 4-22:** Comparison of direct and differential measurement uncertainties.

If  $T = 21^\circ\text{C}$ , the output registers  $21^\circ\text{C}$ , and the associated precision is  $0.21^\circ\text{C}$ .

#### (b) Differential Measurement Approach

The differential system in **Fig. 4-22(b)** also uses  $v_2$  to measure  $T$ , but it also uses a fixed voltage  $v_1$  at the negative terminal, with  $v_1$  set at the desired reference temperature of  $20^\circ\text{C}$ . Hence,  $v_1 = 0.2 \text{ V}$ . The differential output is given by

$$\begin{aligned} v_o &= 100(v_2 - v_1) \pm (v_2 - v_1) \\ &= 100(v_2 - 0.2) \pm (v_2 - 0.2) \\ &= 100(0.01T - 0.2) \pm (0.01T - 0.2) \\ &= (T - 20) \pm 0.01(T - 20). \end{aligned}$$

If  $T = 21^\circ\text{C}$ ,

$$v_o = (1 \pm 0.01)^\circ\text{C}.$$

In the differential system,  $v_o$  measures the deviation from the reference temperature of  $20^\circ\text{C}$ , which is the same information

provided by the direct measurement system, but with an associated precision on the order of 20 times better ( $\pm 0.01^\circ\text{C}$  compared with  $\pm 0.21^\circ\text{C}$  for the direct measurement system).

- ▶ The instrumentation amplifier is perfectly suited for detecting and amplifying a small signal deviation when superimposed on one or the other of two much larger (and otherwise identical) signals. ◀

An instrumentation amplifier consists of three op amps, as shown in **Fig. 4-23**. The circuit configuration for the first two is the same as the one we examined earlier in connection with Example 4-6. According to Eq. (4.50), the voltage difference between the outputs of op amps 1 and 2 is

$$v_{o_2} - v_{o_1} = \left( \frac{R_1 + R_2 + R_3}{R_2} \right) (v_2 - v_1) = G_1(v_2 - v_1), \quad (4.52)$$

where  $G_1$  is the circuit gain of the first stage (which includes op amps 1 and 2) and is given by

$$G_1 = \frac{R_1 + R_2 + R_3}{R_2}. \quad (4.53)$$

The third op amp is a difference amplifier that amplifies  $(v_{o_2} - v_{o_1})$  by a gain factor  $G_2$  given by

$$G_2 = \frac{R_4}{R_5}. \quad (4.54)$$

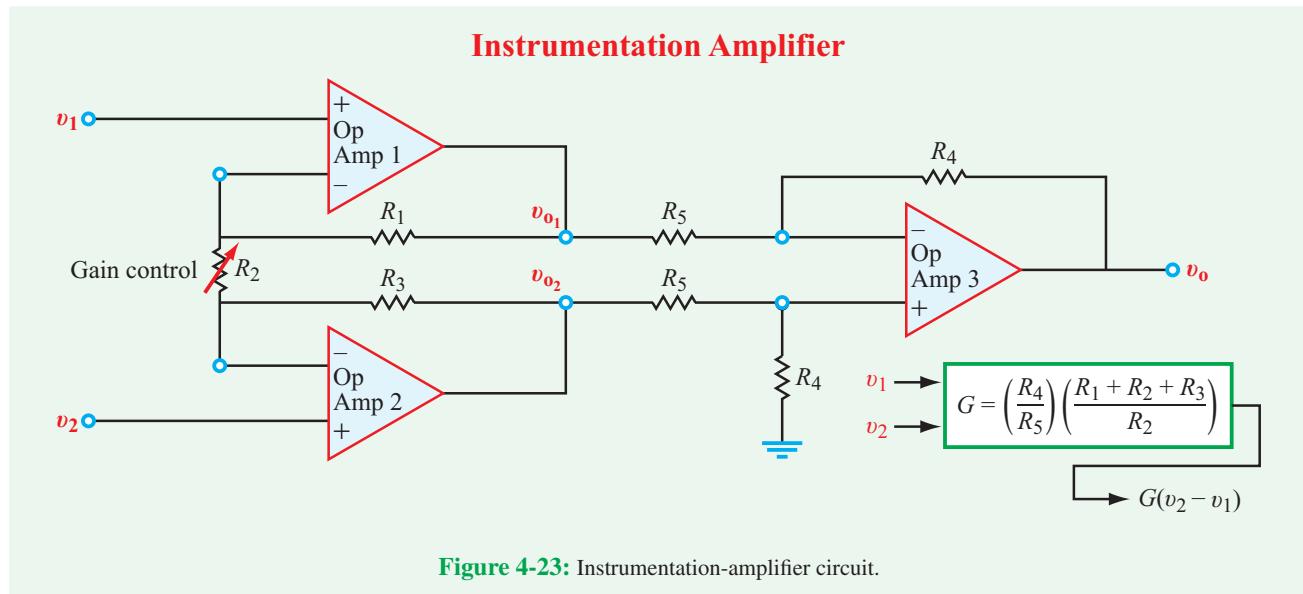
Hence,

$$v_o = G_2 G_1 (v_2 - v_1) = \left( \frac{R_4}{R_5} \right) \left( \frac{R_1 + R_2 + R_3}{R_2} \right) (v_2 - v_1). \quad (4.55)$$

To simplify the circuit, and improve precision, all resistors—with the exception of  $R_2$ —often are chosen to be identical in design and construction, thereby minimizing deviations between their resistances. If we set  $R_1 = R_3 = R_4 = R_5 = R$  in Eq. (4.55), the expression for  $v_o$  reduces to

$$v_o = \left( 1 + \frac{2R}{R_2} \right) (v_2 - v_1). \quad (4.56)$$

In that case,  $R_2$  becomes the **gain-control resistance** of the circuit; its value (relative to  $R$ ) sets the gain. If the expected signal deviation  $(v_2 - v_1)$  is on the order of microvolts to millivolts, the instrumentation amplifier is designed to have an overall gain that would amplify the signal to the order of volts.



**Figure 4-23:** Instrumentation-amplifier circuit.

► The instrumentation amplifier is a high-sensitivity, high-gain, deviation sensor. Several semiconductor manufacturers offer instrumentation-amplifier circuits in the form of integrated packages. ◀

**Concept Question 4-16:** When designing a multistage op-amp circuit, what should the design engineer do to insure that none of the op amps is driven into saturation? (See [CAD](#))

**Concept Question 4-17:** If the goal is to measure small deviations between a pair of input signals, what is the advantage of using an instrumentation amplifier over using a difference amplifier? (See [CAD](#))

**Exercise 4-8:** To monitor brain activity, an instrumentation-amplifier sensor uses a pair of needle-like probes inserted at different locations in the brain to measure the voltage difference between them. If the circuit is of the type shown in [Fig. 4-23](#) with  $R_1 = R_3 = R_4 = R_5 = R = 50 \text{ k}\Omega$ ,  $V_{cc} = 12 \text{ V}$ , and the maximum magnitude of the voltage difference that the brain is likely to exhibit is 3 mV, what should  $R_2$  be to maximize the sensitivity of the brain sensor?

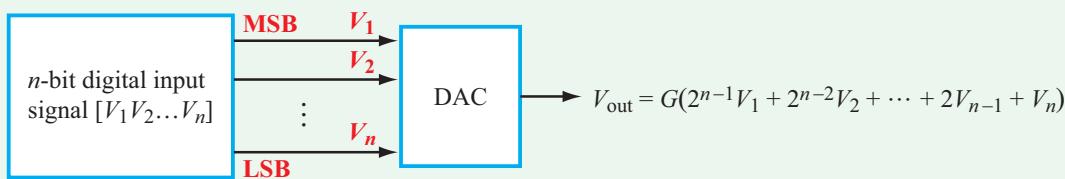
**Answer:**  $R_2 = 25 \Omega$ . (See [CAD](#))

## 4-10 Digital-to-Analog Converters (DAC)

► A **digital-to-analog converter** (DAC) is a circuit that transforms a digital sequence presented to its input into an analog output voltage whose magnitude is proportional to the decimal value of the input signal. ◀

An  $n$ -bit digital signal is described by the sequence  $[V_1 V_2 V_3 \dots V_n]$ , where  $V_1$  is called the **most significant bit** (MSB) and  $V_n$  is the **least significant bit** (LSB). Voltages  $V_1$  through  $V_n$  can each assume only two possible states—either a 0 or a 1. When a bit is in the 1 state, its decimal value is  $2^m$ , where  $m$  depends on the location of that bit in the sequence. For the most significant bit ( $V_1$ ), its decimal value is  $2^{(n-1)}$ ; for  $V_2$  it is  $2^{(n-2)}$ ; and so on. The decimal value of the least significant bit is  $2^{n-n} = 2^0 = 1$ , when that bit is in state 1. Any bit in state 0 has a decimal value of 0. **Table 4-4** illustrates the correspondence between the binary sequences of a 4-bit digital signal and their decimal values. The binary sequences start at [0000] and end at [1111], representing 16 decimal values extending from 0 to 15 and inclusive of both ends. To do so, the DAC in [Fig. 4-24](#) has to sum  $V_1$  to  $V_n$  after weighting each by a factor equal to its decimal value. Thus, for a 4-bit digital sequence, for example, the output voltage of the DAC has to be related to the input by

$$\begin{aligned} V_{\text{out}} &= G(2^{4-1}V_1 + 2^{4-2}V_2 + 2^{4-3}V_3 + 2^{4-4}V_4) \\ &= G(8V_1 + 4V_2 + 2V_3 + V_4), \end{aligned} \quad (4.57)$$



**Figure 4-24:** A digital-to-analog converter transforms a digital signal into an analog voltage proportional to the decimal value of the digital sequence.

**Table 4-4:** Correspondence between binary sequence and decimal value for a 4-bit digital signal and output of a DAC with  $G = -0.5$ .

V <sub>1</sub>	V <sub>2</sub>	V <sub>3</sub>	V <sub>4</sub>	Decimal Value	DAC Output (V)
0000				0	0
0001				1	-0.5
0010				2	-1
0011				3	-1.5
0100				4	-2
0101				5	-2.5
0110				6	-3
0111				7	-3.5
1000				8	-4
1001				9	-4.5
1010				10	-5
1011				11	-5.5
1100				12	-6
1101				13	-6.5
1110				14	-7
1111				15	-7.5

where  $G$  is a scale factor that has no influence on the relative weights of the four terms. The magnitude of  $G$  is selected to suit the range of the output voltage. If the input is a 3-bit sequence whose range of decimal values extends from 0 to 7, one might design the circuit so that  $G = 1$ , because in that case, the maximum output voltage is 7 V, which is below  $V_{cc}$  for most op amps. For digital signals with longer sequences,  $G$  needs to be smaller than 1 in order to avoid saturating the op amp.

The weighted-sum operation of a DAC can be realized by many different signal-processing circuits. A rather straightforward implementation is shown in **Fig. 4-25**, where an inverting summer (**Table 4-3(c)**) uses the ratios of  $R_f$  to the individual resistances to realize the necessary weights, and the positions of the switches determine the 0/1 states of the 4 bits. Reference

to either **Table 4-3(c)** or Eq. (4.34) yields

$$\begin{aligned} V_{\text{out}} &= -\frac{R_f}{R} V_1 - \frac{R_f}{2R} V_2 - \frac{R_f}{4R} V_3 - \frac{R_f}{8R} V_4 \\ &= \frac{-R_f}{8R} (8V_1 + 4V_2 + 2V_3 + V_4), \end{aligned} \quad (4.58)$$

which satisfies the relative weights given in Eq. (4.57). Also, in this case,

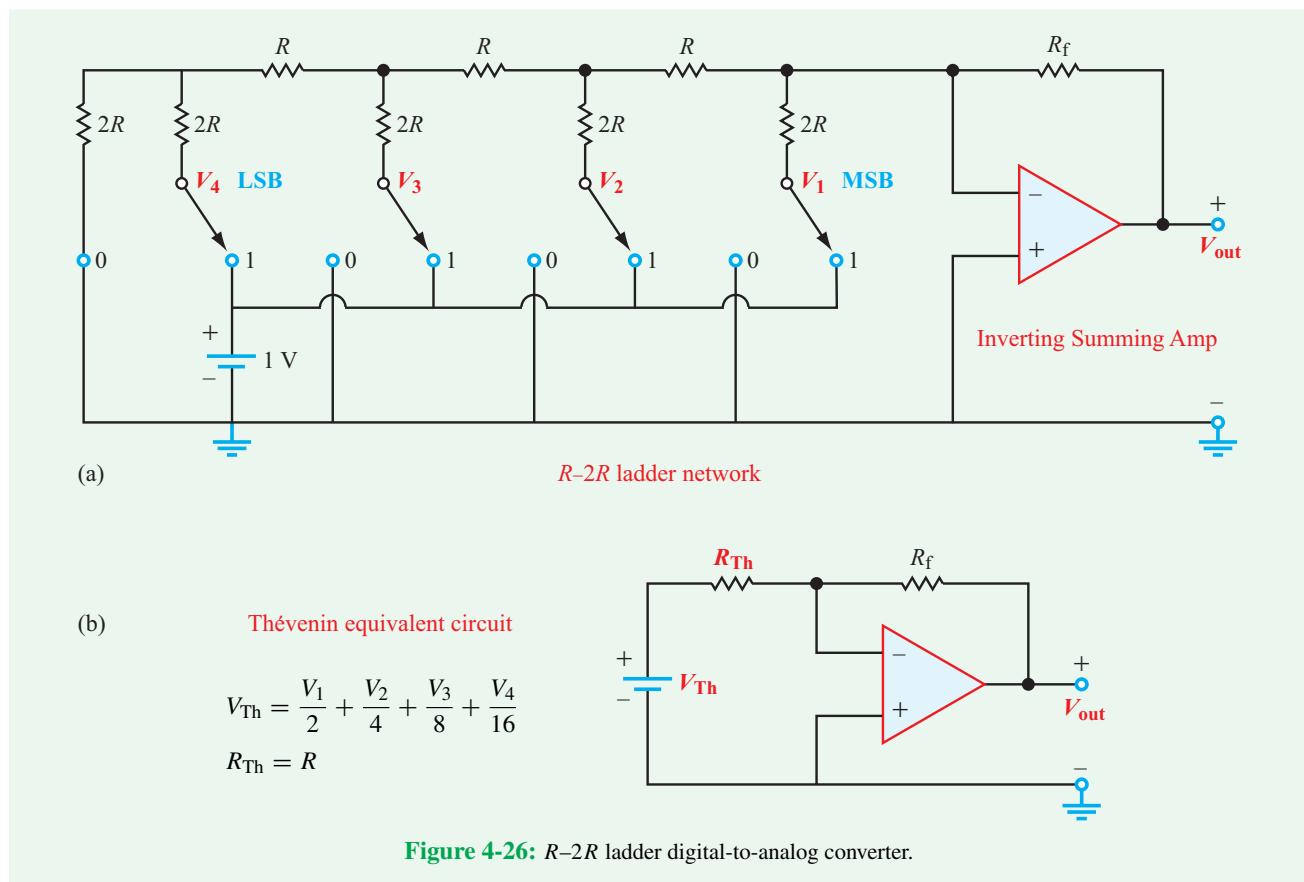
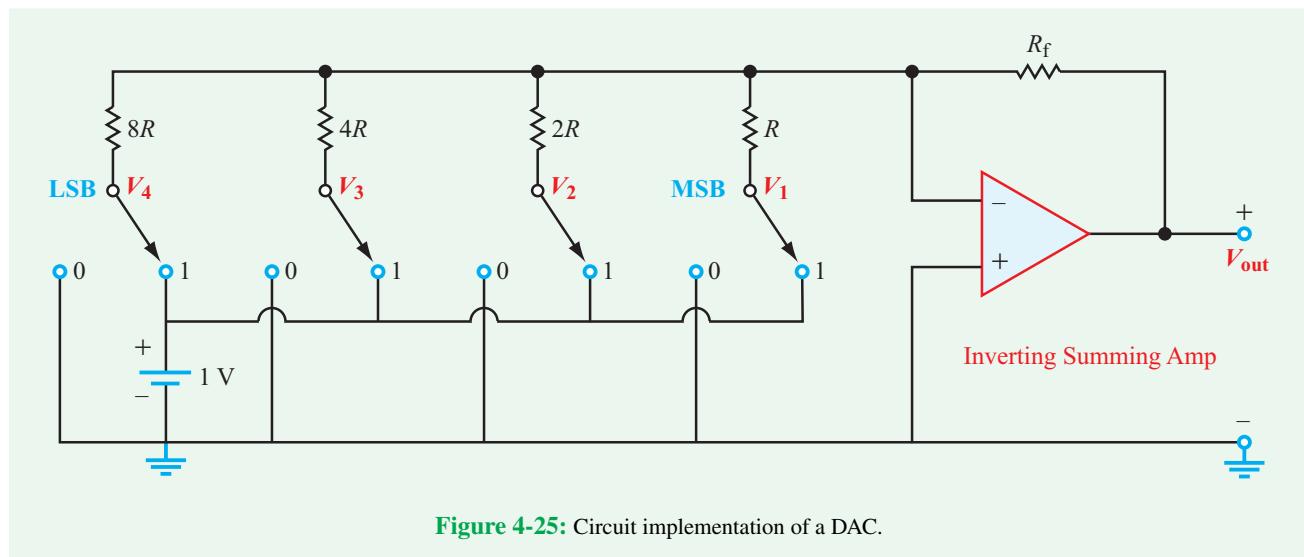
$$G = -\frac{R_f}{8R}. \quad (4.59)$$

For  $[V_1 V_2 V_3 V_4] = [1111]$ ,  $V_{\text{out}} = 15G$ . By selecting  $G = -0.5$  (corresponding to  $R_f = 4R$ ), the output will vary from 0 to -7.5.

#### Example 4-8: R-2R Ladder

The circuit in **Fig. 4-26(a)** offers an alternative approach to realizing digital-to-analog conversion of a 4-bit signal. It is called an  $R-2R$  ladder, because all of the resistors of its input circuit have values of  $R$  or  $2R$ , thereby limiting the input resistance seen by the dc source to a 2 : 1 range no matter how many bits are contained in the digital sequence. This is in contrast with the DAC of **Fig. 4-25**, whose input-resistance range is dependent on the number of bits; 8 : 1 for a 4-bit converter, and 128 : 1 for an 8-bit converter. Additionally, circuit performance and precision depend on resistor tolerance and are superior when fewer groups of resistors are involved in the input circuit. Resistors fabricated in the same production process are likely to exhibit less variability among them than resistors fabricated by different processes.

Show that the  $R-2R$  ladder in **Fig. 4-26(a)** does indeed provide the appropriate weighting for a 4-bit DAC. If  $R = 2 \text{ k}\Omega$  and  $V_{cc} = 10 \text{ V}$ , what is the maximum realistic value that  $R_f$  can have?



**Figure 4-26:** R-2R ladder digital-to-analog converter.

**Solution:** Even though we know that (depending on the positions of the switches)  $V_1$  to  $V_4$  can each assume only 2 binary values, namely 0 or 1 V, let us treat  $V_1$  to  $V_4$  as dc power supplies and apply multiple iterations of voltage-current transformations (starting on the left with the LSB) to arrive at the Thévenin equivalent circuit at the input side of the op amp. The result of such a transformation process is shown in Fig. 4-26(b), in which

$$V_{Th} = \frac{V_1}{2} + \frac{V_2}{4} + \frac{V_3}{8} + \frac{V_4}{16} \quad (4.60a)$$

and

$$R_{Th} = R. \quad (4.60b)$$

Consequently,

$$\begin{aligned} V_{out} &= -\frac{R_f}{R_{Th}} V_{Th} \\ &= -\frac{R_f}{R} \left( \frac{V_1}{2} + \frac{V_2}{4} + \frac{V_3}{8} + \frac{V_4}{16} \right) \\ &= -\frac{R_f}{16R} (8V_1 + 4V_2 + 2V_3 + V_4). \end{aligned} \quad (4.61)$$

The voltage  $|V_{out}|$  is a maximum when  $[V_1 V_2 V_3 V_4] = [1111]$ , in which case

$$V_{out} = -\frac{15}{16} \frac{R_f}{R}.$$

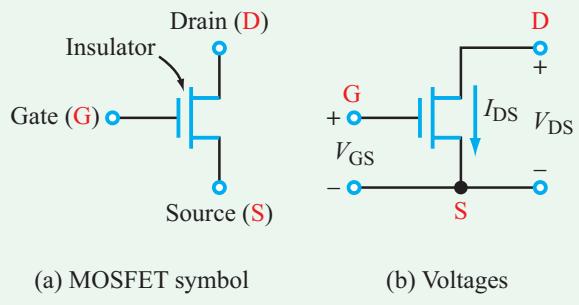
To insure that  $|V_{out}|$  does not exceed  $|V_{cc}| = 10$  V as well as to provide a safety margin of 2 V it is necessary that

$$8 \geq \frac{15}{16} \frac{R_f}{2k},$$

which gives  $R_f \leq 17.1$  kΩ.

**Concept Question 4-18:** In a digital-to-analog converter, what dictates the maximum value that  $R_f$  can assume? (See CAD)

**Concept Question 4-19:** What is the advantage of the  $R-2R$  ladder (Fig. 4-26) over the traditional DAC (Fig. 4-25)? (See CAD)



**Figure 4-27:** MOSFET symbol and voltage designations.

**Exercise 4-9:** A 3-bit DAC uses an  $R-2R$  ladder design with  $R = 3$  kΩ and  $R_f = 24$  kΩ. If  $V_{cc} = 10$  V, write an expression for  $V_{out}$  and evaluate it for  $[V_1 V_2 V_3] = [111]$ .

**Answer:**

$$V_{out} = -\frac{R_f}{8R} (4V_1 + 2V_2 + V_3) = -(4V_1 + 2V_2 + V_3).$$

For  $[V_1 V_2 V_3] = [111]$ ,  $V_{out} = -7$  V, whose magnitude is smaller than  $V_{cc} = 10$  V. (See CAD)

## 4-11 The MOSFET as a Voltage-Controlled Current Source

In earlier sections, we demonstrated how op amps can be used to build buffers and amplifiers. We now examine how to realize the same outcome using MOSFETs. The simplest model of a **MOSFET**, which stands for *metal-oxide semiconductor field-effect transistor*, is shown in Fig. 4-27(a). The vast majority of commercial computer processors are built with MOSFETs; as mentioned in Technology Brief 1 on nanotechnology, a 2010 Intel Core processor contains over 1 billion independent MOSFETs. A MOSFET has three terminals: the **gate** (G), the **source** (S), and the **drain** (D). Actually, it has a fourth terminal, namely its body (B), but we will ignore it for now because for many applications it is simply connected to the ground terminal. The circuit symbol for the MOSFET may look somewhat unusual, but it is actually a stylized depiction of the physical cross section of a real MOSFET. In a real MOSFET, the gate

consists of a very thin layer ( $< 500$  nm thick) of a conducting material adjacent to an even thinner layer ( $< 100$  nm) of insulator. The insulator in turn is placed directly on the surface of a relatively large slab of semiconductor material, usually referred to as “the chip” in everyday conversation (usually made of silicon 0.5 to 1.5 mm thick). The drain and the source sections are fabricated into this semiconductor chip on either side of the gate.

- ▶ Because the gate G is separated from the rest of the transistor by the thin insulating layer, no dc current can flow from G to either D or S. ◀

Nonetheless, it turns out that the voltage difference between terminals G and S is key to the operation of the MOSFET.

Using terminal S as a reference in **Fig. 4-27(b)**, we denote  $V_{DS}$  and  $V_{GS}$  as the voltages at terminals D and G, respectively. We also denote the current that flows through the MOSFET from D to S as  $I_{DS}$ . This simplification is justified by the assumption that no current flows through the gate node to either the drain or source node. The operation of the MOSFET can be analyzed by placing it in the simple circuit shown in **Fig. 4-28(a)**, in which  $V_{DD}$  is a dc power supply voltage usually set at a level close to but not greater than, the maximum rated value of  $V_{DS}$  for the specific MOSFET model under consideration. The resistance  $R_D$  is external to the MOSFET, and its role will be discussed later. The input voltage is synonymous with  $V_{GS}$  and the output voltage is synonymous with  $V_{DS}$ ,

$$V_{in} = V_{GS}, \quad \text{and} \quad V_{out} = V_{DS}. \quad (4.62)$$

Moreover  $V_{out}$  is related to  $V_{DD}$  by

$$V_{out} = V_{DD} - I_{DS} R_D. \quad (4.63)$$

Since current cannot flow from G to either D or S, the only current that can flow through the MOSFET is  $I_{DS}$ . The dependence of  $I_{DS}$  on  $V_{GS}$  and  $V_{DS}$  is shown for a typical MOSFET in **Fig. 4-28(b)** in the form of characteristic curves displaying the response of  $I_{DS}$  to  $V_{DS}$  at specific values of  $V_{GS}$ . We observe that if  $V_{DS}$  is greater than a certain **saturation threshold value**  $V_{SAT}$ , the curves assume approximately constant levels, and that these levels are

approximately proportional to  $V_{GS}$ . These observations allow us to characterize the MOSFET in terms of the simple, equivalent circuit model shown in **Fig. 4-28(c)**, which consists of a single dependent current source given by

$$I_{DS} = g V_{GS}, \quad (4.64)$$

where  $g$  is a **MOSFET gain constant**. The characteristic curves associated with this model, which is valid only if  $V_{DS}$  exceeds  $V_{SAT}$ , are shown in **Fig. 4-28(d)**.

Even though this equivalent circuit is very simple and more sophisticated models usually are required, it nevertheless serves as a useful approximate model for introducing some common uses of MOSFETs. In real MOSFETs, the relationship between  $I_{DS}$  and  $V_{GS}$  at saturation is not strictly linear. How linear the relationship is depends (in part) on the size of the transistor. Modern sub-micron transistors used in digital processors exhibit a linear relationship between  $I_{DS}$  and  $V_{GS}$  at saturation, whereas larger MOSFETs used for power switching may behave nonlinearly. For our purposes, the simplification denoted by Eq. (4.64) will suffice.

#### 4-11.1 Digital Inverter

We now will use the model given by Eq. (4.64) to demonstrate how the MOSFET can function as a **digital inverter** by generating an output state of “0” when the input state is “1,” and vice versa. Combining Eqs. (4.62) to (4.64) gives

$$V_{out} = V_{DD} - g R_D V_{in}. \quad (4.65)$$

The constant  $g$  is a MOSFET parameter, so if we choose  $R_D$  such that  $g R_D \approx 1$ , Eq. (4.65) simplifies to

$$\frac{V_{out}}{V_{DD}} = 1 - \frac{V_{in}}{V_{DD}}. \quad (4.66)$$

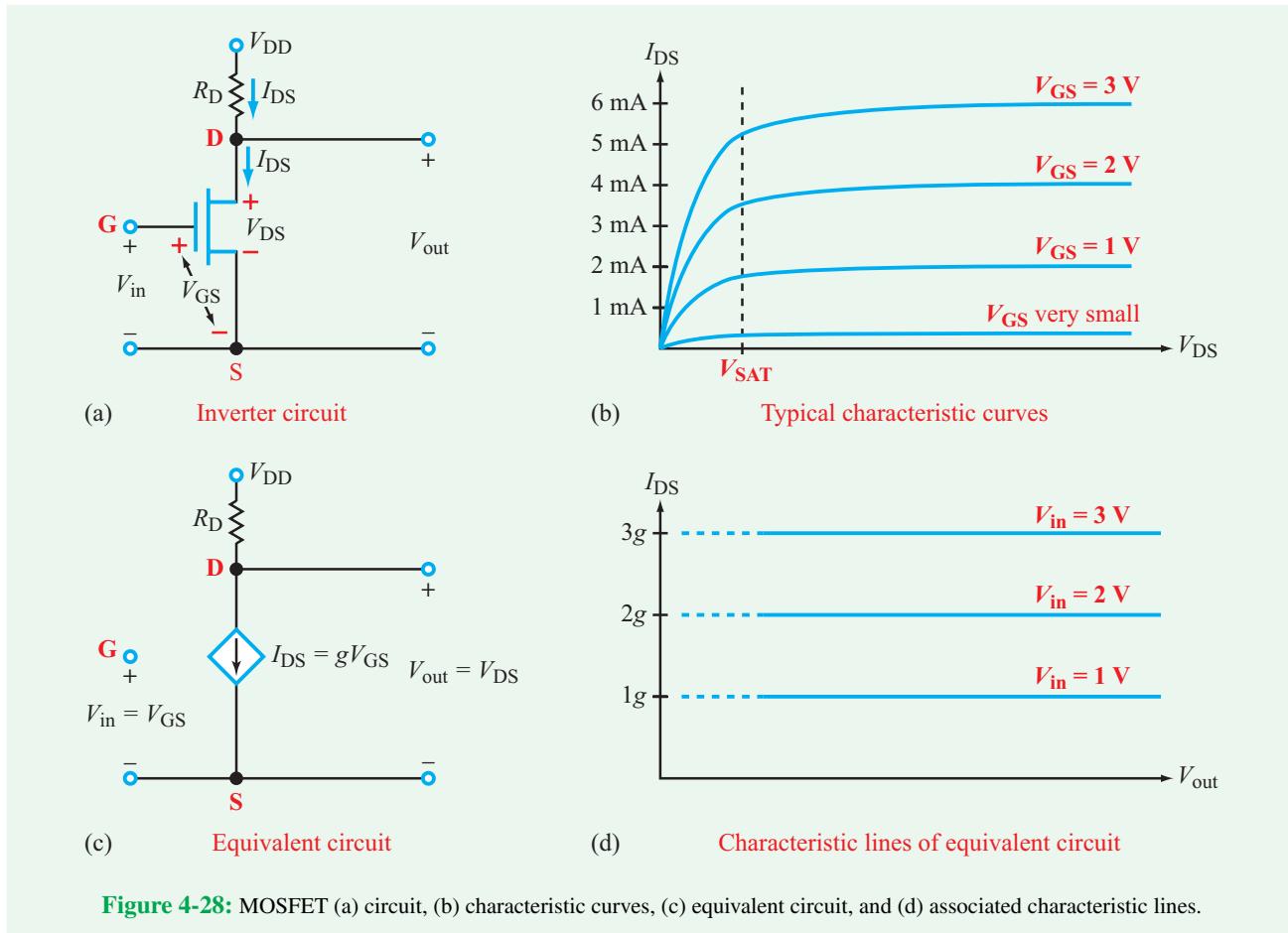
In a digital inverter, we are interested in output responses to only two input states. According to Eq. (4.66):

$$\text{If } \frac{V_{in}}{V_{DD}} = 1, \quad \rightarrow \quad \frac{V_{out}}{V_{DD}} = 0, \quad (4.67a)$$

and

$$\text{if } \frac{V_{in}}{V_{DD}} = 0, \quad \rightarrow \quad \frac{V_{out}}{V_{DD}} = 1. \quad (4.67b)$$

Hence, the MOSFET circuit in **Fig. 4-28(a)** behaves like a digital inverter, provided the model given by Eq. (4.64) holds true and requiring that  $V_{DS}$  exceeds  $V_{SAT}$ . In a real circuit,



**Figure 4-28:** MOSFET (a) circuit, (b) characteristic curves, (c) equivalent circuit, and (d) associated characteristic lines.

$V_{in}$  and  $V_{out}$  are not given by the simple results indicated by Eq. (4.67), but each can be categorized easily into high and low voltage values to satisfy the functionality of a digital inverter.

## 4-11.2 NMOS versus PMOS Transistors

The MOSFET circuit of Fig. 4-28(a) actually is called an n-channel MOSFET or **NMOS** for short. Its operation is limited to the first quadrant in Fig. 4-28(d), where both  $I_{DS}$  and  $V_{DS}$  can assume positive values only. A second type of MOSFET called **PMOS** (p-channel MOSFET) is designed and fabricated to operate in the third quadrant, corresponding to negative values for  $I_{DS}$  and  $V_{DS}$ , as illustrated in Fig. 4-29. To distinguish between the two types, the symbol for PMOS includes a small open circle at terminal  $G$ .

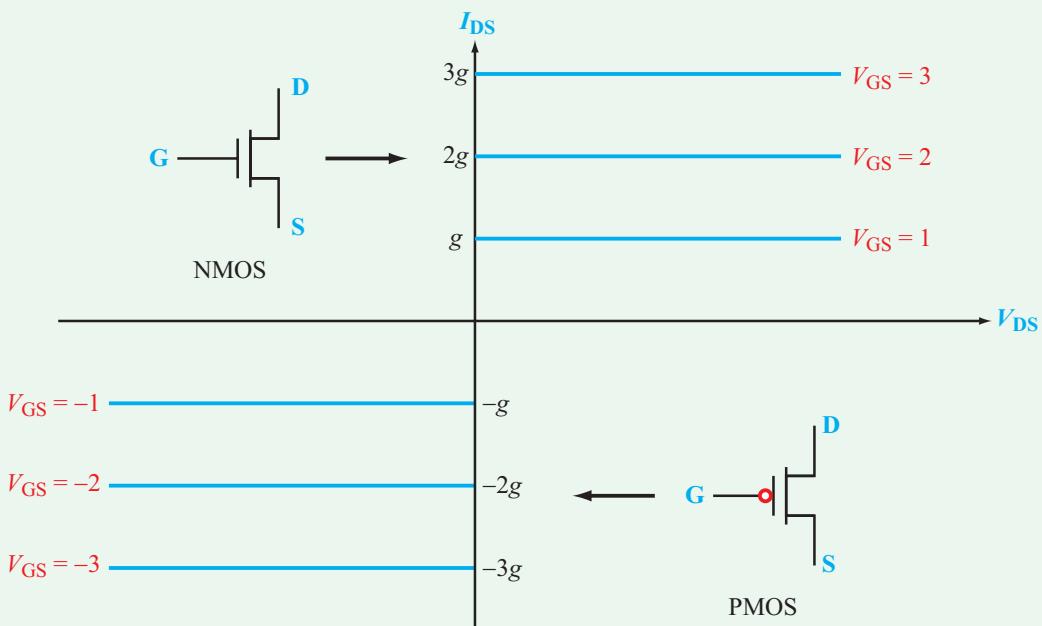
The NMOS inverter circuit of Fig. 4-28(a) provides the correct functionality required from a digital inverter, but it suffers from a serious power-dissipation problem. Let us consider the power consumed by  $R_D$  under realistic conditions:

### Input State 0:

$$\frac{V_{in}}{V_{DD}} = 0 \rightarrow I_{DS} \approx 0 \rightarrow P_{RD} = I_{DS}^2 R_D \approx 0 \quad (4.68a)$$

### Input State 1:

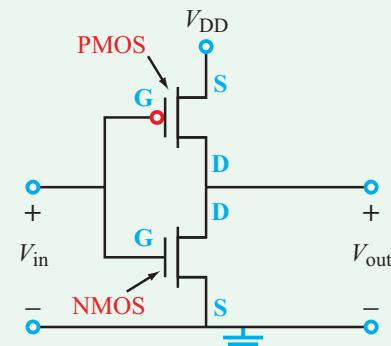
$$\frac{V_{in}}{V_{DD}} = 1 \rightarrow I_{DS} = \frac{V_{DD}}{R_D} \rightarrow P_{RD} = \frac{V_{DD}^2}{R_D}. \quad (4.68b)$$



**Figure 4-29:** Complementary characteristic curves for NMOS and PMOS.

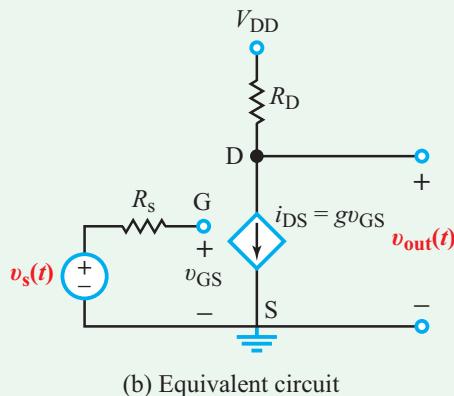
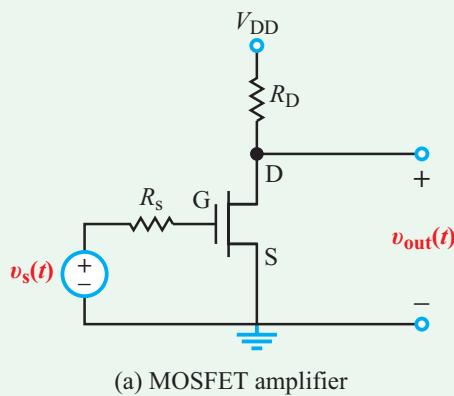
Heat dissipation in  $R_D$  is practically zero for input state 0, but for input state 1, it is equal to  $V_{DD}^2/R_D$ . The value of  $V_{DD}$ , which is dictated by the MOSFET specifications, is typically on the order of volts, and  $R_D$  can be made very large—on the order of  $k\Omega$  or tens of  $k\Omega$ . If  $R_D$  is much larger than that,  $I_{DS}$  becomes too small for the MOSFET to function as an inverter. For  $V_{DD}$  on the order of 1 V and  $R_D$  on the order of 10  $k\Omega$ ,  $P_{R_D}$  for an individual NMOS is on the order of  $100 \mu\text{W}$ . This amount of heat generation is trivial for a single transistor, but when we consider that a typical computer processor contains on the order of  $10^9$  transistors, all confined to a relatively small volume of space, the total amount of heat that would be generated by such an NMOS-based processor would likely *burn a hole through the computer!* To address this heat-dissipation problem, a new technology was introduced in the 1980s called **CMOS**, which stands for **complementary MOS**.

- CMOS has revolutionized the microprocessor industry and led to the rise of the x86 family of PC processors. ◀



**Figure 4-30:** CMOS inverter.

CMOS is a configuration that attaches an NMOS to a PMOS at their drain terminals, as shown in **Fig. 4-30**. The CMOS inverter provides the same functionality as the simpler NMOS inverter, but it has the distinct advantage in that it dissipates



**Figure 4-31:** MOSFET amplifier circuit for Example 4-9.

negligible power for *both* input states. The significance of the inverter is in the role it plays as a basic building block for more complicated logic circuits, such as those that perform AND and OR operations.

### 4-11.3 MOSFETs in Analog Circuits

In addition to their use in digital circuits, MOSFETs also can be used in analog circuits as buffers and amplifiers, as demonstrated by Examples 4-9 and 4-10. As we discussed earlier in Section 4-7, a buffer is a circuit that insulates the input voltage from variations in the load resistance.

#### Example 4-9: MOSFET Amplifier

The circuit shown in Fig. 4-31(a) is known as a common-source amplifier and uses a MOSFET with a dc drain voltage

$V_{DD} = 10\text{ V}$  and a drain resistance  $R_D = 1\text{ k}\Omega$ . The input signal  $v_s(t)$  is an ac voltage with a dc-bias given by

$$v_s(t) = [500 + 40 \cos 300t] \quad (\mu\text{V}).$$

Note that the amplitude of the input ac signal is several orders of magnitude smaller than that of the dc voltage  $V_{DD}$ . Apply the MOSFET equivalent model with  $g = 10\text{ A/V}$  to obtain an expression for  $v_{out}(t)$ .

**Solution:** Upon replacing the MOSFET with its equivalent circuit, we end up with the circuit in Fig. 4-31(b). At the input side, because no current flows through  $R_s$ , it follows that

$$v_{GS}(t) = v_s(t),$$

and at the output side,

$$\begin{aligned} v_{out}(t) &= V_{DD} - i_{DS}R_D \\ &= V_{DD} - gR_Dv_{GS}(t) \\ &= V_{DD} - gR_Dv_s(t). \end{aligned}$$

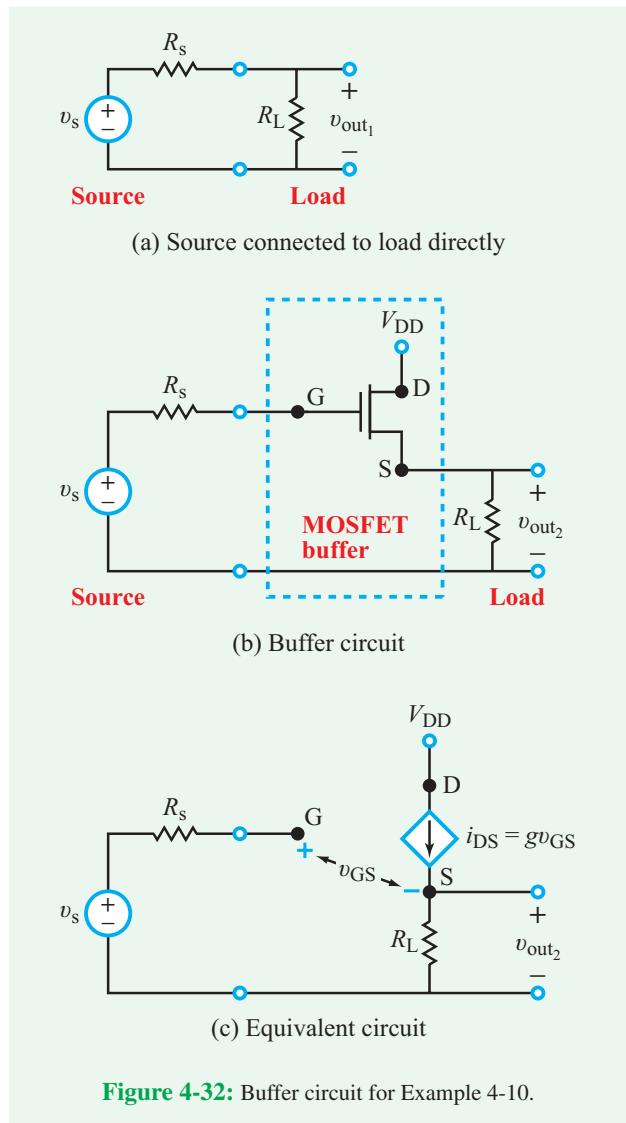
We observe that the output voltage consists of a constant dc component (namely  $V_{DD}$ ) and an ac component that is directly proportional to the input signal  $v_s(t)$ . For the element values specified in the problem,

$$\begin{aligned} v_{out}(t) &= 10 - 10 \times 10^3 \times (500 + 40 \cos 300t) \times 10^{-6} \\ &= 5 - 0.4 \cos 300t \quad \text{V}. \end{aligned}$$

The 5 V dc component is simply a level shift superimposed on which is a sinusoidal signal that is identical to the input signal but is inverted and amplified by an ac gain of  $10^4$  (from  $40\text{ }\mu\text{V}$  to  $0.4\text{ V}$ ).

#### Example 4-10: MOSFET Buffer

The circuit in Fig. 4-32(a) consists of a real voltage source ( $v_s$ ,  $R_s$ ) connected directly to a load resistor  $R_L$ . In contrast, the circuit in Fig. 4-32(b) uses a common-drain MOSFET circuit in between the source and the load to *buffer* (insulate) the source from the load. Let us define the source as being buffered from the load if the output voltage across the load is equal to at



**Figure 4-32:** Buffer circuit for Example 4-10.

least 99 percent of  $v_s$ . For each circuit, determine the condition on  $R_L$  that will satisfy this criterion. Assume  $R_s = 100 \Omega$  and the MOSFET gain factor  $g = 10 \text{ A/V}$ .

### Solution:

#### (a) No-Buffer Circuit

For the circuit in Fig. 4-32(a),

$$v_{out_1} = \frac{v_s R_L}{R_s + R_L}.$$

In order for  $v_{out_1}/v_s \geq 0.99$ , it is necessary that

$$\frac{R_L}{R_s} \geq 99$$

or

$$R_L \geq 9.9 \text{ k}\Omega \quad (\text{for } R_s = 100 \Omega).$$

#### (b) With MOSFET Buffer

For the circuit in Fig. 4-32(c), in which the MOSFET has been replaced with its equivalent circuit, KVL gives

$$-v_s + v_{GS} + v_{out_2} = 0.$$

Also,

$$\begin{aligned} v_{out_2} &= I_{DS} R_L \\ &= g R_L v_{GS}. \end{aligned}$$

Simultaneous solution of the two equations gives

$$v_{out_2} = \left( \frac{g R_L}{1 + g R_L} \right) v_s.$$

With  $g = 10 \text{ A/V}$  and in order for  $v_{out_2}$  to be no less than  $0.99 v_s$ , it is necessary that

$$R_L \geq 9.9 \Omega,$$

which is three orders of magnitude smaller than the requirement for the unbuffered circuit.

**Concept Question 4-20:** What is the major advantage of a CMOS over an NMOS circuit as a digital inverter? (See [CAD](#))

**Concept Question 4-21:** When a MOSFET is used in a buffer circuit,  $v_{out} \approx v_s$ , where  $v_s$  is the input signal voltage. So, why is it used? (See [CAD](#))

**Exercise 4-10:** In the circuit of Example 4-9, what value of  $R_D$  will give the highest possible ac gain while keeping  $v_{out}(t)$  always positive?

**Answer:**  $R_D = 1.85 \text{ k}\Omega$ . (See [CAD](#))

**Exercise 4-11:** Repeat Example 4-10, but require that  $v_{out}$  be at least 99.9 percent of  $v_s$ . What should  $R_L$  be (a) without the buffer and (b) with the buffer?

**Answer:** (a)  $R_L \geq 99.9 \text{ k}\Omega$ , (b)  $R_L \geq 99.9 \Omega$ . (See [CAD](#))

## Technology Brief 11

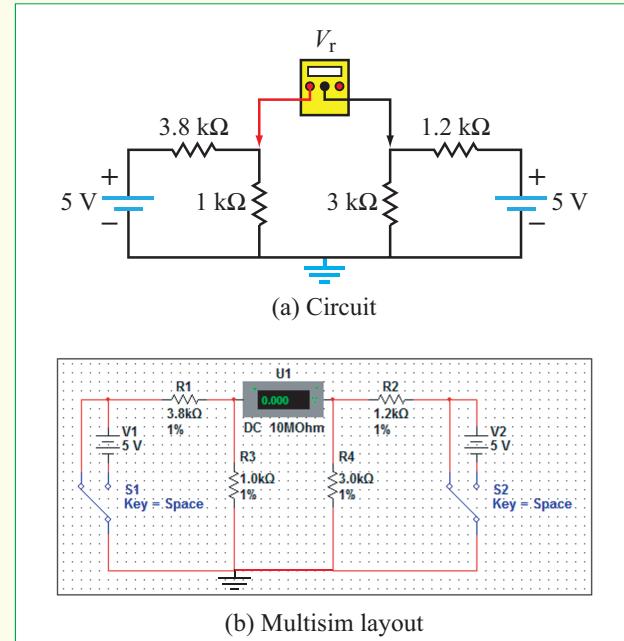
### Circuit Simulation Software

In Chapters 2 and 3 we examined all of the common methods used for analyzing linear electric circuits. In practice, these are used for designing and analyzing the many building blocks that make up larger circuits, or for obtaining approximate solutions for how more complex circuits function. In Technology Brief 1, we noted that **very large scale integrated circuits** (VLSI) have experienced exponential scaling for almost 50 years, so some of today's electrical networks may include as many as 100 billion transistors! The standard circuit analysis methods available to us are accurate and applicable, but it takes a great deal of computer automation to apply them to a 100 billion-transistor network. The **Multisim** circuit analysis software provides an excellent start towards modeling the behavior of complex circuits. Accordingly, Multisim will be the first of two computer-based tools we will explore in this Technology Brief. Whereas Multisim is an excellent tool, it treats a circuit as a 2-D configuration, which does not account for thermal effects associated with heat generation by the circuit elements, nor possible capacitive or inductive cross-coupling of voltages between elements (through the air or insulator medium between them). To account for these effects, we need to use a sophisticated **3-D computer simulation tool**. This is the subject of the second part of this Technology Brief.

#### Multisim Software

##### (1) Using Simulation Tools to Calculate and Understand

Engineers use **electronic design automation** (EDA) tools, such as Multisim, to understand the function of a circuit and calculate its response. Consider the simple example shown in **Fig. TF11-1(a)**, and let us assume we need to determine what voltage  $V_r$  would be measured by the voltmeter shown in the circuit. In this case, because the circuit is very simple, we can analyze it by hand or we can implement it and solve it by Multisim (**Fig. TF11-1(b)**). But if the circuit has more than five nodes, the by-hand approach becomes tedious, and the Multisim option becomes far more practical.

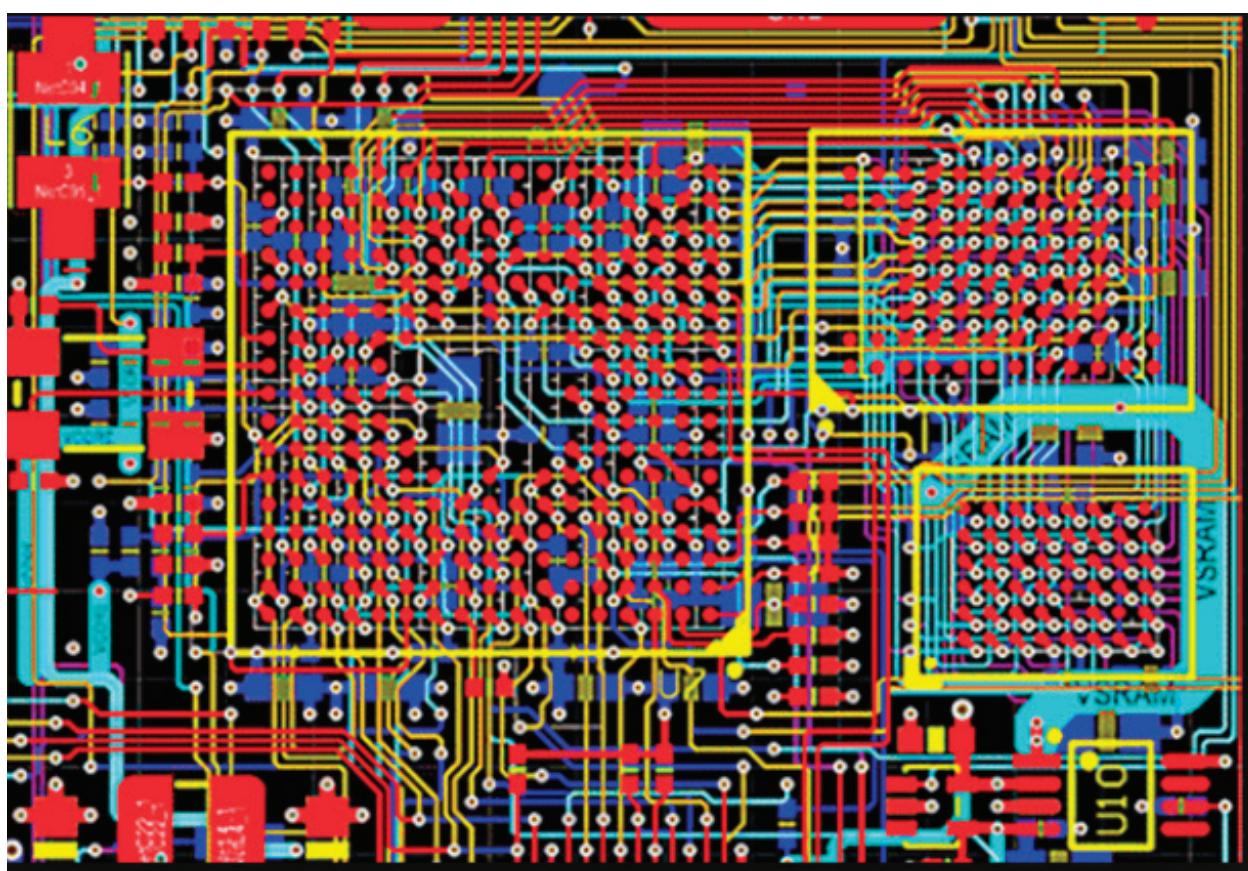


**Figure TF11-1:** Two-source circuit and Multisim representation using switches to switch one or both voltage sources on or off.

##### (2) Using Simulation Tools to Lay Out a Circuit

Once a circuit has been designed, we can either build it on a protoboard or, alternatively, we can have a circuit board built for it and then solder the parts to the board to create the circuit. **Printed circuit board** (PCB) layout tools help us plan the circuit layout and routing architecture, which often are multiple layers deep, as in the circuit of **Fig. TF11-2**.

When using silicon chips, for example, these designs involve hundreds, millions, or trillions of components arranged in one or more layers, and carrying thousands of simultaneous signals throughout the circuit, all acting together to obtain the desired voltage and/or current output of the circuit. Classic EDA tools (such as Multisim) begin with a **graphical user interface** (GUI) that allows users to specify what type of circuit elements (sources, resistors, switches, etc.) are needed and how they are connected together. Circuits made up of several elements can often be grouped or bundled together and stored in **libraries** for later reuse. Often, libraries of complex



**Figure TF11-2:** Multilayer PCB layout, with each layer assigned a different color. Holes and solder pads are planned for each chip and component attached to the board, and multilayer routing built into the circuit board connects them all together. (Courtesy of ZYPEX Inc.)

circuits (such as the core of a computer processor) are shared or purchased to reduce engineering design time. For circuits whose design can be expressed as either logical rules or a desired logical function—primarily digital circuits—modern software tools transform circuit design into an exercise in writing code. In essence, programs can be written in **hardware description languages** (HDL), which define the structure and/or operation of digital circuits. The program is then executed and a circuit description suitable for manufacture, or instantiation into a field-programmable gate array (FPGA), is synthesized. Programming in HDLs is similar to assembly language or C coding, although major

differences exist. Most modern complex digital circuits are designed, simulated, and synthesized with the aid of HDL tools.

Once the elements and their connections are defined, they are then modeled with either more or less detail (by specifying tolerance levels or other relevant parameters) depending on the level of accuracy needed. Simulation results are only as good as the circuit model and input parameters, so this is a very important consideration when using EDA software. The more detailed the model, the more accurate the results can be expected to be, but also the longer it takes the simulation to run. Consider, for example, the ideal and the more realistic models

for voltage and current sources listed in **Table 1-5**. The realistic source models are certainly more accurate than the ideal models, but even the “realistic” models are approximate, because they neglect nonlinearities, stray capacitance and inductance, and potential feedback loops within the sources. For many applications, the ideal model is sufficient, for others the first-order realistic model (including a resistor) is sufficient, but for others, a more detailed nonlinear model is required. How do you, the engineer, know what model to use? The intuition and knowledge gained from working with the common circuit analysis tools from Chapters 2 and 3 help you determine when you may or may not need a more realistic model. Often, we will first try a simplified model, and then one that is slightly more realistic. If there is minimal change, we do not go on to a more complex model, but if there is substantial change, we may try more and more realistic models (each requiring more time and memory for the software to run), until the result converges and we are satisfied that we have modeled the real system at hand.

Now let’s consider VLSI circuits involving trillions of transistors. Even with relatively simple models of the transistor (such as the BJT in Section 3-9 or MOSFET in Section 4-11), there are still more unknowns than we generally care to wait for the computer to solve. In this case, two simplifications are essential. First, we must break the circuit down into **functional blocks**, so we can design each block individually and cascade or connect the blocks together. We have already seen simple examples of doing this using the Thévenin equivalent circuit technique. Thévenin is also used this way in much larger circuits, including VLSI designs. Second, we must simplify the models we use for each circuit element. Fortunately (or perhaps necessarily!) the largest circuits electrical engineers design are digital circuits, for which we can use the simplest models of all. We can assume that all voltages are either **high/on** (digital 1) or **low/off** (digital 0). This flexibility in the voltages allows us to use much simpler models. The transistor, for example, can be modeled as just a switch (on or off), or just as a resistor that is switched in or out of the circuit. Assuming all voltages are either on or off is the simplest assumption. We also can model them as on/off or in transition between on and off. The transition (which is actually a **bouncy switch**) can be modeled as a linear slope from low to high or high to low. The length of this slope is the **rise time** of the transition, and the faster the rise time, the faster the circuit can send data.

### 3-D Modeling Tools

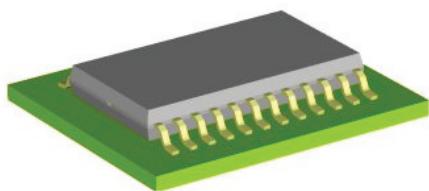
Model-based EDA tools define how a circuit is supposed to function electrically, but sometimes effects not included in the models come into play to make the circuit malfunction. Two of these that are particularly relevant are associated with thermal problems and coupling problems. We know that resistors and other devices are designed with specific power ratings. The power rating is related to the size and material the resistors are made of and their ability to withstand the heat generated by current moving through them. If we start pushing all of the elements of the circuit to their maximum capability, their interactions (hot chips next to other hot chips) may make the most vulnerable of these parts fail. But how do we determine which parts are the most vulnerable, and what solution can we offer to mitigate the heat problem? 3-D simulation tools help us to identify these potential problems or (all too often) diagnose them when they occur. The 3-D simulation process starts with the physical model of a given part, such as the high-speed IC package shown in **Fig. TF11-3(a)**. The spatial distributions of electrical voltage and current are then modeled for part or all of the package, as shown in **Fig. TF11-3(b)**. The current density at a given location is representative of what the temperature will be at that location. If overheating were to occur, it would most likely occur at the points with the highest current. More detailed thermal modeling can include the effects of heat sinks, fans, and other cooling effects. The voltage is used to calculate coupling between nearby electrical signals (such as two adjacent legs of this package).

Another interesting circuit simulation is shown in **Fig. TF11-4**, which displays the amount of power radiated by a crescent antenna.

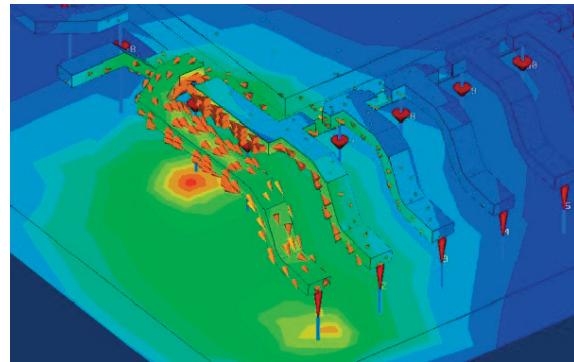
### So WHY Should You Learn the Circuit Analysis Methods Introduced in This Book?

Having learned how to apply the various circuit analysis tools covered in this book thus far, you may wonder why you need to learn so many different methods when they all can give you the same result. And now that you have read this Technology Brief and seen that you can use a computer to analyze circuits, you may wonder why you need to learn these analytical methods at all!

While it is true that automated tools are essential for testing circuits used in practical applications, it is equally true that the success of the design process is highly coupled to one’s understanding of the fundamental



(a) Physical package

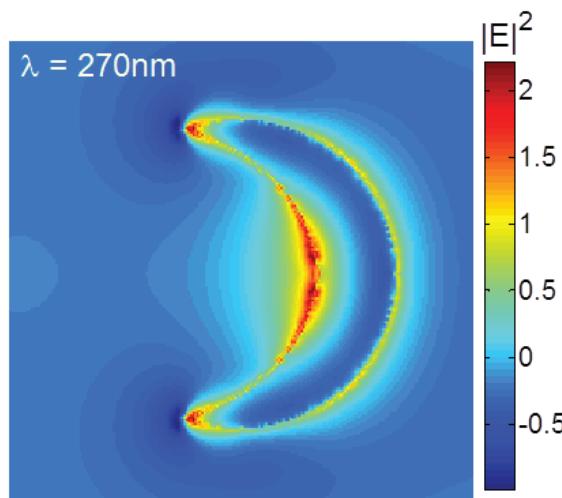


(b) Current density contour

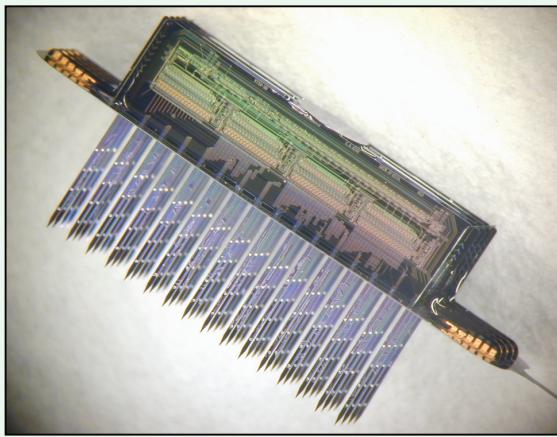
**Figure TF11-3:** High-speed IC package and contour and vector plot of the current density flowing through it at 5 GHz. The brighter/redder colors show higher current density ( $A/m^2$ ) (which also results in higher temperature) than the darker/bluer colors. The arrows show the direction in which the current is flowing, and the size of the arrow is also proportional to the magnitude of the current density. (Courtesy: CST MICROWAVE STUDIO<sup>®</sup> IC Package Simulation.)

concepts in circuit analysis and design. Designing a new circuit to address a specified application is a creative endeavor that relies on one's past experience and fluency in circuit behavior and performance. Once an initial circuit

configuration has been developed, computer simulation tools are then used to fine-tune the design and optimize the circuit performance.



**Figure TF11-4:** This 3D electromagnetic simulation was used to evaluate the fields (in this case the square of the electric field, which is proportional to power) in the nanocrescent antenna shown in Technology Brief 1. We can see the strong fields at the tips (because charge congregates there), and also in the center. (Credit: Miguel Rodriguez.)



**Figure 4-33:** Three-dimensional neural probe ( $5 \text{ mm} \times 5 \text{ mm} \times 3 \text{ mm}$ ). (Courtesy of Prof. Ken Wise and Gayatri Perlin, University of Michigan.)

## 4-12 Application Note: Neural Probes

The human brain is composed, in part, of interconnected networks of individual, information-processing cells known as **neurons**. There are about one trillion ( $10^{12}$ ) neurons in the human brain with each neuron having on average 7000 connections to other neurons. Although the working of the neural system is well beyond the scope of this book, it is important to note that when a neuron transmits information, it causes a change in the concentrations of various ions in its vicinity. This movement of ions gives rise to an electric current through the neuron's membrane which in turn generates a change in potential (voltage) between various parts of the cell and its surroundings. Thus, when a given neuron fires, a small ( $\sim 100 \text{ mV}$ ) but detectable potential drop develops between the cell and its surroundings.

Over the past few decades, various types of devices were built for measuring this electrical phenomenon in neurons. In recent years, however, the field has achieved phenomenal success due in part to the successful development of **neural probes** (also known as **neural interfaces**) with very high sensitivities. An example of a 3-dimensional probe is shown in **Fig. 4-33**. It consists of a 2-D array of very thin probes—each instrumented with a sensor at each of several locations along its length. With such a probe, it is now possible to measure the **action potentials** of firing neurons at a large number of brain locations simultaneously. Modern neural interface systems also have been developed to stimulate or change the electrical state of specific neurons, thereby affecting their operation in the brain. These types of devices not only offer the potential of unraveling

aspects of brain development and operation, but they also are beginning to see use in clinical applications for the treatment of chronic neurological disorders, such as Parkinson's disease (see Technology Briefs 17 and 32 on neural stimulation and computer-brain interfaces, respectively).

Because these voltage signals are so small, on-board amplification, noise-removal, and analog-to-digital circuitry are needed to process the signal from the brain to the recording device.

### Example 4-11: Neural Probe

The neural probe shown in **Fig. 4-34** consists of a long shank at the end of which lie two metal electrodes. This shank is inserted a short distance into the brain and the signal coming from these electrodes is recorded. For simplicity, we will model the brain activity between the two probes just like a realistic voltage source  $V_s$  in series with a resistance  $R_s$ . The source produces inverted pulses with  $-100 \text{ mV}$  amplitudes. Note that neither  $V_a$  nor  $V_b$  are grounded relative to the ground level of the circuit. The neural signal needs to be inverted and amplified so that it can be presented to an analog-to-digital converter (ADC) which only operates in the 0 to 5 V range. Design the amplifier circuit.

**Solution:** The input signal is represented by the difference between  $V_a$  and  $V_b$ , and since neither of those terminals is grounded, some sort of differential amplifier is the logical choice for the intended application.

The amplifier should invert the input signal and amplify it into the 0 to 5 V range required by the ADC. Given these constraints, we propose to use the op-amp instrumentation amplifier circuit of **Fig. 4-23** with  $V_a$  as input  $v_1$  and  $V_b$  as input  $v_2$ . The amplifier output is proportional to  $(v_2 - v_1)$ , so the choice of connections we made will realize the inversion requirement automatically. According to Eq. (4.56), if we choose the circuit resistors such that  $R_1 = R_3 = R_4 = R_5 = R$ , the output voltage is given by

$$\begin{aligned} v_o &= \left(1 + \frac{2R}{R_2}\right)(v_2 - v_1) \\ &= \left(1 + \frac{2R}{R_2}\right)(V_b - V_a) = -\left(1 + \frac{2R}{R_2}\right)(V_a - V_b). \end{aligned}$$

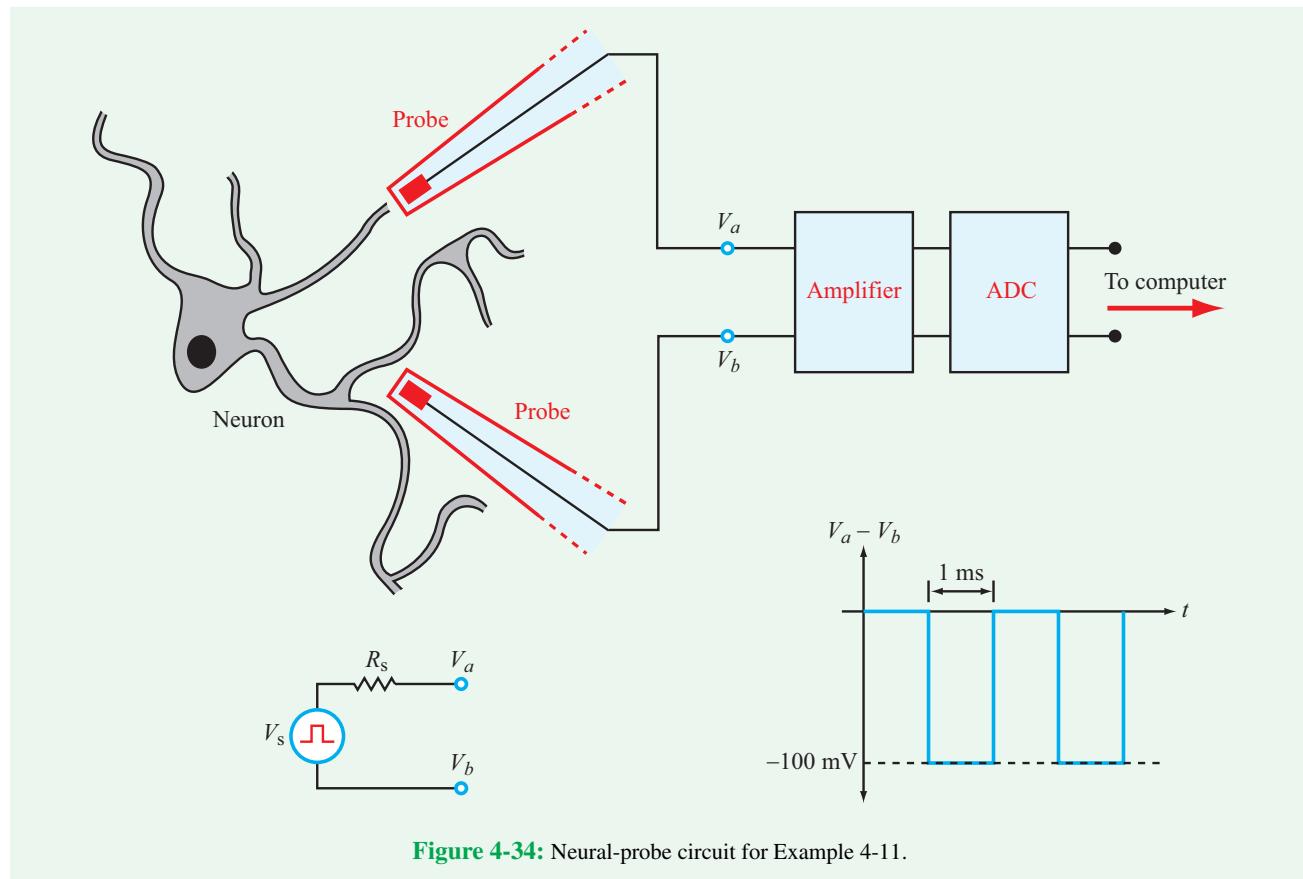
To amplify  $(V_a - V_b)$  from  $-100 \text{ mV}$  to  $+5 \text{ V}$ , the ratio  $(R/R_2)$  should be chosen such that

$$5 = -\left(1 + \frac{2R}{R_2}\right) \times (-100 \times 10^{-3})$$

or, equivalently,

$$\frac{R}{R_2} = 24.5.$$

If we set  $R = 100 \text{ k}\Omega$ , then  $R_2$  should be  $4.08 \text{ k}\Omega$ . This will yield a 5 V pulse to the ADC every time a  $-100 \text{ mV}$  pulse is generated by the neuron.



**Figure 4-34:** Neural-probe circuit for Example 4-11.

## 4-13 Multisim Analysis

One of the most attractive features of Multisim is its interactive-simulation mode, which we began to utilize in Sections 2-7 and 3-8. The simulation mode allows you to connect virtual test instruments to your circuit and to operate them in real time as Multisim simulates the circuit behavior. In this section, we will explore this feature with an op-amp circuit and two MOSFET circuits.

### 4-13.1 Op Amps and Virtual Instruments

The circuit shown in **Fig. 4-35** uses a resistive Wheatstone bridge (Section 2-5) to detect the change of resistance induced in a sensor modeled as a variable resistor (see Technology Brief 4 on resistive sensors). The output of the bridge is fed into a pair of voltage followers and then into a differential amplifier. The circuit can be constructed and tested in Multisim using the components listed in **Table 4-5**. The resistance value of the potentiometer component is adjustable with a keystroke

(the default is the key “a” to change the resistance in one direction and the default key combination Shift-a to change the resistance in the opposite direction) or by using the mouse slider under the component. In order to observe how changes in the potentiometer cause changes in the output, we need to connect the output to an **oscilloscope**. Multisim provides several oscilloscopes to choose from, including a generic instrument and virtual versions of commercial oscilloscopes made by Agilent and Tektronix. For starters, it is easiest to use the generic instrument by selecting **Simulate → Instruments → Oscilloscope**, or by selecting and dragging an oscilloscope from the instrument dock. **Figure 4-36** shows the complete circuit drawn in Multisim. The power supplies for the op amps can be found under **Components → Sources → POWER SOURCES → VDD (or VSS)**. Once placed, double-click the VDD (or VSS) component, select the values tab and set the voltage to 15 V for VDD and -15 V for VSS. Once the circuit is complete, you can begin the simulation by pressing F5 (or **Simulate → Run**) and pause it by pressing F6. Double-click on the oscilloscope element in the schematic to bring up the

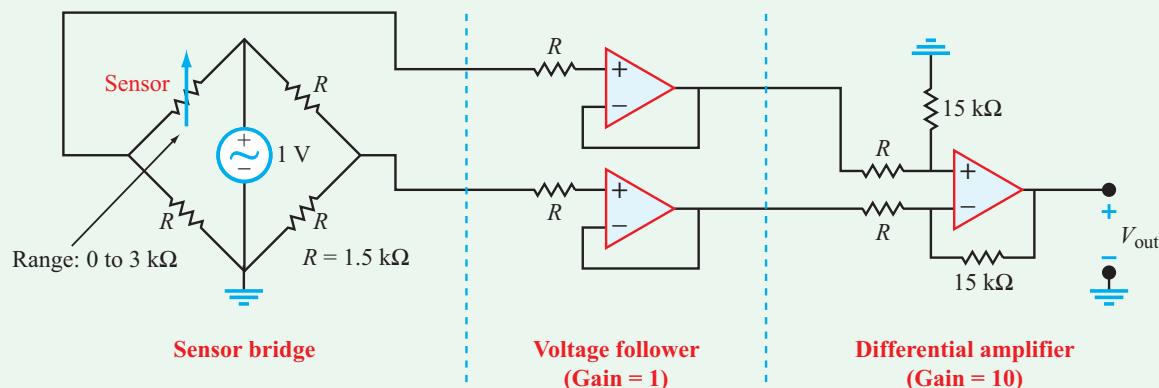


Figure 4-35: Wheatstone-bridge op-amp circuit.

oscilloscope's screen. The output voltage should be visible as Channel A in the oscilloscope window. In order to get a good view of the trace, you might need to adjust both its timebase and voltage scale using the controls found at the bottom of the Oscilloscope window. Observe the change in the amplitude of the output by shifting the resistance value of the sensor potentiometer.

With Multisim, you can modify different parts of the circuit and observe the consequent changes in behavior. Make sure to stop your simulation (not just pause it) before changing components or wiring.

**Concept Question 4-22:** What types of Multisim instruments are available for testing a circuit? (See [CAD](#))

**Concept Question 4-23:** Explain what the timebase is on the oscilloscope. (See [CAD](#))

**Exercise 4-12:** Why are the voltage followers necessary in the circuit of Fig. 4-36? Remove them from the Multisim circuit and connect the resistive bridge directly to the two inputs of the differential amplifier. How does the output vary with the potentiometer setting?

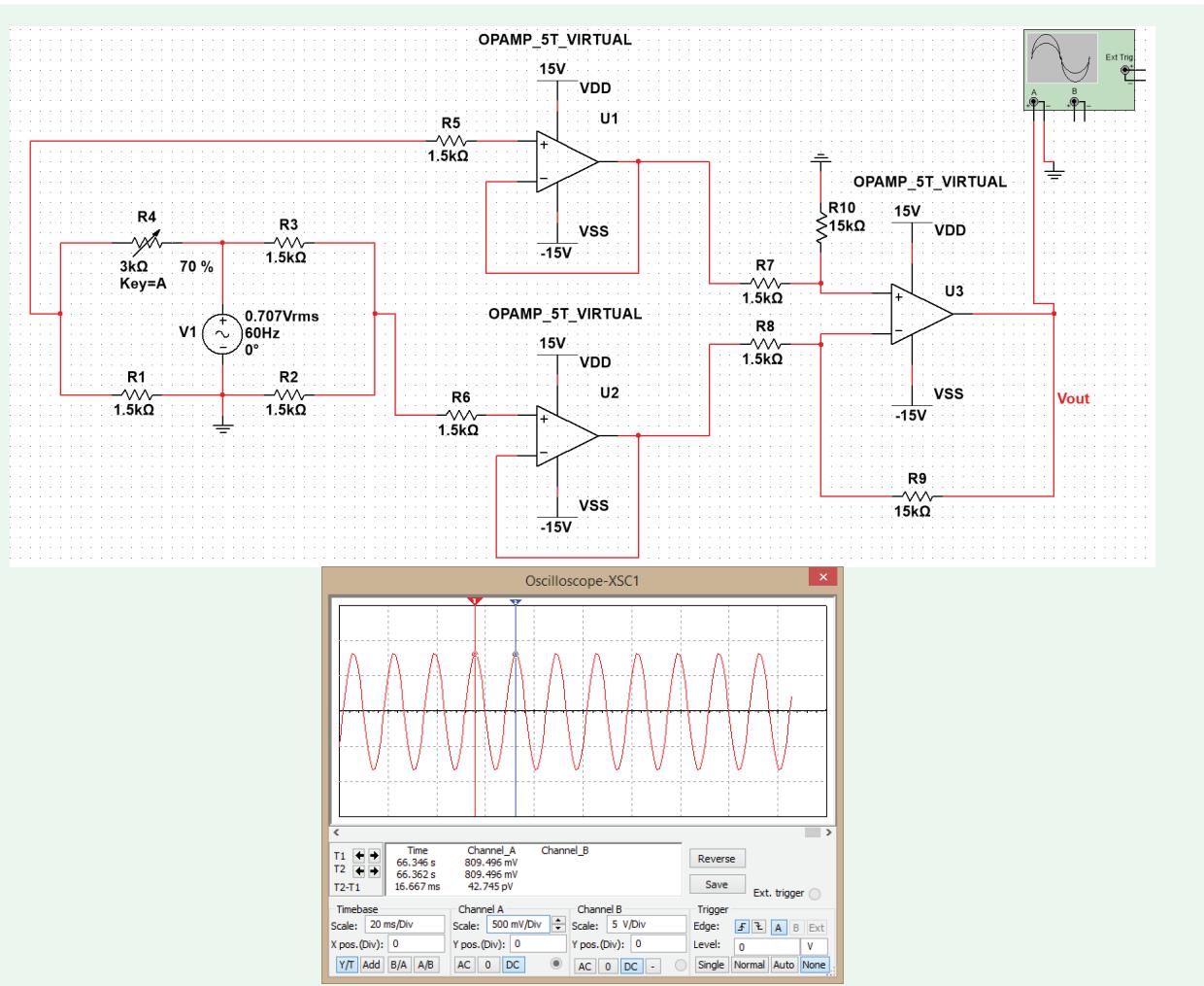
**Answer:** (See [CAD](#))

#### 4-13.2 The Digital Inverter

The MOSFET inverter introduced in Section 4-11.2 provides a good opportunity to explore the difference between steady-state and time-dependent analysis techniques. Consider again the MOSFET digital inverter of Fig. 4-30. When analyzing this type of logic gate, we usually are interested in both the response of the output voltage to a change in input voltage and in how fast the gate generates the output voltage in response to a change in input voltage. Both types of analyses are possible with Multisim.

Table 4-5: List of Multisim components for the circuit in Fig. 4-35.

Component	Group	Family	Quantity	Description
1.5 k	Basic	Resistor	7	1.5 kΩ resistor
15 k	Basic	Resistor	2	15 kΩ resistor
3 k	Basic	Variable resistor	1	3 kΩ resistor
OP_AMP_5T_VIRTUAL	Analog	Analog_Virtual	3	Ideal op amp with 5 terminals
AC_POWER	Sources	Power_Sources	1	1 V ac source, 60 Hz
VDD	Sources	Power_Sources	1	15 V supply
VSS	Sources	Power_Sources	1	-15 V supply



**Figure 4-36:** Multisim window of the circuit of Fig. 4-35. The oscilloscope trace shows the 60 Hz waveform of the output voltage. Had the voltage source been a dc source, the oscilloscope trace would have been a horizontal line.

**Figure 4-37** shows a MOSFET inverter circuit in Multisim. To draw this circuit, you need the components listed in **Table 4-6**.

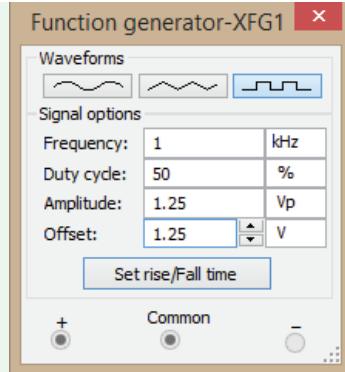
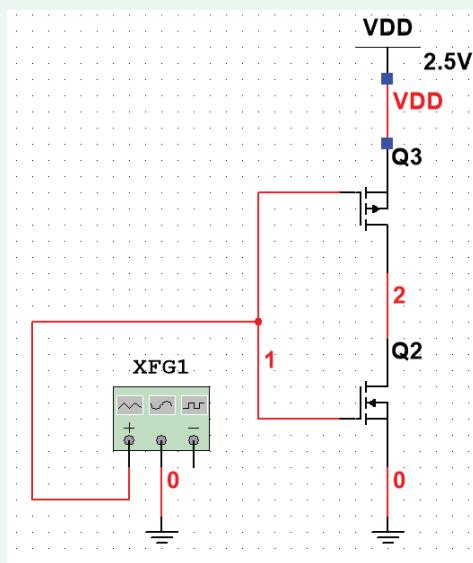
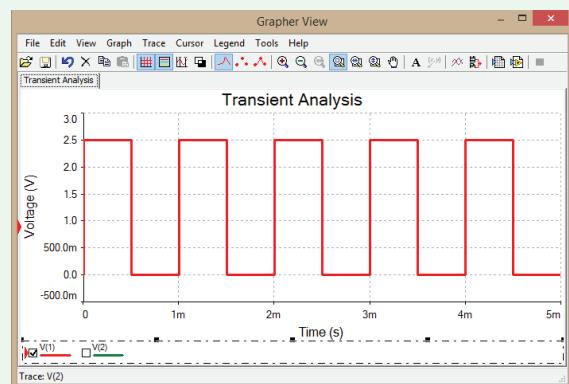
#### Transient Analysis

We can use a function generator (**Simulate** → **Instruments** → **Function Generator**) to observe the inverter output as a function of time. Double-click on the function generator to bring up its control window. Set the function generator to **Square Wave** mode with a frequency of 1 kHz, amplitude of 2.5 V,

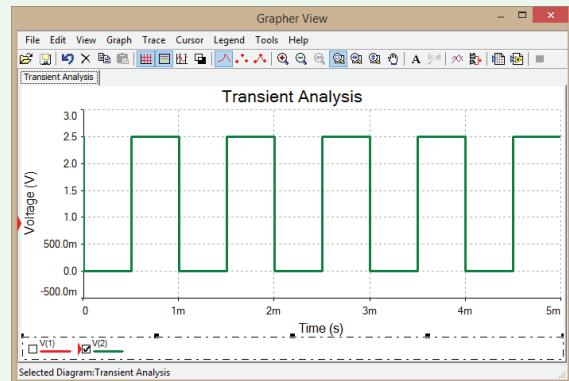
and an offset of 1.25 V. This will generate a 0–2.5 V square-wave input. The input and output can be plotted separately as a function of time using **Simulate** → **Analyses** → **Transient Analysis**. Whereas in Interactive Simulation the course of time is open ended (by default it is limited to a duration of  $1 \times 10^{30}$  s), when using Transient Analysis we can define the start and stop times. Maintain the start time at 0 s, set the final time to 0.005 s, and under the **Output** tab select the input voltage V(1) as the voltage to plot. Click **Simulate**. The input voltage is plotted as a function of time, as in **Fig. 4-38(a)**. Repeat the simulation after removing V(1) and adding V(2) under the **Output** tab.

**Table 4-6:** Components for the circuit in Fig. 4-37.

Component	Group	Family	Quantity	Description
MOS_N	Transistors	Transistors_VIRTUAL	1	3-terminal N-MOSFET
MOS_P	Transistors	Transistors_VIRTUAL	1	3-terminal P-MOSFET
VDD	Sources	Power Sources	1	2.5 V supply
GND	Sources	Power Sources	2	Ground node

**Figure 4-37:** Multisim equivalent of the MOSFET circuit of Fig. 4-30.

(a) Input voltage



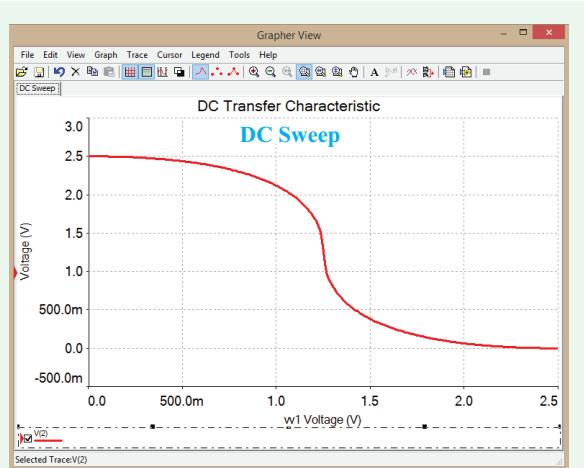
(b) Output voltage

**Figure 4-38:** Input and output voltages V(1) and V(2) in the circuit of Fig. 4-37 as a function of time.

**Figure 4-38(b)** shows the output voltage as a function of time. The input and output plots are essentially mirror images of one another.

### Steady-State Analysis

In order to analyze the steady-state output behavior, we first must remove the function generator and replace it with a



**Figure 4-39:** Output response of the MOSFET inverter circuit of Fig. 4-37 as a function of the amplitude of the input voltage.

dc voltage source. The actual voltage value of the source is unimportant. Once wired, select **Simulate** → **Analyses** → **DC Sweep**. This analysis is similar to the **DC Operating Point Analysis**, but it sweeps through a range of voltages at a node of your choice and solves for the resultant steady-state voltage (or current) at any other node you select. In this way, you can generate and plot input-output relationships for circuits and components.

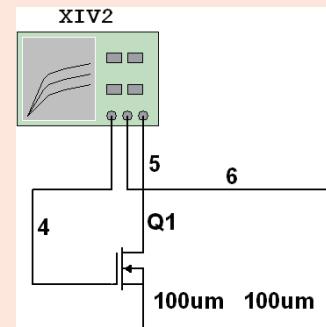
Choose the source name **vv1** as the input and enter 0 V, 2.5 V, and 0.01 V for the **start**, **stop**, and **increment** values, respectively. Under the **Output** tab, select the output voltage **V(2)** as the voltage to plot. Click **Simulate**. **Figure 4-39** shows that the output displays the expected inverter behavior: an input in the 0 to 500 mV range generates an output of  $\sim 2.5$  V; conversely, when the input is in the range between 2 and 2.5 V, the circuit generates an output voltage of  $\sim 0$  V. In between, we see a gradual transition zone.

**Concept Question 4-24:** How do the **DC Operating Point Analysis**, **Transient Analysis**, and **DC Sweep** analyses differ? (See **CAD**)

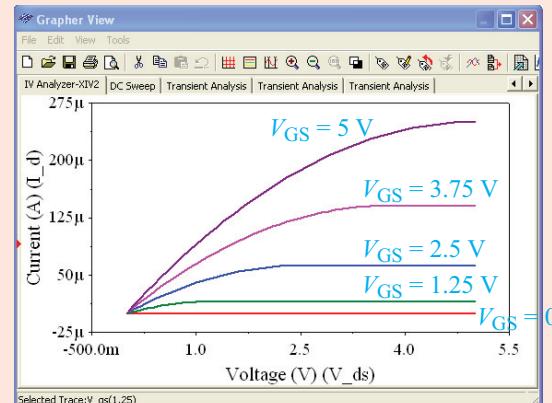
**Concept Question 4-25:** How many types of waveforms can the generic function-generator instrument provide? (See **CAD**)

**Exercise 4-13:** The **IV Analyzer** is another useful Multisim instrument for analyzing circuit performance. To demonstrate its utility, let us use it to generate characteristic curves for an NMOS transistor similar to those in **Fig. 4-28(b)**. **Figure E4.13(a)** shows an NMOS connected to an IV Analyzer. The instrument sweeps through a range of gate (G) voltages and generates a current-versus-voltage (IV) plot between the drain (D) and source (S) for each gate voltage. Show that the display of the IV analyzer is the same as that shown in **Fig. E4.13(b)**.

**Answer:** (See **CAD**)



(a)



(b)

**Figure E4.13** (a) Circuit schematic and (b) IV analyzer traces for  $I_{DS}$  versus  $V_{DS}$  at selected values of  $V_{GS}$ .

## Summary

### Concepts

- Despite its complex circuit architecture, the op amp can be modeled in terms of a relatively simple, linear equivalent circuit.
- The ideal op amp has infinite gain  $A$ , infinite input resistance  $R_i$ , and zero output resistance  $R_o$ .
- Through resistive feedback connections between its output and its two inputs, the op amp can be made to amplify, sum, and subtract multiple input signals.
- Multistage op-amp circuits can be configured to support a variety of signal-processing functions.

- Cascaded circuit blocks can be analyzed or designed individually and then combined together if  $R_o$  of the first circuit is much smaller than  $R_i$  of the second circuit.
- Buffers are used to increase  $R_i$  of the followup circuit.
- The instrumentation amplifier is a high-gain, high-sensitivity detector of small signals, making it particularly suitable for sensing deviations from reference conditions.
- Multisim can accommodate op-amp circuits and simulate their input-output responses.

### Mathematical and Physical Models

**Ideal op amp**

$$\begin{aligned}v_p &= v_n \\i_p &= i_n = 0\end{aligned}$$

**Noninverting amp\***

$$G = \frac{v_o}{v_s} = \frac{R_1 + R_2}{R_2}$$

**Inverting amp\***

$$G = \frac{v_o}{v_s} = -\left(\frac{R_f}{R_s}\right)$$

**Summing amp\***

$$v_o = -R_f \left( \frac{v_1}{R_1} + \frac{v_2}{R_2} \right)$$

**Difference amp\***

$$v_o = G_2 v_2 + G_1 v_1$$

**Voltage follower\***

$$v_o = v_s$$

**Instrumentation amp**

$$v_o = \left(1 + \frac{2R}{R_2}\right) (v_2 - v_1) \quad (\text{with gain-control resistor } R_2)$$

**MOSFET**

$$V_{out} = V_{DD} - g R_D V_{in}$$

\*See Table 4-3.

### Important Terms

Provide definitions or explain the meaning of the following terms:

action potential  
ADC  
adder  
bit  
buffer  
circuit gain  
closed-loop gain  
CMOS  
complementary MOS  
current constraint  
difference amplifier  
digital inverter  
digital-to-analog converter  
DIP configuration  
drain  
dynamic range  
feedback  
feedback resistance  
gain-control resistance

gate  
ideal op-amp current constraint  
ideal op-amp voltage constraint  
input resistance  
input source resistance  
instrumentation amplifier  
inverter  
inverting  
inverting adder  
inverting amplifier  
inverting input  
inverting summing amplifier  
IV Analyzer  
least significant bit  
linear  
linear dynamic range  
loading

metal-oxide semiconductor field-effect transistor  
MOSFET  
MOSFET gain constant  
most significant bit  
negative feedback  
negative saturation  
neural interface  
neural probe  
neuron  
NMOS  
noninverting amplifier  
noninverting  
noninverting input  
noninverting summing amplifier  
oscilloscope  
op amp  
op-amp gain  
open-loop gain

operational amplifier  
output resistance  
overloading  
percent clipping  
PMOS  
positive feedback  
positive saturation  
 $R-2R$  ladder  
saturation threshold value  
scaled inverting adder  
sensor  
signal-processing circuit  
source  
subtraction  
summing amplifier  
unity gain amplifier  
voltage constraint  
voltage follower  
voltage rails

## PROBLEMS

### Sections 4-1 and 4-2: Op-Amp Characteristics and Negative Feedback

**4.1** An op amp with an open-loop gain of  $6 \times 10^5$  and  $V_{cc} = 10$  V has an output voltage of 3 V. If the voltage at the inverting input is  $-2 \mu\text{V}$ , what is the magnitude of the noninverting-input voltage?

\* **4.2** An op amp with an open-loop gain of  $10^6$  and  $V_{cc} = 12$  V has an inverting-input voltage of  $20 \mu\text{V}$  and a noninverting-input voltage of  $10 \mu\text{V}$ . What is its output voltage?

**4.3** With its noninverting-input voltage at  $10 \mu\text{V}$ , the output voltage of an op amp is  $-15$  V. If  $A = 5 \times 10^5$  and  $V_{cc} = 15$  V, can you determine the magnitude of the inverting-input voltage? If not, can you determine its possible range?

\* **4.4** What is the output voltage for an op amp whose noninverting input is connected to ground and its inverting-input voltage is 4 mV? Assume that the op-amp open-loop gain is  $2 \times 10^5$  and its supply voltage is  $V_{cc} = 10$  V.

**4.5** For the op-amp circuit shown in Fig. P4.5:

- Use the model given in Fig. 4-6 to develop an expression for the current gain  $G_i = i_L/i_s$ .
- Simplify the expression by applying the ideal op-amp model (taking  $A \rightarrow \infty$ ,  $R_i \rightarrow \infty$ , and  $R_o \rightarrow 0$ ).

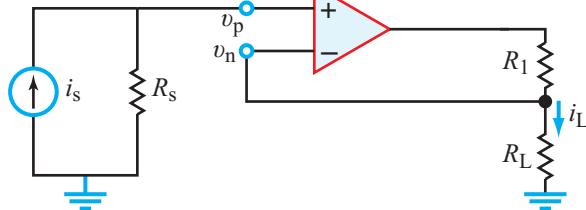


Figure P4.5 Circuit for Problem 4.5.

**4.6** The inverting-amplifier circuit shown in Fig. P4.6 uses a resistor  $R_f$  to provide feedback from the output terminal to the inverting-input terminal.

- Use the equivalent-circuit model of Fig. 4-6 to obtain an expression for the closed-loop gain  $G = v_o/v_s$  in terms of  $R_s$ ,  $R_i$ ,  $R_o$ ,  $R_L$ ,  $R_f$ , and  $A$ .
- Determine the value of  $G$  for  $R_s = 10 \Omega$ ,  $R_i = 10 \text{ M}\Omega$ ,  $R_f = 1 \text{ k}\Omega$ ,  $R_o = 50 \Omega$ ,  $R_L = 1 \text{ k}\Omega$ , and  $A = 10^6$ .
- Simplify the expression for  $G$  obtained in (a) by letting  $A \rightarrow \infty$ ,  $R_i \rightarrow \infty$ , and  $R_o \rightarrow 0$  (ideal op-amp model).

\*(d) Evaluate the approximate expression obtained in (c) and compare the result with the value obtained in (b).

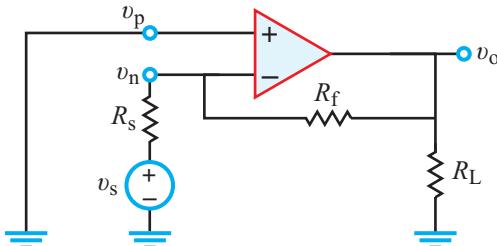


Figure P4.6 Circuit for Problem 4.6.

**4.7** For the circuit in Fig. P4.7:

- Use the op-amp equivalent-circuit model to develop an expression for  $G = v_o/v_s$ .
- Simplify the expression by applying the ideal op-amp model parameters, namely  $A \rightarrow \infty$ ,  $R_i \rightarrow \infty$ , and  $R_o \rightarrow 0$ .

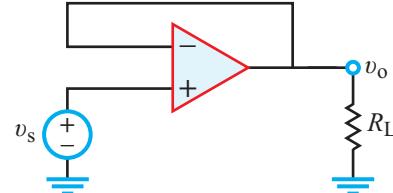


Figure P4.7 Circuit for Problem 4.7.

**4.8** The op-amp circuit shown in Fig. P4.8 has a constant dc voltage of 6 V at the noninverting input. The inverting input is the sum of two voltage sources consisting of a 6 V dc source and a small time-varying signal  $v_s$ .

- Use the op-amp equivalent-circuit model given in Fig. 4-6 to develop an expression for  $v_o$ .
- Simplify the expression by applying the ideal op-amp model, which lets  $A \rightarrow \infty$ ,  $R_i \rightarrow \infty$ , and  $R_o \rightarrow 0$ .

\* Answer(s) available in Appendix G.

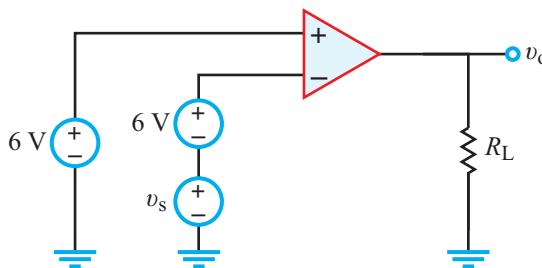


Figure P4.8 Circuit for Problem 4.8.

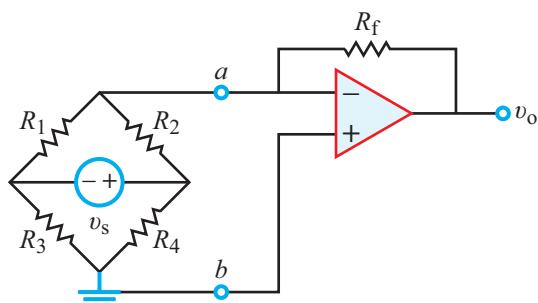


Figure P4.10 Circuit for Problem 4.10.

### Sections 4-3 and 4-4: Ideal Op Amp and Inverting Amp

Assume all op amps to be ideal from here on forward.

- \***4.9** The supply voltage of the op amp in the circuit of Fig. P4.9 is 16 V. If  $R_L = 3 \text{ k}\Omega$ , assign a resistance value to  $R_f$  so that the circuit would deliver 75 mW of power to  $R_L$ .

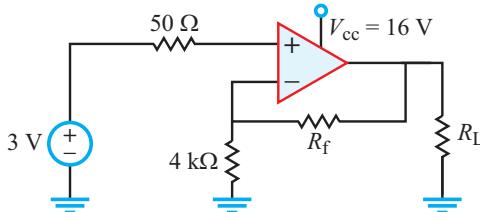


Figure P4.9 Circuit for Problem 4.9.

- 4.10** In the circuit of Fig. P4.10, a bridge circuit is connected at the input side of an inverting op-amp circuit.

- (a) Obtain the Thévenin equivalent at terminals (a, b) for the bridge circuit.
- (b) Use the result in (a) to obtain an expression for  $G = v_o/v_s$ .
- (c) Evaluate  $G$  for  $R_1 = R_4 = 100 \Omega$ ,  $R_2 = R_3 = 101 \Omega$ , and  $R_f = 100 \text{ k}\Omega$ .

- 4.11** Determine the output voltage for the circuit in Fig. P4.11 and specify the linear range for  $v_s$ , given that  $V_{cc} = 15 \text{ V}$  and  $V_0 = 0$ .

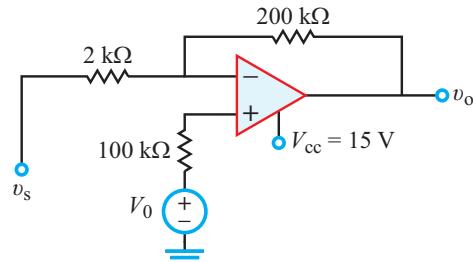


Figure P4.11 Circuit for Problems 4.11 and 4.12.

- 4.12** Repeat Problem 4.11 for  $V_0 = 0.1 \text{ V}$ .

- \***4.13** Obtain an expression for the voltage gain  $G = v_o/v_s$  for the circuit in Fig. P4.13.

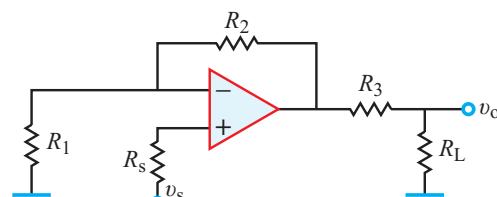


Figure P4.13 Circuit for Problem 4.13.

- 4.14** For the op-amp circuit shown in Fig. P4.14:

- (a) Obtain an expression for the current gain  $G_i = i_L/i_s$ .

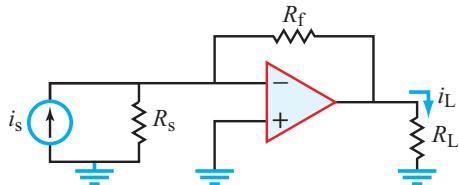


Figure P4.14 Circuit for Problem 4.14.

\*(b) If  $R_L = 12 \text{ k}\Omega$ , choose  $R_f$  so that  $G_i = -15$ .

\* 4.15 For the circuit of Fig. P4.15, what should the resistance value of  $R_L$  be so as to have maximum transfer of power into it?

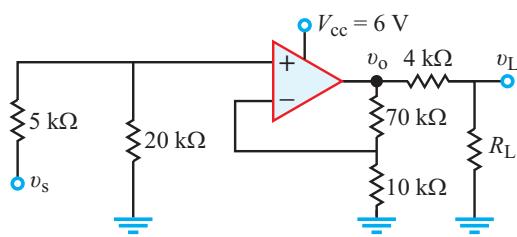


Figure P4.15 Circuit for Problems 4.15 and 4.16.

4.16 Determine the gain  $G = v_L/v_s$  for the circuit in Fig. P4.15 and specify the linear range of  $v_s$  for  $R_L = 4 \text{ k}\Omega$ .

4.17 Determine  $v_o$  across the  $10 \text{ k}\Omega$  resistor in the circuit of Fig. P4.17.

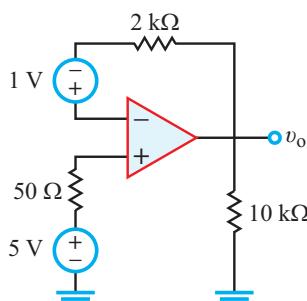


Figure P4.17 Circuit for Problem 4.17.

4.18 Evaluate  $G = v_o/v_s$  for the circuit in Fig. P4.18, and specify the linear range of  $v_s$ . Assume  $R_f = 2400 \Omega$ .

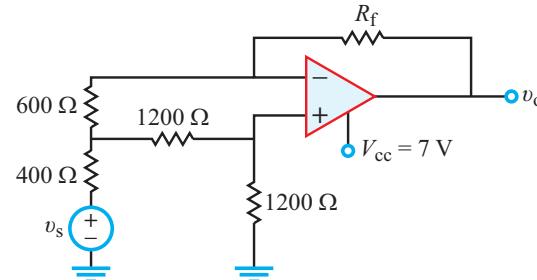


Figure P4.18 Circuit for Problems 4.18 and 4.19.

\* 4.19 Repeat Problem 4.18 for  $R_f = 0$ .

4.20 Determine the linear range of the source  $v_s$  in the circuit of Fig. P4.20.

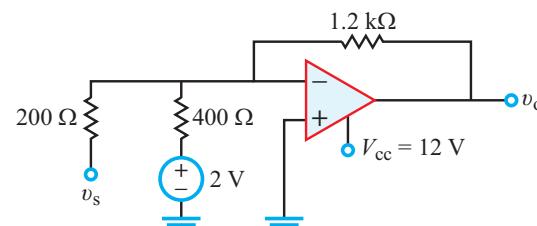


Figure P4.20 Circuit for Problems 4.20 and 4.21.

\* 4.21 Repeat Problem 4.20 after replacing the 2 V dc source in Fig. P4.20 with a short circuit.

4.22 The circuit in Fig. P4.22 uses a potentiometer whose total resistance is  $R = 10 \text{ k}\Omega$  with the upper section being  $\beta R$  and the bottom section  $(1 - \beta)R$ . The stylus can change  $\beta$  from 0 to 0.9. Obtain an expression for  $G = v_o/v_s$  in terms of  $\beta$  and evaluate the range of  $G$  (as  $\beta$  is varied over its own allowable range).

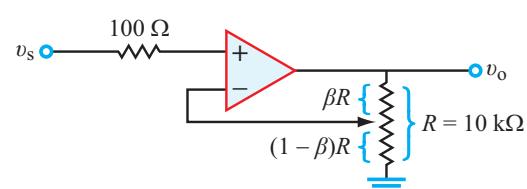


Figure P4.22 Circuit for Problem 4.22.

\* 4.23 Find the value of  $v_o$  in the circuit in Fig. P4.23.

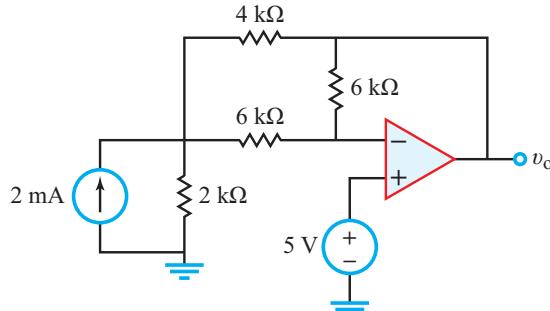


Figure P4.23 Circuit for Problem 4.23.

4.24 For the circuit in Fig. P4.24, obtain an expression for voltage gain  $G = v_o/v_s$ .

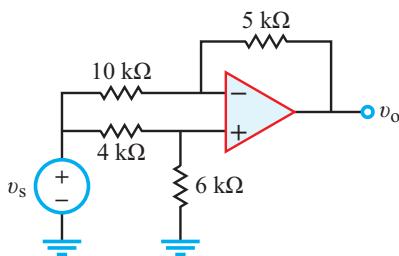


Figure P4.24 Circuit for Problem 4.24.

4.25 Determine the linear range of  $v_s$  for the circuit in Fig. P4.25.

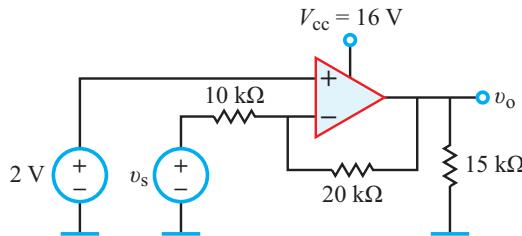


Figure P4.25 Circuit for Problem 4.25.

### Sections 4-5 and 4-6: Summing and Difference Amplifiers

4.26 If  $R_2 = 4 \text{ k}\Omega$ , select values for  $R_{s1}$ ,  $R_{s2}$ , and  $R_1$  in the circuit of Fig. 4-15 so that  $v_o = 3v_1 + 5v_2$ .

4.27 Design an op-amp circuit that performs an averaging operation of five inputs  $v_1$  to  $v_5$ .

4.28 For the circuit in Fig. P4.28, generate a plot for  $v_L$  as a function of  $v_s$  over the full linear range of  $v_s$ .

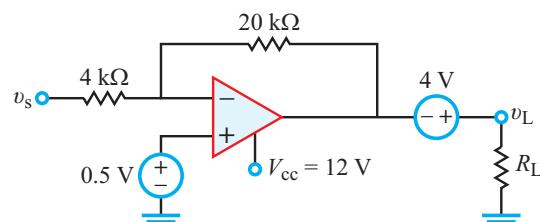


Figure P4.28 Circuit for Problem 4.28.

4.29 Relate  $v_o$  in the circuit of Fig. P4.29 to  $v_s$  and specify the linear range of  $v_s$ . Assume  $V_0 = 0$ .

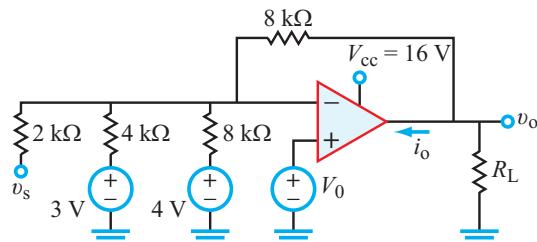


Figure P4.29 Circuit for Problems 4.29 through 4.31.

\* 4.30 Repeat Problem 4.29 for  $V_0 = 6 \text{ V}$ .

4.31 Determine the current  $i_o$  flowing into the op-amp of the circuit in Fig. P4.29 under the conditions  $v_s = 0.5 \text{ V}$ ,  $V_0 = 0$ , and  $R_L = 10 \text{ k}\Omega$ .

4.32 Design a circuit containing a single op amp that can perform the operation  $v_o = 3 \times 10^4(i_2 - i_1)$ , where  $i_2$  and  $i_1$  are input current sources.

4.33 Design a circuit that can perform the operation  $v_o = 3v_1 + 4v_2 - 5v_3 - 8v_4$ , where  $v_1$  to  $v_4$  are input voltage signals.

**4.34** Relate  $v_o$  in the circuit of Fig. P4.34 to  $v_1$ ,  $v_2$ , and  $v_3$ .

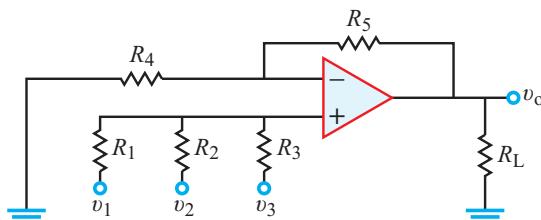


Figure P4.34 Circuit for Problem 4.34.

\* **4.35** For the circuit in Fig. P4.35, obtain an expression for  $v_o$  in terms of  $v_1$ ,  $v_2$ , and the four resistors. Evaluate  $v_o$  if  $v_1 = 0.1$  V,  $v_2 = 0.5$  V,  $R_1 = 100 \Omega$ ,  $R_2 = 200 \Omega$ ,  $R_3 = 2.4 \text{ k}\Omega$ , and  $R_4 = 1.2 \text{ k}\Omega$ .

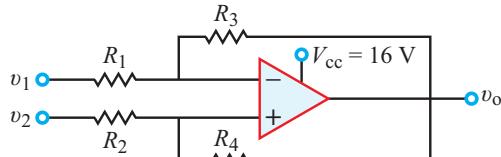


Figure P4.35 Circuit for Problem 4.35.

**4.36** Find the value of  $v_o$  in the circuit in Fig. P4.36.

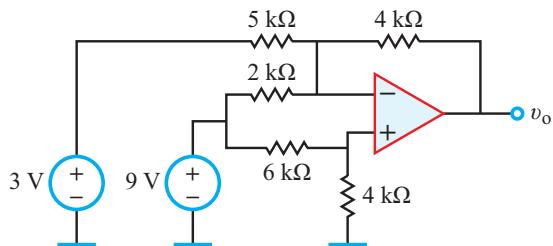


Figure P4.36 Circuit for Problem 4.36.

**4.37** Find the range of  $R_f$  for which the op amp in the circuit of Fig. P4.37 does not saturate.

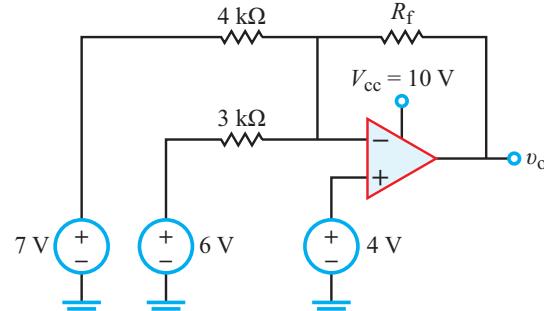


Figure P4.37 Circuit for Problem 4.37.

\* **4.38** Determine  $v_o$  and the power dissipated in  $R_L$  in the circuit of Fig. P4.38.

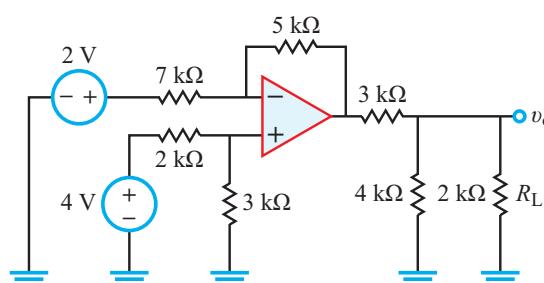


Figure P4.38 Circuit for Problem 4.38.

**4.39** The circuit in Fig. P4.39 contains two single-pole single-throw switches,  $S_1$  and  $S_2$ . Determine the closed-circuit gain  $G = v_o/v_s$  for each of the four possible closed/open switch combinations.

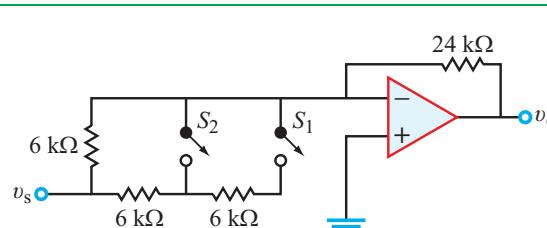
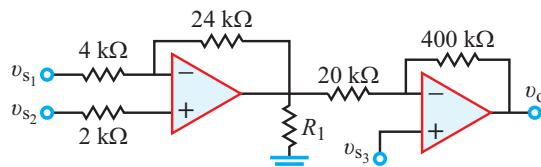


Figure P4.39 Circuit for Problem 4.39.

### Section 4-8: Op-Amp Signal-Processing Circuits

**4.40** Develop a block-diagram representation for the circuit in **Fig. P4.40** for  $v_{s_2} = v_{s_3} = 0$  and

- \*(a)  $R_1 = \text{open circuit}$
- (b)  $R_1 = 10 \text{ k}\Omega$ .



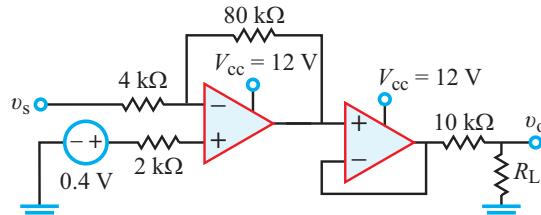
**Figure P4.40** Circuit for Problems 4.40 through 4.42.

**4.41** Develop a block-diagram representation for the circuit in **Fig. P4.40** for  $v_{s_2} = 0$  and  $R_1 = \infty$ .

**4.42** Develop a block-diagram representation for the circuit in **Fig. P4.40** for  $v_{s_3} = 0$  and  $R_1 = \infty$ .

**4.43** For the circuit in **Fig. P4.43**:

- (a) Develop a block-diagram representation with  $R_L$  as a variable parameter.
- (b) Specify the linear range of  $v_s$ .
- (c) Determine  $v_o$  for  $v_s = 0.3 \text{ V}$  and  $R_L = 10 \text{ k}\Omega$ .

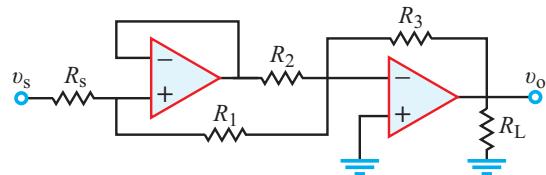


**Figure P4.43** Circuit for Problem 4.43.

**4.44** Design an op-amp circuit that can perform the operation  $v_o = 4v_{s_1} - 3v_{s_2}$ , while simultaneously presenting an input resistance of  $10 \text{ k}\Omega$  on the input side for source  $v_{s_1}$  and an input resistance of  $5 \text{ k}\Omega$  on the input side for source  $v_{s_2}$ .

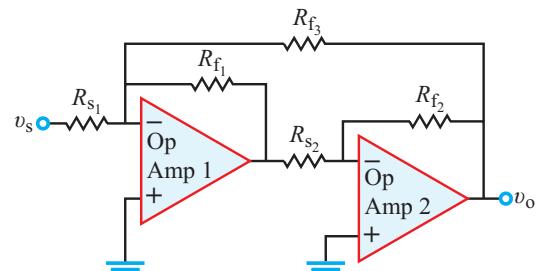
**4.45** Design an op-amp circuit that can perform the operation  $v_o = 12v_{s_1} + 3v_{s_2}$ , while simultaneously presenting an input resistance of  $50 \text{ k}\Omega$  on the input side for source  $v_{s_1}$  and an input resistance of  $25 \text{ k}\Omega$  on the input side for source  $v_{s_2}$ .

\***4.46** Relate  $v_o$  in the circuit of **Fig. P4.46** to  $v_s$ .



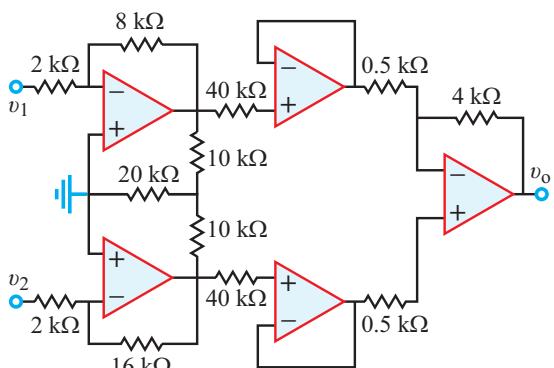
**Figure P4.46** Circuit for Problem 4.46.

**4.47** In the circuit of **Fig. P4.47**, op amp 1 receives feedback at its input from its own output as well as from the output of op amp 2. Relate  $v_o$  to  $v_s$ .



**Figure P4.47** Circuit for Problem 4.47.

**4.48** Relate  $v_o$  in the circuit of **Fig. P4.48** to  $v_1$  and  $v_2$ .



**Figure P4.48** Circuit for Problem 4.48.

**4.49** Design an op-amp circuit that can perform the operation  $i_o = (30i_1 - 8i_2 + 0.6) \text{ A}$  where  $i_1$  and  $i_2$  are input current sources.

\* 4.50 Relate the output voltage  $v_o$  in Fig. P4.50 to  $v_s$ .

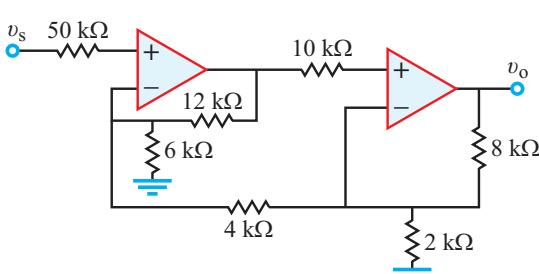


Figure P4.50 Circuit for Problem 4.50.

4.51 Solve for  $v_o$  in terms of  $v_s$  for the circuit in Fig. P4.51.

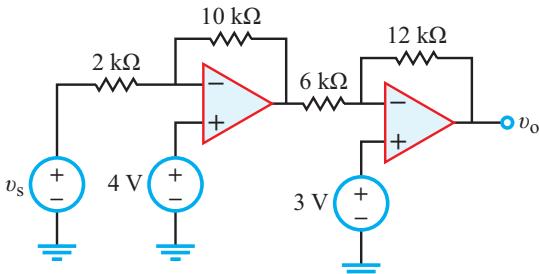


Figure P4.51 Circuit for Problem 4.51.

\* 4.52 Find the value of  $v_o$  in the circuit in Fig. P4.52.

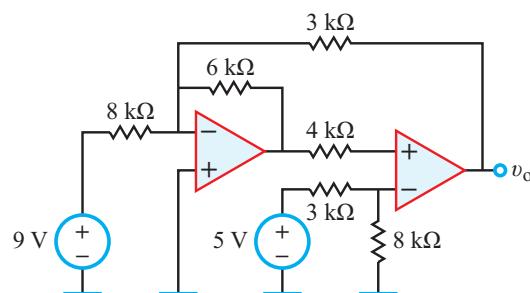


Figure P4.52 Circuit for Problem 4.52.

4.53 Solve for  $v_o$  in the circuit in Fig. P4.53.

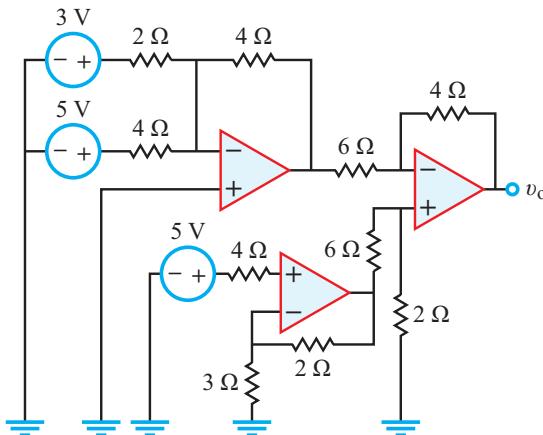


Figure P4.53 Circuit for Problem 4.53.

\* 4.54 If  $v_o = -3$  V, what is the value of  $v_s$  in the circuit in Fig. P4.54?

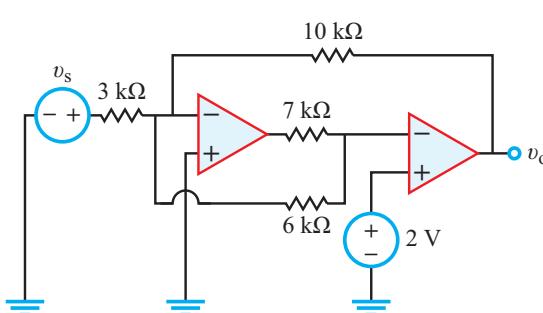


Figure P4.54 Circuit for Problem 4.54.

### Sections 4-9 and 4-10: Instrumentation Amp and D/A Converter

4.55 The instrumentation-amplifier circuit shown in Fig. 4-23 is used to measure the voltage differential  $\Delta v = v_2 - v_1$ . If the range of variation of  $\Delta v$  is from  $-10$  to  $+10$  mV and  $R_1 = R_3 = R_4 = R_5 = 100$  kΩ, choose  $R_2$  so that the corresponding range of  $v_o$  is from  $-5$  to  $+5$  V.

\* 4.56 An instrumentation amplifier with  $R_1 = R_3 = 10$  kΩ,  $R_4 = 1$  MΩ, and  $R_5 = 1$  kΩ uses a potentiometer for the gain-control resistor  $R_2$ . If the potentiometer resistance can be varied

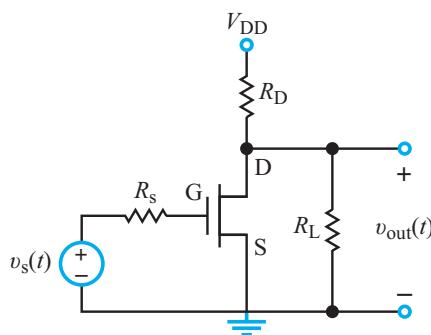
between 10 and 100  $\Omega$ , what is the corresponding variation of the circuit gain  $G = v_o/(v_2 - v_1)$ ?

**4.57** Design a five-bit DAC using a circuit configuration similar to that in [Fig. 4-25](#).

**4.58** Design a six-bit DAC using a  $R-2R$  ladder configuration.

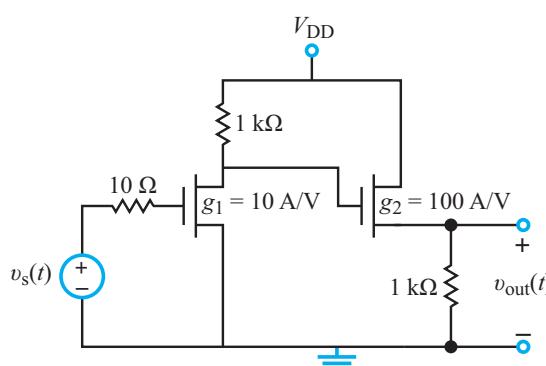
### Section 4-11: MOSFET

**4.59** In Example 4-9, we analyzed a common-source amplifier without a load resistance. Consider the amplifier in [Fig. P4.59](#); it is identical to the circuit in [Fig. 4-31](#), except that we have added a load resistor  $R_L$ . Obtain an expression for  $v_{out}$  as a function of  $v_s$ .



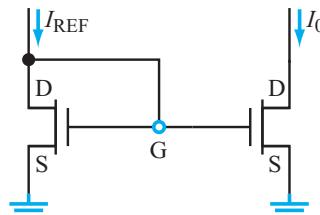
**Figure P4.59** MOSFET circuit for Problem 4.59.

\***4.60** Determine  $v_{out}(t)$  as a function of  $v_s(t)$  for the circuit in [Fig. P4.60](#). Assume  $V_{DD} = 2.5$  V.



**Figure P4.60** Two-MOSFET circuit for Problem 4.60.

**4.61** In Problem 3.73 of Chapter 3, we analyzed a current mirror circuit containing BJTs. Current mirror circuits also can be designed using MOSFETs, as shown in [Fig. P4.61](#). Determine the relationship between  $I_0$  and  $I_{REF}$ .



**Figure P4.61** Circuit for Problem 4.61.

### Section 4-13: Multisim Analysis

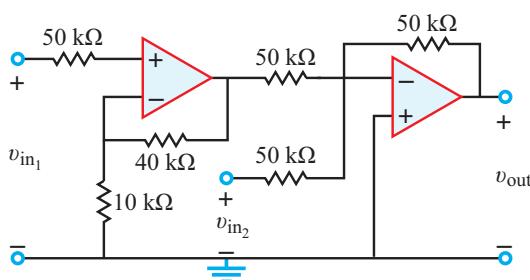
**4.62** Draw a noninverting amplifier ([Fig. 4-7](#)) with a gain of 2 in Multisim. Show that the circuit works as expected by connecting a 1 V pulse source and plotting both the input and the output voltages using the Grapher Tool and Transient Analysis. Use the 3-terminal virtual op-amp component.

**4.63** Draw an inverting amplifier ([Fig. 4-11](#)) with a gain of  $-3.5$  in Multisim. Show that the circuit works as expected by connecting a 1 V dc voltage source and solving the circuit using the DC Operating Point analysis. Use the 3-terminal virtual op-amp component.

**4.64** In Multisim, draw a summing amplifier that adds the values of four different dc voltage sources, each with an inverting gain of 4. Use the DC Operating Point analysis tool to verify the circuit performance.

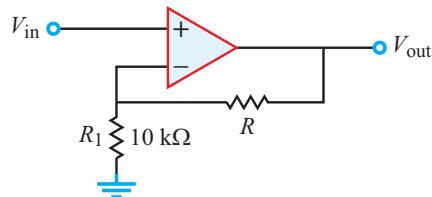
**4.65** In Multisim, draw a noninverting summing amplifier that adds the values of three different dc voltage sources  $V_1$ ,  $V_2$ , and  $V_3$  with gains of 1, 2, and 5, respectively. Apply the DC Operating Point Solution tool to demonstrate that the circuit functions as specified.

**4.66** Draw the op-amp circuit shown in [Fig. P4.66](#) in Multisim, provide a DC Operating Point Analysis solution that demonstrates its operation, and state what function the circuit performs.



**Figure P4.66** Circuit for Problem 4.66.

**4.67** Construct the noninverting amplifier circuit shown in **Fig. P4.67** in Multisim. Set the value of  $R$  to  $50\text{ k}\Omega$  and then perform a DC Sweep analysis of the input voltage from  $-5$  to  $+5\text{ V}$ . Plot the Output. Now change the value of  $R$  to  $80\text{ k}\Omega$  and repeat the DC Sweep analysis. Compare the two plots either side by side or by overlapping them using the Overlay Traces button on the Grapher toolbar. (Use the three-terminal virtual op amp for the simulation.)



**Figure P4.67** Circuit for Problem 4.67.

**4.68** Until the 1970s, much research was carried out on analog computers (as distinguished from the digital computers found everywhere today). In fact, analog computers were one of the originally intended users of operational amplifiers. Op amps easily can be incorporated to perform many mathematical operations.

Using the basic op-amp circuits shown in this chapter, construct a circuit that expresses the following algebraic equation in voltage:

$$v = 2x - 3.5y + 0.2z,$$

where  $v$  is the output voltage and  $x$ ,  $y$ , and  $z$  are three input voltages. Once you have the circuit designed, build it in Multisim and demonstrate that the circuit behaves appropriately by giving it the following inputs:  $x = 1.2$ ,  $y = 0.4$ , and  $z = 0.9$ .

### Potpourri Questions

**4.69** Based on the information provided in **Table TT9-1** of Technology Brief 9, which types of display technologies are best suited for a large football stadium? A home TV? A cell phone screen?

**4.70** What are the limitations of today's computer memory circuits (ROM and RAM), and what emerging technologies are becoming available to improve them?

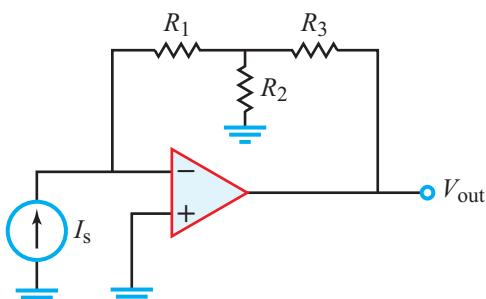
**4.71** Circuit analysis and design can be performed analytically by applying the techniques covered in this book, or they can be performed by computer simulation. Are these competing or complementary approaches? Explain.

### Integrative Problems: Analytical / Multisim / myDAQ

To master the material in this chapter, solve the following problems using three complementary approaches: (a) analytically, (b) with Multisim, and (c) by constructing the circuit and using the myDAQ interface unit to measure quantities of interest via your computer. [myDAQ tutorials and videos are available on .]

#### m4.1 Ideal Op-Amp Model:

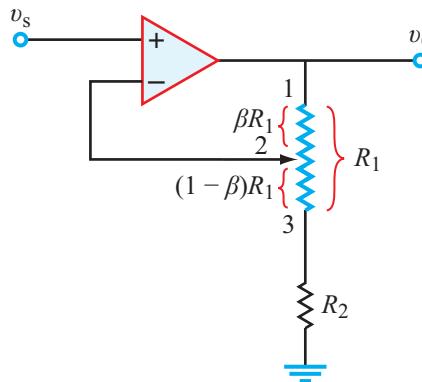
- (a) Determine a general expression for  $v_{\text{out}}$  in terms of the resistor values and  $i_s$  for the circuit of **Fig. m4.1** (no Multisim or myDAQ for this part).
- (b) Find  $V_{\text{out}}$  for these specific component values:  $R_1 = 3.3\text{ k}\Omega$ ,  $R_2 = 4.7\text{ k}\Omega$ ,  $R_3 = 1.0\text{ k}\Omega$ , and  $I_s = 1.84\text{ mA}$ .
- (c) Replace  $R_2$  with a potentiometer. Use myDAQ and the potentiometer to determine  $V_{\text{out}}$  for each of the following values of  $R_2$ :  $2.5\text{ k}\Omega$ ,  $10\text{ k}\Omega$ , and  $25\text{ k}\Omega$ .



**Figure m4.1** Circuit for Problem m4.1.

**m4.2 Noninverting Amplifier:** The circuit in **Fig. m4.2** uses a potentiometer whose total resistance is  $R_1$ . The movable stylus on terminal 2 creates two variable resistors:  $\beta R_1$  between terminals 1 and 2 and  $(1 - \beta)R_1$  between terminals 2 and 3. The movable stylus varies  $\beta$  over the range  $0 \leq \beta \leq 1$ .

- (a) Obtain an expression for  $G = v_o/v_s$  in terms of  $\beta$ .
- (b) Calculate the amplifier gain for  $\beta = 0.0$ ,  $\beta = 0.5$ , and  $\beta = 1.0$  with component values  $R_1 = 10 \text{ k}\Omega$  and  $R_2 = 1.5 \text{ k}\Omega$ .
- (c) Let  $v_s$  be a 100 Hz sinusoidal signal with a 1 V peak value. Plot  $v_o$  and  $v_s$  to scale for  $\beta = 0.0$ ,  $\beta = 0.5$ , and  $\beta = 1.0$ .



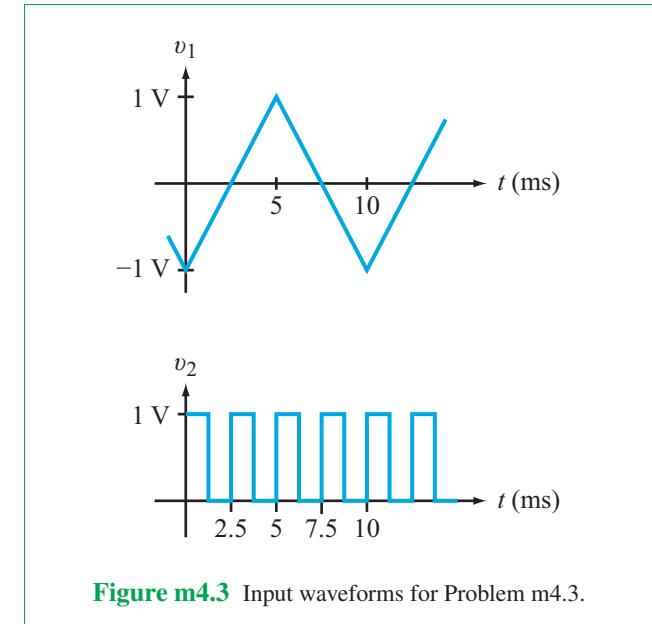
**Figure m4.2** Circuit for Problem m4.2.

### m4.3 Summing Amplifier:

- (a) Design an op-amp summing circuit that performs the operation  $v_o = -(2.14v_1 + 1.00v_2 + 0.47v_3)$ . Use not more than four standard-value resistors with values between  $10 \text{ k}\Omega$  and  $100 \text{ k}\Omega$ . Refer to the resistor parts list in Appendix A of the myDAQ tutorial on the
- (b) Draw the output waveform  $v_o$  for the input waveforms  $v_1$  and  $v_2$  shown in **Fig. m4.3** and  $v_3 = 4.7 \text{ V}$ .
- (c) State the minimum and maximum values of  $v_o$ .

### m4.4 Signal Processing Circuits:

- (a) Design a two-stage signal processor to serve as a “distortion box” for an electric guitar. The first-stage amplifier applies a variable gain magnitude in the range 13.3 to 23.3 while the second-stage amplifier attenuates the signal by 13.3, i.e., the second-stage amplifier has a fixed gain of  $1/13.3$ . Note that when the first-stage amplifier gain is 13.3 the overall distortion box gain is unity. The distortion effect relies on intentionally driving the first-stage amplifier into saturation (also called “clipping”) when its gain is higher than 13.3. Use a  $10 \text{ k}\Omega$  potentiometer and standard-value resistors in the range  $1.0 \text{ k}\Omega$  and  $100 \text{ k}\Omega$ ; see the resistor parts list in



**Figure m4.3** Input waveforms for Problem m4.3.

Appendix A of the myDAQ tutorial on the . You may combine two standard-value resistors in series to achieve the required amplifier gains.

- (b) Derive a general formula for **percent clipping** of a unit-amplitude sinusoidal test signal; this is the percent of time during one period in which the signal is clipped. The formula includes the peak sinusoidal voltage  $V_p$  that would appear at the output of the first-stage amplifier with saturation ignored and the actual maximum value  $V_s$  due to saturation.
- (c) Apply your general formula to calculate percent clipping of a 1 V peak amplitude sinusoidal signal for the potentiometer dial in three positions: fully counter-clockwise (no distortion), midscale (moderate distortion), and fully clockwise (maximum distortion). Assume the op-amp outputs saturate at  $\pm 13.5 \text{ V}$ .
- (d) Apply a 1 V peak amplitude sinusoidal signal with 100 Hz frequency to the distortion box input and plot its output for the potentiometer dial in the same three positions as above. State the maximum and minimum values of the distortion box output.

### m4.5 Multiple Op-Amp Stages:

Determine  $V_{out}$  in each of the two circuits in **Fig. m4.5**.

**m4.6 The Importance of Voltage Followers:** Suppose you are asked to design a circuit to power a certain gadget and the only source available to you is the 15 V source from your NI myDAQ. Your boss tells you that in order for the gadget to operate properly, its input voltage should be 10.3 V. Moreover, you are told that the input equivalent load resistance of the gadget is exceedingly high