You may use the following resources:

1. Textbook
2. Personal notes, graded homework assignments
3. Printouts of the course slides
4. Calculator
5. Personal laptop or in-lab computer for the following purposes ONLY:
   a. Viewing course materials on Canvas
   b. Calculator application (not in browser)
   c. Online version of the textbook
   d. MIPS references – Wikipedia or U.Idaho

Phones/smartphones are not allowed - not even for calculator apps
Use of computers for purposes other than those listed is considered cheating

EE/CS/CPE 3760 Final Exam
Winter 2020

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Begin exam at 1:00 PDT
End exam by 3:00 PDT
Email questions to the instructor.

1. A 128-byte cache is organized with 2-way set associativity and 2-word blocks. Each word is 4 bytes. Assume the addresses are 32 bits wide.

128 Byte | Set | Block | Byte
2 blocks | 2 words | 4 bytes = 8 bits

Index bits: $\log_2(2) = 3$
Block offset: $\log_2(2) = 1$
$4 + 2 + 3 = 9$ bits

a. Determine which parts of the 32-bit address are the tag, index, block and byte offset. Mark each bit in the diagram below as T, I, BL or BY.

b. A program accesses the following twelve 32-bit memory addresses (listed in binary). Identify each access as a hit or miss by circling the 'H' or 'M' to the left. Use a LRU block replacement policy.

Note: In this problem, the high-order 20 bits of the address are always zero and may be ignored.

Ignore | Tag | I | BO

H (M) 0000 0000 0000 0000 0000 0101 1010 0100
H (M) 0000 0000 0000 0000 0000 0010 0011 0010
H (M) 0000 0000 0000 0000 0000 0111 1100 1000
H (M) 0000 0000 0000 0000 0000 0000 0110 0001
(H) M 0000 0000 0000 0000 0000 0010 0011 0011
H (M) 0000 0000 0000 0000 0000 0011 0000 0100
(H) M 0000 0000 0000 0000 0000 0011 0000 0010
(H) M 0000 0000 0000 0000 0000 0101 1010 0111
(H) M 0000 0000 0000 0000 0000 0010 0011 0000
H (M) 0000 0000 0000 0000 0000 0011 0110 0110
(H) M 0000 0000 0000 0000 0000 0111 1100 1111
H (M) 0000 0000 0000 0000 0000 0000 0110 0000
H (M) 0000 0000 0000 0000 0000 0101 1010 0101

	V	Tag
000	1	01100 (LRU)
	0	
001	1	11111 (LRU)
	0	
010	0	
	0	
011	0	
	0	
100	1	00001 (LRU)
	1	10110
101	0	
	0	
110	1	01000 (LRU)
	0	
111	0	
	0	

2. a. Assume the minimum time required for each of the five stages of the original MIPS pipeline are as follows:

IF: 0.275 ns
RF: 0.250 ns
EX: 0.450 ns
M: 0.325 ns
WB: 0.260 ns

0.275+0.25+0.45+0.325+0.26 = 1.56

What is the minimum clock period for this pipelined system? 0.25 ns
What is the latency for one instruction (no stalls)? 1.56 ns
What is the throughput once the pipeline is full (no stalls)? 1 instr/cycle = 0.641 instr/ns

b. You propose to split up the execute stage into two cycles (0.300 ns each), creating a six-stage pipeline, as shown below. In the illustration, two instructions are shown in the pipeline so you can see how the stages line up.

IF: 0.275 ns
RF: 0.250 ns
EX1: 0.300 ns
EX2: 0.300 ns
M: 0.325 ns
WB: 0.260 ns

0.275+0.25+0.3+0.3+0.325+0.26 = 1.71 ns

What is the minimum clock period for this pipelined system? 0.25 ns
What is the latency for one instruction (no stalls)? 1.71 ns
What is the throughput once the pipeline is full (no stalls)? 1 instr/cycle = 0.585 instr/ns

c. With register forwarding in the original five-stage pipeline we found:
No stall on a register-to-register data hazard (read after write).
1 cycle stall for a LW hazard (read after load).
3 cycle stall for branches (when we guess wrong).

Are any of these different in the six-stage pipeline described in part b? How?

Register-to-Register Data Hazards Yes, the written register isn't written until WB, so there would be a stall to the second instruction of 3 cycles instead of just 1 in order to read from memory

Read after LW Hazard Yes, splitting the EX stage into two cycles means we need 2 cycles stalls

Branch Hazard No, it will always 3 cycle stalls if we guess incorrectly on a branch, thus this pipeline hazard is no different than the original

3. a) A virtual memory system has a 32GB virtual address space and 4GB of physical memory. Pages are 256 KB each. Determine the following:

Number of bits in virtual addresses: 35
Number of bits in physical addresses: 32
Number of bits in the page offset: 18
Number of bits in virtual page numbers: 17
Number of bits in physical page numbers: 14

b) A different system has 32-bit virtual addresses, 256 MB of physical memory and 1 MB pages. The OS has the following page table for a process (only the first eight entries are shown). Assume that all physical memory is allocated and in use.

Virtual Page Number (binary)	Valid Bit	Physical Page Number (binary)/Disk Address
0000 0000 0000	1	0111 0001
0000 0000 0001	0	sector 23...
0000 0000 0010	1	1111 0000
0000 0000 0011	0	sector 910...
0000 0000 0100	1	Sector 87...
0000 0000 0101	0	1100 1100
0000 0000 0110	1	0000 1101
0000 0000 0111	0	sector 56...

The following virtual memory addresses are accessed (read from) in the order presented. Show the physical addresses each one corresponds to. **Make sure to show any changes to the page table.** Assume that the virtual memory system uses an LRU replacement policy. Be as specific as possible in your answer.

i) 0000 0000 0101 1010 0000 1111 0000 1010 → 1100 1100

ii) 0000 0000 0010 0010 0011 0100 0101 0110 → 1111 0000

iii) 0000 0000 0110 1100 1110 1111 0111 0011 → 0000 1101

iv) 0000 0000 0000 0110 1010 0010 1100 1010 → 0111 0001

v) 0000 0000 0100 1111 0000 1110 0000 1111 → 1100 1100

4. Assemble the following MIPS assembly-language code by writing out the corresponding machine language instructions. The address of each instruction is given to the left of each instruction. Please fill out the decimal values for each field, convert to binary, and then convert the whole instruction to hexadecimal.

10000 addi $8, $9, 9

	Instruction breakdown by binary bit					
	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
Dec	8	9	8		9	
Bin	001000	01001	01000	00000	00000	001001
Hex	2	1	2	8	0	0	0	9

10004 frodo: sub $3, $4, $5

Dec	0	4	5	3	0	34		
Bin	000000	00100	00101	00011	00000	100010		
Hex	0	0	8	5	1	8	2	2

10008 sam: sll $2, $1, 7

Dec	0	0	1	2	7	0		
Bin	000000	00000	00001	00010	00011	000000		
Hex	0	0	0	1	1	1	c	0

-3

10012 beq $10, $11, frodo

Dec	4	11	10		-3			
Bin	000100	01011	01010	1111	1111	111101		
Hex	1	1	b	a	f	f	f	d

10008 / 4 = 2502

10016 j sam

Dec	2			2502				
Bin	000010	00000	00000	00000	00001	001110	000110	
Hex	0	8	0	0	0	9	c	6

$2502_{10} = 100111000110_2$

3 = 0011
-3 → 1100 + 1
→ 1101

Honor Statement

Sign the following statement before scanning and submitting your exam.

On my honor, I have neither given nor received any unauthorized aid on this exam.

Stop working by 3pm PDT. Scan in your completed exam and submit on Canvas in pdf format by 3:15pm PDT. Any issues with scanning? Just take some photos and email them to the instructor by 3:15 and submit scans later.