

- b. Improve the pipeline by adding branch prediction. Assume the branch is predicted correctly, and diagram below.

we predict branch will or won't happen so we don't stall for 4+1
 If we assume that the branch is correct, then we have no stalls in our pipeline
 Cycle

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
lw St1, 0(Sa0)	IF	RF	E	M	WB										IF	RF	E	M	WB				
beq St1, S0, targ1		IF	RF	E	M	WB									IF	RF	E	M	WB				
addi Sa0, Sa0, 4			IF	RF	E	M	WB								IF	RF	E	M	WB				
add St1, St1, St3				IF	X	RF	E	M	WB						IF	X	RF	E	M	WB			
lw St1, 0(St1)					IF	X	X	X	RF	E	M	WB					IF	X	X	X	RF		
add Sv0, Sv0, St1								IF	X	X	X	RF	E	M	WB							IF	

Still depends!

X = Stalls

- c. Further improve the pipeline by adding register forwarding. Diagram below.

Still have branch prediction
 St1 is compared in E stage

LW now comes from memory

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
lw St1, 0(Sa0)	IF	RF	E	M	WB				IF	RF	E	M	WB				IF	RF	E	M	WB		
beq St1, S0, targ1		IF	RF	E	M	WB				IF	RF	E	M	WB				IF	RF	E	M	WB	
addi Sa0, Sa0, 4			IF	RF	E	M	WB				IF	RF	E	M	WB				IF	RF	E	M	WB
add St1, St1, St3				IF	RF	E	M	WB				IF	RF	E	M	WB				IF	RF	E	M
lw St1, 0(St1)					IF	X	RF	E	M	WB			IF	X	RF	E	M	WB			IF	X	RF
add Sv0, Sv0, St1							IF	X	RF	E	M	WB			IF	X	RF	E	M	WB			IF

Stall, we depend on find

registers are found in execute stages