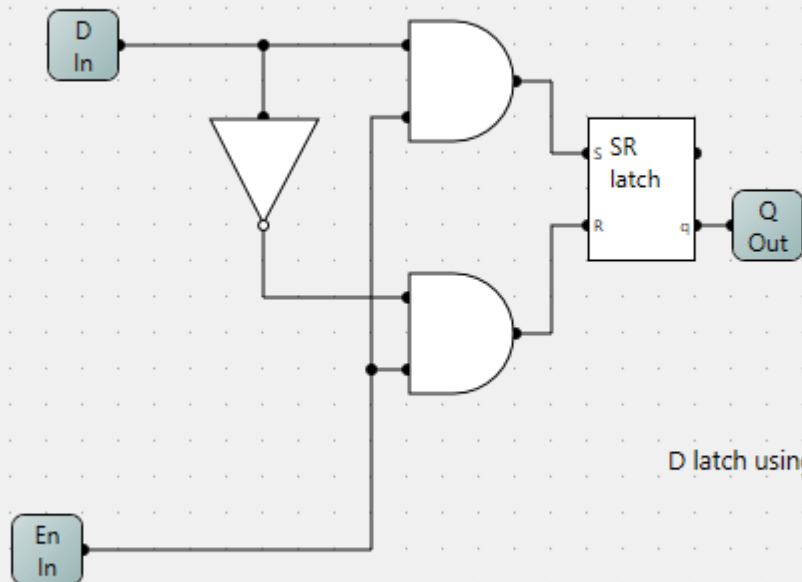
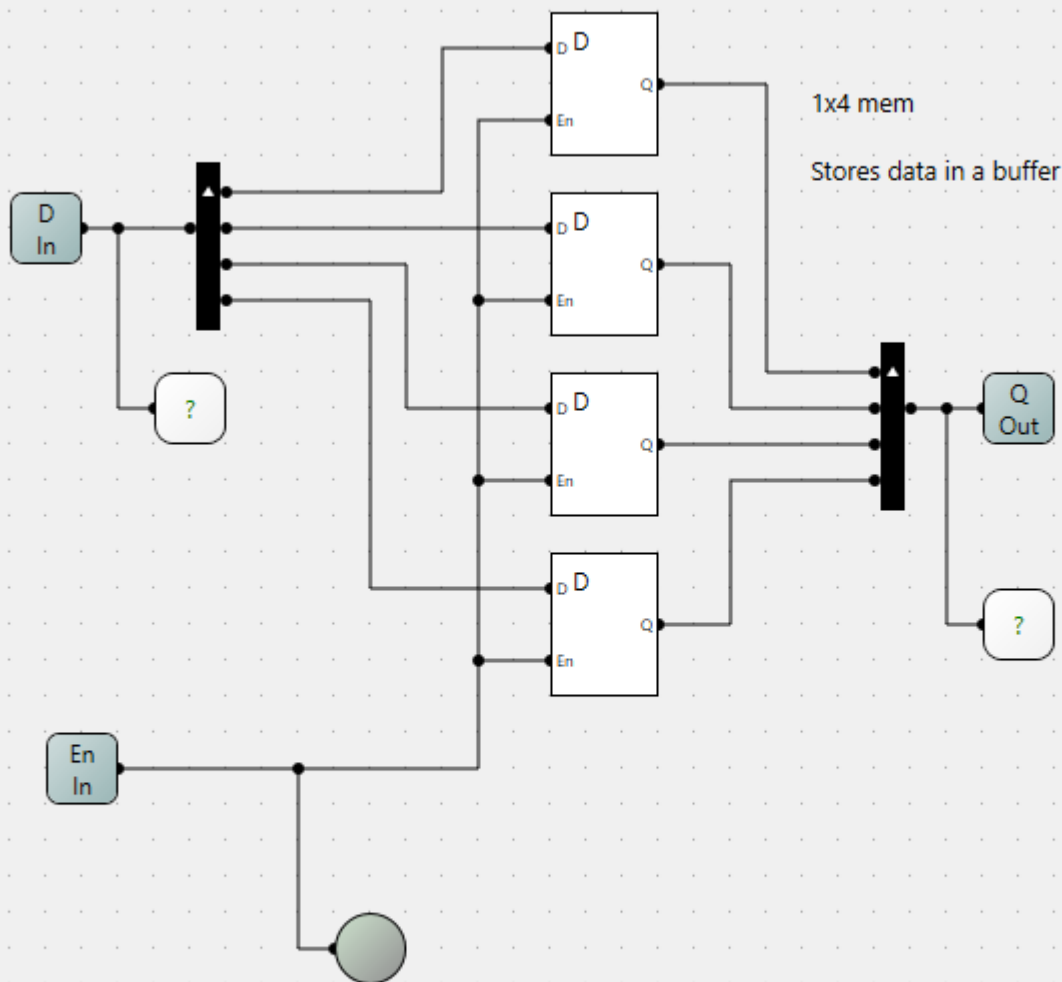


CHRIS ORTIZ  
7804453

Set reset latch



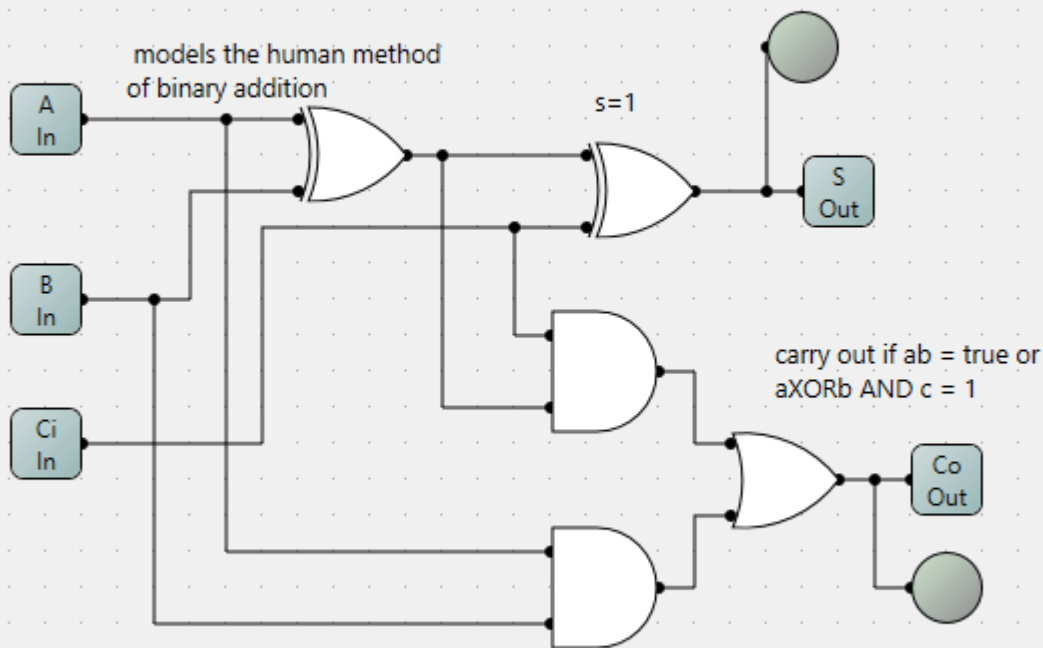
D latch using Sr latch



## 1 bit adder

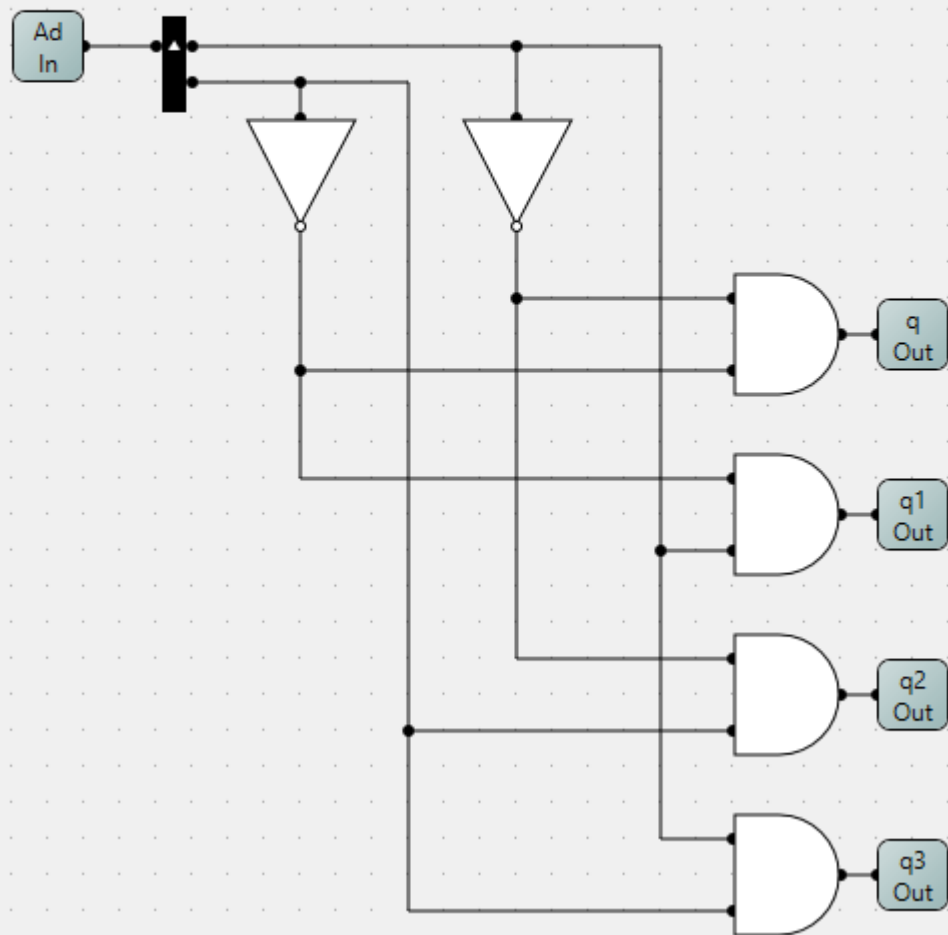
manages carry out when  
needed, accounts for a carry  
in value,

models the human method  
of binary addition

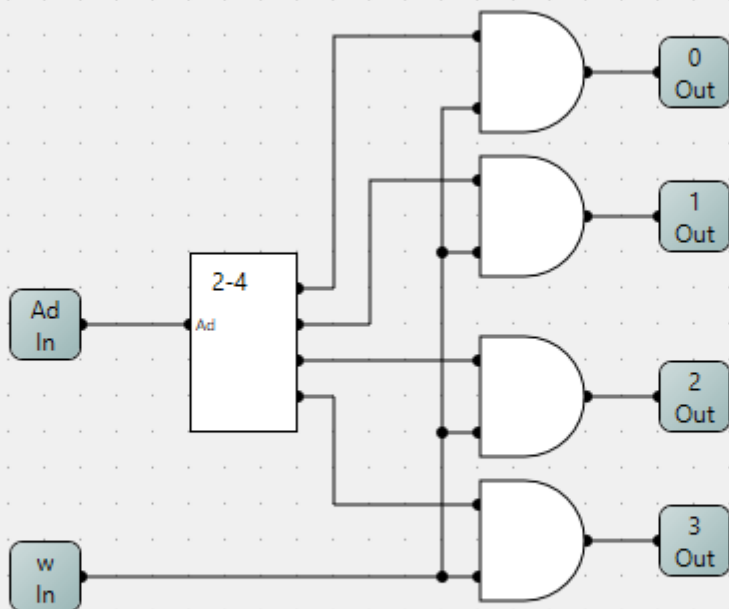


## 2-4 decoder

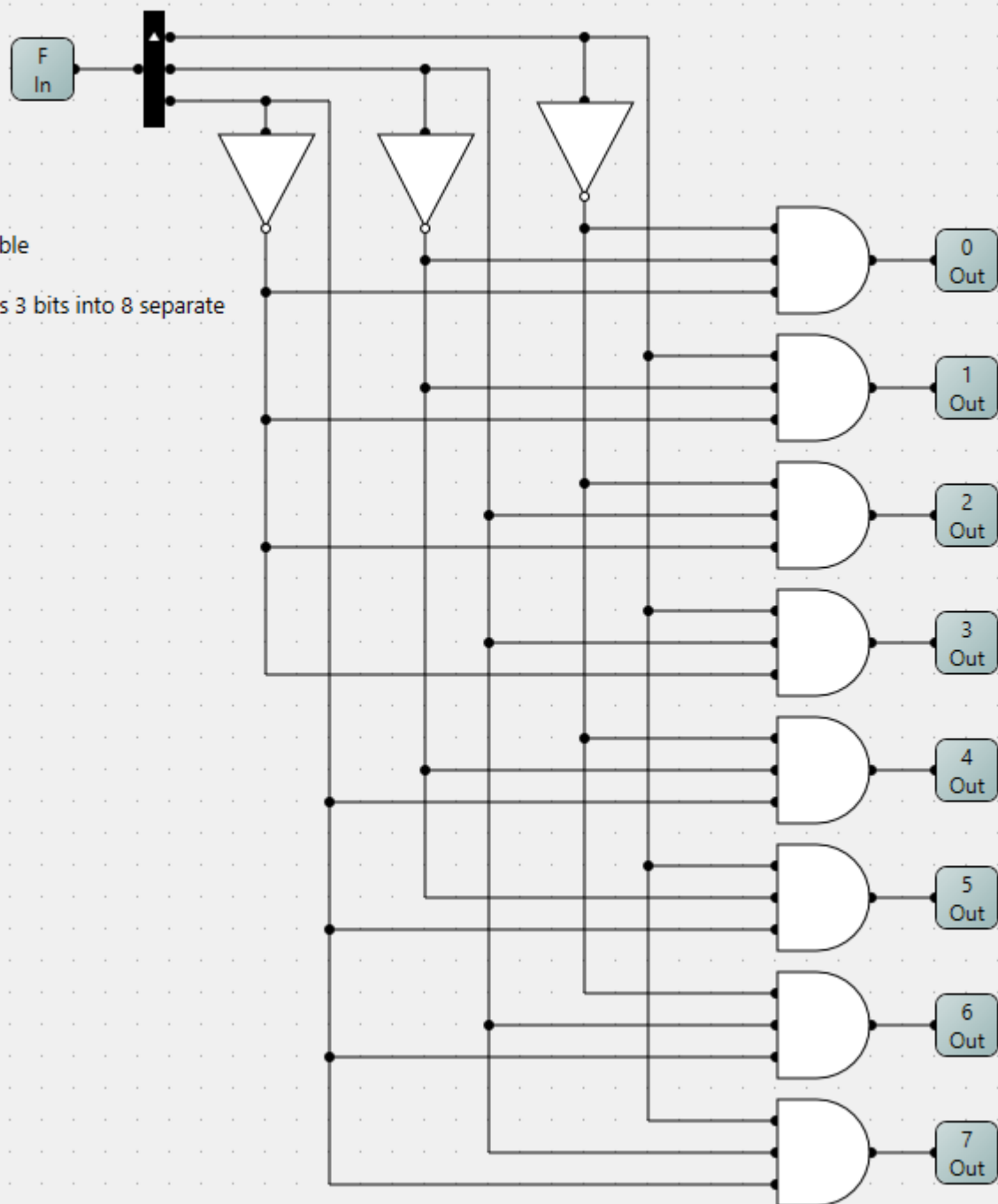
Decodes 2bit to 4 separate states

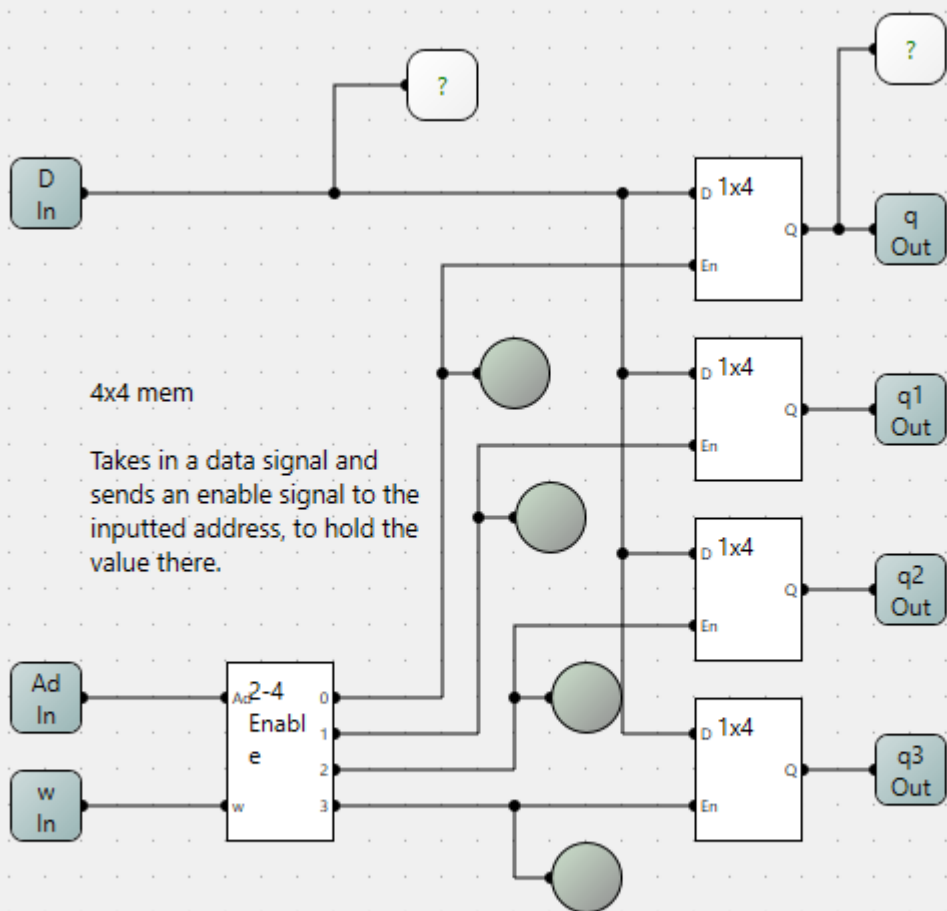


## 2-4 Enable

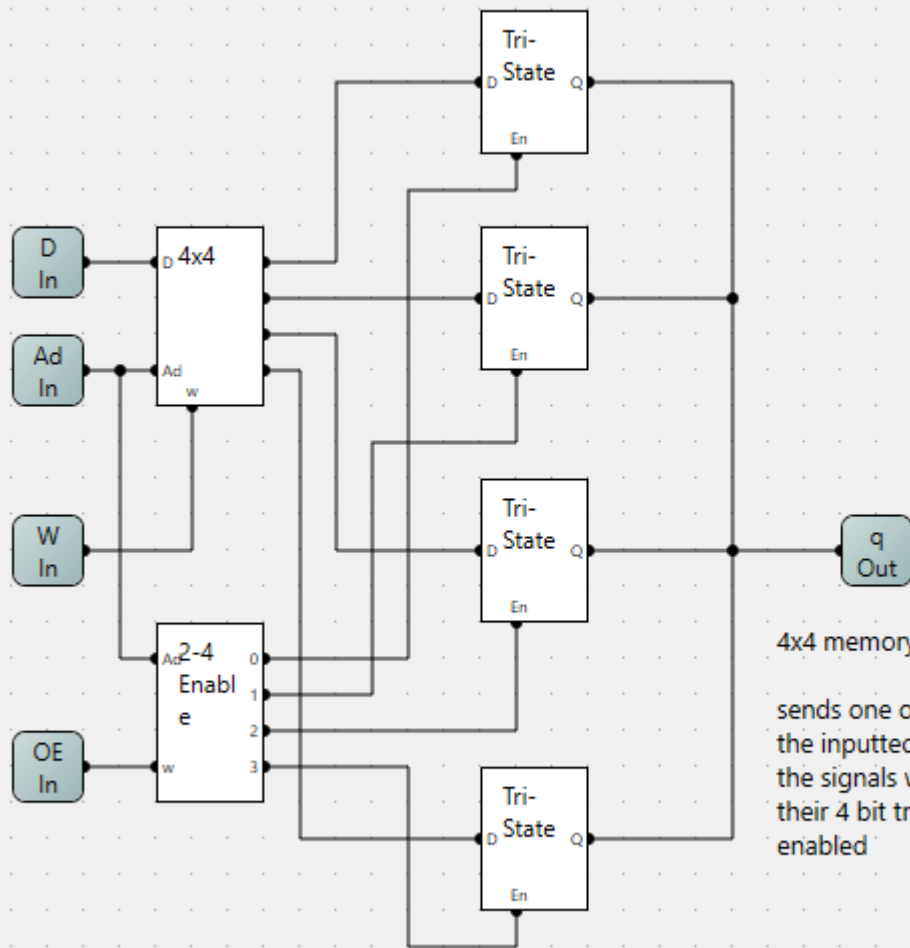


Sends single decoded signal  
PENDING  $w = 1$



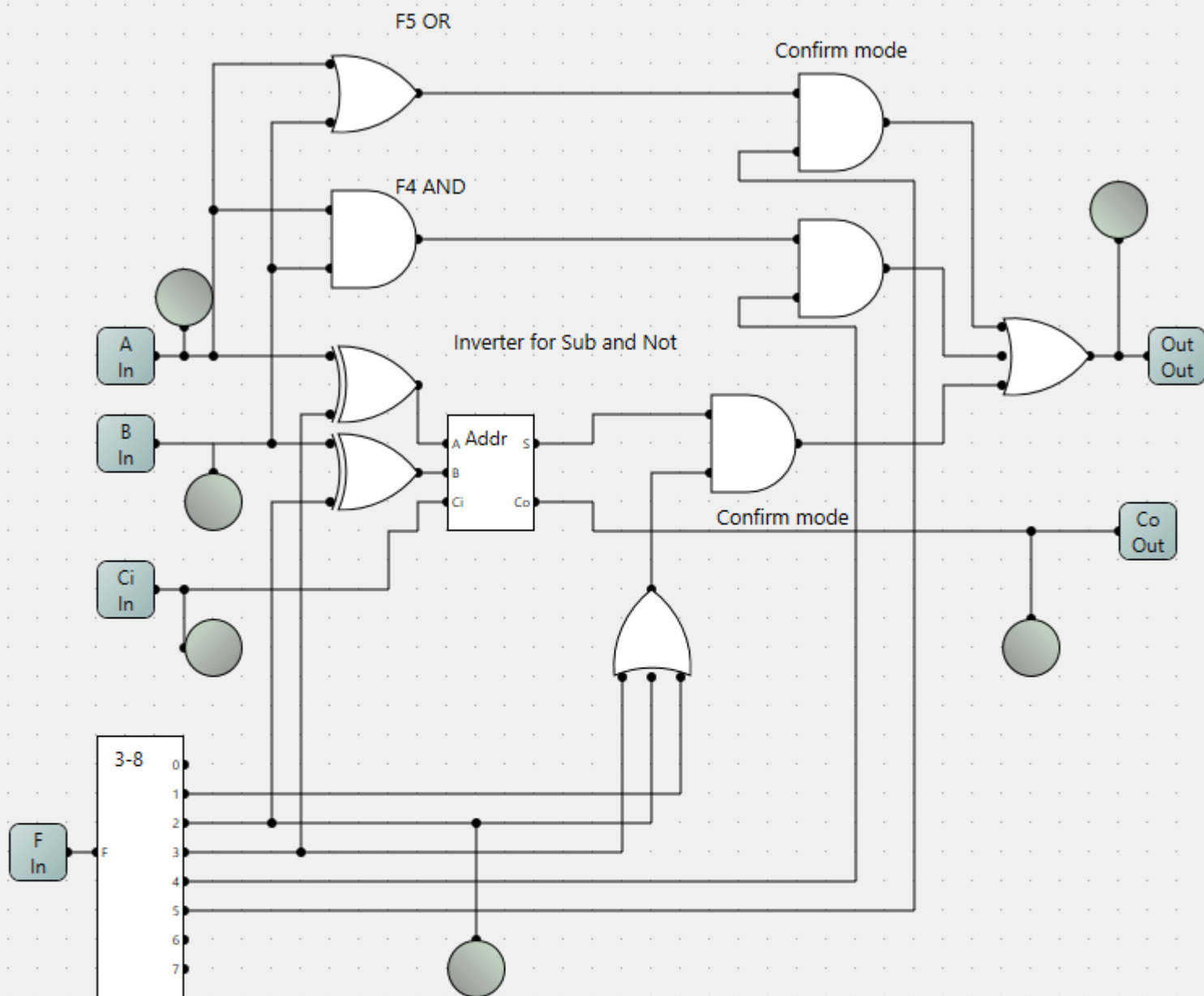






4x4 memory w/ enable

sends one output based on the inputted address, rest of the signals will be low due to their 4 bit tri state not being enabled



0: None

1: Add

2: Subtract

3: Not A

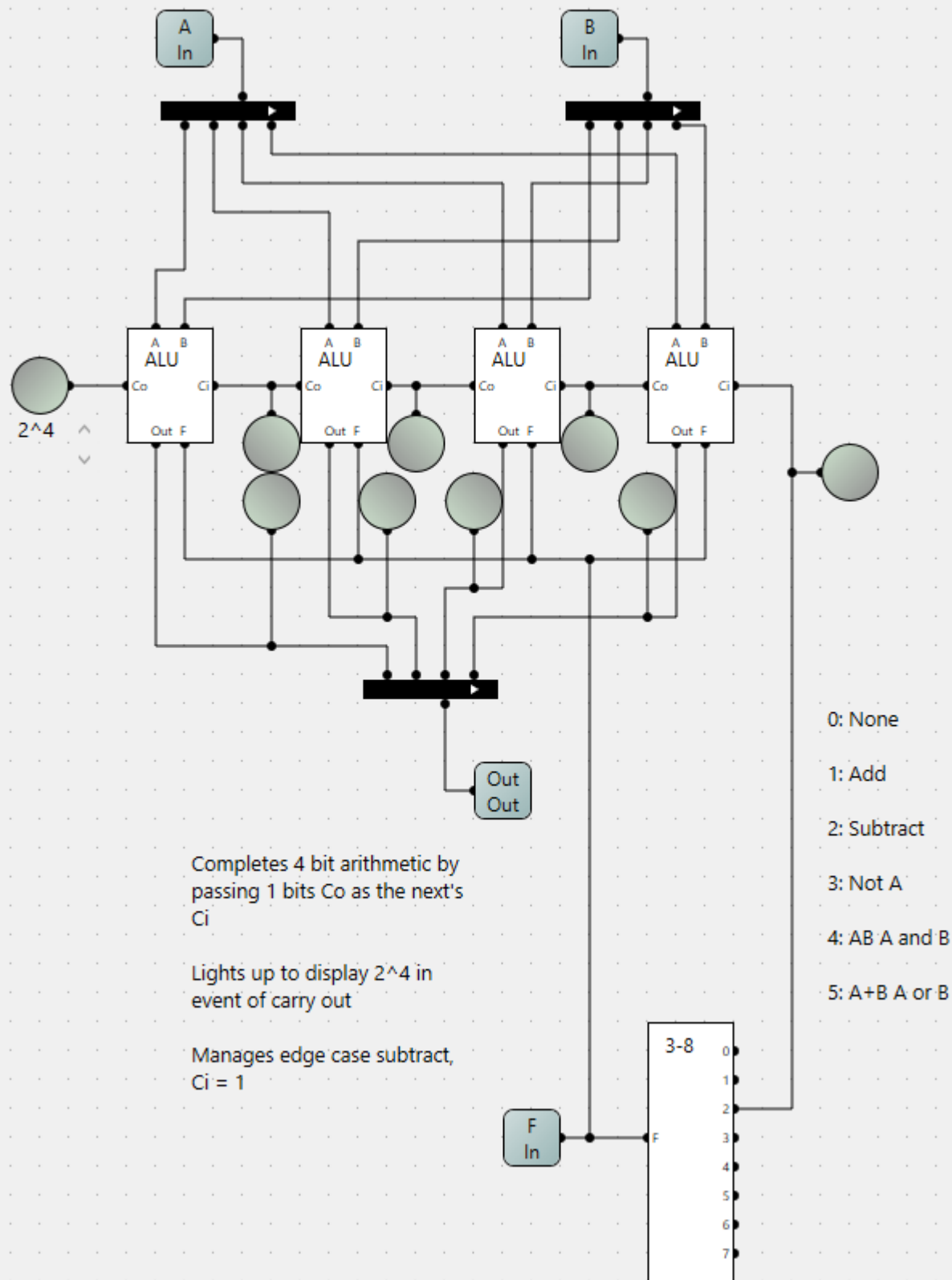
4: AB A and B

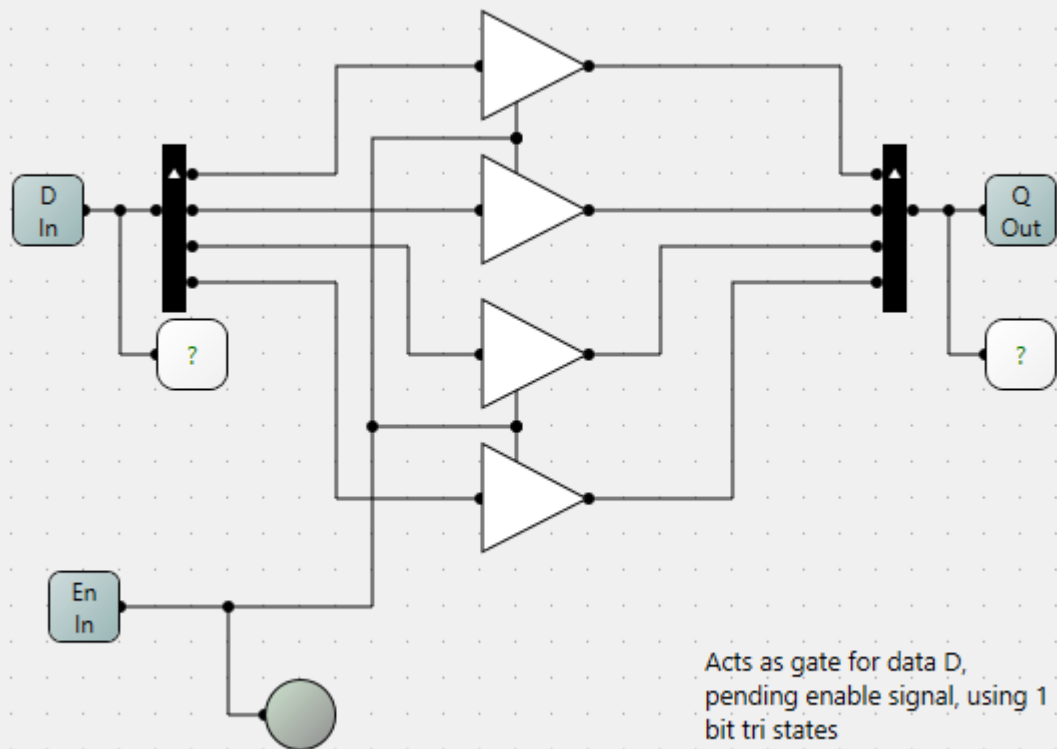
5: A+B A or B

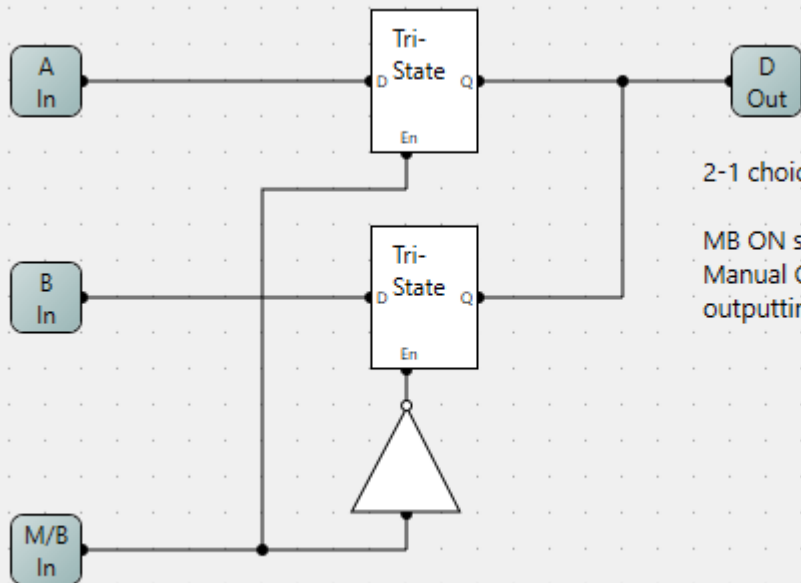
ALU that supports the following 5 functions for 1 bit operations,

Makes use of the adder to manage Ci,Co

Decodes function input and manages edge cases if need (sub, not)







2-1 choice

MB ON sends signal to  
Manual OFF to Buffer,  
outputting only one signal

