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Cascode Current Mirror Rev2

**Overview**

The cascode current mirror has an improved output resistance compared to the source degenerated current mirror, but at the cost of reduced headroom. The minimum operating range for the input voltage to the cascade current mirror is 2(Vtn + Vov). The minimum operating voltage for the output port is Vtn + 2Vov. Using the 50nm cmosedu\_models library gives a VTHO = 0.22V spice parameter for the threshold voltage. This means that the current mirror can function with input and output voltages of as low as 0.44V and 0.22V, but only with a negligible current of several microamps. Our Ibias current is chosen as 50uA which the cascade current source cannot sustain with a vdd = 1V operating rail. See Figure 1 *Cascode Current Mirror*

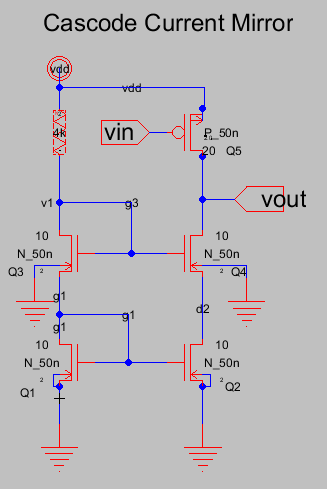


Figure Cascode Current Mirror showing Resistive current source. Note that *v1* is the input voltage of the current mirror and *vout* is the output voltage of the current mirror that determine the operating range of the cascade current mirror. Q5 isthe common source amplifier.

**Schematic Analysis**

**Transistor and SPICE model parameters**

The parameters that we are using for this simulation are:

Vdd = 1(V)

Ibias= 50(uA)

W/L = 5

VTHO = 0.22(V)

**Output Voltage Range of The Cascode Current Mirror**

The cmosedu\_models.txt spice file is a level 54 spice simulation meaning that we cannot readily get the for the circuit. Instead we bias the circuit properly so that all the transistors are in saturation, then produce the signal on the waveform.

which is not remotely far from the 280 listed for the 45nm CMOS process in table 1.5. What does this mean for the Ibias and input voltage of our circuit?

Suppose Ibias = 50uA. Then 0.47V .

Then the input voltage would be 2(Vtn + Vov) = 2(.22 + .47) = 1.38V > Vdd = 1V. If we put a 50uA ideal current source for Ibias, we show the input voltage to be simulated at 1.6V. In other words, the cascode current source lacks the headroom to source or sink a significant current with a low supply rail. For the sake of comparison, let’s increase the supply rail to 1.8V and sweep the output node vout to produce a graph that shows the operation of the cascade current mirror. See Figure 3.

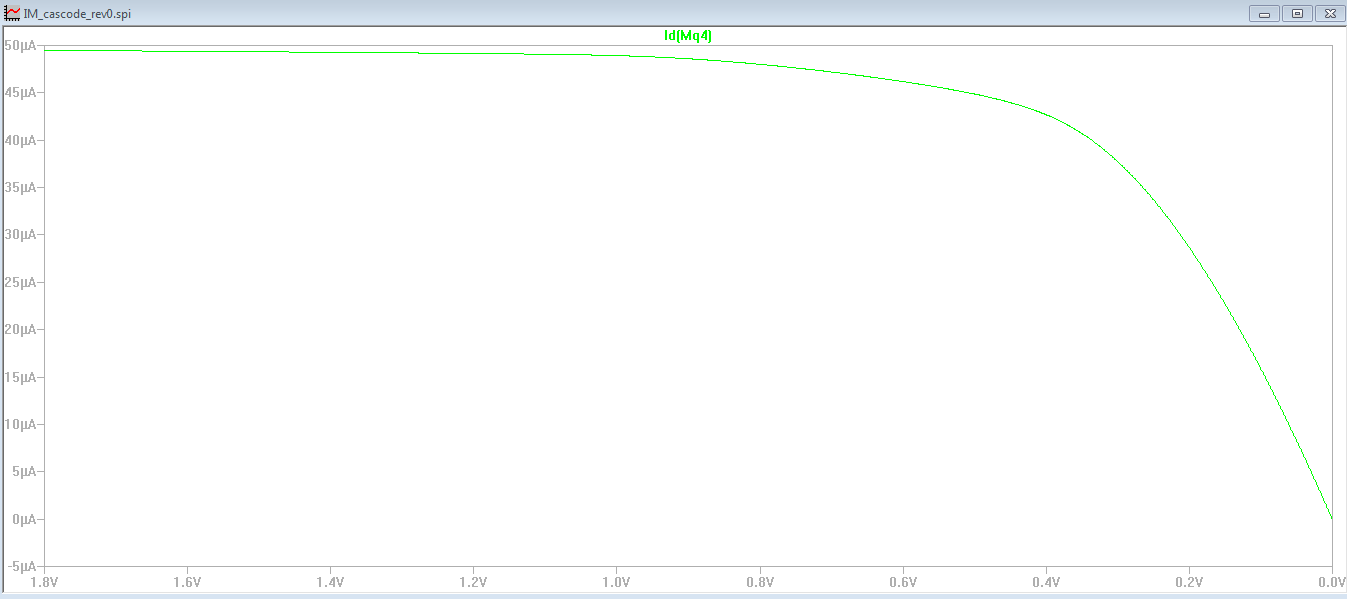


Figure DC sweep of the output voltage *vout* showing the current mirror falling off when *vout* approaches Vtn + 2Vov = 550mV. This sweep is with a rail voltage of Vdd = 1.8V.

The current matching of the output Id(Mq4) and the Ibias = 50uA is very close when *vout* is near the supply rail. As *vout* falls toward the minimum output voltage, then the matching begins to deteriorate.

If we define the current mirror to be in operation when Iout = Ibias +- 10%, then

Vout minimum = 500mV with Ibias supplied by an ideal current source. When using a resistive current source (R = 4kΩ for Ibias = 50uA) and a 1.8V supply rail, Vout minimum = 550mV. Without the higher Vdd, the circuit would not be able to source 50uA. See Figure 4 .

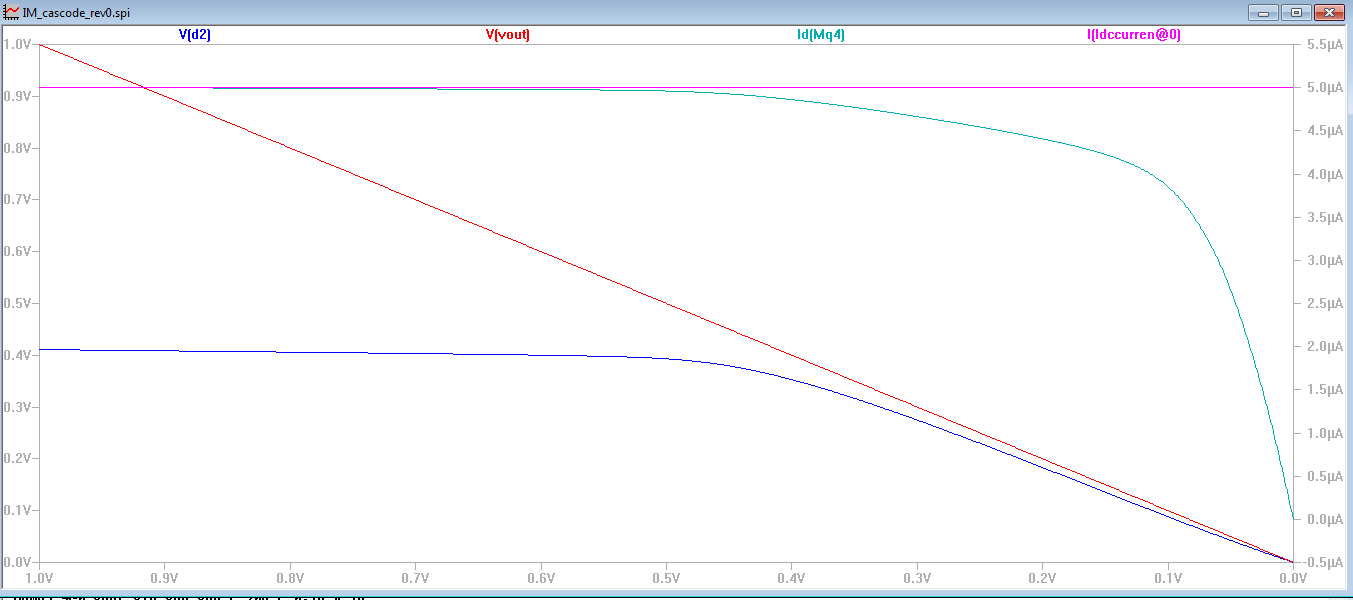


Figure The cascade current can operate at a lower vout approaching Vtn provided that the bias current is sufficiently small. The output current I(Mq4) (blue) falls off as Vout drops below 250mV. With negligible current, Vov Note that this result is from a 5uA ideal current source.

For the PMOS common source amplifier, it is required that *vin* – *vdd* < vtho = -.22V. Then the operating range of the current mirror extends up to *vdd*  - 0.22V. Without the common source amp, the current mirror can operate with *vout* going up to the rail.

The range of *v1* the input voltage is essentially 0, because the *v1* is fixed by the bias current.

This means that any change in the input voltage *v1* will necessarily change the and thus change the bias current. With the 4kΩ resistor and *a* 1.8V supply rail, *v1* = 1.64V.

This then is what we want to see in improved versions of the current mirror:

1. Minimize voltage supply.
2. Minimize the output voltage *vout* and input voltage *v1* of the current mirror to maximize range of operation.

**Input and Output Resistance**

One of the most important parameters of current mirror is the output resistance . For example when used as the load on an op-amp, the output resistance multiplies the gain of the amplifier. The output resistance of the cascade current mirror is:

= 22.6kΩ

Finding the drain source resistance can be done by hand calculation which is often off by a factor of two, or can be inferred from simulation results. First the hand calculations:

Here we assume that 𝜆 = 2.0(m/V) using the 45nm CMOS process value from table 5.1 from  *Analog Integrated Circuit Design[[1]](#footnote-1)*.

To get the lambda value from simulation, we take a single N\_50n transistor and run a DC sweep of the drain to source voltage, then we get the familiar I-V curve of the MOSFET given here in . Calculating the intersection of the I-V curve with the X axis gives us an early voltage of Then .



Figure I-V curve of the N\_50n transistor. The intersection of the slope line with the X axis is the early voltage.

To find the transconductance, we do a DC sweep of the gate voltage of a cmosedu\_models MOSFET and measure the slope of the drain current.

= 0.12ms (estimated as = from a DC sweep of v1)

To check these calculations with simulation, we disconnect the common source transistor from the current mirror, and run a DC sweep of the vout terminal. See Figure 4.

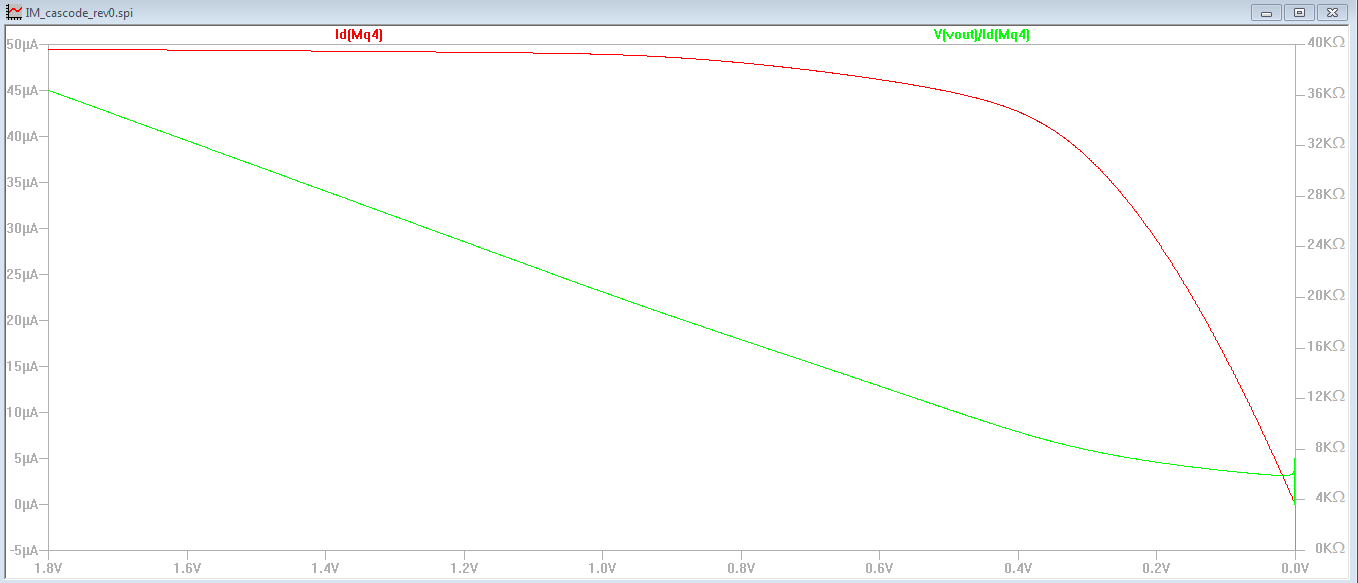


Figure 4. Output Resistance of Cascode Current Mirror with 4k resistive current source, and Vdd = 1.8V. When the transistors are all in saturation at *vout* = 500mV, the output resistance is 10k.

The results of the simulation show that the output impedance = taken when *vout* = 500mV which is at the lower operating range of the output voltage. This is in agreement with our hand calculations. To increase we would need to increase the drain to source resistance (by decreasing the drain current), or increasing the transconductance of Q4. The transconductance parameter is dependent upon and that are under the control of the circuit designer.

Then this makes

which suggests that when Ibias = 100uA, = = .35\*10kΩ = 3.5kΩ.

Changing to an ideal Ibias current source and sweeping from 50uA to 100uA we expect to see the output impedance decrease. In the simulation, at *vout* = 550mV, the output impedance ranges from 12kΩ (at Ibias = 50uA) to 7.1kΩ (at Ibias = 100uA) which is twice what we’d expect, but does prove the concept that increasing the bias current decreases the output resistance. See Figure 5 .

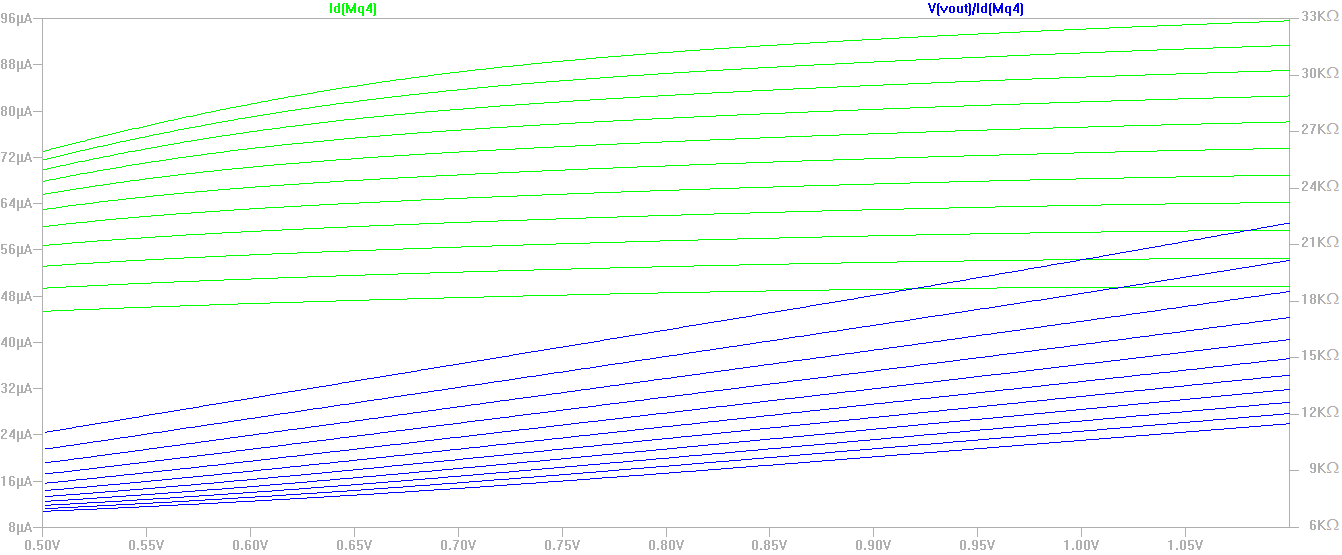


Figure 5. Effect of increasing Id on output resistance. Here Id is swept from 50uA to 100uA. As Id increases, the output resistance goes down proportional to .

The input resistance of the circuit is calculated from the small signal model.

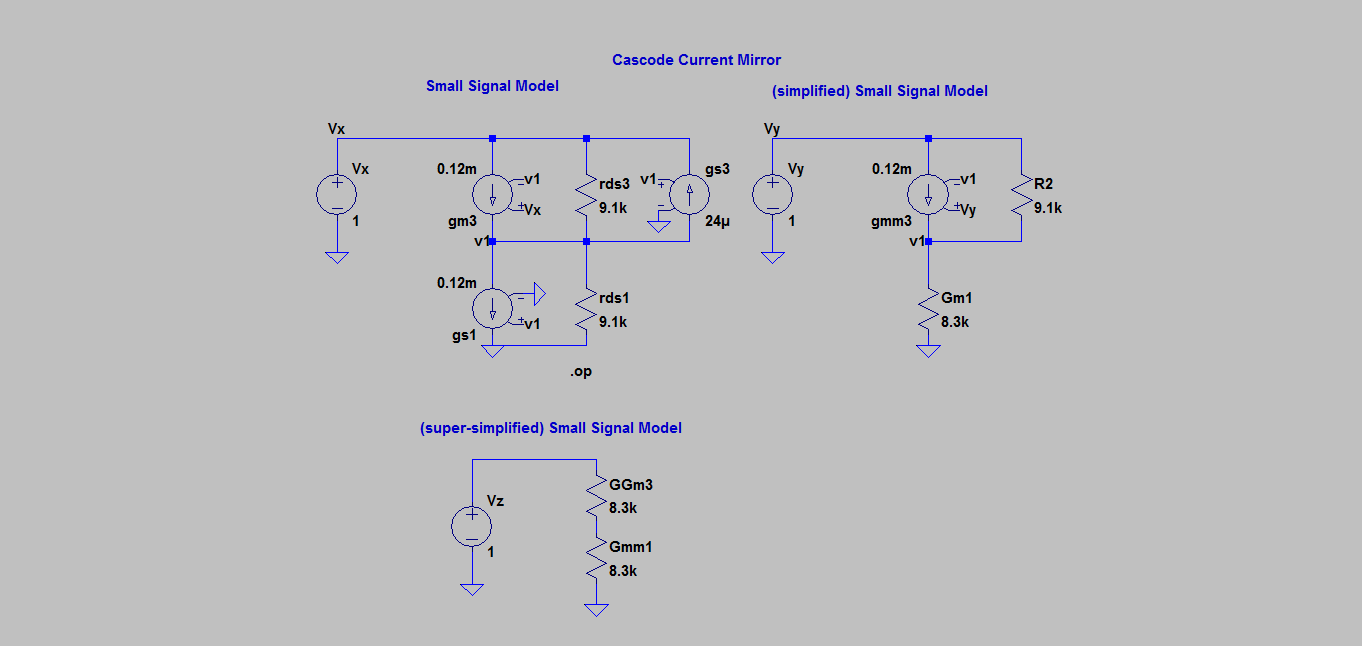


Figure Small signal model of the Cascode Current mirror. The input resistance Rin = vx/ix.

Running a spice simulation to find the operating point of the circuit yields the following:

--- Operating Point ---

V(vx): 1 voltage

V(v1): 0.551195 voltage

V(vy): 1 voltage

V(n001): 1 voltage

V(n002): 0.5 voltage

I(Ggm3): 6.0241e-005 device\_current

I(Gmm1): 6.0241e-005 device\_current

I(Rds1): 6.05708e-005 device\_current

I(Gm1): 6.6409e-005 device\_current

I(R2): 4.93193e-005 device\_current

I(Rds3): 4.93193e-005 device\_current

I(Gmm3): 5.38566e-005 device\_current

I(Gs3): 1.32287e-005 device\_current

I(Gs1): 6.61434e-005 device\_current

I(Gm3): 5.38566e-005 device\_current

I(Vz): -6.0241e-005 device\_current

I(Vy): -0.000103176 device\_current

I(Vx): -8.99473e-005 device\_current

Full small signal model

Simplified small signal model (no body effect)

Super-simplified model (for hand analysis)

The electric-vlsi calculation of Rin yields an input resistance of 32kΩ. See Figure 5 .

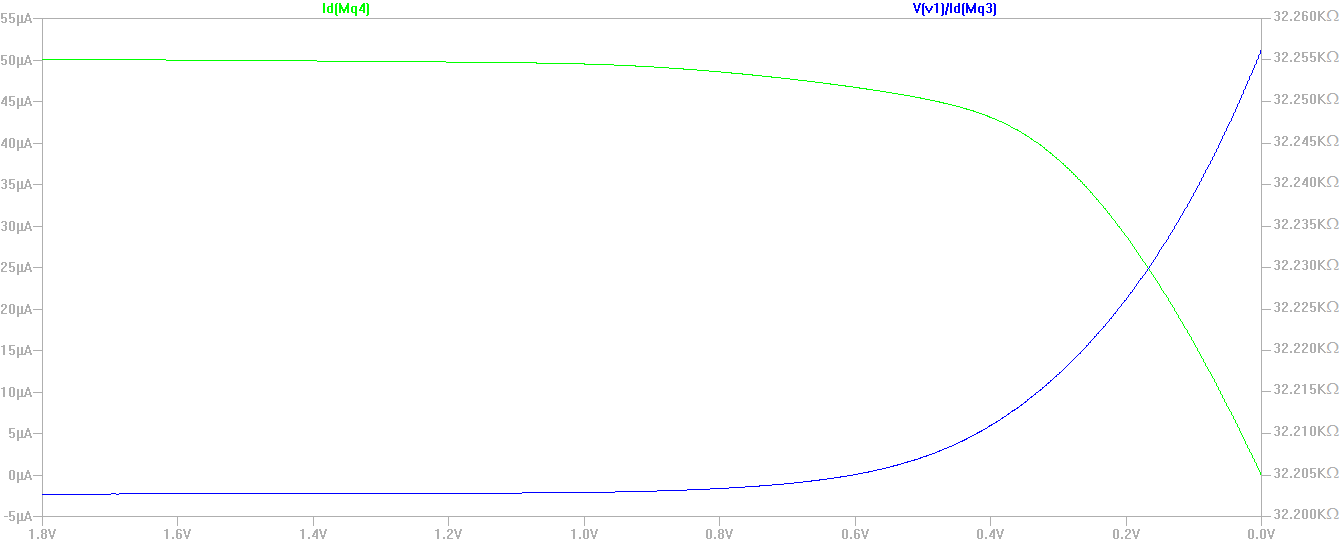


Figure Input resistance of the cascode current mirror is a very constant 32.2kΩ while the transistors are in saturation.

The electric-vlsi simulation of the cascode circuit shows Rin = V(v1)/Id(Mq3) = 32kΩ. The difference between the hand calculations and the electric simulation probably lies with my assumptions about the drain source resistance and the transconductance parameter.

The gain of the common source amplifier can be characterized once the DC operating point is found. The dc operating point can be found by sweeping *vin* and setting the dc operating point where the slope of is highest. This is shown in the DC sweep below in Figure 6 .

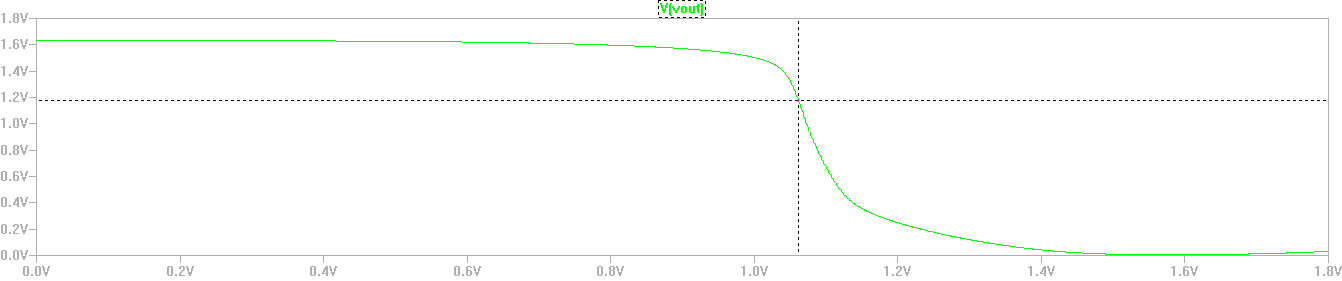


Figure DC sweep of the input voltage of the common source amplifier to find the dc operating point where the gain is maximized.

Setting *vdd* = 1.06V we can run the transfer function command to find the DC small signal transfer function of the system.

--- Transfer Function ---

Transfer\_function: -51.3026 transfer

vin#Input\_impedance: 3.31806e+006 impedance

output\_impedance\_at\_V(vout): 486646 impedance

The DC transfer function of our amplifier is -51.3026.

**Frequency Response**

To estimate the bandwidth of the circuit, we need to know the capacitances of the PMOS common source amplifier. The two main capacitances are and (the miller capacitance). The small signal model of the transistor includes these capacitances derived from the cmosedu\_models file[[2]](#footnote-2). The relevant spice parameters are CGSO and CGDO:

Where CGSO and CGDO are given in capacitance per unit channel width. The width of the PMOS transistor in our design of the cascode current mirror is 1000nm. This does seem suspicious because typically is bigger than the miller capacitance by several factors. Less than a femto farad of capacitance also seems extraordinarily small.

For the small signal model (see Figure 7), I also made very arbitrary estimations of the load impedance and thevenin equivalent resistance at the gate, . Assuming that the load capacitance is 100pF, which is many orders of magnitude bigger than the other capacitances of the transistor, then we can find the dominant pole:

The frequency sweep of the LTspice small signal model shows the cutoff frequency at 160KHz. This suggests that there is something abnormal about the transistor and the assumptions that went into the approximation are not entirely valid.

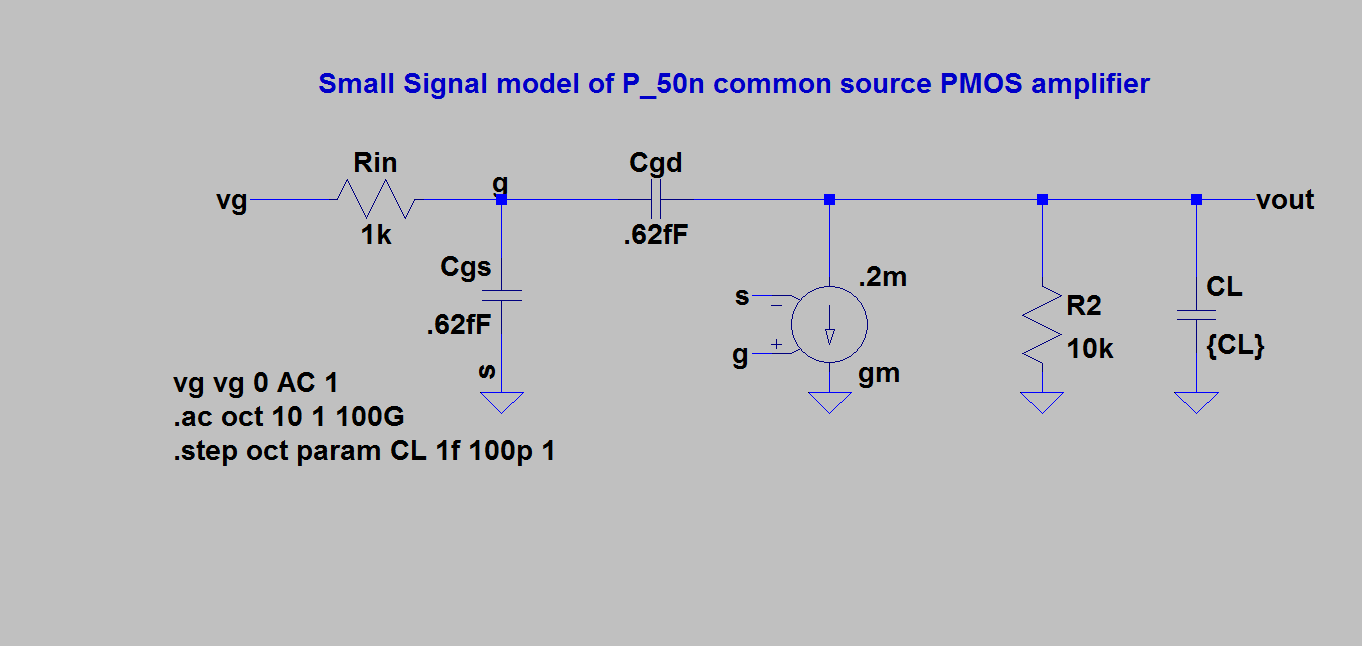


Figure Spice small signal model of the PMOS common source amplifier with Cgs and Cgd and a load capacitor CL.

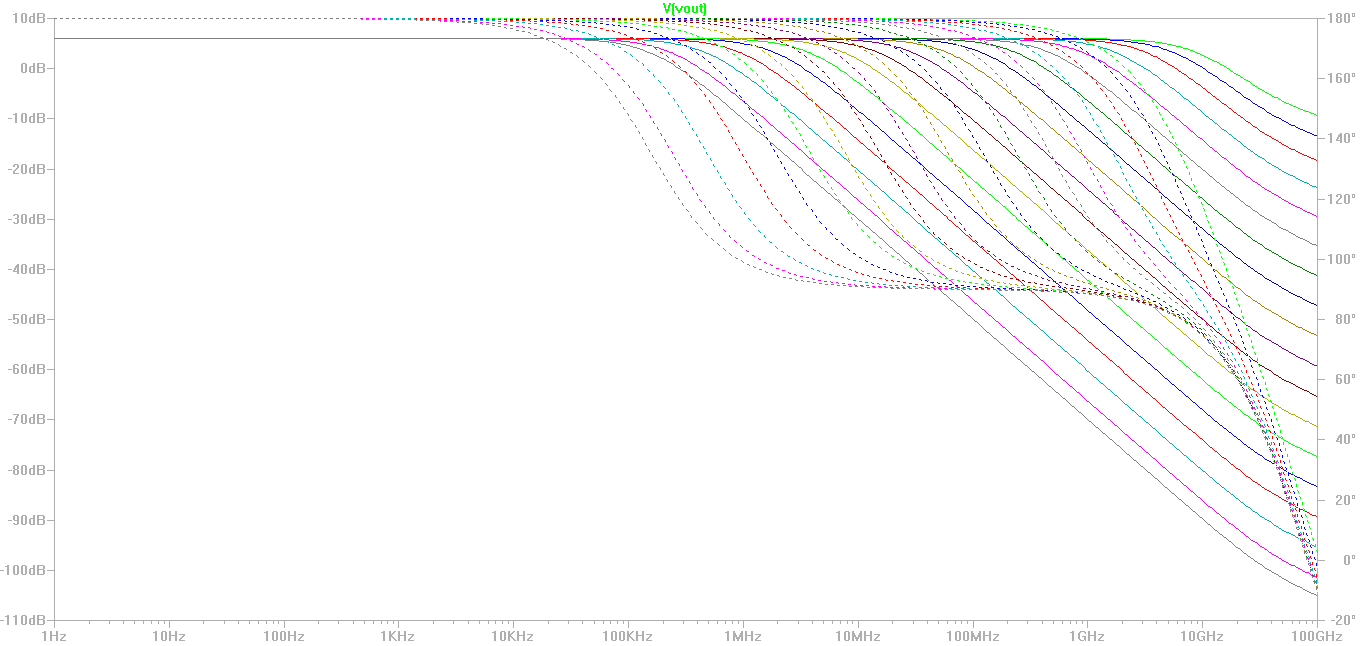


Figure Small signal LTspice simulated frequency response of the common source PMOS amplifier with CLoad swept from 1fF - 100pF

To find the bandwidth of the circuit we set the DC operating point of the *vin* node, then do an AC sweep of the circuit. See schematic below Figure 7.

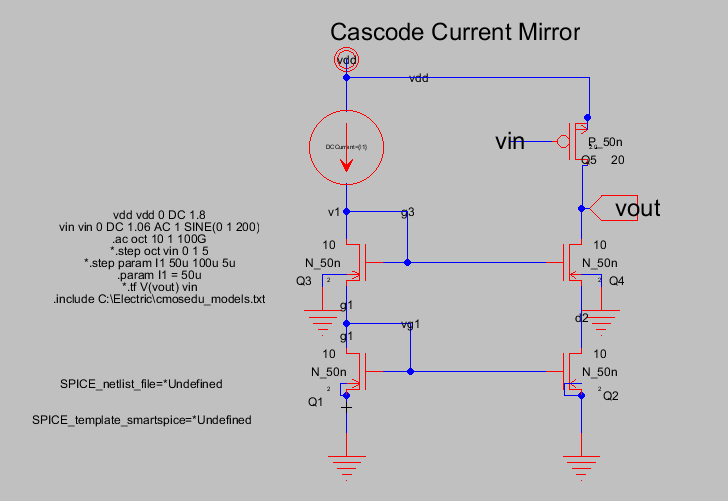


Figure Complete Cascode Current Mirror circuit with PMOS common source amplifier. Spice code for simulating an AC sweep is included.

The simulation shows a cutoff frequency of 525MHz. Note that the DC gain is 24dB = 15.8 . This is less than the .tf analysis of gain = -51, however the gain is highly susceptible to dc bias point. Setting the DC bias point as a parameter, and sweeping the parameter gives the following graph showing the sensitivity of the gain to the dc bias point. See Figure 8. However, the DC gain is maximized at about 16, so this still does not explain why the AC sweep gives a different gain than the .tf small signal analysis of the DC operating point.

We did not include a load capacitor, and the transistors in the circuit are all 50nm models with W/L = 5 or perhaps 10 in the case of the PMOS. This will contribute to a very high bandwidth. When the current mirror is connected to a capacitive load, the bandwidth will necessarily decrease significantly.

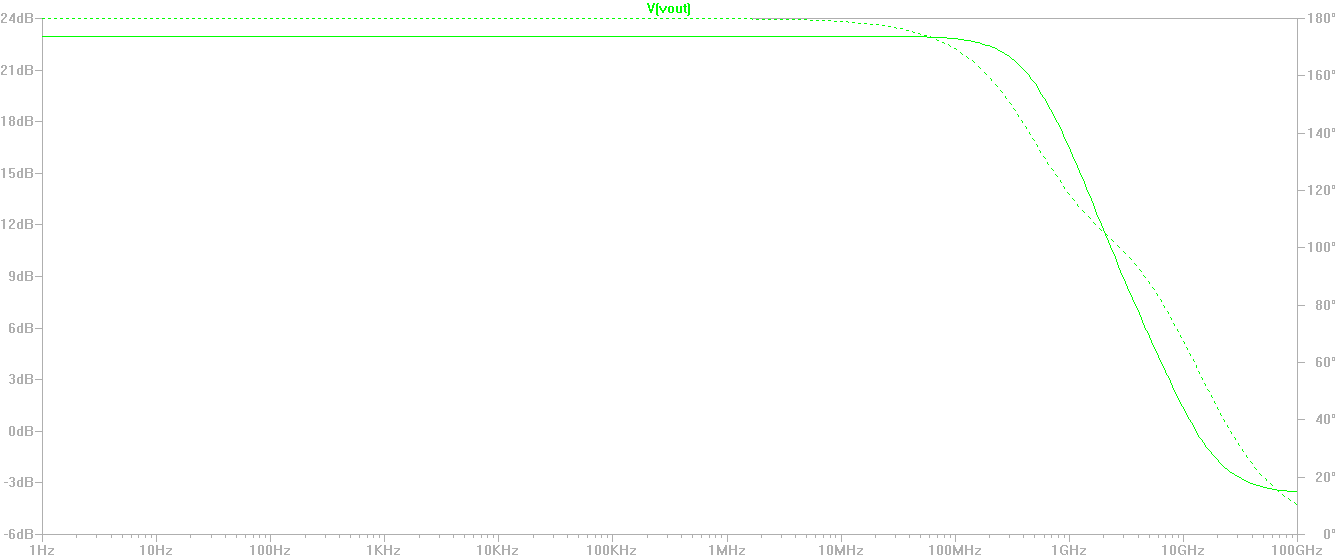


Figure Bode Plot of cascode current mirror with common source amplifier.

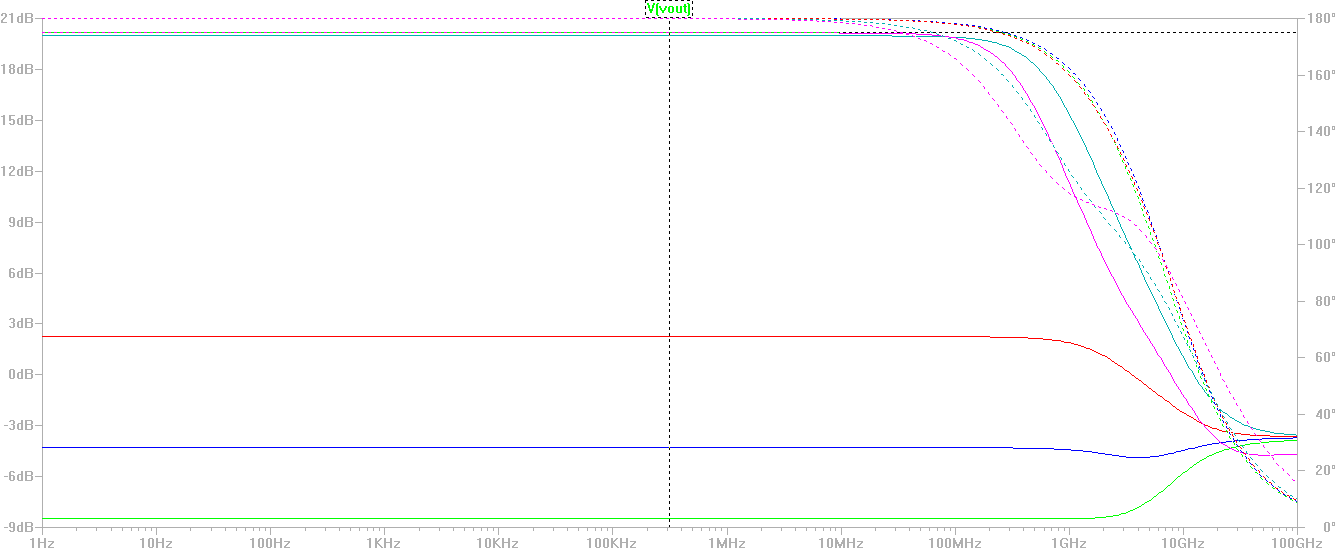


Figure AC sweep of the common source amplifier with *vin* = {900,950,1000,1050,1100}mV showing the variability of gain when the dc bias point is moved.

The Power Supply Rejection Ratio (PSRR) is the susceptibility of the system to changes in the power supply[[3]](#footnote-3). For the current mirror, this is:

This is one of the most important parameters for a current amp, because the precision of op-amps, ADC’s, DAC’s and reference currents directly affect the overall precision of the system. The power supply signal is expected to have a spectrum of high frequency noise from switching power supplies and digital electronics. Proper filtering and isolation of the analog circuitry can mitigate this noise only to a certain extent. In addition, there may be a certain amount of DC and transient changes on the *vdd* signal due to load changes, temperature effects on the power supply and batteries, etc. A high quality current source should have a high power supply rejection ratio.

To test the PSRR, the common source amp with the gate terminal *vin* is set at the maximum gain level (*vin* = 1.07V for *vdd* = 1.8V) . An AC ripple is applied on top of the DC = 1.8V *vdd* supply. The correct simulation would frequency sweep the AC component of the *vdd* signal and measure the amplitude of the accompanying AC ripple in the *vout*. I cannot figure out how to do this in LTspice, so I will plot a low frequency (200Hz) and a high frequency switching power supply band 1MHz signal. We will use a .tran analysis with spice code:

vdd vdd 0 DC 0 AC sin(1.8 .025 1G)

vin vin 0 DC 1.07

.tran 10n

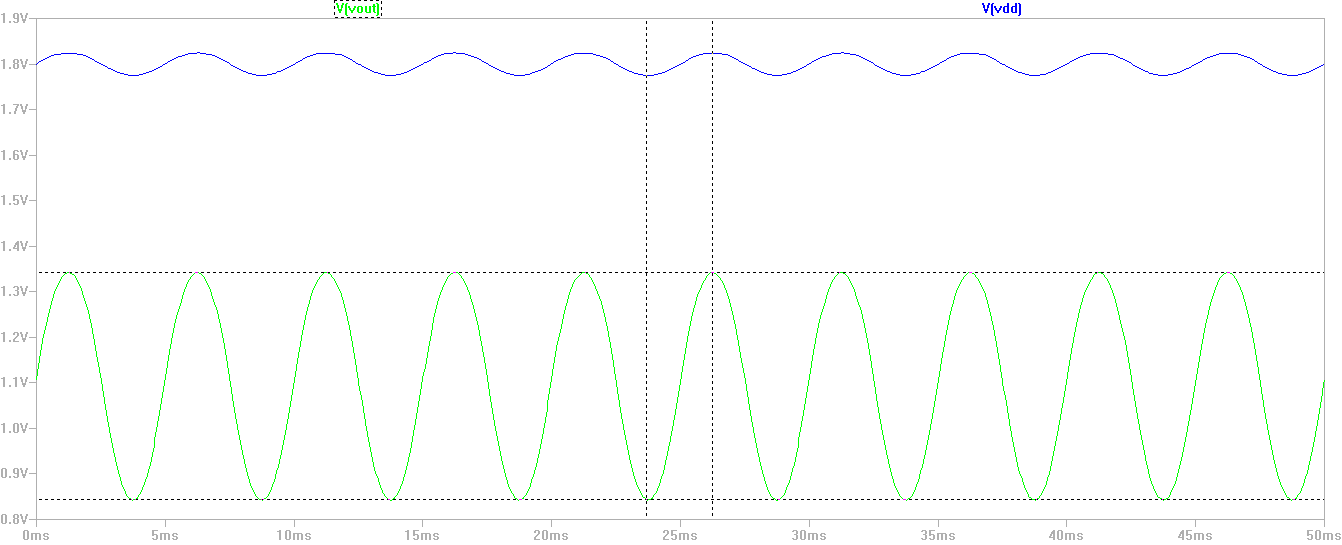


Figure 200Hz Vdd power supply ripple seen at *vout*.

At low frequency (see Figure 13)

At the 1MHz the PSRR is essentially unchanged. At 1GHz the PSRR is -14.5dB. These are terrible PSRR numbers. We would like to see PSRR > 40dB. Part of the reason for the poor performance is that the bias current is that we are using a resistive current supply. For Q1 and Q3, the bias current is proportional to . There is a squared relationship between change in *vdd* and changes in the bias current. This causes the gain of the common source amp to be strongly affected because:

Showing the strong relationship between changes in *vdd* and changes in the output signal.

**Temperature Dependence**

The threshold voltage and mobility of mosfet transistors is temperature dependent. For small Vdd transistors where the threshold voltage is approximately 200mV, the negative temperature coefficient of the threshold voltage surmounts the mobility degradation with the effect that the drain current increases with temperature. Note that this temperature relationship is different for micron scale higher Vdd transistors. The drain current is affected proportionally2

where

T = temperature

= room temperature (300 K)

K = threshold voltage coefficient (typically 2.5mV/K)

m = mobility temperature exponent (typically 1.5)[[4]](#footnote-4)

= velocity saturation index (typically 1.3 for short channel mosfets)

Also define the temperature coefficient for change in drain voltage over temperature:

Applying a temperature sweep to an N\_50n NMOS and P\_50n PMOS transistor from the cmosedu\_models library creates the following I-V curve. See Figure 11.

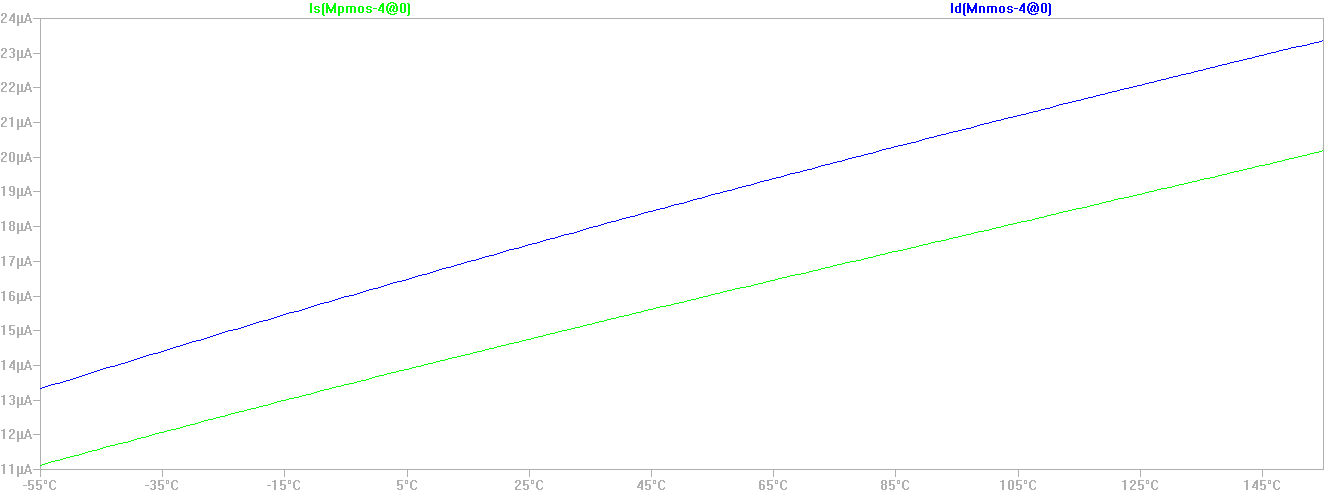


Figure Temperature dependence of PMOS (green) and NMOS (blue) transistors currents for *vdd*=1.0V, gate voltage = .5V. Short channel mosfets have a positive temperature coefficient.

We would expect the drain current of the single N\_50n NMOS transistor current mirror to increase with temperature over a 50K sweep

This shows that the drain current decreases with increasing temperature. That is opposite what the authors of the paper suggested. It could be that the values for velocity saturation and *m* mobility temperature exponent are estimated incorrectly. It is also possible that the temperature equations that I am using, are meant to apply to a smaller Vdd than 1V. As an experiment I swept the Vdd parameter on the full cascode current mirror from 1.3V to 1.8V while doing a temperature sweep. The result is interesting because it shows the temperature coefficient changing sign from a positive value at Vdd= 1.3V to a basically *Tempco* = 0 at Vdd = 1.5V, to a negative value when Vdd = 1.8V. See Figure 12.

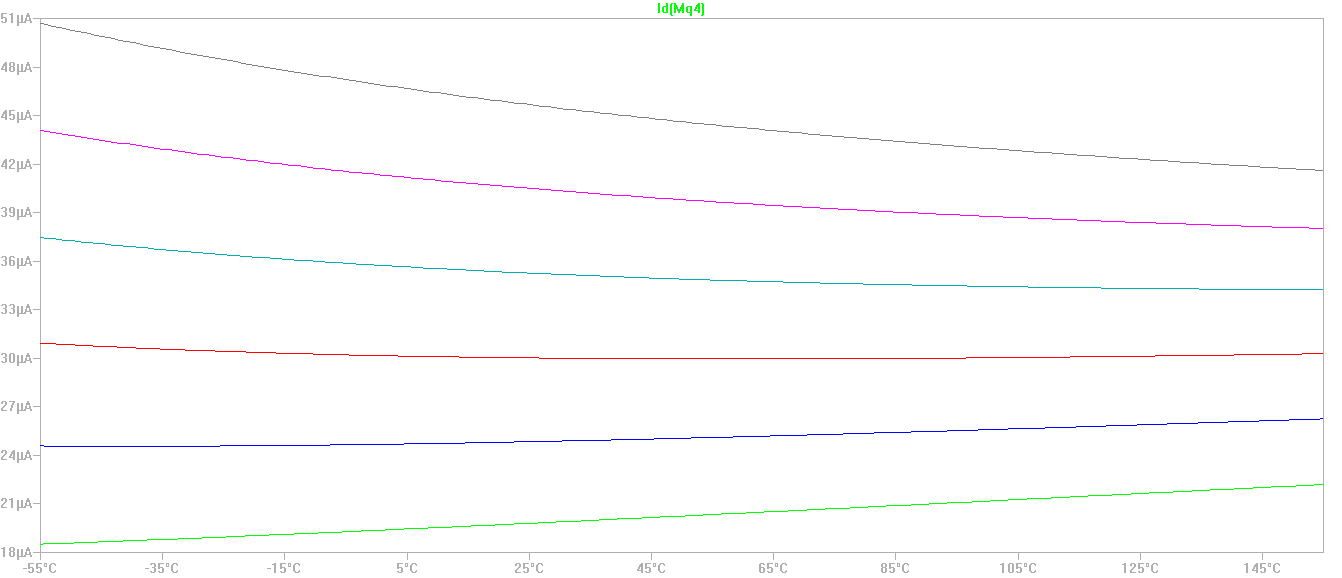


Figure Effect of Temperature and Vdd on short channel MOSFET cascode current mirror. Note that *Tempco* is positive for *vdd* = 1.3V (green line on bottom of graph), and *Tempco* is strongly negative for *vdd* = 1.8V.

For the graph above, choosing the *vdd* = 1.8V (the 4k resistor was sized for a rail voltage of 1.8V which is why the drain current equals 50uA for *vdd* = 1.8V, and only 20uA for *vdd* = 1.3V) and for consistency with the other cascode current parameters, the *Tempco* of the circuit at *vout* is:

The slew rate is a measure of the response speed of the amplifier. The slew rate is defined as:

Where is the initial time when the input waveform makes a step change. It is important to distinguish between the RC response and slew rate of the amplifier under discussion. The step at the input response must be large enough so that the linear slew rate is clearly visible from the exponential RC response. Giving a step signal to around the operating point of the circuit gives the output waveform of Figure 13. The slew rate is measured as

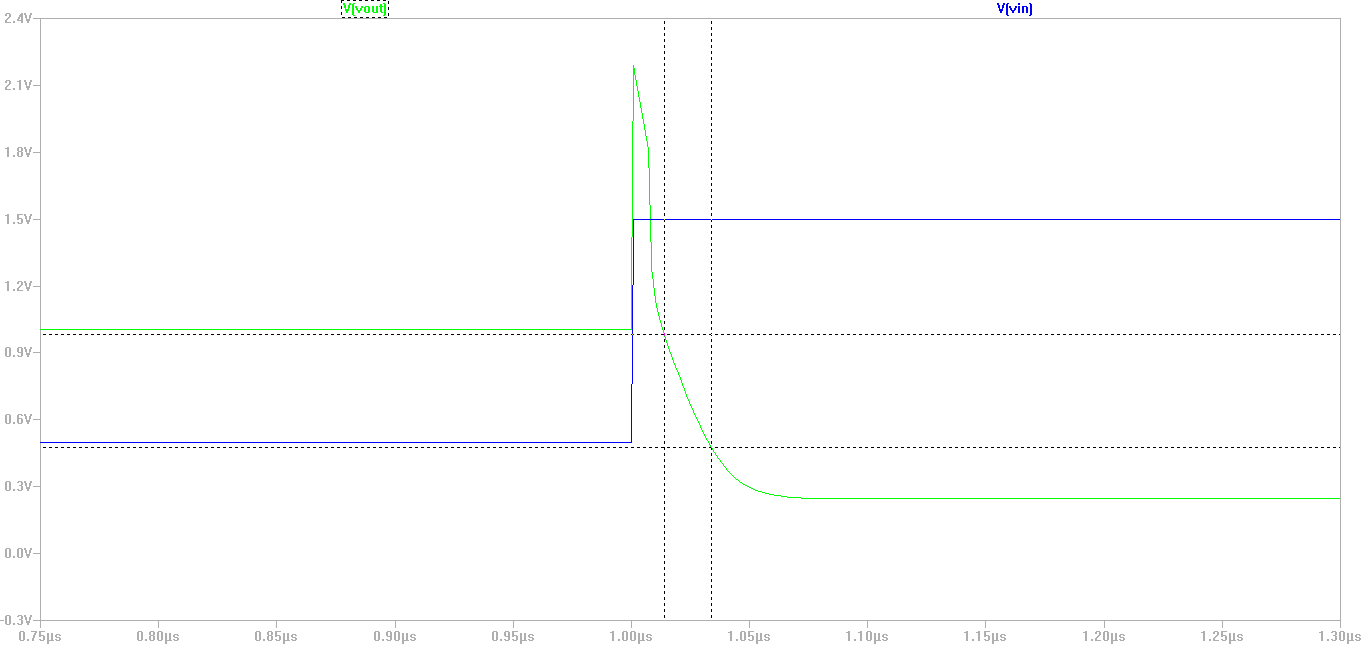


Figure Slew rate of the common source PMOS amplifier. The slew rate is visible as the linear section of the waveform highlighted between the crosshairs. The spike in the green *vout* signal is probably caused by inductance.

**Layout Analysis**

The analysis so far has been based on the cmosedu\_models spice file. This necessarily makes assumptions about geometric based parameters such as parasitic capacitances. We did a layout of the cascode current mirror and ran a series of simulations to check the parameters of the circuit and compare them with the schematic pure SPICE based results.

The layout introduces the concept of the footprint. Silicon real estate is expensive, and for most applications there is a premium placed on efficient layout and use of space. For our cascode current mirror layout we decided it was more important to demonstrate that we could use the electric-vlsi SPICE toolchain, then to try and optimize this preliminary current mirror.

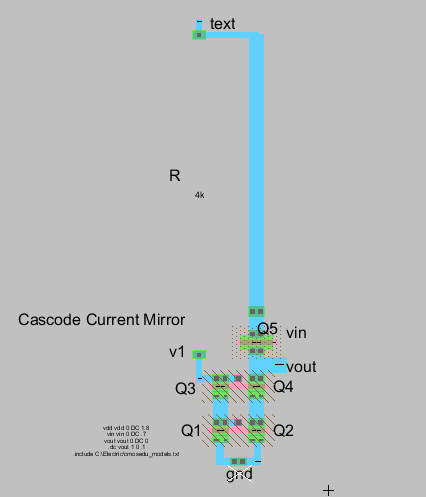


Figure Layout of Cascode Current Mirror

**Footprint**

The circuit uses 5 transistors including the PMOS common source.

There is 1 passive element (the resistor).

The collective **gate length** is 60 units = 3um.

The **area** of the rectangle that would enclose the circuit is 36um2.

**Total Power Consumption** = .18mW

**Total Bias Power** = 90uW

**Total leakage Power**

where is some appropriate leakage voltage < *vdd* for all the transistors.

Setting *vout* = 500mV and *vin* = .7V, and running the .op operating point analysis we get:

Ig(Mq5): -1.51323e-008 device\_current

Ib(Mq5): 2.32593e-009 device\_current

Is(Mq5): 0.00011777 device\_current

Id(Mq4): -4.55874e-005 device\_current

Ig(Mq4): 9.13425e-009 device\_current

Ib(Mq4): -1.98804e-009 device\_current

Is(Mq4): 4.55803e-005 device\_current

Id(Mq3): -4.93894e-005 device\_current

Ig(Mq3): 1.44961e-009 device\_current

Ib(Mq3): -1.89107e-011 device\_current

Is(Mq3): 4.9388e-005 device\_current

Id(Mq2): -4.5588e-005 device\_current

Ig(Mq2): 4.47265e-010 device\_current

Ib(Mq2): -6.27307e-013 device\_current

Is(Mq2): 4.55875e-005 device\_current

Id(Mq1): -4.9389e-005 device\_current

Ig(Mq1): 4.40984e-010 device\_current

Ib(Mq1): -9.4603e-013 device\_current

To save the trouble of summing and multiplying the whole stack of base currents and gate currents let’s take a guestimate and call the leakage power :

(5 transistors)\*(leakage current/transistor)\*(1V median voltage) = 50nW

We can do a more definitive measurement on the final wide swing current implementation.

**Temperature Coefficient**: Running a temperature sweep while sweeping *vdd* from 1.3V to 1.8V shows the same range of positive and negative temperature coefficients as the SPICE model for short channel low voltage MOSFETS. The *Tempco* for *vdd* = 1.8V is -42nA/C which matches very closely with the SPICE *Tempco* value of *40uA*/C.

The **output resistance** is found from disconnecting the PMOS amp, setting *vout* = 550mV, and then running the .op analysis. Rout = *vout*/Id(Mq4) = 12.2kΩ which is reasonably close to the 10kΩ of the SPICE analysis.

The **input resistance** is found with a .op analysis similar to the output resistance. The input resistance measures 32.6kΩ which matches the SPICE based analysis.

**vout-minimum** = 550mV.

**vout-maximum** = rail voltage (with no common source amp).

**Vin** is set by the operating point of the Q3-Q1 transistors and R. 1.602V.

**Gain** = -15.8 This is dramatically lower than the -51 from the SPICE analysis. Moving around the bias point proves that -15.8 is the maximum gain for the dc small signal transfer function. Considering that gain is:

and that the output resistance of the layout matches the SPICE model, either the transconductance of Q5 or the drain source resistance of Q5 are different in the layout model.

**Bandwidth =** 437MHz (Only slightly less than the SPICE model simulation. The discrepancy is probably due to real geometric capacitances that the layout model incorporates).

**Gain Bandwidth =** 437MHz

**PSRR** = -19dB This is a parameter that we should improve in the wide swing design. The easiest way to improve it would be to use a current source with better PSRR.

**Slew Rate** = 3.2GV/s which is about 100 times better than the SPICE simulation. Normally the layout simulation should be “slower” featuring more parasitic capacitances.

The layout matches the SPICE schematic based simulation fairly closely. In the wide swing current mirror rev 2, we will try to optimize the layout for peak performance to reduce parasitic.

**Current Matching**. Though this parameter was not required, it is an important characteristic for current mirrors. Sweeping the output voltage produces

**Summary**

The cascode current mirror has an improved output impedance over the source degeneration current mirror, however it suffers serious drawbacks in terms of supply voltage and operational voltage limitations. The strong trend across the electronics industry is for lower power consumption and lower voltage rails making the cascode current mirror difficult to implement in many low power applications. In the wide swing current mirror, we preserve the Rout of the cascode current mirror, but change the topology to allow a lower operating voltage both at the supply rail and at the *vout .*

**Design Improvements**

The ideal current mirror should have high PSRR, high output impedance, large output swing, low voltage supply requirements, precise current matching. The output swing and voltage supply limits will be improved by the wide swing current mirror topology. The PSRR is the area most in need of improvement. Changing from the resistive current source to an active current source with better PSRR will improve the circuit. The current matching ability of the cascode current source suffers from the relatively high output voltage. This should be improved in the wide swing version.

1. Carusone, Tony Chan. *Analog Integrated Circuit Design, 2nd Ed.* , Table 5.1 [↑](#footnote-ref-1)
2. A reference of BSIM4 SPICE parameters can be found at <http://www.ece.uci.edu/docs/hspice/hspice_2001_2-173.html> . The BSIM4.3.0 MOSFET manual can be found at http://www.idea2ic.com/PlayWithPerl/Bsim\_Ref/BSIM4\_manual.pdf [↑](#footnote-ref-2)
3. Sanjay, Pathadia et. al. pg 1. LDO PSRR Measurement Simplified. Texas Instruments Application Report 2009. http://www.ti.com/lit/an/slaa414/slaa414.pdf [↑](#footnote-ref-3)
4. Design Impact of Positive Temperature Dependence on Drain Currents in sub-1V CMOS VLSIs. Kouichi, Kanda et. al. Pg 1559, IEEE Journal of Solid State Circuits. Vol. 36, No. 10. http://lowpower.iis.u-tokyo.ac.jp/~kawapy/publications/IEEEJSSC01PTD.pdf [↑](#footnote-ref-4)