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Cascode Current Mirror Rev2

**Overview**

The cascode current mirror has an improved output resistance compared to the source degenerated current mirror, but at the cost of reduced headroom. The minimum operating range for the input voltage to the cascade current mirror is 2(Vtn + Vov). The minimum operating voltage for the output port is Vtn + 2Vov. Using the 50nm cmosedu\_models library gives a VTHO = 0.22V spice parameter for the threshold voltage. This means that the current mirror can function with input and output voltages of as low as 0.44V and 0.22V, but only with a negligible current of several microamps. Our Ibias current is chosen as 50uA which the cascade current source cannot sustain with a vdd = 1V operating rail. See Figure 1 *Cascode Current Mirror*

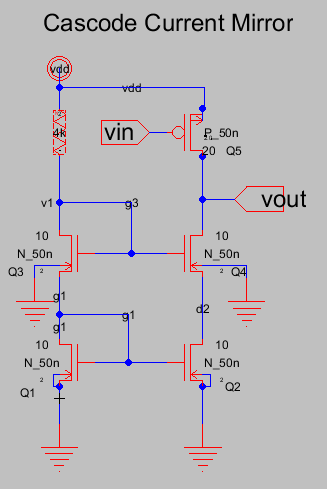


Figure Cascode Current Mirror showing Resistive current source. Note that *v1* is the input voltage of the current mirror and *vout* is the output voltage of the current mirror that determine the operating range of the cascade current mirror. Q5 isthe common source amplifier.

The parameters that we are using for this simulation are:

Vdd = 1(V)

Ibias= 50(uA)

W/L = 5

VTHO = 0.22(V)

The cmosedu\_models.txt spice file is a level 54 spice simulation meaning that we cannot readily get the for the circuit. Instead we bias the circuit properly so that all the transistors are in saturation, then produce the signal on the waveform.

which is not remotely far from the 280 listed for the 45nm CMOS process in table 1.5. What does this mean for the Ibias and input voltage of our circuit?

Suppose Ibias = 50uA. Then 0.47V .

Then the input voltage would be 2(Vtn + Vov) = 2(.22 + .47) = 1.38V > Vdd = 1V. If we put a 50uA ideal current source for Ibias, we show the input voltage to be simulated at 1.6V. In other words, the cascode current source lacks the headroom to source or sink a significant current with a low supply rail. For the sake of comparison, let’s increase the supply rail to 1.8V and sweep the output node vout to produce a graph that shows the operation of the cascade current mirror. See Figure 3.

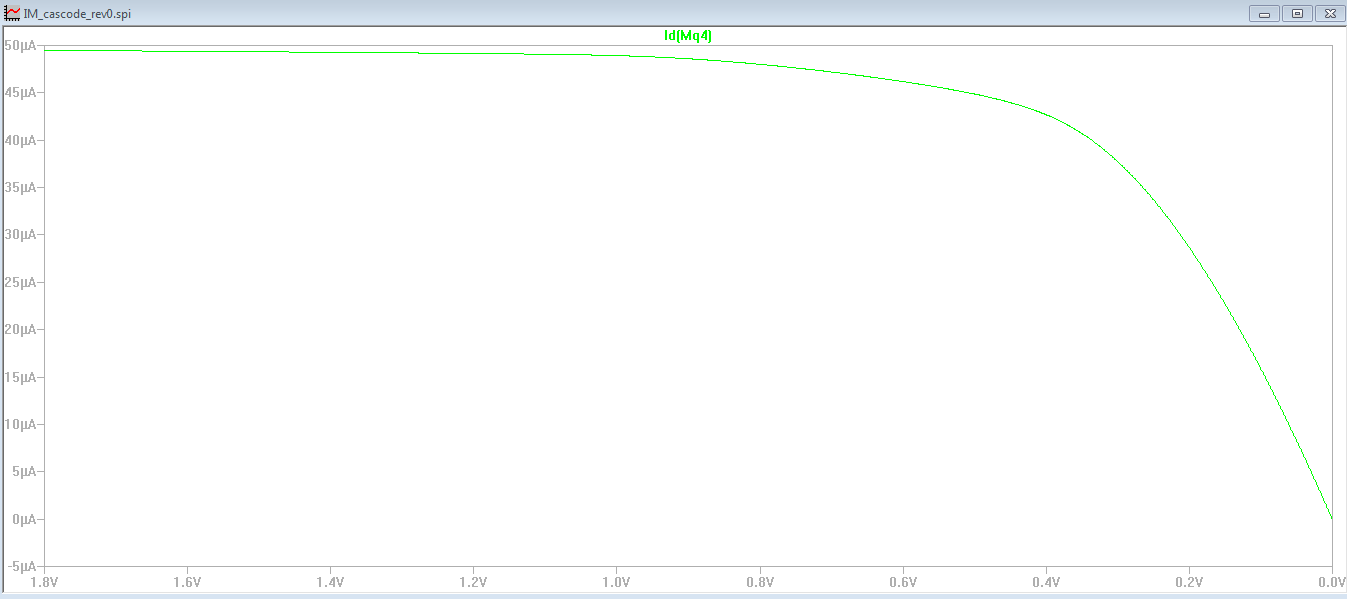


Figure DC sweep of the output voltage *vout* showing the current mirror falling off when *vout* approaches Vtn + 2Vov = 550mV. This sweep is with a rail voltage of Vdd = 1.8V.

If we define the current mirror to be in operation when Iout = Ibias +- 10%, then

Vout minimum = 500mV with Ibias supplied by an ideal current source. When using a resistive current source (R = 4kΩ for Ibias = 50uA) and a 1.8V supply rail, Vout minimum = 550mV. Without the higher Vdd, the circuit would not be able to source 50uA. See Figure 4 .

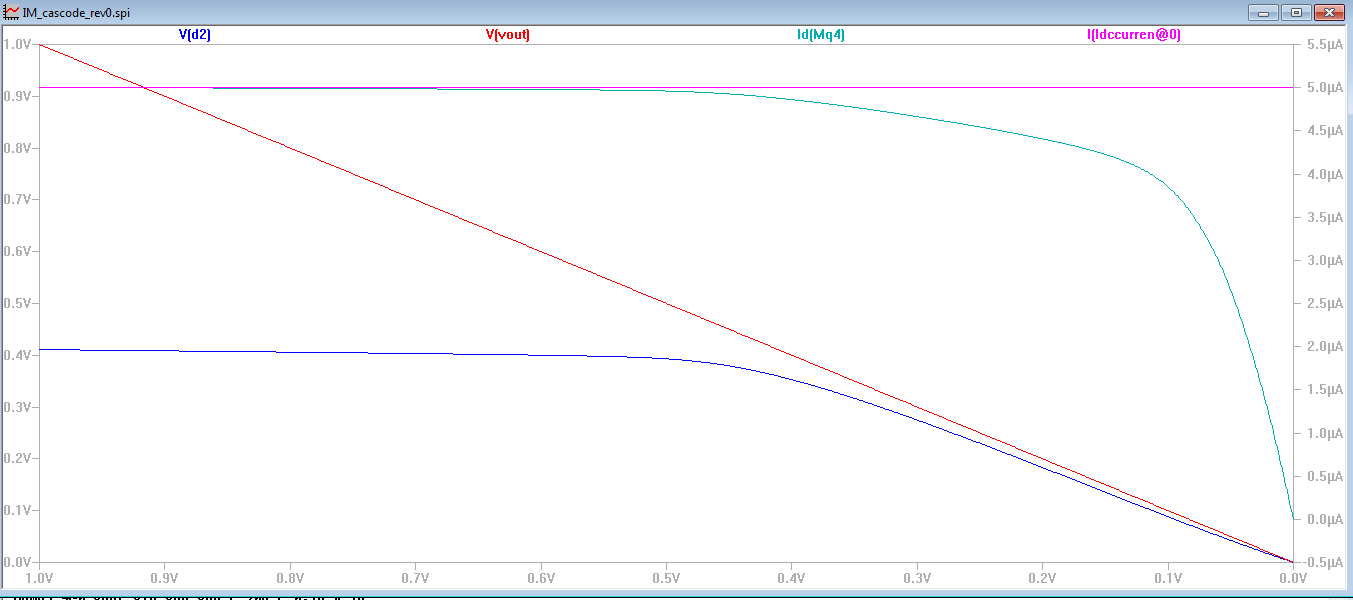


Figure The cascade current can operate at a lower vout approaching Vtn provided that the bias current is sufficiently small. The output current I(Mq4) (blue) falls off as Vout drops below 250mV. With negligible current, Vov Note that this result is from a 5uA ideal current source.

For the PMOS common source amplifier, it is required that *vin* – *vdd* < vtho = -.22V. Then the operating range of the current mirror extends up to *vdd*  - 0.22V.

The range of *v1* the input voltage is essentially 0, because the *v1* is fixed by the bias current.

This means that any change in the input voltage *v1* will necessarily change the and thus change the bias current. With the 4kΩ resistor and *a* 1.8V supply rail, *v1* = 1.64V.

This then is what we want to see in improved versions of the current mirror:

1. Minimize voltage supply.
2. Minimize the output voltage *vout* and input voltage *v1* of the current mirror to maximize range of operation.

One of the most important parameters of current mirror is the output resistance . For example when used as the load on an op-amp, the output resistance multiplies the gain of the amplifier. The output resistance of the cascade current mirror is:

= 22.6kΩ

Where Here we assume that 𝜆 = 2.0(m/V) using the 45nm CMOS process value from table 5.1 from  *Analog Integrated Circuit Design[[1]](#footnote-1)*.

= 0.12ms (estimated as = from a DC sweep of v1)

To check these calculations with simulation, we disconnect the common source transistor from the current mirror, and run a DC sweep of the vout terminal. See Figure 4.

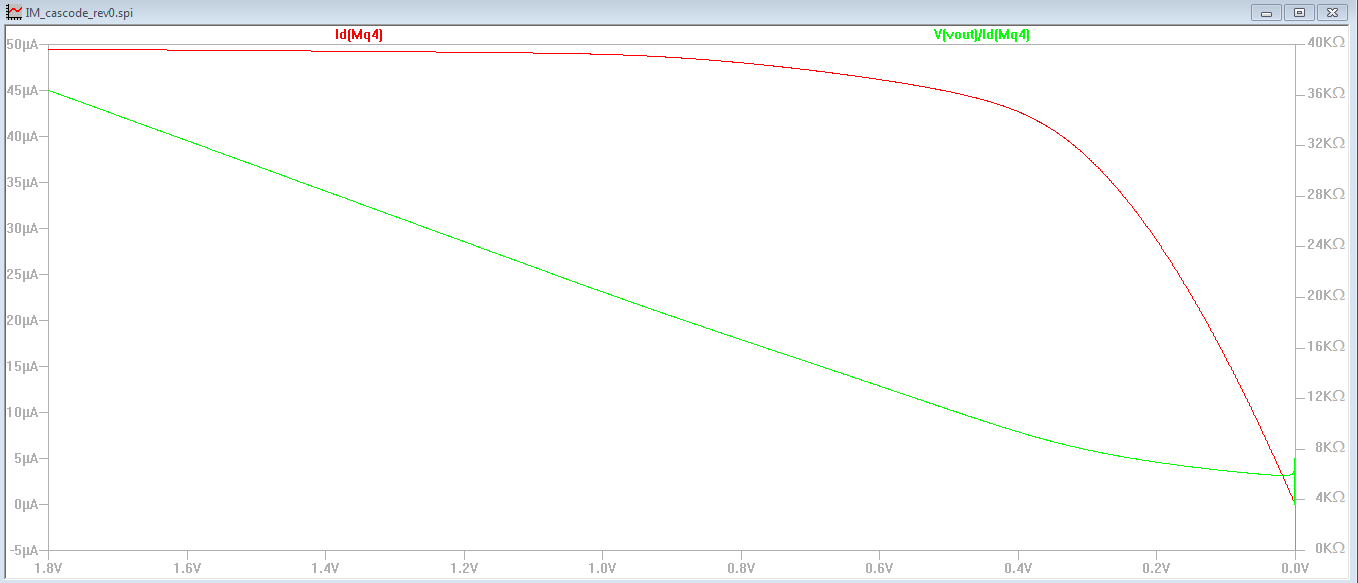


Figure 4. Output Resistance of Cascode Current Mirror with 4k resistive current source, and Vdd = 1.8V. When the transistors are all in saturation at *vout* = 500mV, the output resistance is 10k.

The results of the simulation show that the output impedance = taken when *vout* = 500mV which is at the lower operating range of the output voltage. This is in agreement with our hand calculations. To increase we would need to increase the drain to source resistance (by decreasing the drain current), or increasing the transconductance of Q4. The transconductance parameter is dependent upon and that are under the control of the circuit designer.

Then this makes

which suggests that when Ibias = 100uA, = = .35\*10kΩ = 3.5kΩ.

Changing to an ideal Ibias current source and sweeping from 50uA to 100uA we expect to see the output impedance decrease. In the simulation, at *vout* = 550mV, the output impedance ranges from 12kΩ (at Ibias = 50uA) to 7.1kΩ (at Ibias = 100uA) which is twice what we’d expect, but does prove the concept that increasing the bias current decreases the output resistance. See Figure 5 .

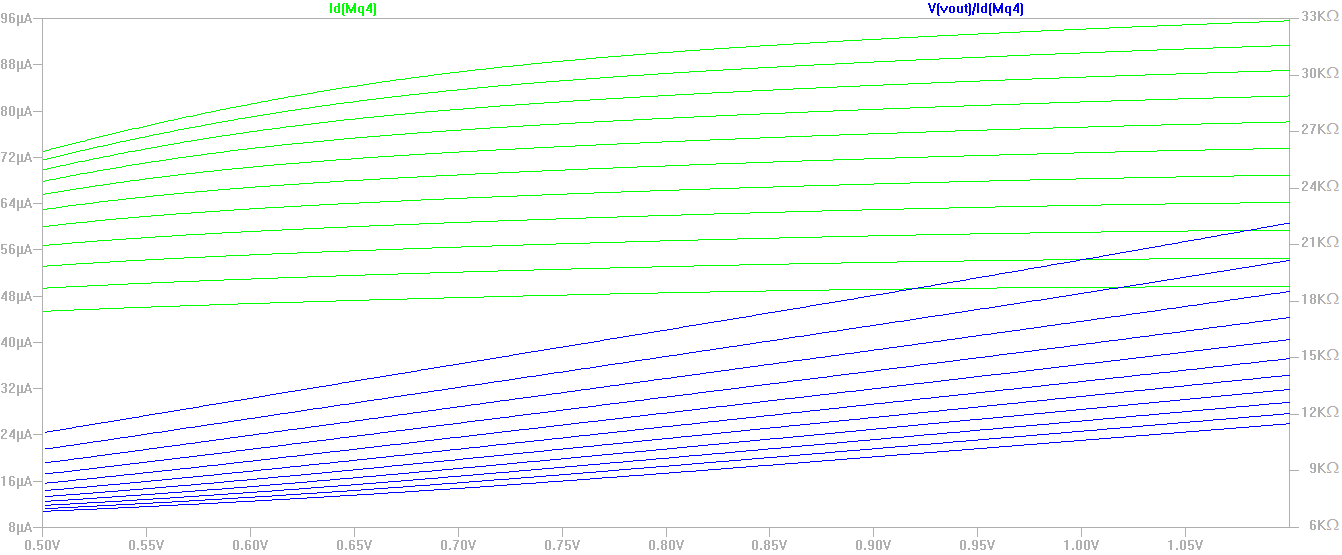


Figure 5. Effect of increasing Id on output resistance. Here Id is swept from 50uA to 100uA. As Id increases, the output resistance goes down proportional to .

The input resistance of the circuit is calculated from the small signal model.

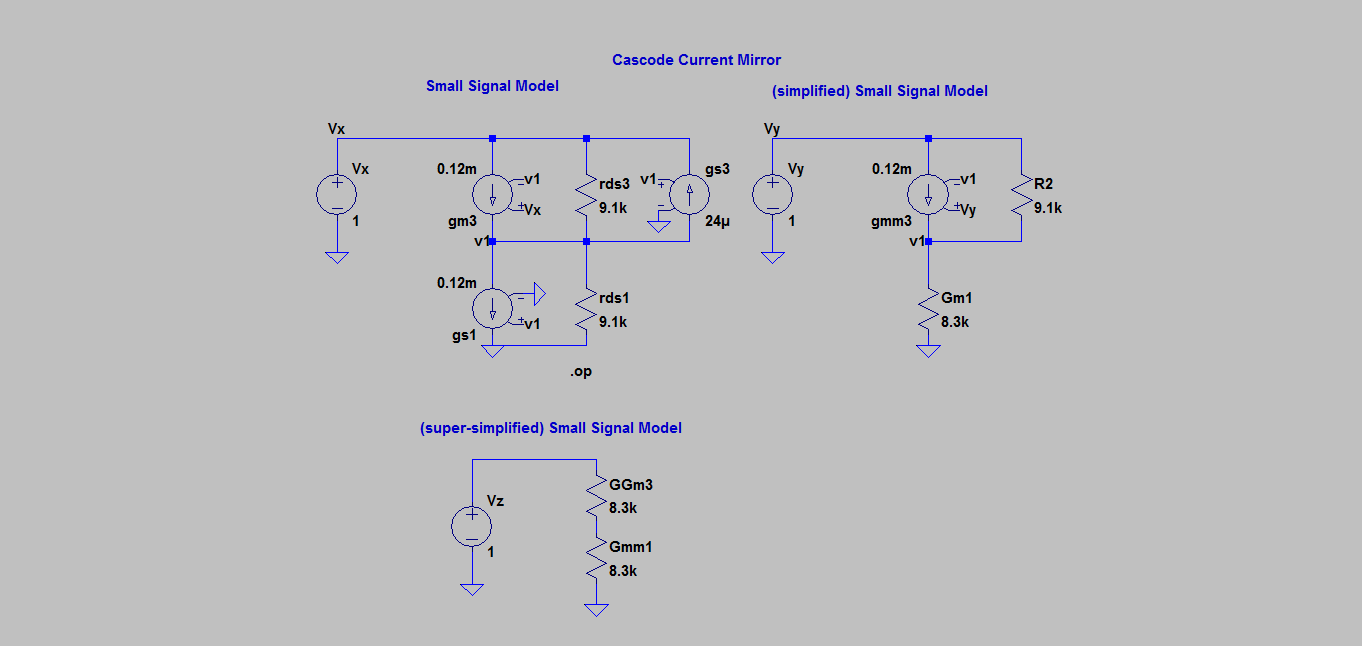


Figure Small signal model of the Cascode Current mirror. The input resistance Rin = vx/ix.

Running a spice simulation to find the operating point of the circuit yields the following:

--- Operating Point ---

V(vx): 1 voltage

V(v1): 0.551195 voltage

V(vy): 1 voltage

V(n001): 1 voltage

V(n002): 0.5 voltage

I(Ggm3): 6.0241e-005 device\_current

I(Gmm1): 6.0241e-005 device\_current

I(Rds1): 6.05708e-005 device\_current

I(Gm1): 6.6409e-005 device\_current

I(R2): 4.93193e-005 device\_current

I(Rds3): 4.93193e-005 device\_current

I(Gmm3): 5.38566e-005 device\_current

I(Gs3): 1.32287e-005 device\_current

I(Gs1): 6.61434e-005 device\_current

I(Gm3): 5.38566e-005 device\_current

I(Vz): -6.0241e-005 device\_current

I(Vy): -0.000103176 device\_current

I(Vx): -8.99473e-005 device\_current

Full small signal model

Simplified small signal model (no body effect)

Super-simplified model (for hand analysis)

The electric-vlsi calculation of Rin yields an input resistance of 32kΩ. See Figure 5 .

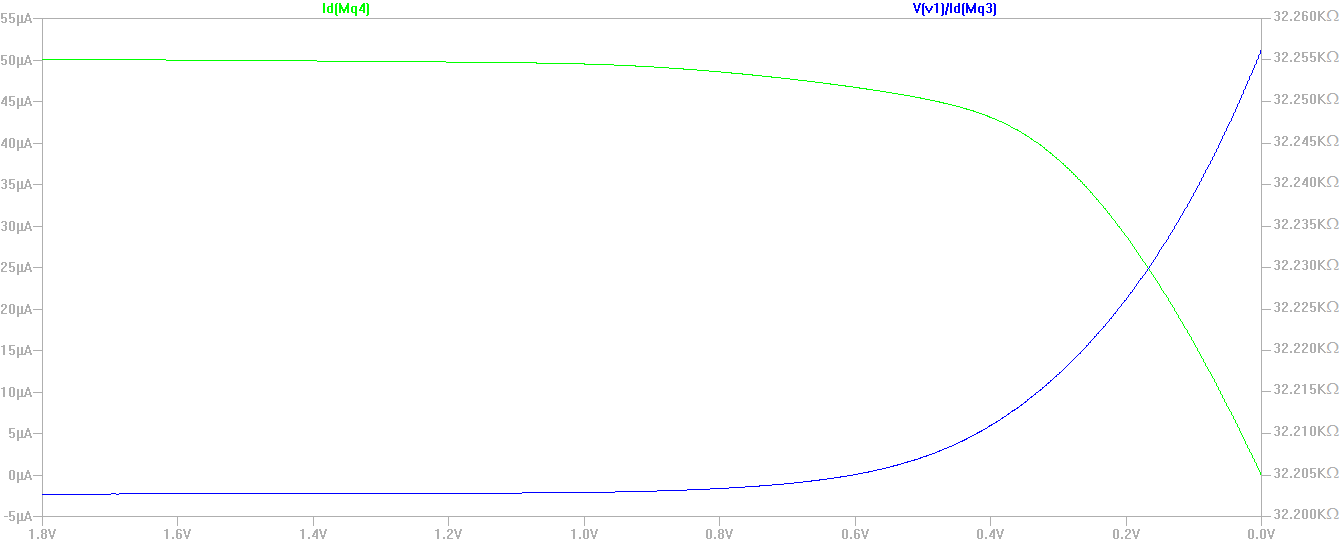


Figure Input resistance of the cascode current mirror is a very constant 32.2kΩ while the transistors are in saturation.

The electric-vlsi simulation of the cascode circuit shows Rin = V(v1)/Id(Mq3) = 32kΩ. The difference between the hand calculations and the electric simulation probably lies with my assumptions about the drain source resistance and the transconductance parameter.

The gain of the common source amplifier can be characterized once the DC operating point is found. The dc operating point can be found by sweeping *vin* and setting the dc operating point where the slope of is highest. This is shown in the DC sweep below in Figure 6 .

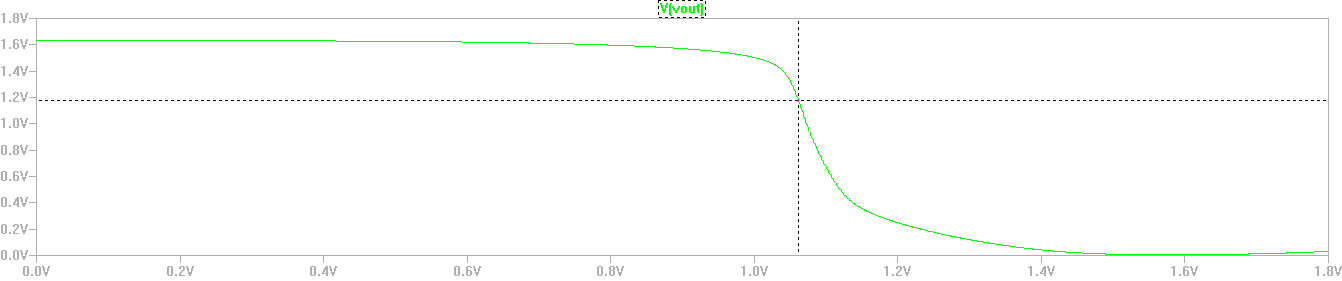


Figure DC sweep of the input voltage of the common source amplifier to find the dc operating point where the gain is maximized.

Setting *vdd* = 1.06V we can run the transfer function command to find the DC small signal transfer function of the system.

--- Transfer Function ---

Transfer\_function: -51.3026 transfer

vin#Input\_impedance: 3.31806e+006 impedance

output\_impedance\_at\_V(vout): 486646 impedance

To find the bandwidth of the circuit we set the DC operating point of the *vin* node, then do an AC sweep of the circuit. See schematic below Figure 7.

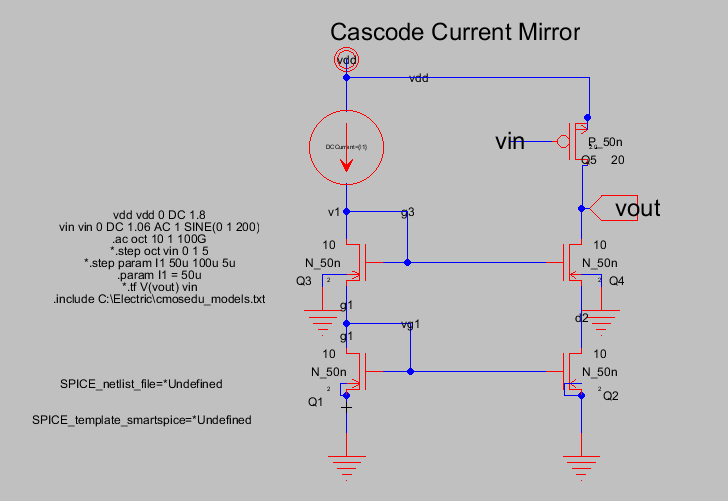


Figure Complete Cascode Current Mirror circuit with PMOS common source amplifier. Spice code for simulating an AC sweep is included.

The simulation shows a cutoff frequency of 525MHz. Note that the DC gain is 24dB = 15.8 . This is less than the .tf analysis of gain = -51, however the gain is highly susceptible to dc bias point. Setting the DC bias point as a parameter, and sweeping the parameter gives the following graph showing the sensitivity of the gain to the dc bias point. See Figure 8. However, the DC gain is maximized at about 16, so this still does not explain why the AC sweep gives a different gain than the .tf small signal analysis of the DC operating point.

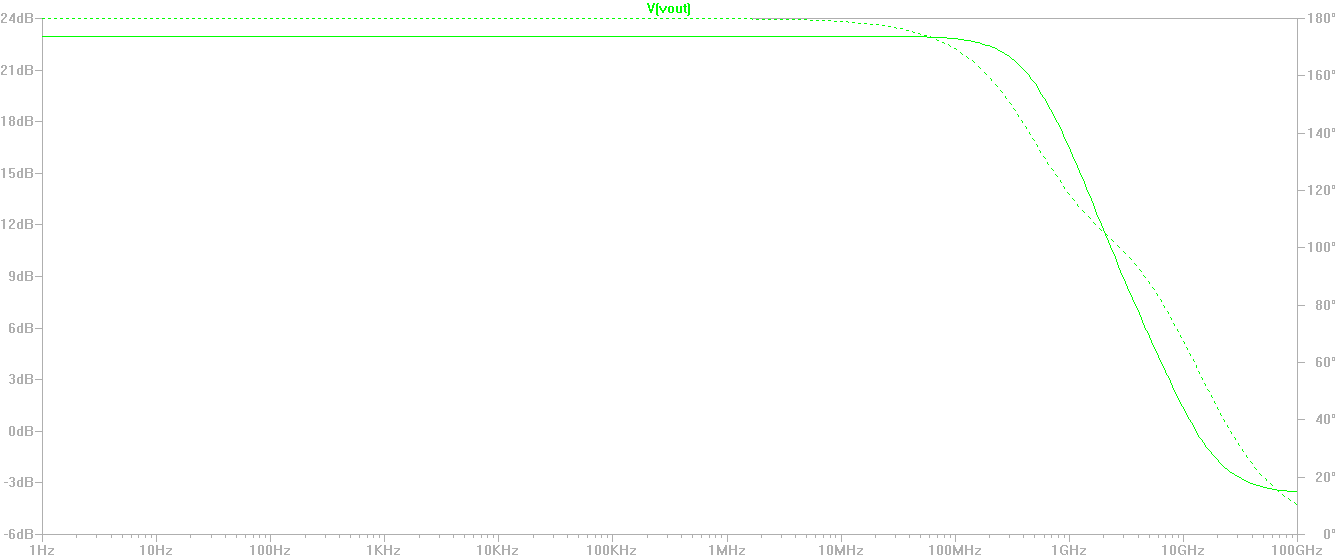


Figure Bode Plot of cascode current mirror with common source amplifier.

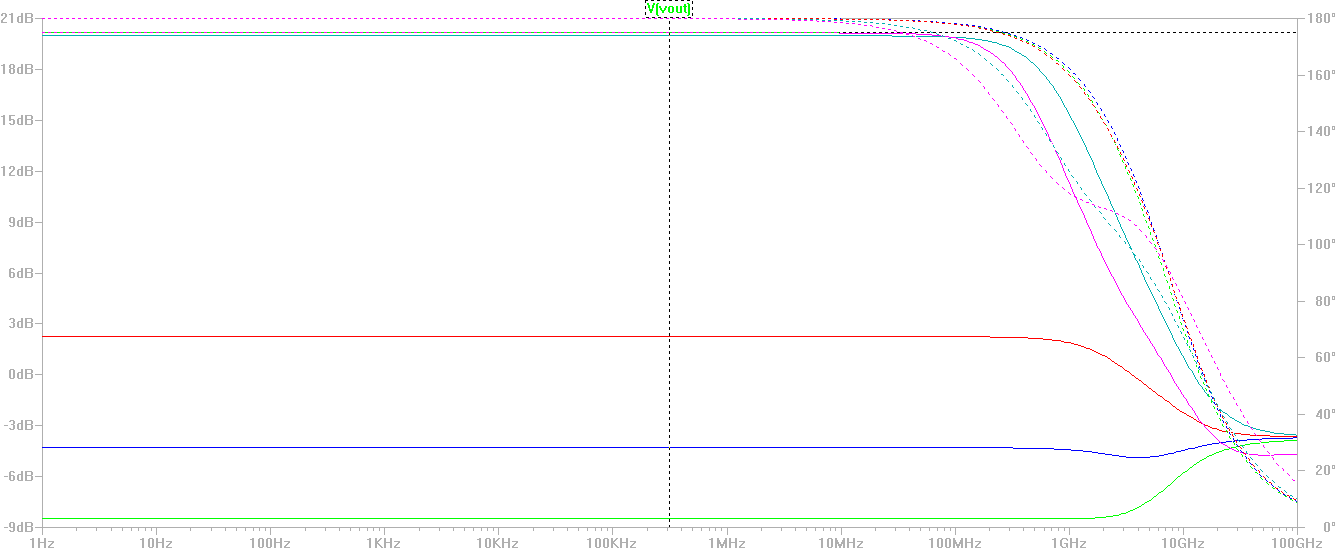


Figure AC sweep of the common source amplifier with *vin* = {900,950,1000,1050,1100}mV showing the variability of gain when the dc bias point is moved.

The Power Supply Rejection Ratio (PSRR) is the susceptibility of the system to changes in the power supply. For the current mirror, this is:

The common source amp is disconnected, the current source is a resistive source, and a DC sweep of *vdd* is performed. Note that both *vout* and *v1* are swept within the operating range of the current mirror. The change in *vdd* has a linear effect on the output current, where the change in the output voltage *vout* is neglible. See Figure 10.

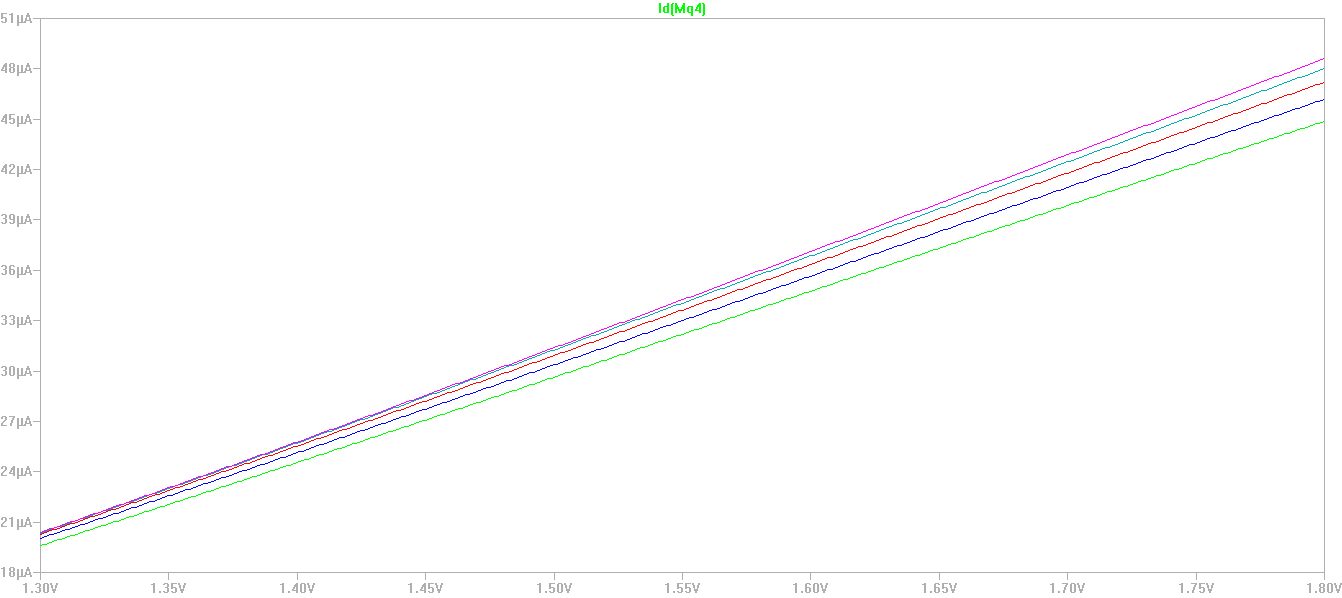


Figure The PSRR for a resistive current source is very very poor! There is a strong and linear relationship between the supply rail voltage and the output current.

This number should be high, because any change in vdd will directly effect the overdrive voltage of the Q1 and Q2 bias current transistors.

The threshold voltage and mobility of mosfet transistors is temperature dependent. For small Vdd transistors where the threshold voltage is approximately 200mV, the negative temperature coefficient of the threshold voltage surmounts the mobility degradation with the effect that the drain current increases with temperature. Note that this temperature relationship is different for micron scale higher Vdd transistors. The drain current is affected proportionally2

where

T = temperature

= room temperature (300 K)

K = threshold voltage coefficient (typically 2.5mV/K)

m = mobility temperature exponent (typically 1.5)[[2]](#footnote-2)

= velocity saturation index (typically 1.3 for short channel mosfets)

Also define the temperature coefficient for change in drain voltage over temperature:

Applying a temperature sweep to an N\_50n NMOS and P\_50n PMOS transistor from the cmosedu\_models library creates the following I-V curve. See Figure 11.

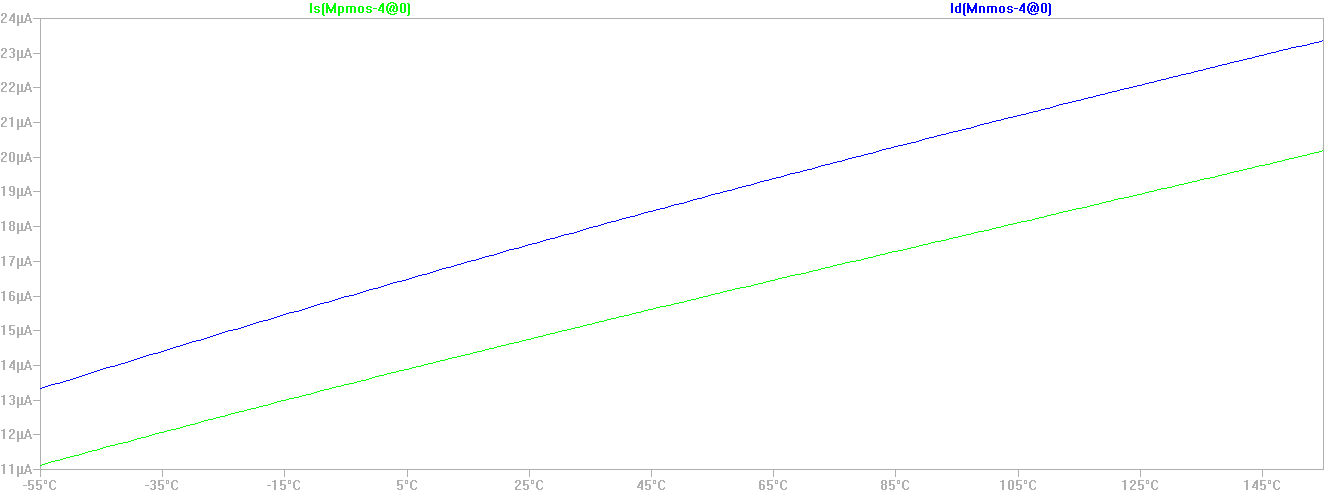


Figure Temperature dependence of PMOS (green) and NMOS (blue) transistors currents for *vdd*=1.0V, gate voltage = .5V. Short channel mosfets have a positive temperature coefficient.

We would expect the drain current of the single N\_50n NMOS transistor current mirror to increase with temperature over a 50K sweep

This shows that the drain current decreases with increasing temperature. That is opposite what the authors of the paper suggested. It could be that the values for velocity saturation and *m* mobility temperature exponent are estimated incorrectly. It is also possible that the temperature equations that I am using, are meant to apply to a smaller Vdd than 1V. As an experiment I swept the Vdd parameter on the full cascode current mirror from 1.3V to 1.8V while doing a temperature sweep. The result is interesting because it shows the temperature coefficient changing sign from a positive value at Vdd= 1.3V to a basically *Tempco* = 0 at Vdd = 1.5V, to a negative value when Vdd = 1.8V. See Figure 12.

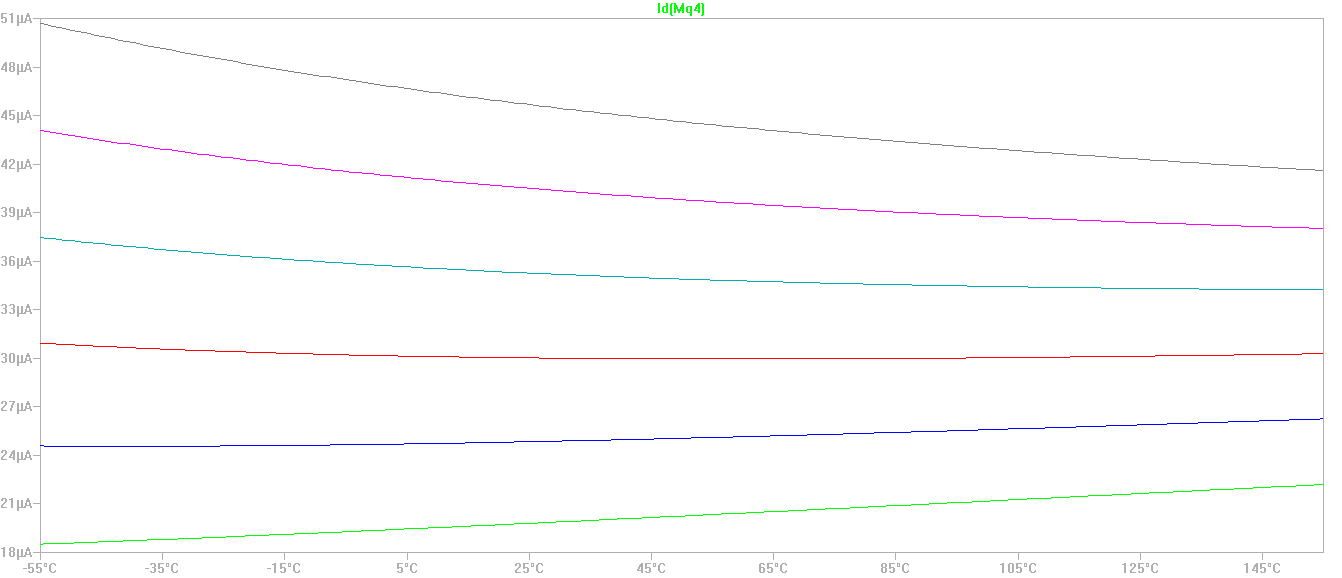


Figure Effect of Temperature and Vdd on short channel MOSFET cascode current mirror. Note that *Tempco* is positive for *vdd* = 1.3V (green line on bottom of graph), and *Tempco* is strongly negative for *vdd* = 1.8V.

For the graph above, choosing the *vdd* = 1.8V (the 4k resistor was sized for a rail voltage of 1.8V which is why the drain current equals 50uA for *vdd* = 1.8V, and only 20uA for *vdd* = 1.3V) and for consistency with the other cascode current parameters, the *Tempco* of the circuit at *vout* is:

The slew rate is a measure of the response speed of the amplifier. The slew rate is defined as:

Where is the initial time when the input waveform makes a step change. It is important to distinguish between the RC response and slew rate of the amplifier under discussion. The step at the input response must be large enough so that the linear slew rate is clearly visible from the exponential RC response. Giving a step signal to around the operating point of the circuit gives the output waveform of Figure 13. The slew rate is measured as

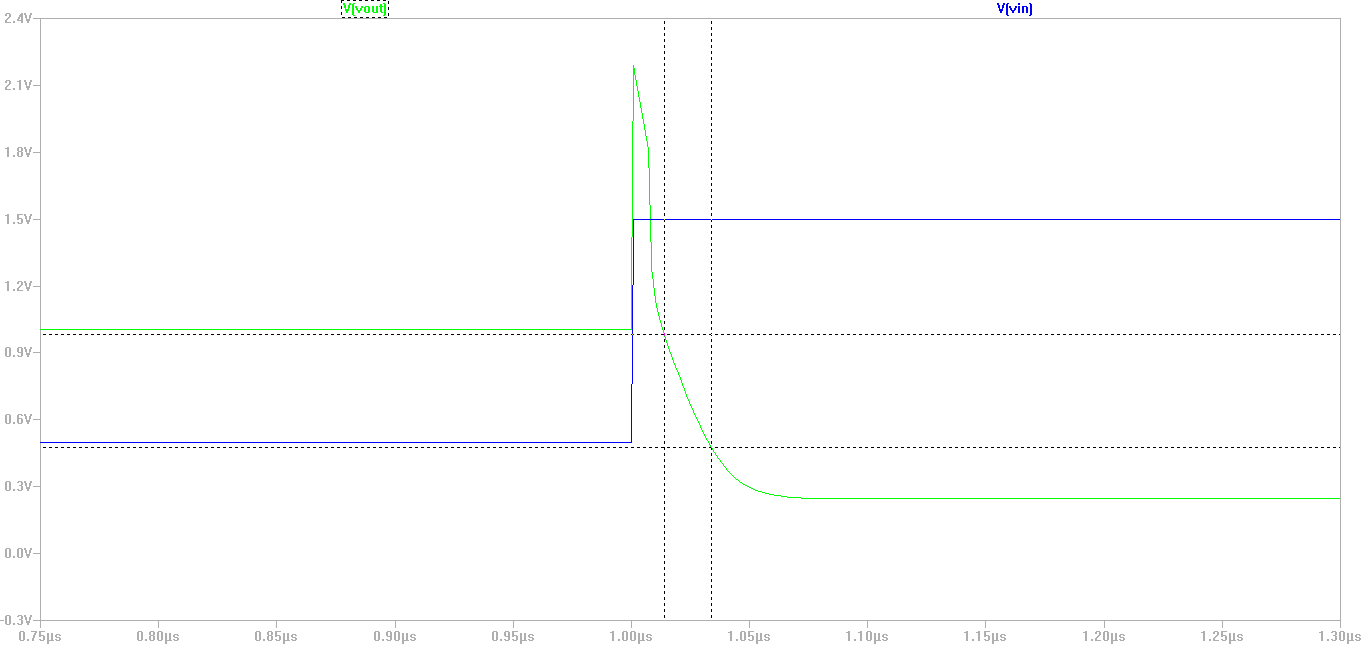


Figure Slew rate of the common source PMOS amplifier. The slew rate is visible as the linear section of the waveform highlighted between the crosshairs. The spike in the green *vout* signal is probably caused by inductance.

Discussion: Why does the wide-swing offer the best tradeoff? Why is low Vout current mirror important in circuits with steadily declining voltage supply overhead? What are the tradeoffs between Wide-swing rev0 and rev1? What would a current mirror normally interface with? What is the frequency response of the IM with a common-source amp at the output?

Sweeping Vout from 5V to 0V, it is clear that the current mirror decays once Q2 and Q4 leave saturation.

Note that where

=.6696 + .6()

= .736V

\* BSIM3 models for AMI Semiconductor's C5 process

\*

\* Don't forget the .options scale=300nm if using drawn lengths

\* and the MOSIS SUBM design rules

\*

\* 2<Ldrawn<500 10<Wdrawn<10000 Vdd=5V

\* Note minimum L is 0.6 um while minimum W is 3 um

\* Change to level=49 when using HSPICE or SmartSpice

.MODEL NMOS NMOS ( LEVEL = 8

+VERSION = 3.1 TNOM = 27 TOX = 1.39E-8

+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.6696061

+K1 = 0.8351612 K2 = -0.0839158 K3 = 23.1023856

+K3B = -7.6841108 W0 = 1E-8 NLX = 1E-9

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 2.9047241 DVT1 = 0.4302695 DVT2 = -0.134857

+U0 = 458.439679 UA = 1E-13 UB = 1.485499E-18

+UC = 1.629939E-11 VSAT = 1.643993E5 A0 = 0.6103537

+AGS = 0.1194608 B0 = 2.674756E-6 B1 = 5E-6

+KETA = -2.640681E-3 A1 = 8.219585E-5 A2 = 0.3564792

+RDSW = 1.387108E3 PRWG = 0.0299916 PRWB = 0.0363981

+WR = 1 WINT = 2.472348E-7 LINT = 3.597605E-8

+XL = 0 XW = 0 DWG = -1.287163E-8

+DWB = 5.306586E-8 VOFF = 0 NFACTOR = 0.8365585

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.0246738 ETAB = -1.406123E-3

+DSUB = 0.2543458 PCLM = 2.5945188 PDIBLC1 = -0.4282336

+PDIBLC2 = 2.311743E-3 PDIBLCB = -0.0272914 DROUT = 0.7283566

+PSCBE1 = 5.598623E8 PSCBE2 = 5.461645E-5 PVAG = 0

+DELTA = 0.01 RSH = 81.8 MOBMOD = 1

+PRT = 8.621 UTE = -1 KT1 = -0.2501

+KT1L = -2.58E-9 KT2 = 0 UA1 = 5.4E-10

+UB1 = -4.8E-19 UC1 = -7.5E-11 AT = 1E5

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 2E-10 CGSO = 2E-10 CGBO = 1E-9

+CJ = 4.197772E-4 PB = 0.99 MJ = 0.4515044

+CJSW = 3.242724E-10 PBSW = 0.1 MJSW = 0.1153991

+CJSWG = 1.64E-10 PBSWG = 0.1 MJSWG = 0.1153991

+CF = 0 PVTH0 = 0.0585501 PRDSW = 133.285505

+PK2 = -0.0299638 WKETA = -0.0248758 LKETA = 1.173187E-3

+AF = 1 KF = 0)

\*

.MODEL PMOS PMOS ( LEVEL = 8

+VERSION = 3.1 TNOM = 27 TOX = 1.39E-8

+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.9214347

+K1 = 0.5553722 K2 = 8.763328E-3 K3 = 6.3063558

+K3B = -0.6487362 W0 = 1.280703E-8 NLX = 2.593997E-8

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 2.5131165 DVT1 = 0.5480536 DVT2 = -0.1186489

+U0 = 212.0166131 UA = 2.807115E-9 UB = 1E-21

+UC = -5.82128E-11 VSAT = 1.713601E5 A0 = 0.8430019

+AGS = 0.1328608 B0 = 7.117912E-7 B1 = 5E-6

+KETA = -3.674859E-3 A1 = 4.77502E-5 A2 = 0.3

+RDSW = 2.837206E3 PRWG = -0.0363908 PRWB = -1.016722E-5

+WR = 1 WINT = 2.838038E-7 LINT = 5.528807E-8

+XL = 0 XW = 0 DWG = -1.606385E-8

+DWB = 2.266386E-8 VOFF = -0.0558512 NFACTOR = 0.9342488

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.3251882 ETAB = -0.0580325

+DSUB = 1 PCLM = 2.2409567 PDIBLC1 = 0.0411445

+PDIBLC2 = 3.355575E-3 PDIBLCB = -0.0551797 DROUT = 0.2036901

+PSCBE1 = 6.44809E9 PSCBE2 = 6.300848E-10 PVAG = 0

+DELTA = 0.01 RSH = 101.6 MOBMOD = 1

+PRT = 59.494 UTE = -1 KT1 = -0.2942

+KT1L = 1.68E-9 KT2 = 0 UA1 = 4.5E-9

+UB1 = -6.3E-18 UC1 = -1E-10 AT = 1E3

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 2.9E-10 CGSO = 2.9E-10 CGBO = 1E-9

+CJ = 7.235528E-4 PB = 0.9527355 MJ = 0.4955293

+CJSW = 2.692786E-10 PBSW = 0.99 MJSW = 0.2958392

+CJSWG = 6.4E-11 PBSWG = 0.99 MJSWG = 0.2958392

+CF = 0 PVTH0 = 5.98016E-3 PRDSW = 14.8598424

+PK2 = 3.73981E-3 WKETA = 5.292165E-3 LKETA = -4.205905E-3

+AF = 1 KF = 0)

1. Carusone, Tony Chan. *Analog Integrated Circuit Design, 2nd Ed.* , Table 5.1 [↑](#footnote-ref-1)
2. Design Impact of Positive Temperature Dependence on Drain Currents in sub-1V CMOS VLSIs. Kouichi, Kanda et. al. Pg 1559, IEEE Journal of Solid State Circuits. Vol. 36, No. 10. http://lowpower.iis.u-tokyo.ac.jp/~kawapy/publications/IEEEJSSC01PTD.pdf [↑](#footnote-ref-2)