Simulated Annealing Results

Phase 2's goal was to implement simulated annealing to reduce the wire length, HPWL of the input circuit's chip. To achieve this, my annealing process makes up to 167 passes over the nodes where at each pass, the algorithm makes n, the number of gates, swaps. My algorithm recalculates the total HPWL for each solution. This is inefficient and future improvements could focus on only recalculating HPWL for gates that require updating. For each new solution, the cost is calculated using the function:

$$cost = 0.7*actual_chip_width*height+0.3*total_HPWL$$

This cost function takes into account both the chip area and HPWL to minimize. This is because initial implementations of the cost function without chip area caused some rows of the chip to expand more than expected. By incorporating area into the cost, row width still goes out of the initial set bounds but not by much.

To try and combat the long runtime of this simulated annealing algorithm, I implemented an early termination condition to exit annealing if more than 10 passes occur without accepting a swap. The runtimes are still long but the idea with this approach was that, by continuing to run, we may find a few more good swaps but the solution is good where continuation is not worth the extra runtime.

The results from annealing are shown in the table below. We can see the runtime of this algorithm increases quickly and may not be viable for very large net lists. If you look at the initial HPWL in the output files compared to the final HPWL reported below, smaller net lists can see over a 50% reduction in wire length but as we increase the number of gates, that gain is still great but not as large as 50%.

Circuit Name	Chip Width	Chip Height	HPWL	Runtime
c17	5	4	24	0.166 seconds
c17_dummy	5	5	21	0.169 seconds
c423	23.5	22	1702	51.94 seconds
c499	32	30	2531.5	92.27 seconds
c880	35	33	6254.5	274.19 seconds
c1355	38.5	35	8224	531.71 seconds
c1908	45	43	14943	19.95 minutes
c2670	60	57	25554	53.93 minutes
c3540	68.5	64	41251	75.50 minutes
c5315	87.5	81	128946	3.00 hours
c6288	87	85	134674	2.87 hours
c7552	101.5	93	206584	6.09 hours