XLSEMI

上海芯龙半导体技术股份有限公司

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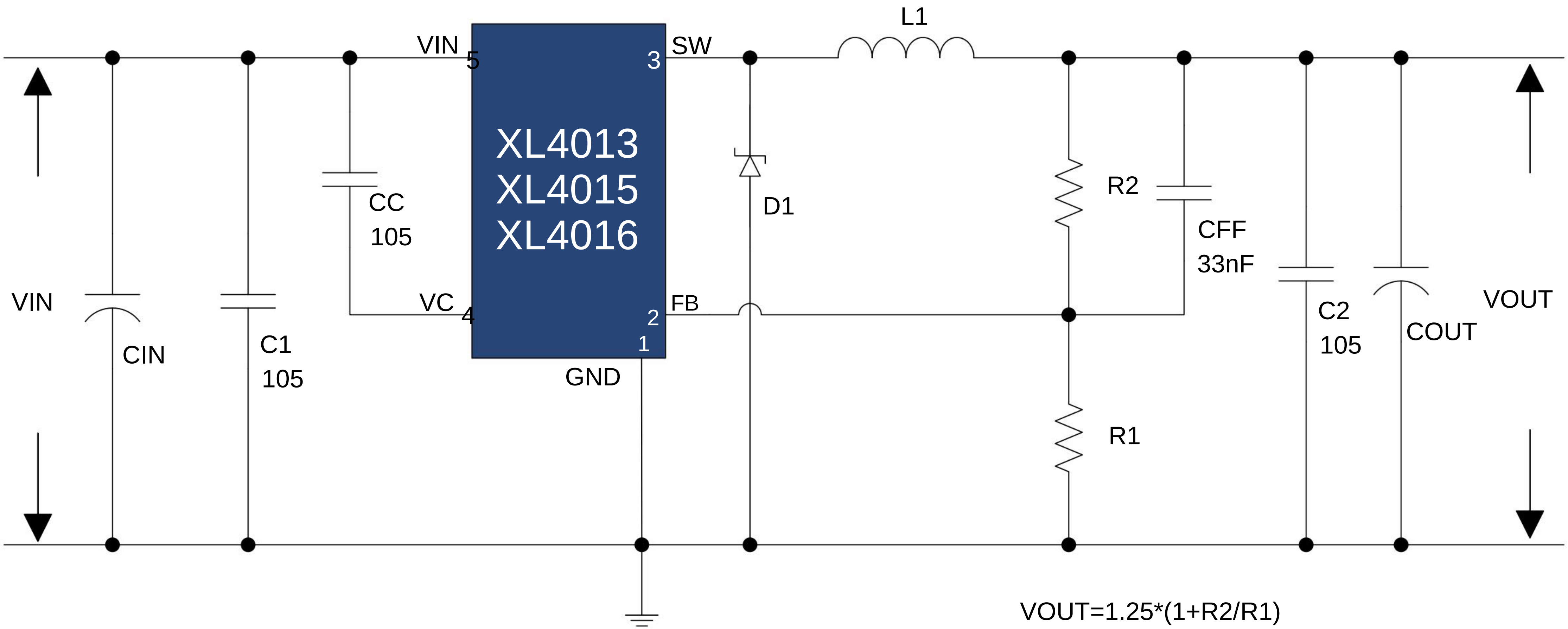
Design Guide for XL401X Series Buck Constant Voltage Products

V1.4

XL401X Series Quick Selection Table

product model	Input voltage range	switching current	switching frequency	output voltage	typical application	efficiency (Max)	package type	power
XL4013	8V-36V	4A	180KHz	1.25V~32V	5V/3A 12V/2A	94%	TO252-5L	ÿ20W
XL4015	8V-36V	5A	180KHz	1.25V~32V	5V/4A 12V/3A	94%	TO263-5L	ÿ100W
XL4016	8V-40V	12A	180KHz	1.25V~32V	5V/12A 12V/6A	94%	TO220-5L	ÿ100W

Typical application circuit diagram



Capacitor ÿThe non-

continuous input current of the buck converter will generate a large ripple current on the input capacitor. The maximum RMS current of the input capacitor is calculated as follows. The maximum RMS current of the input capacitor is generated at about 50% duty cycle :

$$IRMS = IOUT * \sqrt{\frac{VOUT * (VIN - VOUT)}{(VIN)^2}}$$

ÿThe input capacitor plays the role of energy storage, filtering and providing transient current. In continuous mode, the input current of the converter is a set of square waves with a duty ratio of about VOUT/VIN. To protect against large transient voltages, low ESR (equivalent series resistance) input capacitors selected for maximum RMS current requirements must be used.

$$CIN = \frac{IOUT_{MAX} * VOUT}{ÿVIN * f_{SW} * VIN_{MIN}}$$

ÿVIN is the input voltage ripple, and FSW is the switching frequency; ÿThe

withstand voltage of the input capacitor should be selected according to

1.5*VINMAX; ÿWhen ceramic capacitors are not used, it is recommended to connect a 0.1uF~1uF high-frequency chip ceramic capacitor in parallel with the input capacitor for high frequency decoupling.

CC Capacitor

ÿVC is the internal voltage regulation bypass capacitor of the chip. The internal voltage regulation bypass capacitor needs to connect a 1uF capacitor in parallel between VC and VIN.

Output voltage design ÿFB

is the input terminal of the internal reference error amplifier of the chip, and the internal reference is stable at

1.25V; ÿFB is adjusted by detecting the output voltage through an external resistor divider network, and the output voltage calculation formula is:

$$VOUT = 1.25V * (1 + \frac{R2)}{R1}$$

The value range of R1 is 1Kÿ~10Kÿ; ÿThe

accuracy of the output voltage depends on the accuracy of the chip VFB, R1 and R2. Select a resistor with higher precision to obtain a higher precision output voltage. The accuracy of R1 and R2 needs to be controlled within ±1%.

design ÿThe selection

of the inductance depends on the voltage difference between VIN and VOUT, the required output current and the switching frequency of the chip. The calculation formula for the minimum value of the inductance is as follows:

$$L_{MIN} = \frac{(VIN_{MAX} - VOUT) * D_{MIN}}{0.3 * IOUT * F_{SW}}$$

$$D = \frac{VOUT}{VIN}$$

ÿThe minimum inductor saturation current is 1.5*IOUTMAX; choose an inductor with low DC resistance to obtain higher conversion efficiency. Freewheeling

diode selection ÿThe freewheeling

diode has current passing through when the switch tube is turned off, forming a freewheeling path; Schottky diodes need to be selected, the lower the VF value of the Schottky diode, the higher the conversion efficiency; ÿThe rated

current value of the freewheeling diode greater than the maximum output current, the average forward current during normal operation can be calculated as follows:

$$IDAVG = IOUTMAX * \frac{VIN - VOUT}{VIN}$$

ÿThe reverse withstand voltage of the freewheeling diode is greater than the maximum input voltage, it is recommended to reserve more than 30% margin.

Output Capacitor Selection

ÿLow ESR capacitors should be selected at the output to reduce the output ripple voltage. Generally speaking, once the capacitor ESR is satisfied, the capacitor is enough to meet the demand. The ESR of any capacitor, together with its own capacity, will generate a zero point for the system. The larger the ESR value, the lower the frequency band where the zero point is located, and the zero point of the ceramic capacitor is at a higher frequency, which can usually be ignored. However, compared with electrolytic capacitors, large-capacity, high-voltage ceramic capacitors will be larger in size and higher in cost. Therefore, it is a good choice to use 0.1uF to 1uF ceramic capacitors in combination with low-ESR

electrolytic capacitors. ÿThe output voltage ripple is composed of ÿVOUT_C (caused by capacitor discharge) and ÿVOUT_ESR (caused by capacitor ESR), calculated as follows:

$$ÿVOUT\_C = \frac{0.3 * IOUT}{8 * F_{SW} * COUT} \qquad ÿVOUT\_ESR = 0.3 * IOUT * ESR$$

$$ÿVOUT = ÿVOUT\_C + ÿVOUT\_ESR$$

ÿ VCOUTÿ1.5*VOUT

Output capacitor selection

ÿThe output capacitor value and ESR depend on the allowable maximum output voltage ripple and the maximum offset of the output voltage when the load current changes suddenly; when the load suddenly increases, the converter needs 2 to 3 clocks cycle to react to a drop in output voltage, the output capacitor needs to supply the sudden change in load current before the converter can react. ÿThe minimum output

capacitor capacity required for proper output voltage undershoot is calculated as follows:

$$COUT \;\text{ÿ}\; \frac{3*(I_{Oh} - I_{OL})}{f_{SW} * V_{US}}$$

ÿThe minimum output capacitor capacity required for proper output voltage overshoot is calculated as follows:

$$COUT \;\text{ÿ}\; \frac{I_{Oh}^{2} - I_{OL}^{2}}{(VOUT + V_{OS})^{2} - VOUT^{2}} * L$$

IOL: low value of load transient current;

IOH: high value of load transient current;

VUS: output undershoot voltage;

VOS: output overshoot voltage.

Precautions for PCB design: ÿVIN,

GND, SW, VOUT+, VOUT- are high current paths, pay attention to the trace width to reduce the impact of parasitic parameters on system performance;

Chip ceramic capacitors are used in combination; ÿFB traces are far away from inductors and Schottky and other

places with switching signals, where stability is required, feedback is required, FB traces are better surrounded by ground wires; ÿChips, inductors, and

Schottky are the main sources of heat Devices, pay attention to the even distribution of PCB heat to avoid local temperature rise.

Design example

system input and output specifications

ÿInput voltage: VIN=8V~30V, typical value is 12V; ÿOutput

voltage: VOUT=5V; ÿOutput current:

IOUT=3A; ÿOutput ripple voltage:

0.1V; ÿTransient Response

(1A~3A): 5%; ÿChip selection XL4013;

ÿSwitching frequency:

FSW=180KHz. Calculate the input

capacitance:

$$IRMS = IOUT * \sqrt{\frac{VOUT * (VIN - VOUT)}{(VIN)^2}} = 3* \sqrt{\frac{5* (12 - 5)}{(12)^2}} = 1479mA$$

$$CIN = \frac{IOUT_{MAX} *VOUT}{\text{ÿ}VIN* f_{SW} *VIN_{MIN}} = \frac{3* 5}{0.2* 180K * 8} = 52.08uF$$

VCIN=1.5*VINMAX=1.5*30=45V select CIN

capacity 100uF, RMS current greater than 1500mA, withstand voltage greater than or equal to 45V.

capacitor selection: Select

the CC capacitor with a capacity of 1uF and a withstand voltage of 50V.

Calculate the voltage divider

resistance: assume R1=3.3K;

$$VOUT = 1.25*\ (1 + \frac{R2)}{R1} \qquad R2 = \frac{(VOUT\ 1.25)*R1\ 1.25}{} = \frac{(5\ 1.25)*3.3\ 1.25}{} = 9.9K$$

Choose R1=3.3K, R2=10K, 1% accuracy. The calculated output voltage center value is 5.038V

Choose an inductor:

$$L_{MIN} = \frac{(VIN\ VOUT)_{MAX} * D_{MIN}}{0.3*IOUT*F_{SW}} = \frac{(30\ 5)*30\ \frac{5}{0.3*}}{3*180K} = 25.7uH$$

The minimum saturation current of the inductor = 1.5*3 = 4.5A,

select the inductance of 47uH, and the saturation current of 5A.

Freewheeling diode selection:

ÿWhen the diode is working, the maximum forward average current is generated at the maximum input voltage:

$$I_{DAVG} = I_{OUTMAX} * \frac{V_{IN} - V_{OUT}}{V_{IN}} = 3 * \frac{30 - 5}{30} = 2.5A$$

ÿSelect a Schottky diode with a reverse withstand voltage of 40V and a current capability greater

than 4A. Select output

capacitor: ÿConsider load transient response first

Output undershoot voltage <0.25V

$$C_{OUT} \text{ ÿ } \frac{3*(I_{Oh} - I_{OL})}{f_{SW} * V_{US}} = \frac{3*(3-1)}{180KHz * 0.25V} = 133uF$$

Output overshoot voltage <0.25V

$$C_{OUT} \text{ ÿ } \frac{I_{Oh}^2 - I_{OL}^2}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} * L$$

$$= \frac{3^2 - 1^2}{(5 + 0.25)^2 - 5^2} * 47uH = 146.7uF$$

Select the output capacitor capacity as 220uF.

to select the output

capacitor: ÿCalculate the output ripple voltage

$$ÿVOUT\_C = \frac{0.3* IOUT}{8* F_{SW} * COUT} = \frac{0.3* 3}{8* 180K * 220uF} = 2.84mV$$

ÿVOUT ÿVOUT_C ÿVOUT_ESR + ÿVOUT_ESR ÿVOUT ÿVOUT_C = − = −

ÿ ÿVOUT_ESR 100mV 2.84mV 97.16mV = − =

$$ÿVOUT\_ESR = 0.3* IOUT * ESR \quad ÿ= ESR = \frac{ÿVOUT\_ESR}{0.3* IOUT}$$

$$ÿ= ESR = \frac{97.16mV}{0.3* 3} = 107.96mÿ$$

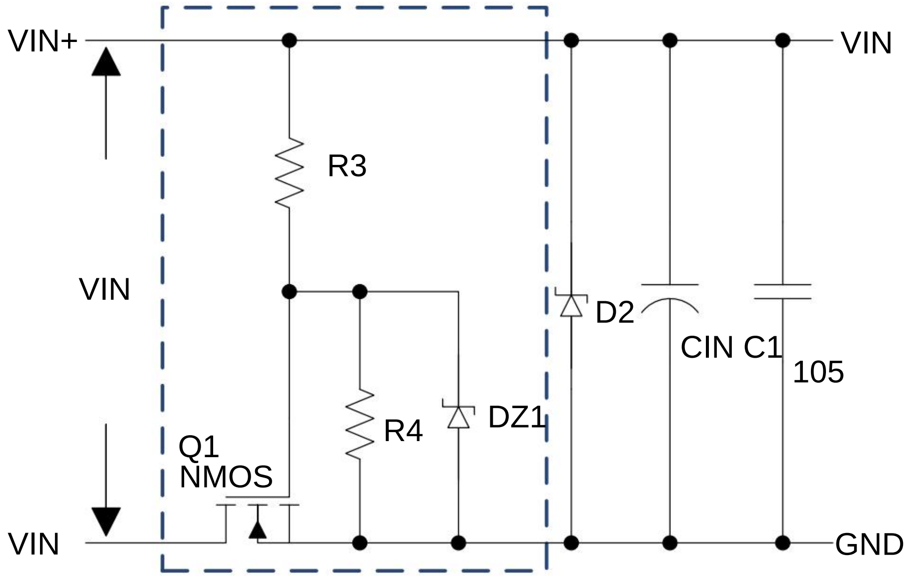
ÿFinally calculate

withstand voltage VCOUTÿ1.5*VOUT=1.5*5=7.5V

Select the output capacitor with a capacity of 220uF, an ESR of less than 0.12ÿ, and a withstand voltage of 10V.

Input positive and negative polarity reverse chip damage solution: add an anti-reverse circuit (the circuit in the blue dotted line box on the right).

Q1: VDSÿ1.5*VINMAX
DZ: VDZ=10V, 500mW
R3, R4: 20K



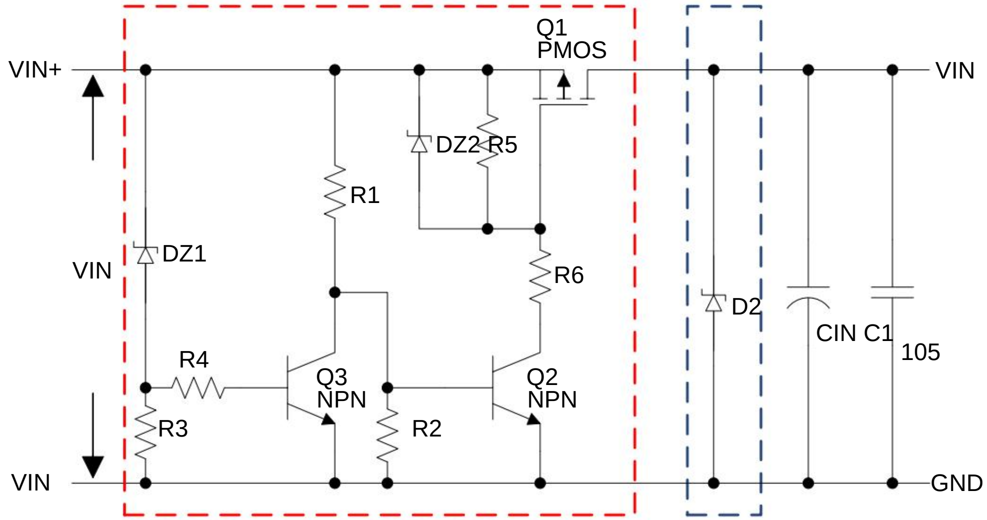
ÿQ2. Input peak voltage damage chip Solution

1: Add a transient peak voltage absorption circuit to the input (the circuit in the blue dotted line box on the right);

D2: VD2=1.2*VINMAXÿ40V

Solution 2: Add an overvoltage protection circuit to the input (The circuit in the red dotted line box on the right).

Q1: VDSÿ1.5*VINMAX
DZ1: VDZ1=1.2*VINMAX, 500mW
DZ2: VDZ2=10V, 500mW
R1, R3, R4, R5, R6: 20K; R2: 10K; Q2, Q3: VCEÿ1.5*VINMAX



Common Problems and Solutions

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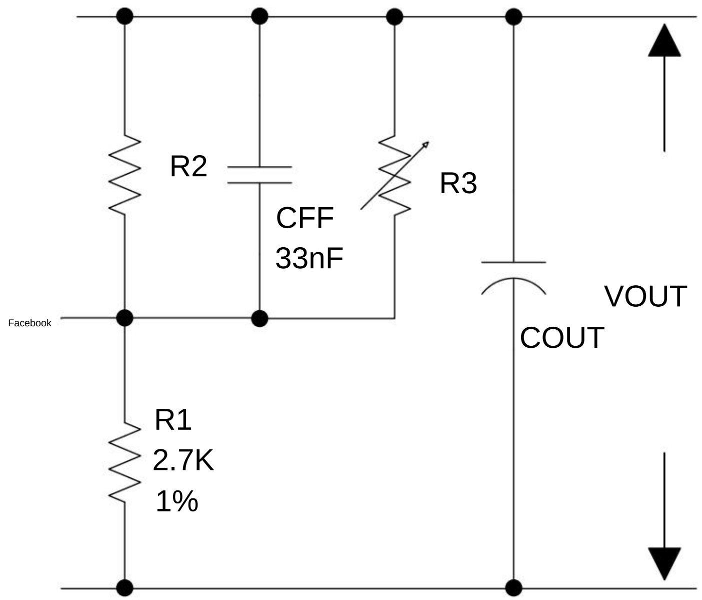
ÿQ3. How to adjust the output voltage

ÿSolution 1: Adjust the voltage divider resistor (R3 in the figure

on the

right); ÿSolution 2: Change the duty cycle of the PWM signal to adjust

the output voltage (the circuit in the blue dotted line box in the figure on the right).



PWM: frequency 1KHz~10KHz;

When the high level is 5V, R3 selects 4K; when the

high level is 3.3V, R3 selects

0.5K.

$$VOUT = \text{ÿ} VFB \quad \frac{R1*V_{PWM}*DUTY}{R1 + R3 \quad R4} \quad \text{ÿ ÿ ÿ} * 1 \ \text{ÿ} + \text{ÿ ÿ ÿ} \frac{R2}{R1} \ \text{ÿ}$$

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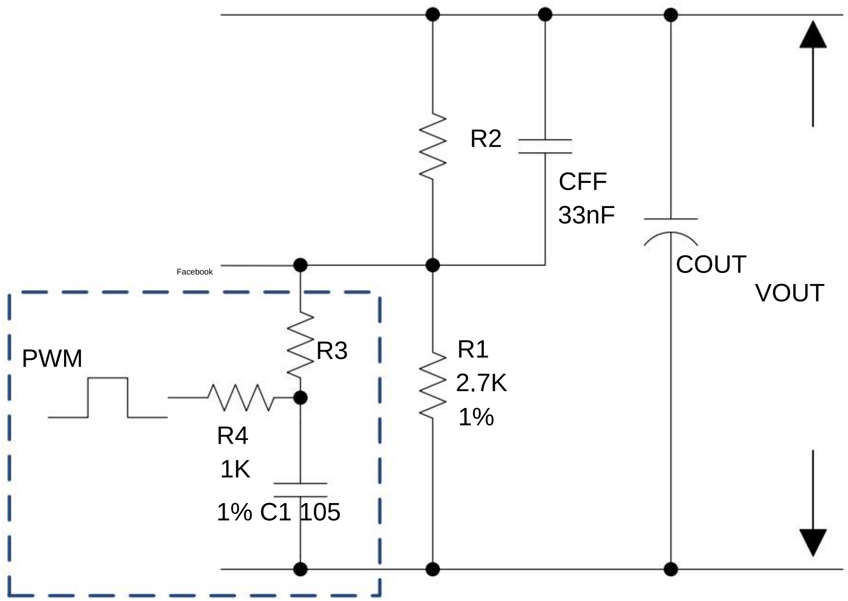
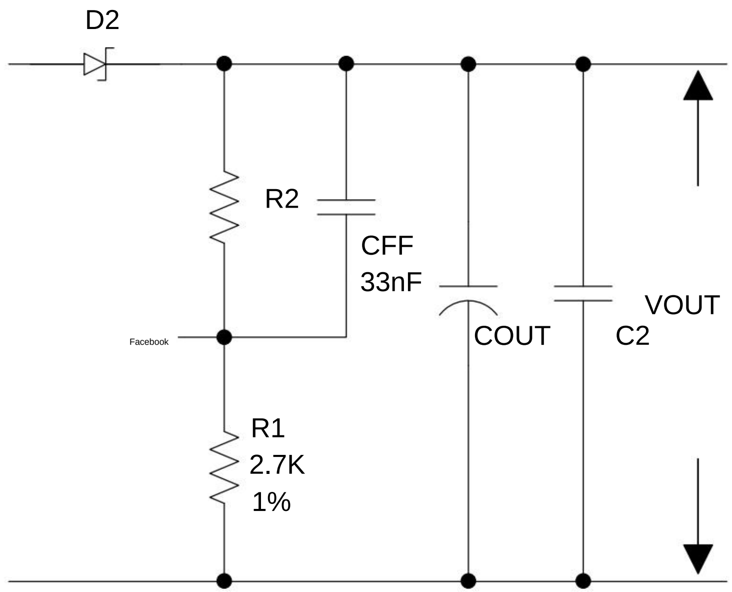


Common Problems and Solutions

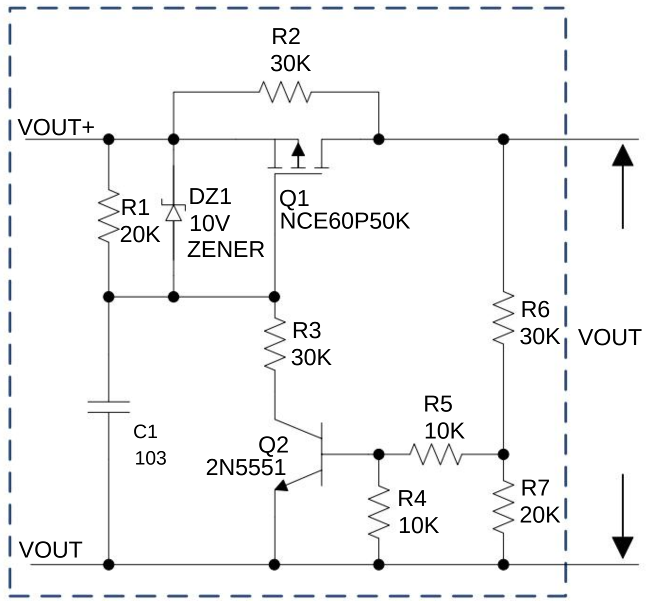
ÿQ4. When the output is connected to a battery or an inductive load, the input power-off chip is

damaged ÿSolution: add an isolation circuit to the output (D2 in the right figure)

D2: VD2ÿ1.5*VOUT; IDÿ2*IOUT



ÿQ5. How to implement the output short circuit protection ÿSolution: Add a short circuit protection circuit to the output (the circuit in the blue dotted line box on the right)



Common problems and solutions ÿQ6.

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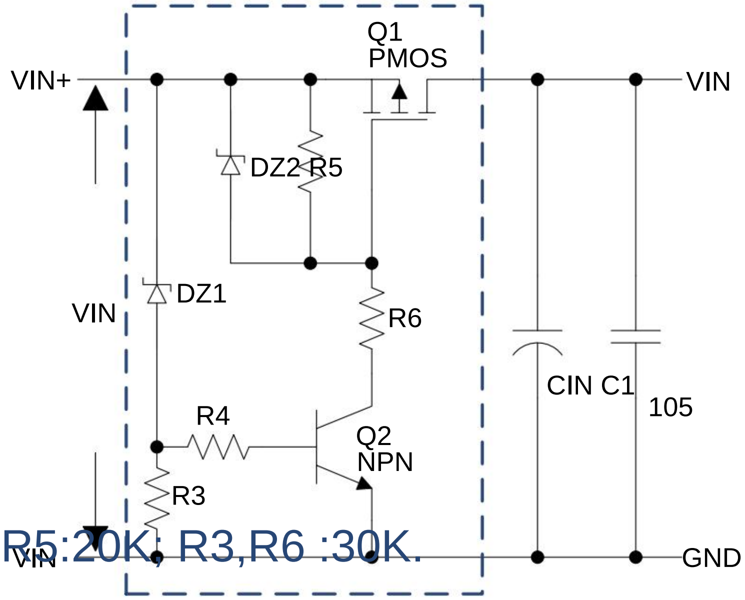
How to implement input undervoltage protection

ÿSolution: Add an undervoltage protection circuit to the input.

DZ1:VDZ1=undervoltage protection voltage; 500mW;

DZ2:VDZ2=10V, 500mW;



Q1:VDS=1.5*VINMAX,IDÿ2*IINMAX; Q2:VCE=1.5*VINMAX; R4,R5:20K; R3,R6 :30K.

ÿQ7. The electrical properties of the chip back iron

ÿThe electrical properties of the chip back iron are consistent with the third pin, which is

SW.

Common Problems and Solutions

ÿQ8. How to turn off the output

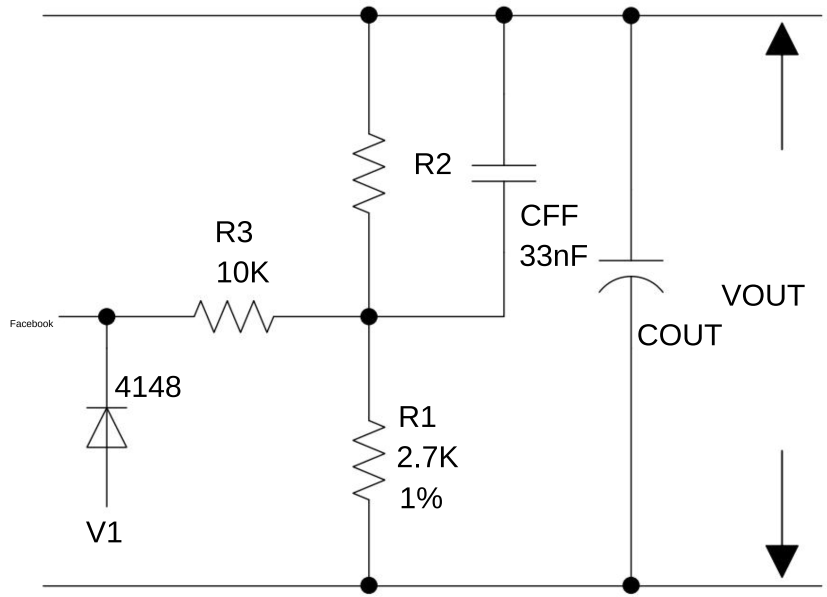
ÿSolution 1: Add high level to FB (upper right picture);

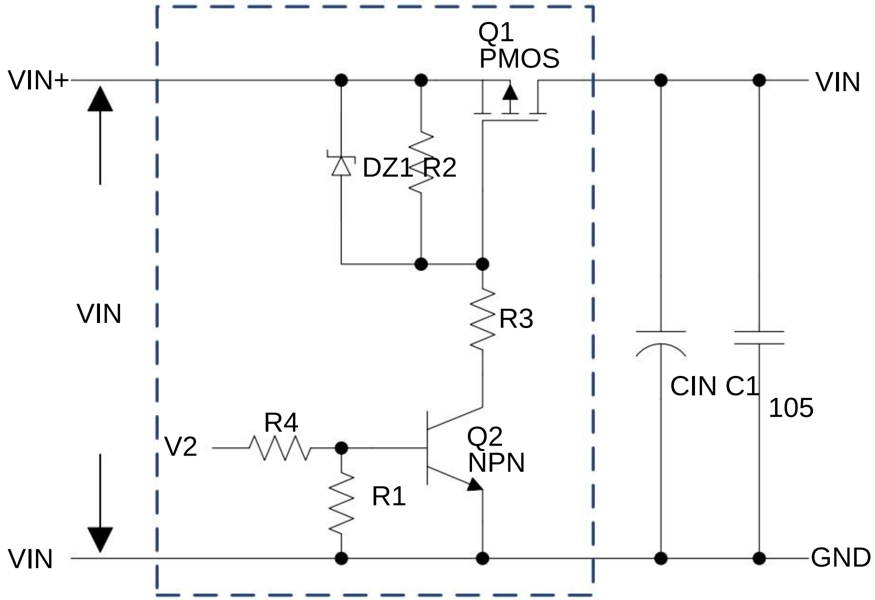
V1:2.5ÿV1ÿVIN

ÿSolution 2: Input plus MOS shutdown (the circuit in the dotted box in the lower right figure).

V2: V2ÿ0.6V turns off the output, V2ÿ1.4V turns on Q1 and restores the output; Q1: VDSÿ1.5*VINMAX; DZ1: VDZ1=10V, 500mW;

R1, R2, R4: 20K; R3: 30K; Q2: VCE ÿ1.5*VINMAX.





Common Problems and Solutions

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ÿQ9. There is a large difference between the output voltage

and the set value ÿConfirm whether the voltage divider resistors R1 and R2 are

soldered or missing; ÿWhether the input capacitor is placed close to the VIN

and GND of the chip; ÿWhether the PCB trace width of the large

current path is sufficient; ÿ Whether the inductor is a power inductor, whether the inductance and

current capacity are sufficient; ÿWhether the freewheeling diode is Schottky.

ÿQ10. Low conversion

efficiency ÿTest error: use a multimeter to test the input voltage, input current, output voltage, and output

current to calculate the conversion efficiency, and the data displayed by the power supply and

load cannot be used, and the error is large; ÿPCB wiring: ensure large The trace width of the current path can

reduce the influence of parasitic parameters on

system performance. The input capacitor should be placed close to the VIN and GND of the chip ; Schottky,

the power inductor with small core loss and sufficient saturation current capability. Generally , the inductance

of the ring sendust core is about 5% higher than the inductance efficiency of the yellow and white ring iron powder c