EE354L: Introduction to Digital Circuits

Course Number & Title: **EE354L: Introduction to Digital Circuits**

Units: 4

Semester and time: Spring 2018 semester
http://classes.usc.edu/term-20181/classes/ee-354
Lecture: MW 10:00-11:50 AM in RTH105
Lecture: TTh 12:00- 1:50 PM in OHE230
Labs: 4 labs each lab 2H 50M in OHE336
(i) 6:00-8:50 PM Mon. (ii) 5:00-7:50 PM Tues. (iii) 5:00-7:50 PM Wed. (iv) 6:00-8:50 PM Thurs.

Location: Lecture: RTH105; Lecture: OHE230; Lab in OHE336

Instructor: Gandhi Puvvada

Office: EEB 238

Office hours: 4 hours per week (1:10-3:00PM MW) in EEB 238 / EEB 203
http://www-classes.usc.edu/engr/ee-s/457/Gandhi_Office_Hours/Gandhi_Office_Hours_Sp2018.pdf

Contact information: gandhi@usc.edu, Office: (213) 740-4461, Cell: (310) 733-8025

Catalog Description:
http://catalogue.usc.edu/preview_course_nopop.php?catoid=7&coid=103783

EE 354L Introduction to Digital Circuits (4, FaSpSm) Digital system design and implementation; synchronous design of datapath and control; schematic/Verilog-based design, simulation, and implementation in Field Programmable Gate Arrays; timing analysis; semester-end project. *Prerequisite:* EE 101 or EE 209. (Duplicates credit in EE 254.)

Learning objectives:

Upon completion of this course students will be able to:
1. Design, simulate, and build (implement on a FPGA board) a substantial digital system
2. Design a digital system using Verilog HDL (Hardware Description Language)
3. Understand RTL design (DPU and CU) and Timing design
4. Understand the use of an embedded processor in a digital system design
5. Compare dedicated hardware implementation with a processor-based implementation
6. Understand 8-bit processor pinout, address decoding and SRAM memory interface
7. Understand issues with Clock domain crossing, 4-way and 2-way handshake, single-clock and two-clock FIFOs (First-In First-Out buffers) and their application
8. Understand sizing of Simple CMOS gates
9. Understand tristate buffers, open-drain devices, buses, bus arbiters, rotating prioritizer
10. Understand how serial busses work, and get to know I2C bus operational details
11. Finally design and implement a semester-end project

Website: https://blackboard.usc.edu/

TAs:
EE354L Head TA -- Pezhman Mamdouh <mamdouh@usc.edu>
EE354L TA -- Naveen Katam <nkatam@usc.edu>
EE354L TA -- Avinash Somanathan <somanata@usc.edu>

Grader: EE354L HW Grader --Pratyush Chandrapati <pratyusc@usc.edu>

Office hours: 1. Gandhi 1:10-3:00 PM MW ~~Gandhi_Office_Hours_Sp2018.pdf~~
2. TAs: Pezhman, Naveen, Avinash Hours: TBA
3. Grader: Pratyush Hours: TBA

Prerequisite: EE 101 or EE109 or EE209
Recommended Preparation: Basic programming skills taught in courses like EE109L (Introduction to Embedded Systems)

Optional Textbook: Digital Design: Principles and Practices, 4/E By John F. Wakerly
http://www.ddpp.com/
Required class-notes and lab manual: Class-notes and Lab Manual distributed online progressively

Recommended Reading: Readings will be posted on Blackboard or communicated via emails

Course Material: Class-notes and Lab Manual

EE354L is an intensive design course, reinforcing class-room lectures with homework and lab assignments.
Textbooks often fail to cover the design process adequately. The lecture material and the lab assignments were developed over the last 30 years of teaching this subject.

Attendance policy: http://www-classes.usc.edu/engr/ee-s/254/ee354l_attendance.html

Grading Policy (approximate weights) (approximately 49% in assignments and 51% in exams)**:**

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Homework:          7%
Participation:     1% (short exercises on each topic)
Labs:             26%
Project:          10%
TA:                3%
Quiz:              8%
Midterm:          20%
Final:            25%
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Class Tentative Schedule: Topics and the order of lectures may change.
Listed below are the dates for the lecture and the lab.

http://classes.usc.edu/term-20181/classes/ee-354

We have four lab sessions every week. The detailed lab schedule is posted at
http://www-classes.usc.edu/engr/ee-s/254/ee254l_lab_manual/EE254L_Lab_Plan.pdf
MTWT (in the lab rows below) stands for Monday, Tuesday, Wednesday, and the Thursday and refers to the four labs every week.

Lec/Lab	Date	Day	Topics and Assignments
	January		
Lec#1	8	Mon	Course intro., DPU & CU (Data Path Unit and Control Unit), One-hot state assignment for CU design pdf .wmv , Detour lab pdf State diagram Design examples .pdf .avi
Lec#2	10	Wed	Nexys-3 (FPGA Board) Intro. Time-Division multiplexed 7-segment Common Anode Display pdf pdf .avi HW#5 Example of One-hot state assignment for CU design pdf dir
Lab#1		MTWT	Lab introduction pdf, Tools installation pdf (ISE for Synthesis, Modelsim for Simulation, etc.) , VDI
Lec#3	15	Mon	MLK Holiday
Lec#4	17	Wed	Mealy machine example -- Divider Design pdf .avi , Data registers -- clocking and controlling pdf .avi
Lab#2		MTWT	Detour Signal State Machine (Schematic) pdf .avi
Lec#5	22	Mon	Verilog HDL Introduction pdf .avi , behavioral modeling pdf .avi
Lec#6	24	Wed	Verilog HDL Data types pdf .avi and Sequential Statements pdf .avi
Lab#3		MTWT	Verilog Introduction Labs (Synchronous and Asynchronous FF resets, and Divider RTL design in Verilog example design, Divider Moore machine design) .pdf .pdf .avi .pdf .zip
Lec#7	29	Mon	Verilog Blocking and Non-blocking assignments, .pdf .avi RTL coding in Verilog .pdf .avi .pdf .zip
Lec#8	31	Wed	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi ME (Mutually Exclusive) and AI (All Inclusive) rules in designing a state diagram pdf .avi Loop Counter Incrementation and Terminal Value Checking pdf .avi
	February		
Lab#4		MTWT	Number Lock State Machine, Nexys-3 Top design, all in Verilog .dir pdf
Lec#9	5	Mon	HW#8A .pdf Q#2 Make A close to B The following is a quick introduction to the topics below as a prelude to introducing PicoBlaze in the next lecture. Introduction to Memories, Processors, Processor pinout, Processor Address Map, Byte Addressability, Processor address decoding, I/O addresses, I/O ports, Input port may or may not require a storage register to hold input data before collection by the processor, Output port needs a storage register to hold the output data sent by the processor for display or transmission, Interrupts, Interrupt service routine, sharing a single interrupt request (INTR) pin and identifying the requester. PicoBlaze is not for data crunching, it is meant to provide control sequences to perform a job such as UART, etc.
Lec#10	7	Wed	Picoblaze introduction, Picoblaze Assembly Language, dir pdf pdf pdf 1.mp4 2.mp4
Lab#5		MTWT	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
Lec#11	12	Mon	Data-path design (a) small system design .pdf .avi BCD to Binary and reverse conversion Chapter 7 , Inches to Yards-Feet-Inches conversion pdf .avi, GCD design pdf .avi

Lec#12	14	Wed	Quiz preparation
Lab#6		MTWT	GCD (Greatest Common Divisor) design .pdf
Lec#13	19	Mon	Presidents' Day, university holiday
Lec#14	21	Wed	Picoblaze interface to external hardware, input and output ports, Hex Keypad .pdf .pdf
Lab#7		MTWT	Picoblaze introduction, EE354L_Get_acquainted_with_PicoBlaze.pdf .pdf
	23	Fri	**Quiz Exam: 8:00AM - 9:50 AM Please let me know if you have serious time conflict.**
Lec#15	26	Mon	Array processing in RTL, pointers and pointer incrementation, HW#8A .pdf Due dates and info: .pdf Directory .dir
Lec#16	28	Wed	Picoblaze Interrupts
	March		
Lab#8		MTWT	Keypad interface to Picoblaze .pdf , Demo: Divider on Pico .zip
Lec#17	5	Mon	Timing Design part 1 setup and hold margins, synchronizing asynchronous inputs .pdf HW#8 on Data Path Unit Design .pdf .wmv.zip
Lec#18	7	Wed	Timing Design part 2 reset synchronization, Shannon's expansion theorem applications .pdf Midterm review, Q#2, Q#3 from Sp2013 .pdf
Lab#9		MTWT	Writing Testbenches .dir .pdf
	12	Mon	March 12-19 Spring recess
	14	Wed	March 12-19 Spring recess
			March 12-19 Spring recess
Lec#19	19	Mon	Tristate Buffers, muxes and tristate buffers in Data-path design Q#2 MT_Sp12.pdf MT_Sp12_sol.pdf
Lec#20	21	Wed	Decade counter pdf .zip Verilog HDL Blocking and Non-blocking assignments Last two pages pdf .avi Verilog Exam questions review .pdf P1.avi P2.avi
Lab #10		MTWT	Picoblaze Interrupts (i) using polling (ii) with no polling .pdf
Lec#21	26	Mon	Slack (make up), Midterm Review
Lec#22	28	Wed	Preparation for the midterm
Lab #11		MTWT	Timing Analysis and Timing Constraints .pdf Prepare for the semester end project: PMODs, VGA demo, LCD demo, File I/O demo, Logic Analyzer Demo, ChipScope Demo, Final Project proposals
	30	Fri	**Midterm Exam: 8:00AM - 10:50 AM Please let me know if you have serious time conflict.**
	April		
Lec#23	2	Mon	Chapter 11 Memories .pdf .wmv
Lec#24	4	Wed	Memories lecture completion and FIFO lecture introduction, FIFOs .pdf .wmv
Lab #12		MTWT	Final Project proposals approvals, Final Project Week 1
Lec#25	9	Mon	FIFO completion, Gray code, Binary<->Gray conversion, .pdf
Lec#26	11	Wed	Epp protocol, and File I/O between PC and the FPGA using Epp protocol
Lab #13		MTWT	Final Project Week 2

Lec#27	16	Mon	File I/O completion
Lec#28	18	Wed	Ch 4_mux, Barrel shifters, priority encoders, Totem-pole and Open-collector output devices dir
Lab #14		MTWT	Final Project Week 3
Lec#27	23	Mon	UART Basics .pdf , I2C Bus Protocol .pdf
Lec#28	25	Wed	Special Counters Exam questions .pdf Review for the Final exam .pdf
Lab #15		MTWT	Final Project demonstration, presentation, and report submission
	May		
	7	Mon	**Final exam 7:30 AM – 10:30AM (Extended hours**, please let me know if you have conflict) http://classes.usc.edu/term-20181/finals/

Statement on Academic Conduct and Support Systems

Academic Conduct

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in *SCampus* in Section 11, *Behavior Violating University Standard* https://policy.usc.edu/scampus-part-b/ . Other forms of academic dishonesty are equally unacceptable. See additional information in *SCampus* and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct/.

Discrimination, sexual assault, and harassment are not tolerated by the university. You are encouraged to report any incidents to the *Office of Equity and Diversity* http://equity.usc.edu/ or to the *Department of Public Safety* http://dps.usc.edu/online-forms/contact-us . This is important for the safety whole USC community. Another member of the university community – such as a friend, classmate, advisor, or faculty member – can help initiate the report, or can initiate the report on behalf of another person. *The Center for Women and Men* https://engemannshc.usc.edu/rsvp/ provides 24/7 confidential support, and the sexual assault resource center webpage sarc@usc.edu describes reporting options and other resources.

Support Systems

A number of USC's schools provide support for students who need help with scholarly writing. Check with your advisor or program staff to find out more. Students whose primary language is not English should check with the *American Language Institute* http://ali.usc.edu/, which sponsors courses and workshops specifically for international graduate students. *The Office of Disability Services and Programs* http://dsp.usc.edu/ provides certification for students with disabilities and helps arrange the relevant accommodations. If an officially declared emergency makes travel to campus infeasible, *USC Emergency Information* http://emergency.usc.edu/ will provide safety and other updates, including ways in which instruction will be continued by means of blackboard, teleconferencing, and other technology.