```
// Top-level module that defines the I/Os for the DE-1 SoC board
 3
      module DE1_SoC (HEX0, HEX1, HEX2, HEX3, HEX4, HEX5, KEY, LEDR, SW);
        output logic [6:0] HEXO, HEX1, HEX2, HEX3, HEX4, HEX5; output logic [9:0] LEDR;
 4
 5
 6
7
                 loğic [3:0] KEY;
        input
        input logic [9:0] SW;
 8
        // Default values, turns off the HEX displays
seg7 zero(.bcd(SW[3:0]), .leds(HEX0));
seg7 one (.bcd(SW[7:4]), .leds(HEX1));
assign HEX2 = 7'b11111111;
 9
10
11
12
        assign HEX3 = 7'b111111111:
13
        14
15
        assign HEX5 = 7'b11111111;
16
        // Logic to check if SW[3]..SW[0] match your bottom digit,
// and SW[7]..SW[4] match the next.
17
18
19
        // Result should drive LEDR[0].
20
        assign LEDR[0] = (SW[0] & SW[1] & SW[2] & ~SW[3] & ~SW[4] & SW[5] & ~SW[6] & ~SW[6] ;
21
        // 27 = 00100111 //
22
23
24
      endmodule
      module seg7 (bcd, leds);
  input logic [3:0] bcd;
  output logic [6:0] leds;
25
26
27
           always_comb begin
28
               case (bcd)
                  // 3210 6543210
4'b0000: leds = 7'b1000000;
4'b0001: leds = 7'b1111001;
29
30
31
                   4'b0010: leds = 7'b0100100
32
                   4'b0011: leds = 7'b0110000;
33
                   4'b0100: leds = 7'b0011001;
34
                  4'b0101: leds = 7'b0010010;
4'b0110: leds = 7'b0000010;
4'b0111: leds = 7'b1111000;
35
36
37
                   4'b1000: leds = 7'b00000000;
38
                   4'b1001: leds = 7'b0010000:
39
                   default: leds = 7'b1111111;
40
41
               endcase
42
           end
43
      endmodule
44
45
      module DE1_SoC_testbench();
46
        logic [6:0] HEXO, HEX1, HEX2, HEX3, HEX4, HEX5;
47
        logic [9:0] LEDR;
        logic [3:0] KEY;
logic [9:0] SW;
48
49
50
51
        DE1_SOC dut (.HEX0, .HEX1, .HEX2, .HEX3, .HEX4, .HEX5, .KEY, .LEDR,
52
       .SW);
53
54
        // Try all combinations of inputs.
        integer i;
initial begin
Sw[9] = 1'b0;
Sw[8] = 1'b0;
55
56
57
58
59
        for(i = 0; i < 256; i++) begin
60
        SW[7:0] = i; #10;
61
        end
62
        end
63
       endmodule
```