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```
module Light2(clk, reset, is_center, in, out);
          logic clk, reset, is_center;
logic [3:0] in;
   input
   input
   output logic out;
   typedef enum logic {ON, OFF} state;
   state ps, ns;
   always_comb begin
      case (ps)
                 if ((in == 4'b0100) | (in == 4'b1000)) ns = OFF;
          ON:
                 if ((in == 4'b0110) | (in == 4'b1001)) ns = ON;
          OFF:
                                                             ns = OFF;
       endcase
   end
   assign out = (ps == ON);
   always_ff @(posedge clk) begin
       if (reset)
          if (is_center) ps <= ON;</pre>
          else
                           ps <= OFF;
       else
          ps <= ns;
   end
endmodule
module CenterLight_testbench();
                 clk, reset, is_center, l_in, r_in, l_on, r_on;
   logic
                 out;
   assign is_center = 1;
   Light2 dut(clk, reset, is_center, {l_in, r_in, l_on, r_on}, out);
   parameter CLOCK_PERIOD=100;
   initial begin
       clk <= 0
       forever #(CLOCK_PERIOD/2) clk <= ~clk;</pre>
   initial begin
                                                                          @(posedge clk);
                                                                           @(posedge clk);
          reset \leftarrow 1;
          reset \leftarrow 0; 1_{in} \leftarrow 0; r_{in} \leftarrow 0; 1_{on} \leftarrow 0; r_{on} \leftarrow 0;
                                                                          @(posedge clk);
                                                                          @(posedge c]k);
                                                                          @(posedge clk);
                                                                          @(posedge c]k);
          r_in <= 1
                                                                          @(posedge clk)
          r_{in} <= 0; r_{on} <= 1;
                                                                          @(posedge clk);
                                                                          @(posedge clk);
                                                                          @(posedge clk);
          r_in <= 1;
          r_in <= 0; r_on <= 0;
                                                                          @(posedge clk);
                                                                          @(posedge clk);
                                                                          @(posedge clk)
          1_in <= 1;
                                                                          @(posedge clk):
          l_i = 0; r_o <= 1;
                                                                          @(posedge clk);
                                                                          @(posedge clk);
                                                                          @(posedge clk)
          l_in <= 1;
l_in <= 0; r_on <= 0;</pre>
                                                                          @(posedge clk);
                                                                          @(posedge clk);
                                                                          @(posedge clk)
                                                                          @(posedge clk);
          l_in <= 1;
                                                                          @(posedge clk);
          1_{in} <= 0; 1_{on} <= 1;
                                                                          @(posedge clk);
                                                                          @(posedge clk);
                                                                          @(posedge clk);
                                                                          @(posedge clk)
          l_in <= 1;
          1_{in} <= 0; 1_{on} <= 0;
                                                                          @(posedge clk):
                                                                          @(posedge clk);
                                                                          @(posedge clk);
                                                                          @(posedge clk);
          r_{in} \ll 1;
          r_{in} <= 0; l_{on} <= 1;
                                                                           @(posedge clk);
                                                                          @(posedge clk);
```

```
@(posedge clk);
 78
79
                   r_in <= 1;
r_in <= 0; l_on <= 0;
                                                                                            @(posedge clk);
                                                                                            @(posedge clk);
@(posedge clk);
 80
 81
                                                                                            @(posedge clk);
 82
                                                                                            @(posedge clk);
                   reset <= 1;
 83
                   reset \leftarrow 0;
                                                                                            @(posedge clk);
 84
85
           end
 86
       endmodule
 87
 88
       module NormalLight_testbench();
 89
 90
                           clk, reset, is_center, l_in, r_in, l_on, r_on;
 91
92
93
94
95
96
           logic
           assign is_center = 0;
           Light2 dut(clk, reset, is_center, {l_in, r_in, l_on, r_on}, out);
 97
           parameter CLOCK_PERIOD=100;
 98
99
            initial begin
               c1k \ll 0;
100
               forever #(CLOCK_PERIOD/2) clk <= ~clk;</pre>
101
102
103
                                                                 @(posedge clk);
           initial begin
104
                                                                                            @(posedge clk);
105
                   reset \leftarrow 0; 1_{in} \leftarrow 0; r_{in} \leftarrow 0; 1_{on} \leftarrow 0; r_{on} \leftarrow 0;
                                                                                            @(posedge clk);
                                                                                            @(posedge clk);
106
107
                                                                                            @(posedge clk);
108
                   r_in <= 1;
r_in <= 0; l_on <= 1;
                                                                                            @(posedge clk);
109
                                                                                            @(posedge clk);
                                                                                            @(posedge clk);
110
111
                                                                                            @(posedge clk)
                                                                                            @(posedge clk);
@(posedge clk);
                   r_in <= 1;
r_in <= 0; l_on <= 0;
112
113
                                                                                            @(posedge clk)
114
115
                                                                                            @(posedge clk);
116
                                                                                            @(posedge clk);
                   r_in <= 1;
117
                   r_in <= 0; r_on <= 1;
                                                                                            @(posedge clk);
118
                                                                                            @(posedge clk);
@(posedge clk);
119
                                                                                            @(posedge clk);
120
                   r_{in} \leftarrow 1;
                   r_in <= 0; r_on <= 0;
121
                                                                                            @(posedge clk);
                                                                                            @(posedge clk);
@(posedge clk);
122
123
124
                   l_in <= 1;
l_in <= 0; r_on <= 1;</pre>
                                                                                            @(posedge clk)
                                                                                            @(posedge clk);
@(posedge clk);
125
126
127
                                                                                            @(posedge clk)
128
                                                                                            @(posedge clk);
                   l_in <= 1;
                   1_{in} <= 0; r_{on} <= 0;
129
                                                                                            @(posedge clk);
130
                                                                                            @(posedge clk);
                                                                                            @(posedge clk);
@(posedge clk);
131
                   l_in <= 1;
l_in <= 0; l_on <= 1;</pre>
                                                                                            @(posedge clk);
133
                                                                                            @(posedge clk);
134
                                                                                            @(posedge clk);
135
                                                                                            @(posedge clk);
136
                   l_{in} <= 1;
                   1_{in} <= 0; 1_{on} <= 0;
                                                                                            @(posedge clk);
137
                                                                                            @(posedge clk);
138
                                                                                            @(posedge clk);
139
140
                                                                                            @(posedge clk)
                   reset \leftarrow 1;
141
                   reset \leftarrow 0;
                                                                                            @(posedge clk);
142
143
           end
       endmodule
144
```