```
module UPC(discounted, stolen, u, p, c, m);
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
          output_logic discounted, stolen;
          input logic u, p, c, m;
          assign discounted = (u&p)|(p&c)|(u&c);
assign stolen = (\sim p&\sim c&\sim m)|(u&\sim p&\sim m);
      endmodule
      module UPC_testbench();
          logic u, p, c, m;
logic discounted, stolen;
          UPC dut(.discounted, .stolen, .u, .p, .c, .m);
          18
19
20
          end
21
      endmodule
```