	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
1	|DE1_SoC	18 (0)	23 (4)	0	0	67	0	|DE1_SoC	DE1_SoC	work
1	|Light:eight|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light:eight	Light	work
2	|Light:five|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light:five	Light	work
3	|Light:four|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light:four	Light	work
4	|Light:nine|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light:nine	Light	work
5	|Light:one|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light:one	Light	work
6	|Light:seven|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light:seven	Light	work
7	|Light:six|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light:six	Light	work
8	|Light:three|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light:three	Light	work
9	|Light:two|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light:two	Light	work
10	|UserIn:Left|	2 (2)	1 (1)	0	0	0	0	|DE1_SoC|UserIn:Left	UserIn	work
11	|UserIn:Right|	2 (2)	1 (1)	0	0	0	0	|DE1_SoC|UserIn:Right	UserIn	work
12	|Victory:V|	5 (5)	8 (8)	0	0	0	0	|DE1_SoC|Victory:V	Victory	work