	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
1	|DE1_SoC	85 (2)	61 (4)	0	0	67	0	|DE1_SoC	DE1_SoC	work
1	| Comparator_10b:Compr|	7 (0)	0 (0)	0	0	0	0	|DE1_SoC| Comparator_10b:Compr	Comparator_10b	work
1	| F_Adder:eachFA[6].FA|	4 (4)	0 (0)	0	0	0	0	|DE1_SoC| Comparator_10b:Compr| F_Adder:eachFA[6].FA	F_Adder	work
2	| F_Adder:eachFA[8].FA|	1 (1)	0 (0)	0	0	0	0	|DE1_SoC| Comparator_10b:Compr| F_Adder:eachFA[8].FA	F_Adder	work
3	| F_Adder:eachFA[9].FA|	2 (2)	0 (0)	0	0	0	0	|DE1_SoC| Comparator_10b:Compr| F_Adder:eachFA[9].FA	F_Adder	work
2	| Counter_3b:Computer|	3 (3)	3 (3)	0	0	0	0	|DE1_SoC| Counter_3b:Computer	Counter_3b	work
3	| Counter_3b:Player|	3 (3)	3 (3)	0	0	0	0	|DE1_SoC| Counter_3b:Player	Counter_3b	work
4	| Light2:EachLed[1].Led|	2 (2)	1 (1)	0	0	0	0	|DE1_SoC| Light2:EachLed[1].Led	Light2	work
5	| Light2:EachLed[2].Led|	4 (4)	1 (1)	0	0	0	0	|DE1_SoC| Light2:EachLed[2].Led	Light2	work
6	|	4 (4)	1 (1)	0	0	0	0	|DE1_SoC|	Light2	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
	Light2:EachLed[3].Led|							Light2:EachLed[3].Led		
7	|Light2:EachLed[4].Led|	4 (4)	1 (1)	0	0	0	0	|DE1_SoC|Light2:EachLed[4].Led	Light2	work
8	|Light2:EachLed[5].Led|	1 (1)	1 (1)	0	0	0	0	|DE1_SoC|Light2:EachLed[5].Led	Light2	work
9	|Light2:EachLed[6].Led|	4 (4)	1 (1)	0	0	0	0	|DE1_SoC|Light2:EachLed[6].Led	Light2	work
10	|Light2:EachLed[7].Led|	4 (4)	1 (1)	0	0	0	0	|DE1_SoC|Light2:EachLed[7].Led	Light2	work
11	|Light2:EachLed[8].Led|	4 (4)	1 (1)	0	0	0	0	|DE1_SoC|Light2:EachLed[8].Led	Light2	work
12	|Light2:EachLed[9].Led|	2 (2)	1 (1)	0	0	0	0	|DE1_SoC|Light2:EachLed[9].Led	Light2	work
13	|UserInput:U_In|	4 (4)	2 (2)	0	0	0	0	|DE1_SoC|UserInput:U_In	UserInput	work
14	|Victory2:v|	6 (6)	4 (4)	0	0	0	0	|DE1_SoC|Victory2:v	Victory2	work
15	|clock_divider:cdiv|	16 (16)	16 (16)	0	0	0	0	|DE1_SoC|clock_divider:cdiv	clock_divider	work
16	|lfsr_10:LFSR|	1 (1)	20 (20)	0	0	0	0	|DE1_SoC|lfsr_10:LFSR	lfsr_10	work
17	|seg7:left|	7 (7)	0 (0)	0	0	0	0	|DE1_SoC|	seg7	work

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
								seg7:left		
18	| seg7:right|	7 (7)	0 (0)	0	0	0	0	|DE1_SoC| seg7:right	seg7	work