```
module Counter_3b (clk, reset, in, out);
 2
3
          input logic clk, reset, in;
          output logic [2:0] out;
 4
 5
6
7
8
9
          logic [2:0] ps, ns;
          always_comb begin
             ns = ps + in;
1Ŏ
11
          assign out = ps;
12
13
          always_ff @(posedge clk) begin
14
              if (reset)
15
                 ps <= 3'b0;
16
17
              else
                 ps <= ns;
18
          end
19
20
21
22
23
24
25
26
27
      endmodule
      module Counter_3b_testbench();
          logic clk, reset, in;
          logic [2:0] out;
          Counter_3b dut(.clk, .reset, .in, .out);
          parameter CLOCK_PERIOD = 100;
28
29
30
          initial begin
              clk \ll 0;
              forever #(CLOCK_PERIOD/2) clk <= ~clk;</pre>
31
          end
32
33
          initial begin
                                                                   @(posedge clk);
34
35
              reset \leftarrow 1;
                                                                   @(posedge clk);
              reset \leftarrow 0; in \leftarrow 0;
                                                                   @(posedge clk);
                                                                   @(posedge clk);
@(posedge clk);
36
37
              in \leftarrow= 1;
                                                                   @(posedge clk);
38
              in \leq 0;
39
                                                                   @(posedge clk);
40
              in \leq 1;
                                                                   @(posedge clk);
41
                                                                   @(posedge clk);
42
43
                                                                   @(posedge clk);
                                                                   @(posedge clk);
@(posedge clk);
44
45
                                                                   @(posedge clk);
46
              in \leq 0;
                                                                   @(posedge clk);
47
                                                                   @(posedge clk);
48
              in \leftarrow= 1;
                                                                   @(posedge clk);
                                                                   @(posedge clk);
@(posedge clk);
49
              in \ll 0;
              reset <= 1;
reset <= 0;
50
                                                                   @(posedge clk);
51
52
              $stop;
53
          end
```

endmodule