

Revision: DE1 SoC

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77                                     @(posedge clk);
78         r_in <= 1;                    @(posedge clk);
79         r_in <= 0; l_on <= 0;        @(posedge clk);
80                                     @(posedge clk);
81                                     @(posedge clk);
82         reset <= 1;                  @(posedge clk);
83         reset <= 0;                  @(posedge clk);
84     $stop;
85 end
86 endmodule
87
88 module NormalLight_testbench();
89     logic        clk, reset, is_center, l_in, r_in, l_on, r_on;
90     logic        out;
91
92     assign is_center = 0;
93
94     Light2 dut(clk, reset, is_center, {l_in, r_in, l_on, r_on}, out);
95
96     parameter CLOCK_PERIOD=100;
97     initial begin
98         clk <= 0;
99         forever #(CLOCK_PERIOD/2) clk <= ~clk;
100    end
101
102    initial begin                                @(posedge clk);
103        reset <= 1;                                @(posedge clk);
104        reset <= 0; l_in <= 0; r_in <= 0; l_on <= 0; r_on <= 0;  @(posedge clk);
105                                                    @(posedge clk);
106                                                    @(posedge clk);
107        r_in <= 1;                                @(posedge clk);
108        r_in <= 0; l_on <= 1;                    @(posedge clk);
109                                                    @(posedge clk);
110                                                    @(posedge clk);
111        r_in <= 1;                                @(posedge clk);
112        r_in <= 0; l_on <= 0;                    @(posedge clk);
113                                                    @(posedge clk);
114                                                    @(posedge clk);
115        r_in <= 1;                                @(posedge clk);
116        r_in <= 0; r_on <= 1;                    @(posedge clk);
117                                                    @(posedge clk);
118                                                    @(posedge clk);
119        r_in <= 1;                                @(posedge clk);
120        r_in <= 0; r_on <= 0;                    @(posedge clk);
121                                                    @(posedge clk);
122                                                    @(posedge clk);
123        l_in <= 1;                                @(posedge clk);
124        l_in <= 0; r_on <= 1;                    @(posedge clk);
125                                                    @(posedge clk);
126                                                    @(posedge clk);
127        l_in <= 1;                                @(posedge clk);
128        l_in <= 0; r_on <= 0;                    @(posedge clk);
129                                                    @(posedge clk);
130                                                    @(posedge clk);
131        l_in <= 1;                                @(posedge clk);
132        l_in <= 0; l_on <= 1;                    @(posedge clk);
133                                                    @(posedge clk);
134                                                    @(posedge clk);
135        l_in <= 1;                                @(posedge clk);
136        l_in <= 0; l_on <= 0;                    @(posedge clk);
137                                                    @(posedge clk);
138                                                    @(posedge clk);
139        reset <= 1;                                @(posedge clk);
140        reset <= 0;                                @(posedge clk);
141    $stop;
142 end
143 endmodule
144

```