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CM – 401

Friday 10/4/19

- Discussed for one hour at 4:00 – 5:00 PM
- Decided to make processor with Stack architecture
- Discussed possible calling conventions and addressing modes
- Created three ISA for pushing/popping, jumps/branches, and arithmetic/stack manipulation.

Sunday 10/6/19

- Met in O259 from 5:30 – 8:45 PM
- Most of the time was used to discuss the Stack architecture and make sure all team members are on the same page
- Will and I worked on framing some calling conventions and designed the assembly code for relPrime and GCD
- Used the idea that memory would store return addresses and argument values when making a procedure call
- Tori designed instruction set that we could use to get around our ISA and the 16-bit limitations.

Monday 10/7/19

- Met with Sid from 1:20 PM – 2:10 PM to discuss advice and clarification on addressing modes. Realize that using the stack for return addresses will be better than using memory.
- Met with group from 3:30 – 6:45 PM to redesign assembly code and instruction set.
- Removed ‘jal’ and added ‘dup’ and ‘flip’ instructions for better stack manipulation
- Rewrote code for relPrime and GCD in our new instruction set using polished calling conventions where the return address and arguments are placed within the stack, and the return value is placed in memory.
- Side notes:
    - It feels as though without pseudocode, our code will be complicated to efficiently program
    - While everyone has contributed in some way to the project, I feel as though I have created most of the assembly code. So, I am worried that my teammates might not understand how we are implementing our design through code.

Tuesday 10/8/19

- Met in F225 from 3:50 – (ins) to make final changes and commit Document for Milestone 1.
- Made documentation a bit neater by formatting and inserting a header with some footnotes
- Push personal journal and Document
- Discuss about how we are going to complete Milestone 2 so we can talk to Sid tomorrow and not sound like idiots
- I think that communication is key for this milestone because we are doing it during the break time.

Friday 10/11/19

- Self-conducted meeting at home.
- Polished up Milestone 1 using critiques that Sid gave at group meeting
- Worked on adding more common operations.
- Thought of a new method of procedure calling. Use a jump and link instruction that takes the PC and puts it on the stack.

Sunday 10/13/19

- Group met in F225 from 7 PM – 10:15 PM to fix remaining Milestone 1 issues and begin Milestone 2.
- Created RTL code for all instructions except duplicate and flip, which we are asking Sid about how to implement in hardware
- Make a better table of contents and organization of document
- Settle on pushM and pushR for more efficient coding. Also, memory allocation will be used by offsetting from the $sp register. Still need to have the $sp address on the execution stack
- This meeting went far better than the previous. It seems that everyone understood each change and new implementation.

Monday 10/14/19

- Group met in F225 from 4 PM- 6 PM to finish the RTL code and change some hardware components after talking with Sid.
- Created diagrams that show the inputs and outputs of each required piece of hardware
- Decided on what control signals might be needed for each hardware component
- Implemented a barrel shifter that will both shift right and shift left.
- Put all of the RTL code into a Table so that it is neater and, for the most part, split into a multicycle process. (Might have to change later when designing the datapath)
- Update the code for relPrime and GCD with our new instructions and calling procedures that changed throughout Milestone 2
- This meeting went well, but it seemed that there is still a bit of confusion within the group on duplicated and the execution stack hardware components. Resolved before submitting document.

Tuesday 10/15/19

- Tori and I met in F225 from 4-5 PM to polish document one more time
- Finished the RTL verification section by adding pictures of add command
- Change pushNum -> dupNum for better clarity
- Committed and pushed Milestone 2

Saturday 10/19/19

- Started to work on the components for milestone 3.
- Realized that I have no clue how to do Verilog, so I worked on tutorials instead
- This was solo time at Starbucks when I was at home

Monday 10/21/19

- Worked on my own time throughout the day.
- Completed components for Sign and Zero extenders as well as their tests
- Finished the register and register file, but their tests need some work
- I am a little worried that Tori and Will have not worked on M3 and focused on the labs instead.

Tuesday 10/22/19

- Met with Sid to discuss Lab 08 and some of the execution stack component
- Completed the tests for the register and register file. Tori said that she will work on the memory unit.
- I think I finished the component for the execution stack, but the unit test did not work as I wanted.

Wednesday 10/23/19

- Will said that he completed the datapath. Tori and I checked it and agreed that it looked good, but there might need to be a few changes depending on testing.
- Tori finished the Memory and started working on describing implementation
- I finished the execution stack and started figuring out the control unit and how everything fit together within the datapath.

Friday 10/25/19

- Rewriting some of the unit test explanations in the document for better understanding.
- Work by myself because it was hard to find a time today to get together with the group

Sunday 10/27/19

- Met with group in F225 for about two hours. Started to create the control unit with Will, while Tori was working on combining components together.
- Created a table to write down all of the control values for each instruction.
- Realized that we need to edit the RTL code a little bit to allow multiple execution stack operations

Monday 10/28/19

- In class, talked with Sid for better understanding how to tell the Execution Stack to do multiple operations in different cycles.
- Realize that we needed to update the ES component for an enable bit. Also got rid of the extra output registers because we never really used them.
- Found out that the group could not get together until Wednesday, in which I will not be on campus. Asked Sid for extension.

Tuesday 10/29/19

- Today, I wanted to update all of the RTL code so that it correlates to how we want the operations in our ES to execute and be called.
- After updating all of the RTL code, I wrote all of the Bubble-Control diagram for each instruction excluding branching and shifting (due to Will saying that we might be changing the slr and sll into one instruction).
- Updated the Verilog for the execution stack so that it will go along with our updated datapath/control system.
- Tori and Will said that they are able to finish M4 tomorrow.