University of California, Irvine Fall 2016

EECS 119 Introduction to VLSI Design

Design Project #2

Design a static CMOS logic gate that implements the following logic function.

$$F = ((A.B) + C + (D.E))'$$

1. Draw the complete circuit.
2. Determine the order of inputs that will result in uninterrupted diffusion strips.
3. Draw the layout of the circuit using uninterrupted diffusion strips.
4. Simulate the circuit and verify that the circuit performs the given logic function.
5. Submit a neat and readable report with all the computer outputs properly attached.

Deadline: Nov. 8, 2016.