teuscher Lab
teuscher-lab.com

Christof Teuscher
ECE 410/510
Spring 2025

Portland State
UNIVERSITY

Week 6
Codefest: Practice HW/SW co-design with design iterations
ECE 410/510
Spring 2025

Challenge #21

Overview and context:
The goal for this week is go back to the drawing board and to do a design iteration using your workflow.

Learning goals:

- Re-consider your initial HW/SW boundary
- Re-evaluate the bottlenecks
- Apply co-design principles

Things to (re-)consider and think about:

Workload analysis and characterization

- Profile/benchmark your algorithm again to understand computation patterns
- Identify key operations (matrix multiplications, convolutions, etc.)
- Analyze memory access patterns and data locality requirements
- Quantify performance bottlenecks in existing solutions

Architecture exploration

- Evaluate trade-offs between different accelerator architectures (systolic arrays, dataflow, etc.)
- Simulate performance with different memory hierarchies
- Consider scalability across different model sizes and types
- Explore different dataflow models (weight-stationary, output-stationary)

Microarchitecture design iteration

- Start with high-level models to validate architectural concepts
- Gradually refine RTL models with increasing fidelity
- Implement critical paths first to identify timing challenges
- If available, use emulation platforms (e.g., FPGA prototypes) for early validation

Progressive physical design

- Perform early performance/power analysis to guide microarchitecture decisions
- Iterate on critical paths identified through static timing analysis
- Use hierarchical design approaches for complex accelerators

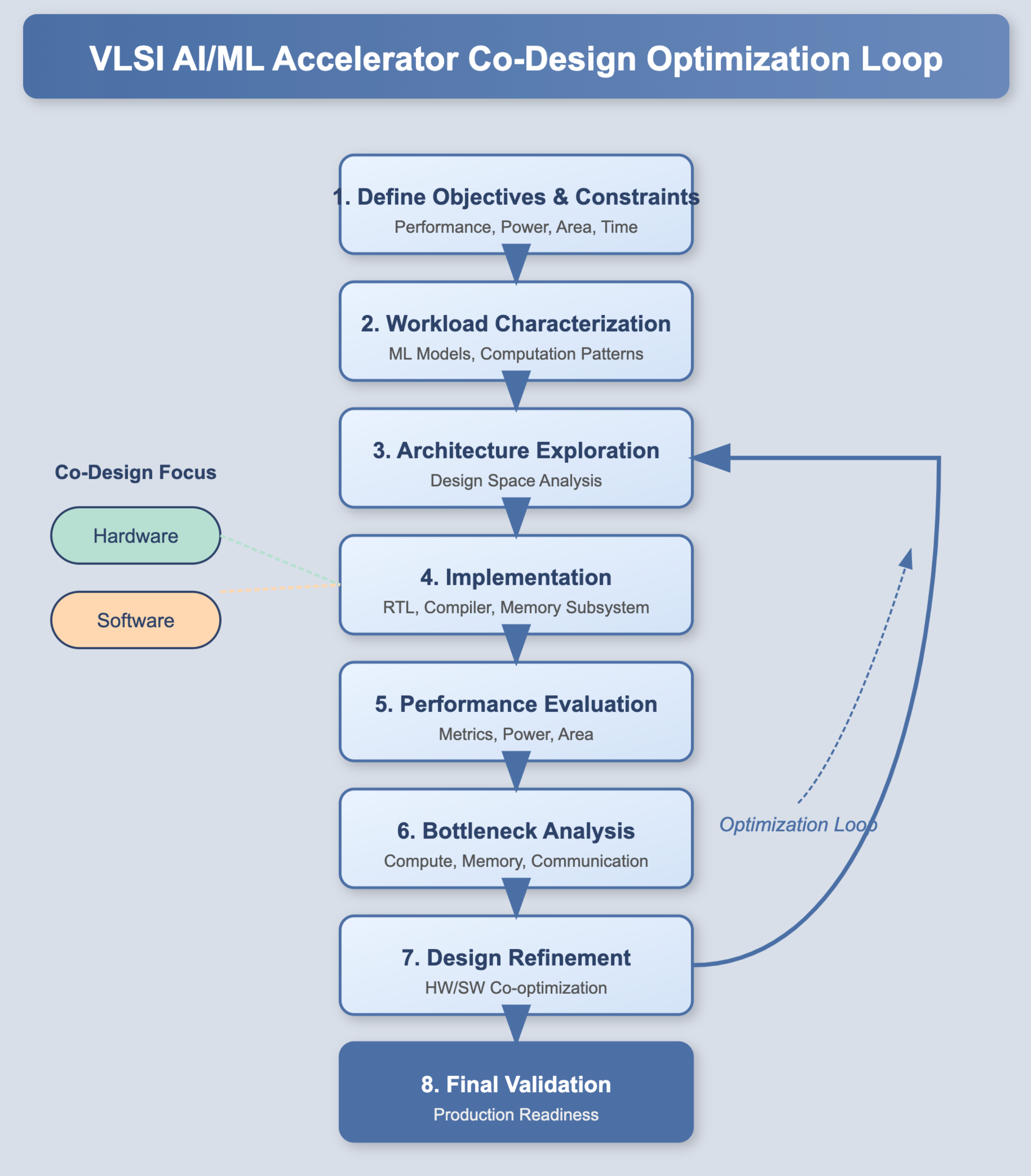
Integrated verification strategy

- Develop multi-level testbenches (unit, block, system)
- Create golden models for functional verification
- Implement power and performance verification methodologies
- Use hardware-in-the-loop testing with actual ML workloads

Hardware-aware algorithm optimization

- Adapt your algorithm/model to match hardware capabilities
- Implement quantization strategies optimized for your hardware
- Explore pruning techniques that leverage hardware efficiencies

Co-design optimization loop [More advanced]
Consider parametrizing your algorithm, HW design, and more, then implement an optimization loop that searches for optimal configurations.



VLSI AI/ML Accelerator Co-Design Optimization Loop

1. Define Objectives & Constraints
Performance, Power, Area, Time

2. Workload Characterization
ML Models, Computation Patterns

3. Architecture Exploration
Design Space Analysis

4. Implementation
RTL, Compiler, Memory Subsystem

5. Performance Evaluation
Metrics, Power, Area

6. Bottleneck Analysis
Compute, Memory, Communication

7. Design Refinement
HW/SW Co-optimization

8. Final Validation
Production Readiness