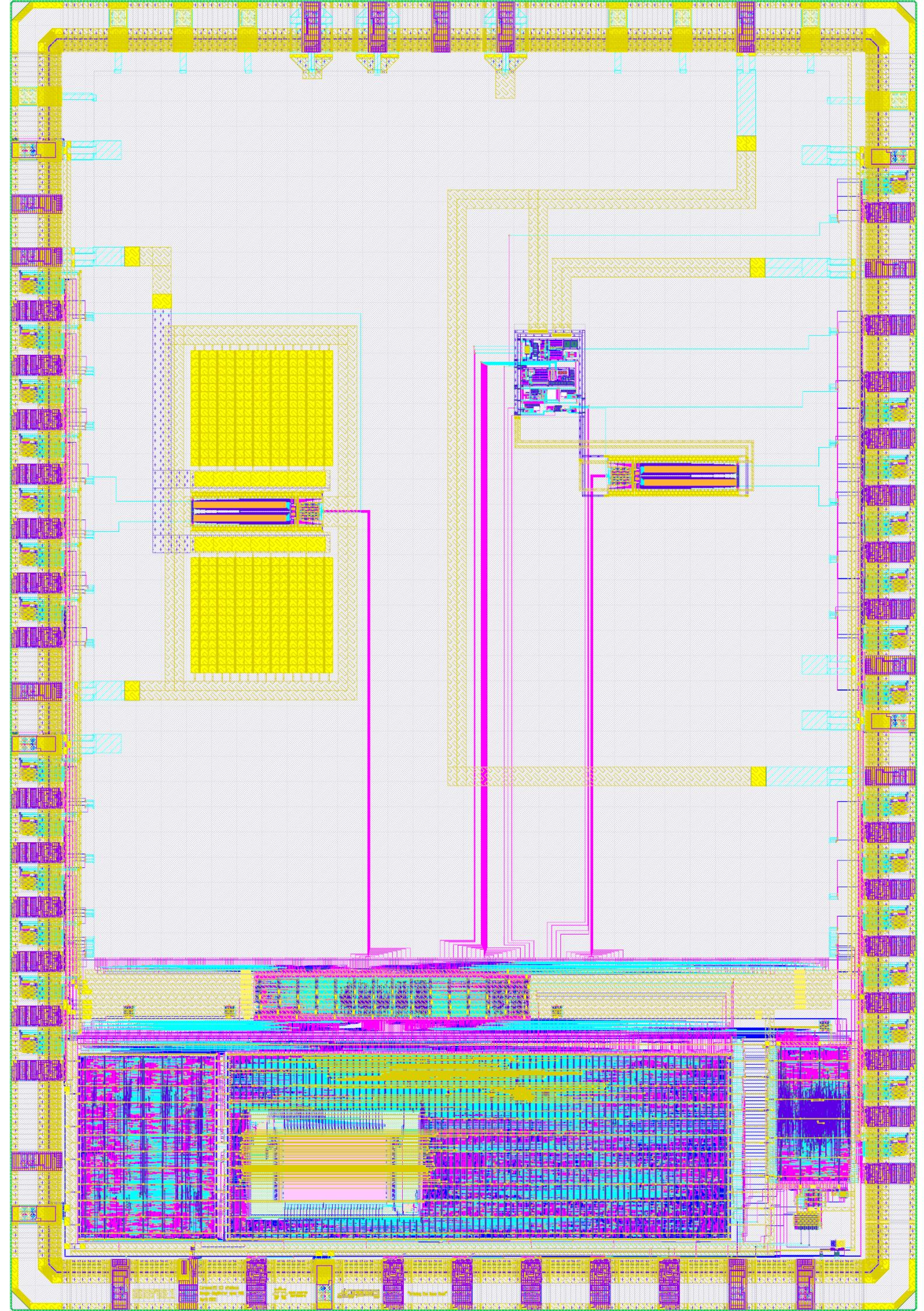


Measurement Report

MPW-6 B7, SLOT-013

January 2024



1 Main

This section concerns itself with the verification of the main analog block mostly referred to as the main block.

The main block consists of:

- Basis Current Source. (BCS)
- Bandgap Reference Voltage. (BGR)
- Bias Generator. (BIAG)
- Two Low Dropout Regulators. (LDO)
- Testbuffer. (TB)
- Current Starved Ring Oscillator. (OSC)

Each of the parts above will be discussed in detail in the following sections.

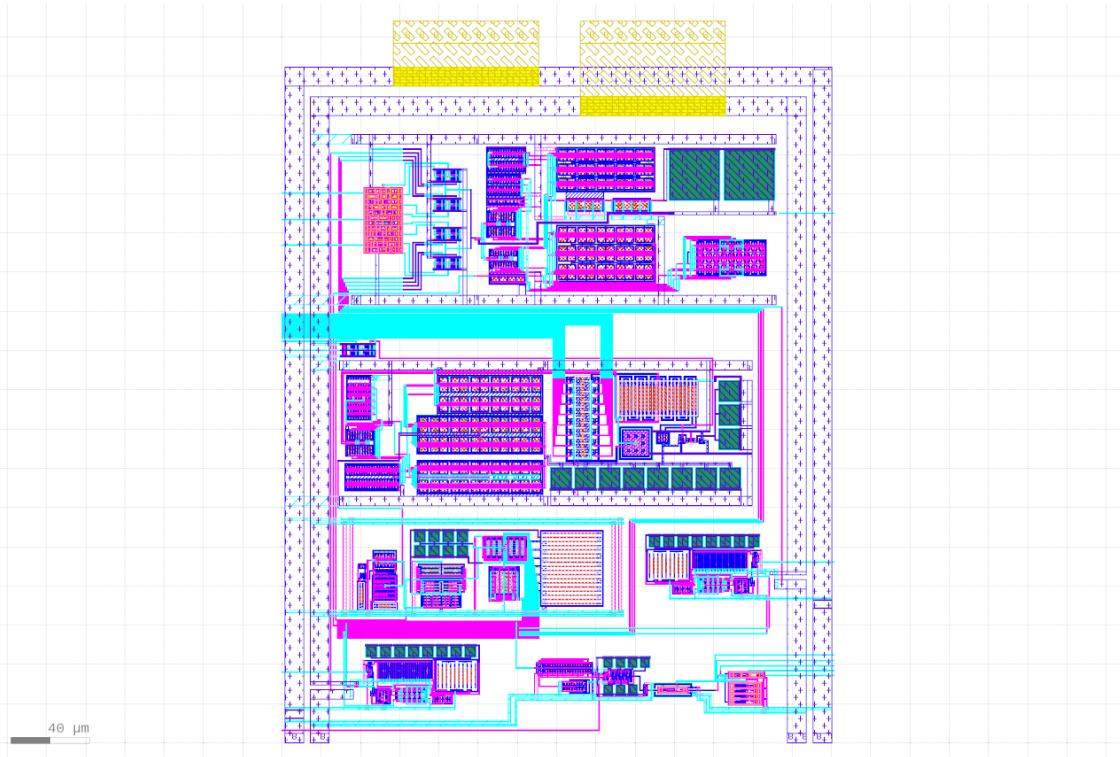
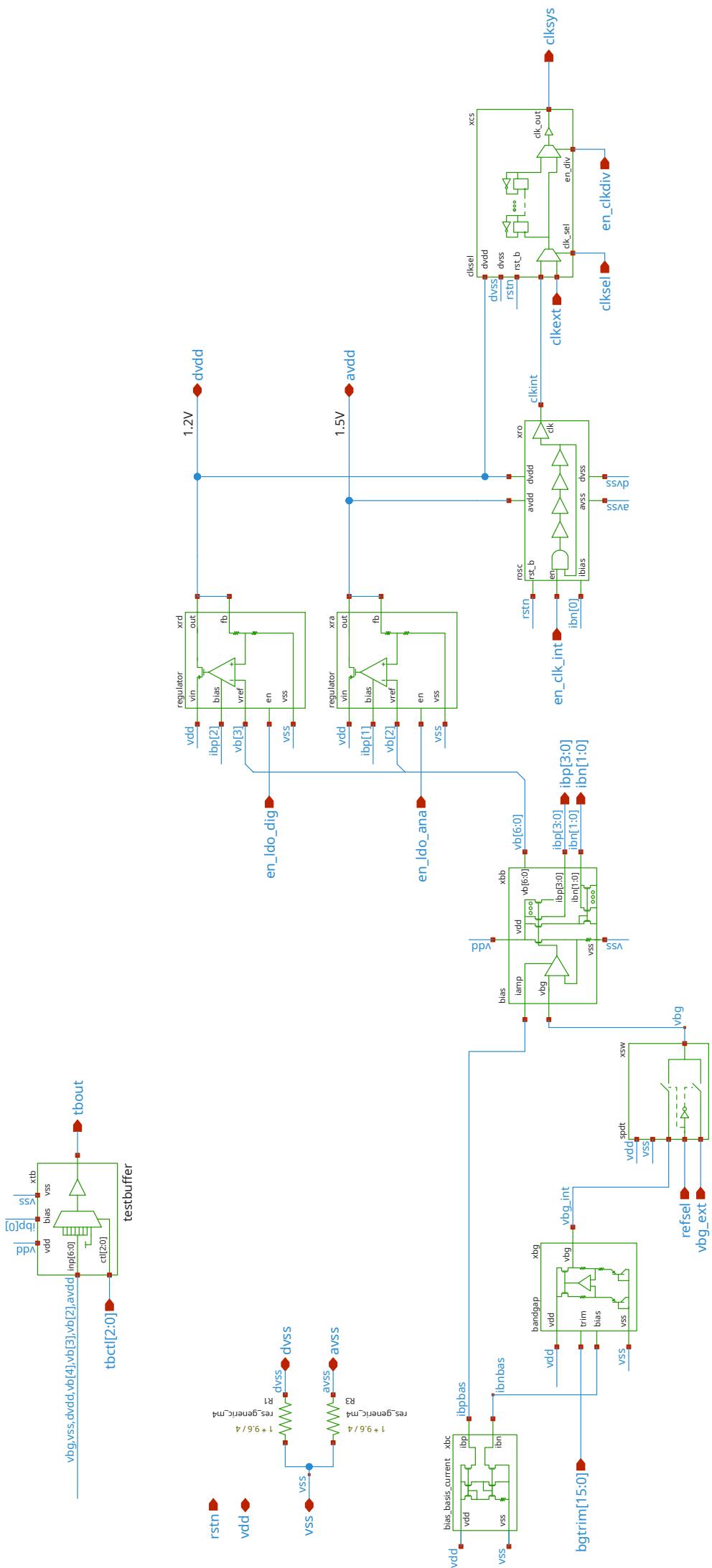


Figure 1: Main layout



1.1 Basis Current Source (BCS)

There is no direct measurement that can confirm the operation of the BCS. However the indirect verification of this block can be done by checking the BGR and BIAG, as these blocks directly depend on the BCS to provide a bias current for their respective amplifiers.

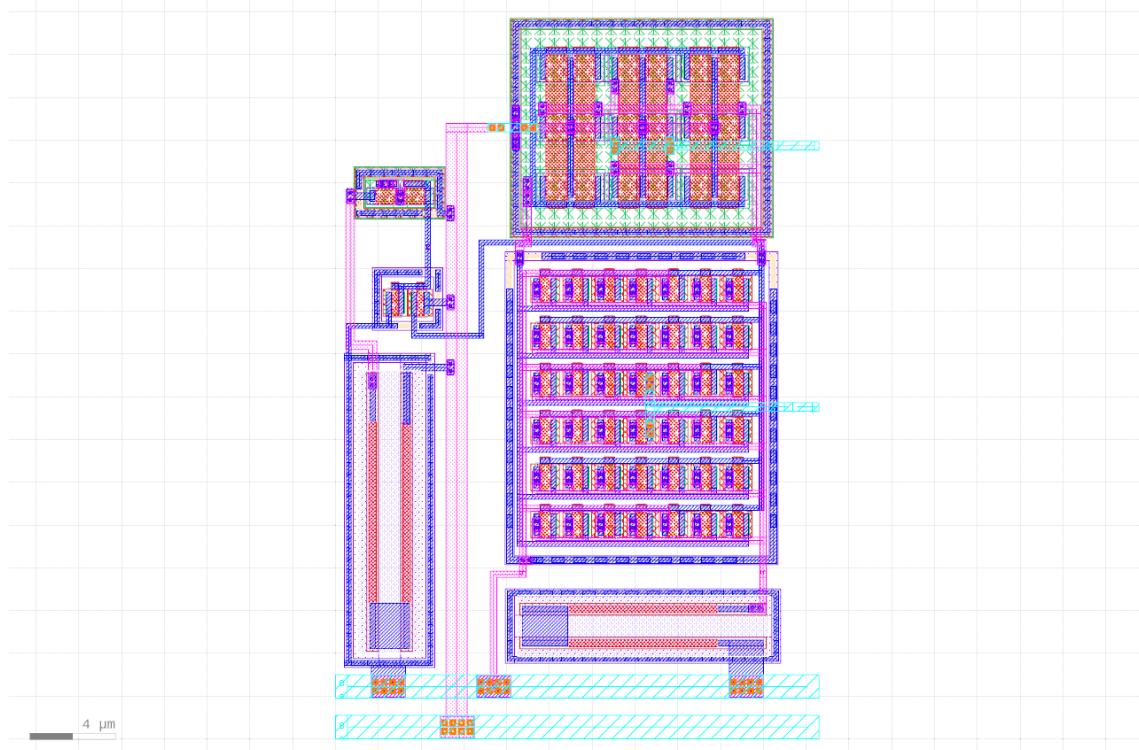
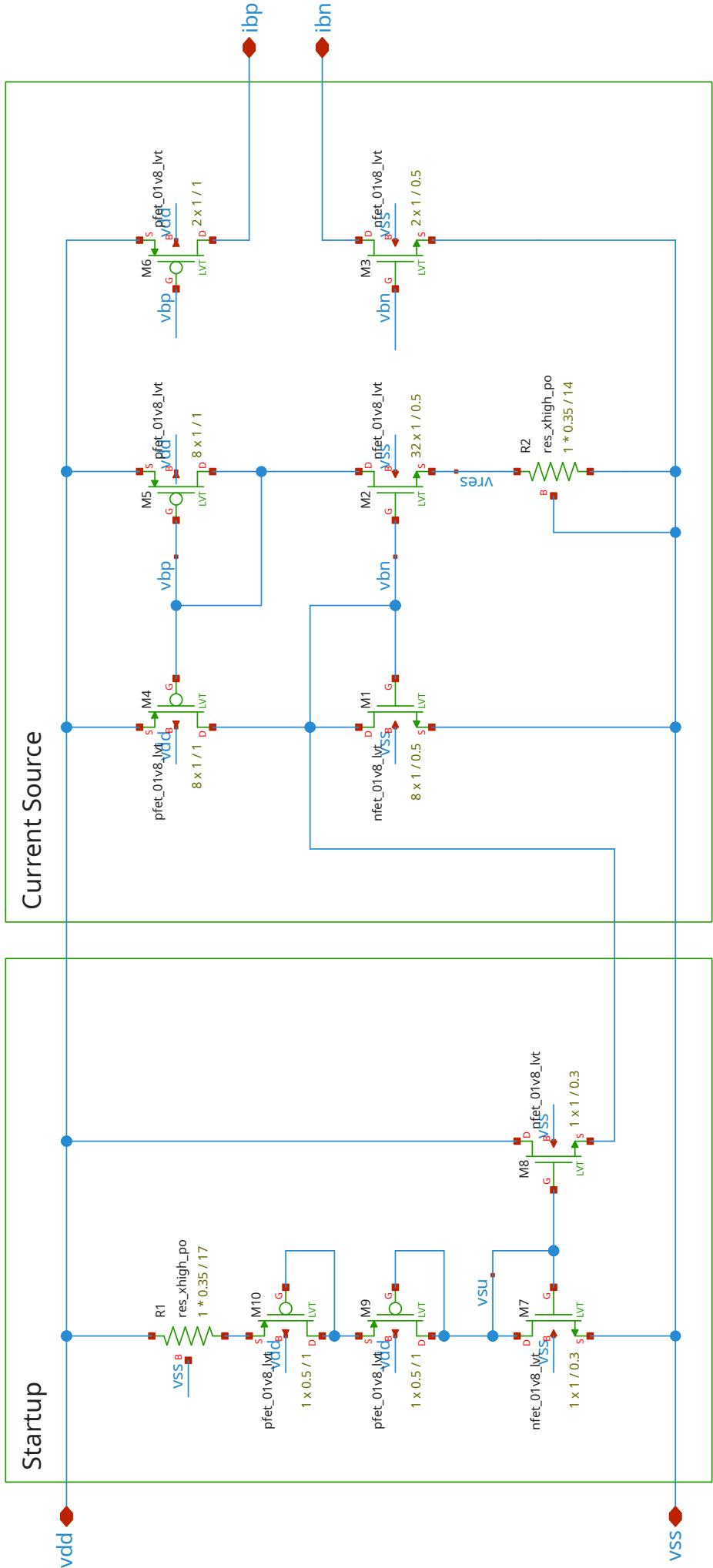


Figure 2: BCS layout



1.2 Bandgap Reference Voltage (BGR)

The bandgap reference voltage is designed to nominal 1.214V at room temperature with a trim value: 8 out of 16. The trim value was intended to give sufficient room for inaccuracies in both directions for the first tapeout.

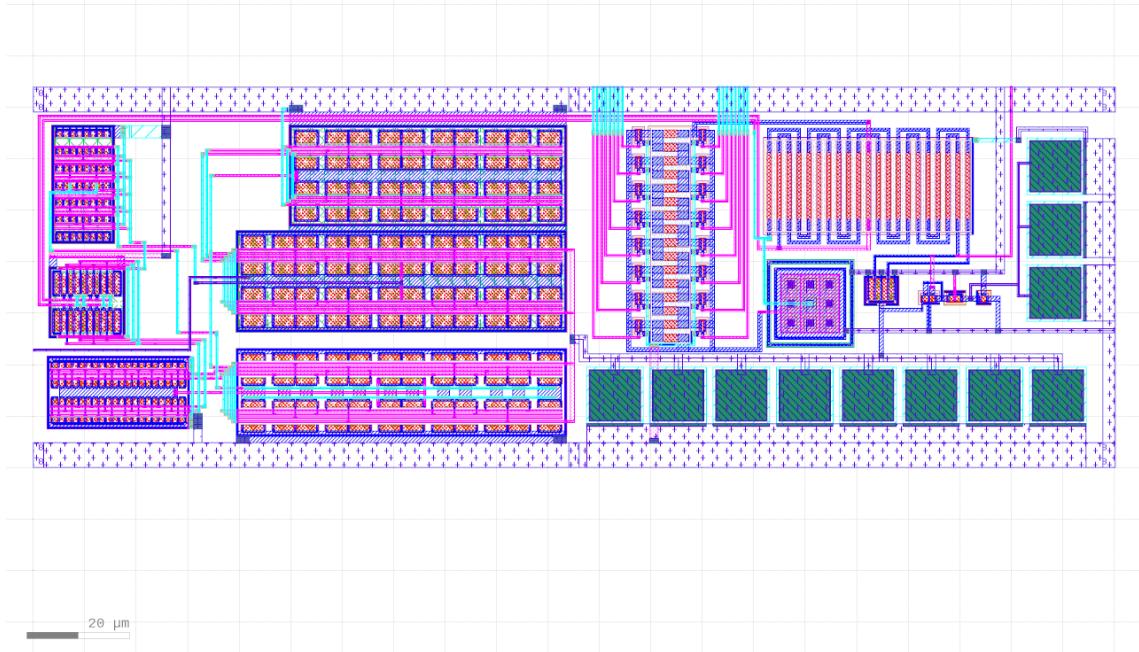


Figure 3: BGR layout

The following plot shows a iteration through the trim range. Due to the physical arrangement of the logic analyzer pins controlling the trimvalues the stepping order in decimal is:

2,4,6,8,10,12,14,15,13,11,9,7,5,3,1,0,none

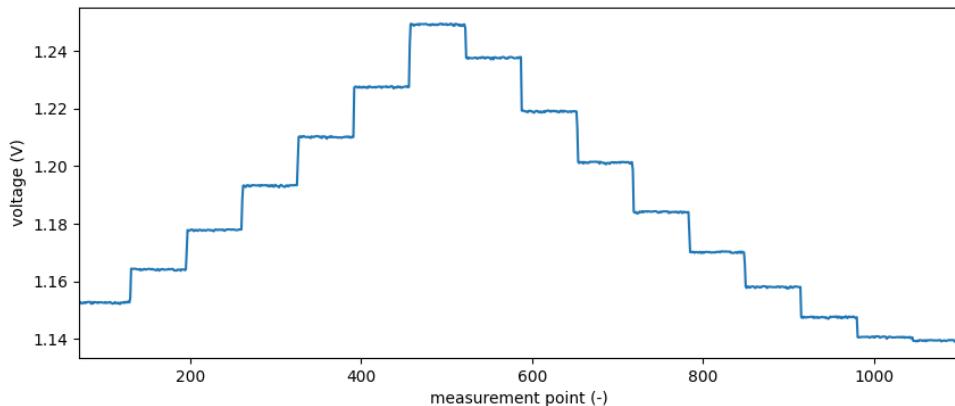


Figure 4: BGR Voltage during trimming

the target value obtained from simulation is 1.214V at room temperature.

Note that the measurement is made using the TB which depends on the BCS, BGR and BIAG. So offset, drift and noise is subject to all other parts of the verification chain as much at the BGR itself. This does therefore imply that those circuits are in fact operational and working at least to some degree as intended.

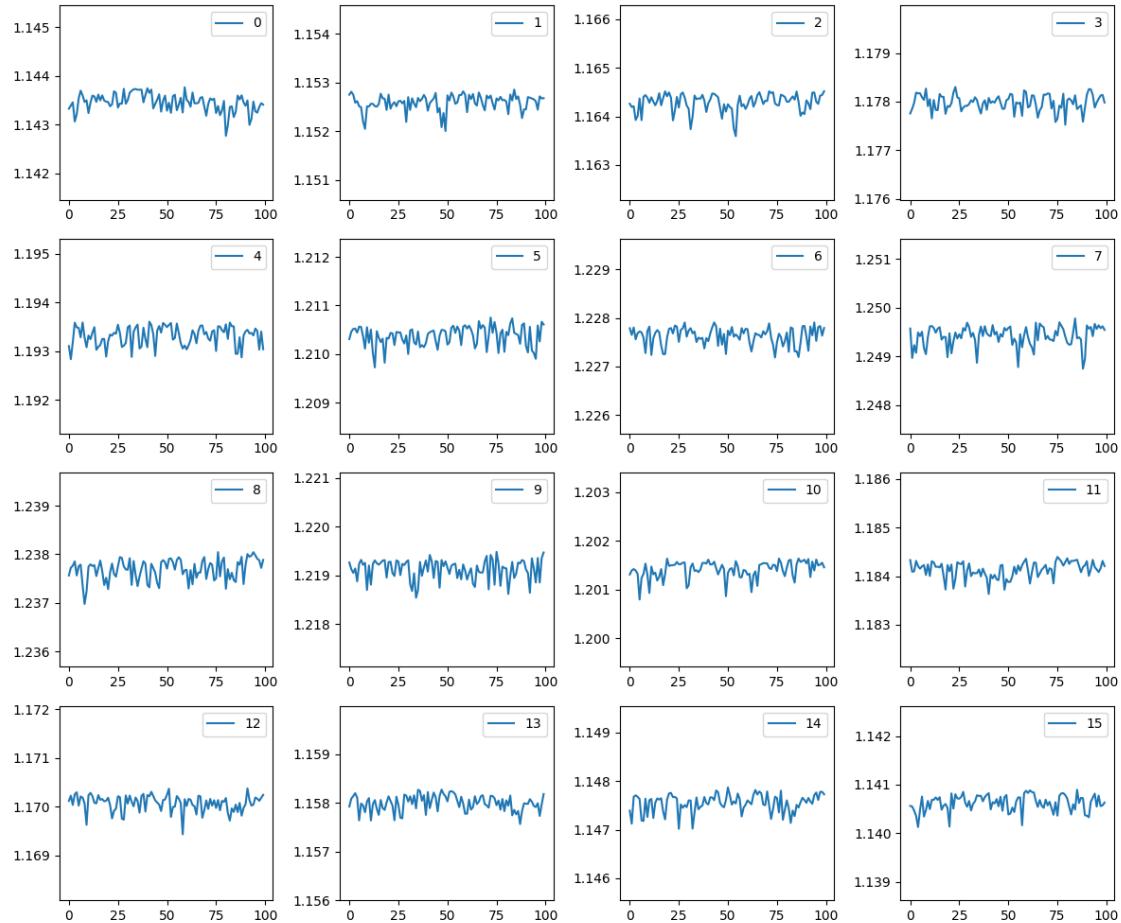


Figure 5: BGR Voltages for all trim settings (Same scaling)

Next the circuit is setup with a trimvalue of 5. Then the vdda1 is varied and the change in bandgap voltage is measured.

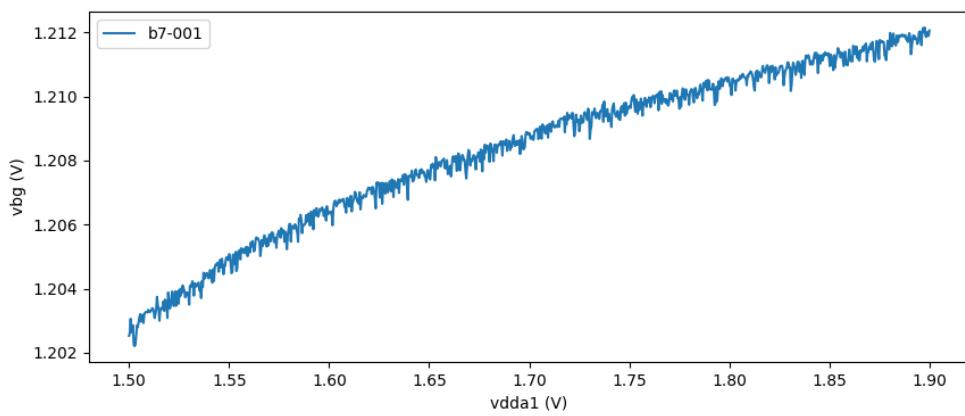


Figure 6: BGR Voltage as function of supply voltage. (trim setting 5)

1.2.1 Measurement Setup

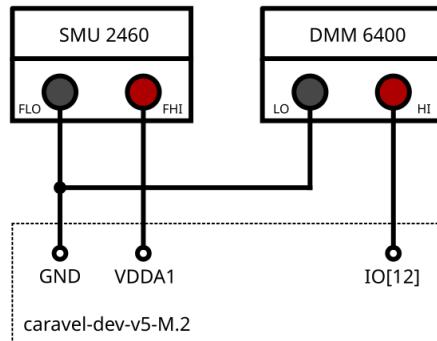
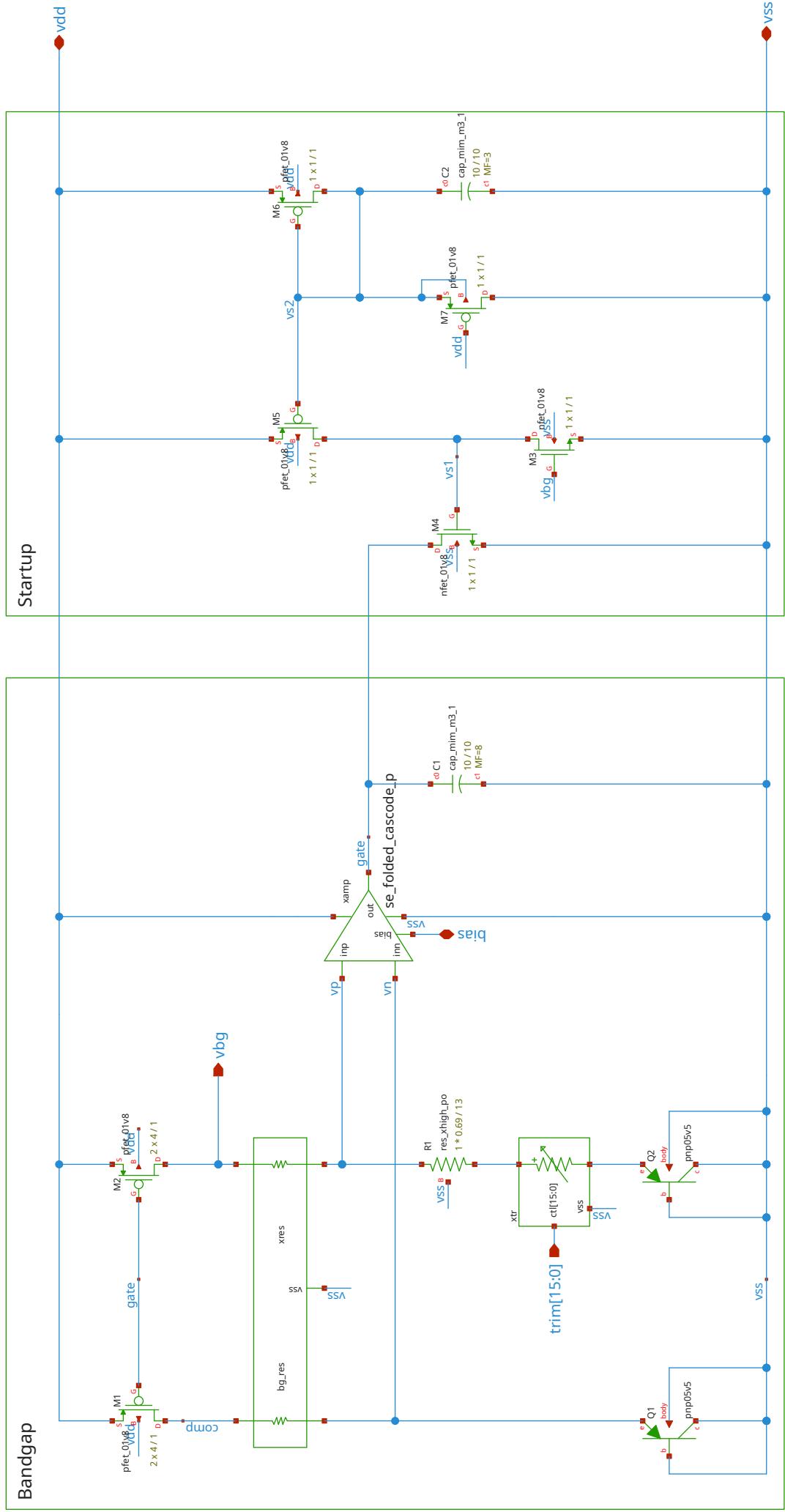


Figure 7: Measurement Setup for obtaining vbg values

1.2.2 TODO

- Measure the bandgap voltage over temperature



1.3 Bias Generator (BIAG)

The BIAG provides bias currents and voltages. several of the voltages can be measured using the TB.

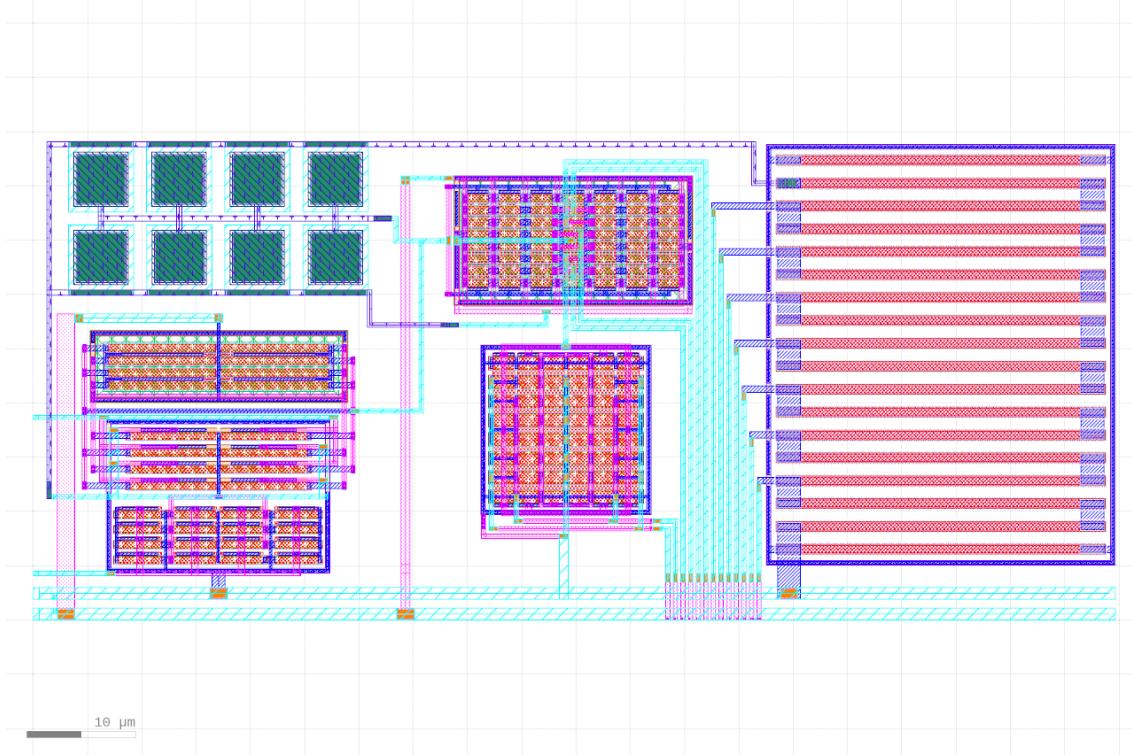


Figure 8: BIAG layout

With the input provided by the BGR that we have verified working, we have some expectation for the voltages at the $vb[6:0]$ output. Of those we can directly measure some fraction of the Bandgap voltage.:.

$$vb[2] = V_{bg} \cdot \frac{10R_u}{10R_u + 6R_u} = \frac{5}{8}V_{bg} \approx 750mV \quad (1)$$

$$vb[3] = V_{bg} \cdot \frac{8R_u}{8R_u + 8R_u} = \frac{1}{2}V_{bg} \approx 600mV \quad (2)$$

$$vb[4] = V_{bg} \cdot \frac{6R_u}{10R_u + 6R_u} = \frac{3}{8}V_{bg} \approx 450mV \quad (3)$$

The results of the measurement is shown below. The testbuffer switches between the 3 voltages. The measurement is repeated for 4 different supply voltages applied to vdda1.

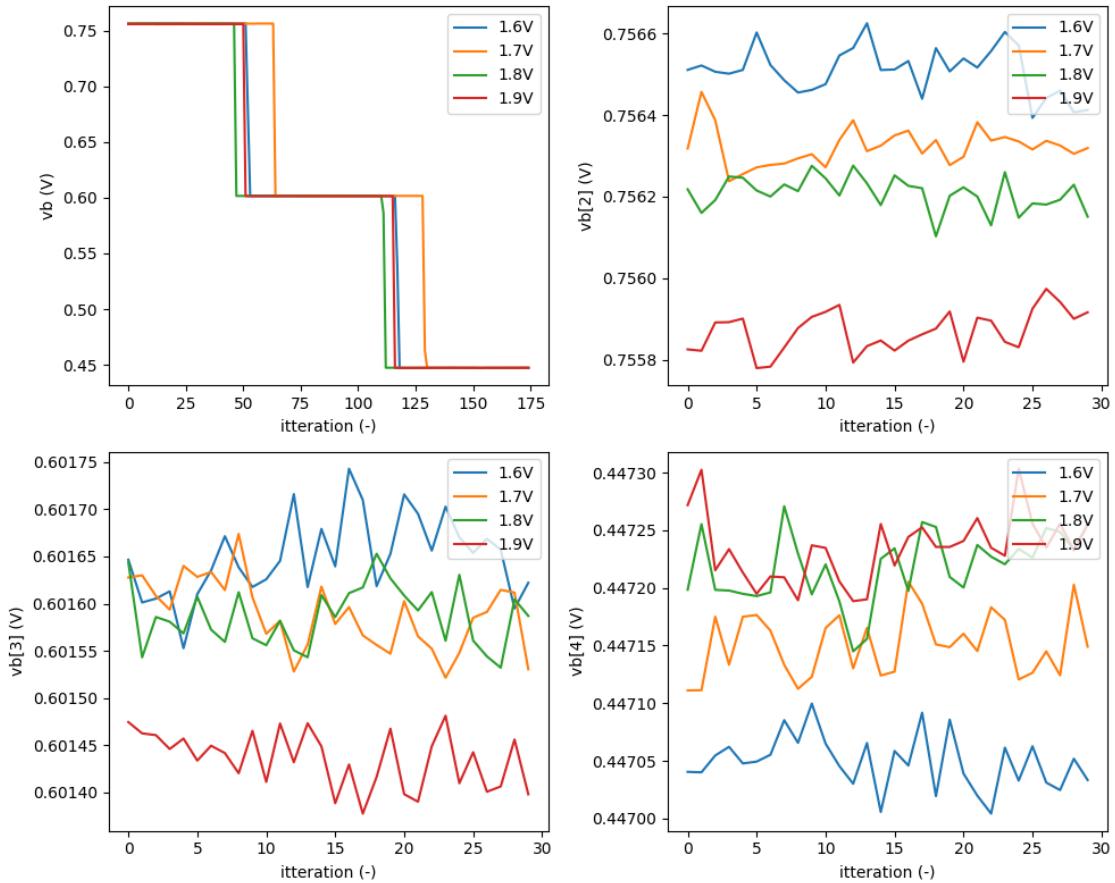


Figure 9: $v_{b[4:2]}$ voltages for different supply voltages

The values show good stability across supply variations and are quite close to the intended values.

1.3.1 Measurement Setup

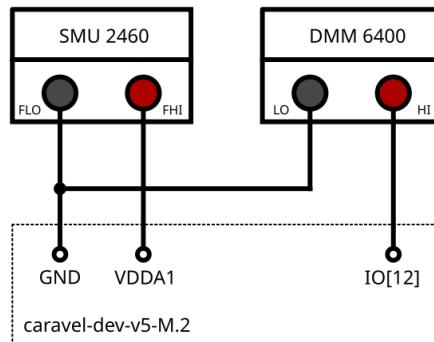
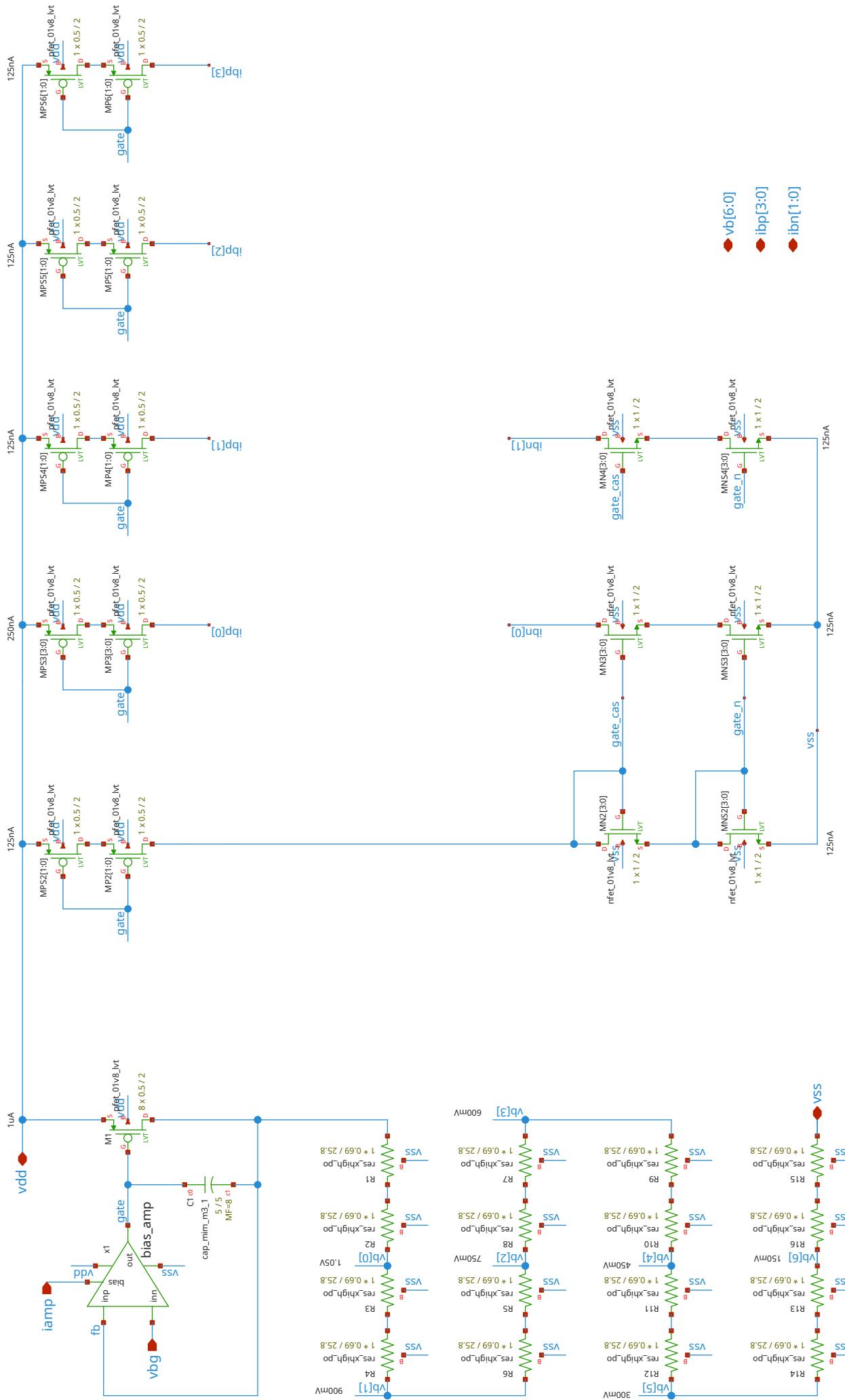


Figure 10: Measurement Setup for obtaining v_b values



1.4 Testbuffer (TB)

In the previous section it was already established that the testbuffer is operational, as it was used to measure both the BGR voltage and the output voltages the BIAG.

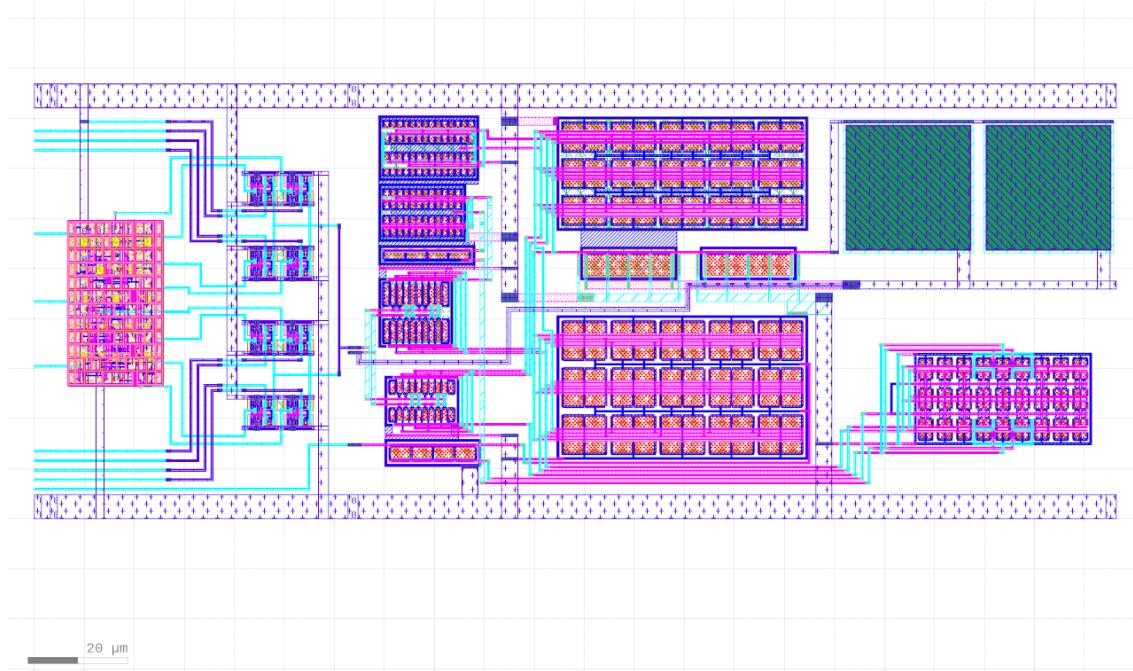


Figure 11: TB layout

The testbuffer has a multiplexer in front of it which lets us select one of 8 input signals. It defaults to vdd for 0 as the input code. Below is a measurement where the testbuffer is cycled through all of its inputs. The inputs are switched in a gray-code manner to provide a clear picture of all inputs and transistions.

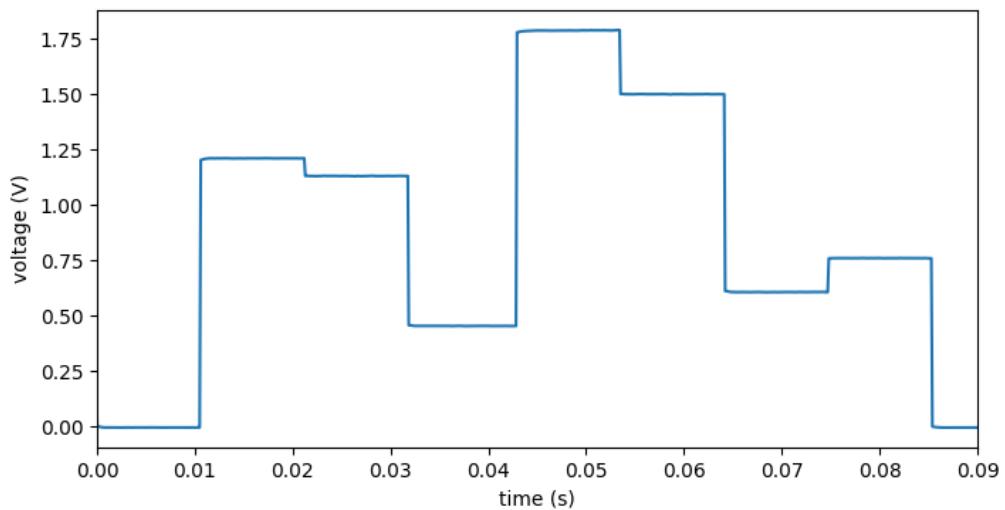


Figure 12: TB cycling through its inputs

Since the testbuffer can switch between vdd and vss as inputs it is possible to measure the slewrate of the amplifier directly. The resulting measurement can be seen in the picture below, where the measurement is overlayed by the results from the typical corner SPICE simulation.

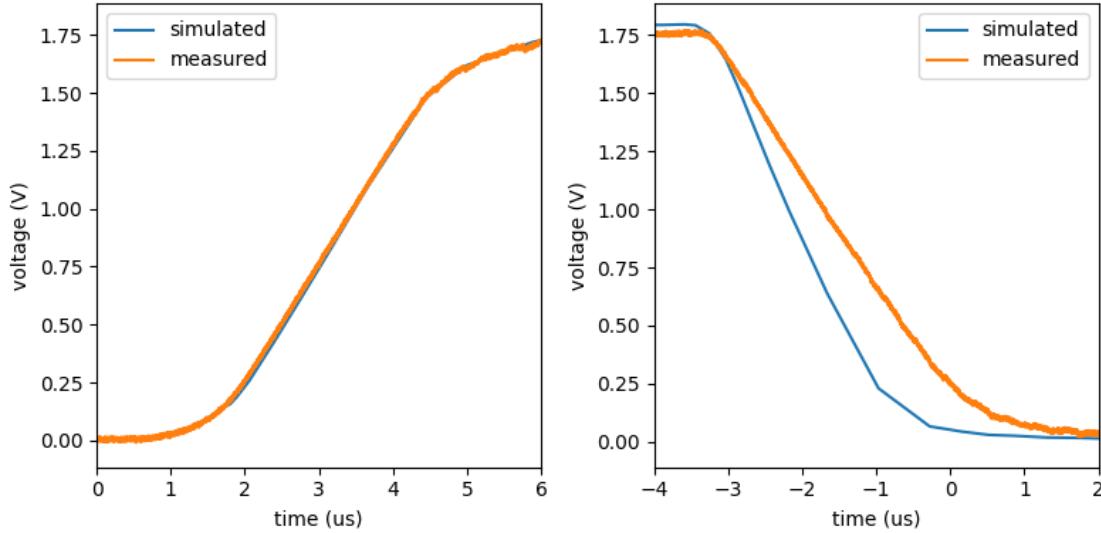


Figure 13: TB transitions

Finally the testbuffer is set to measure vbg.

The measurement bandwidth of the oscilloscope is set to 20MHz. The observed output can be seen below.

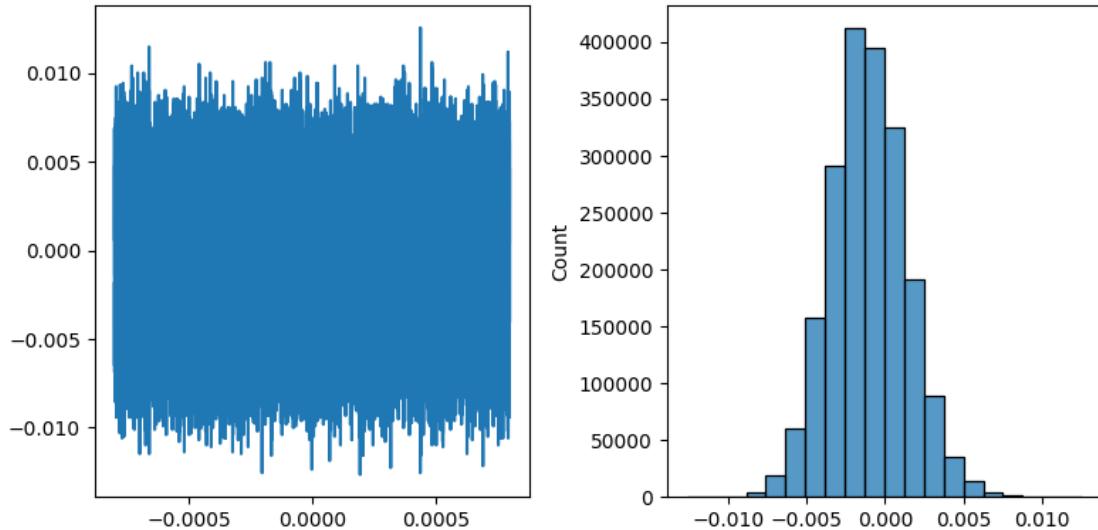
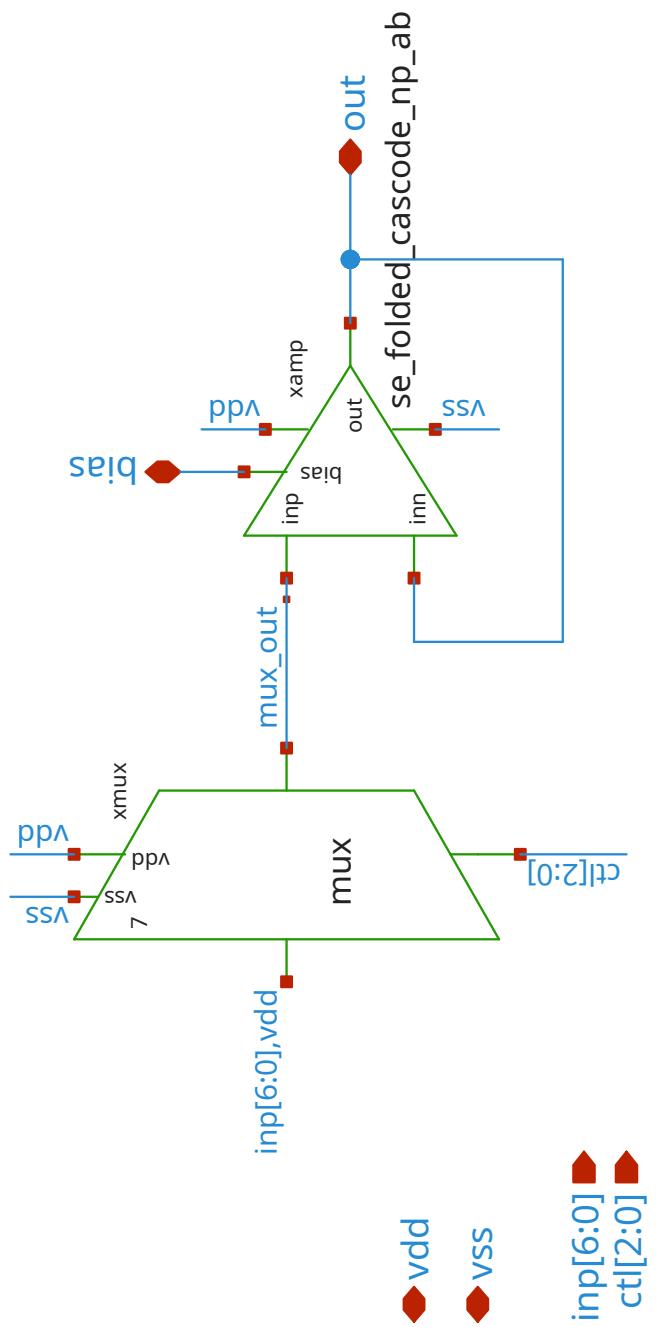
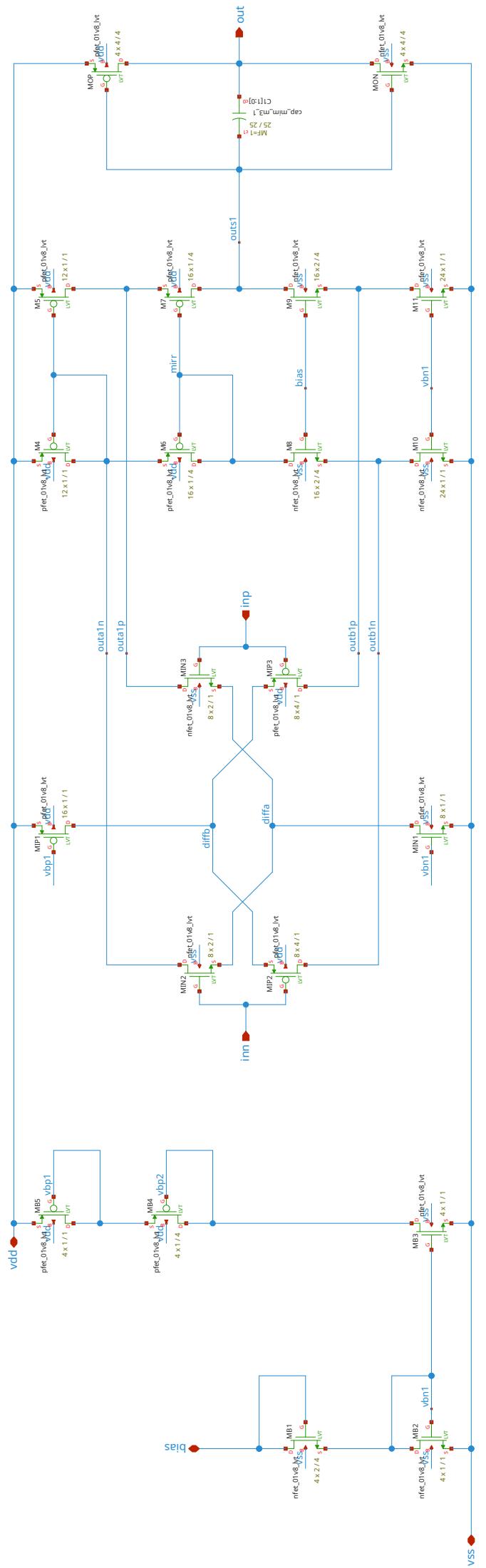


Figure 14: TB 20MHz BW noise measurement





1.5 Low Dropout Regulator (LDO)

There are two separate LDO providing 1.2V and 1.5V respectively. The reference voltage is provided by the BIAG and is multiplied by 2 inside the LDO.

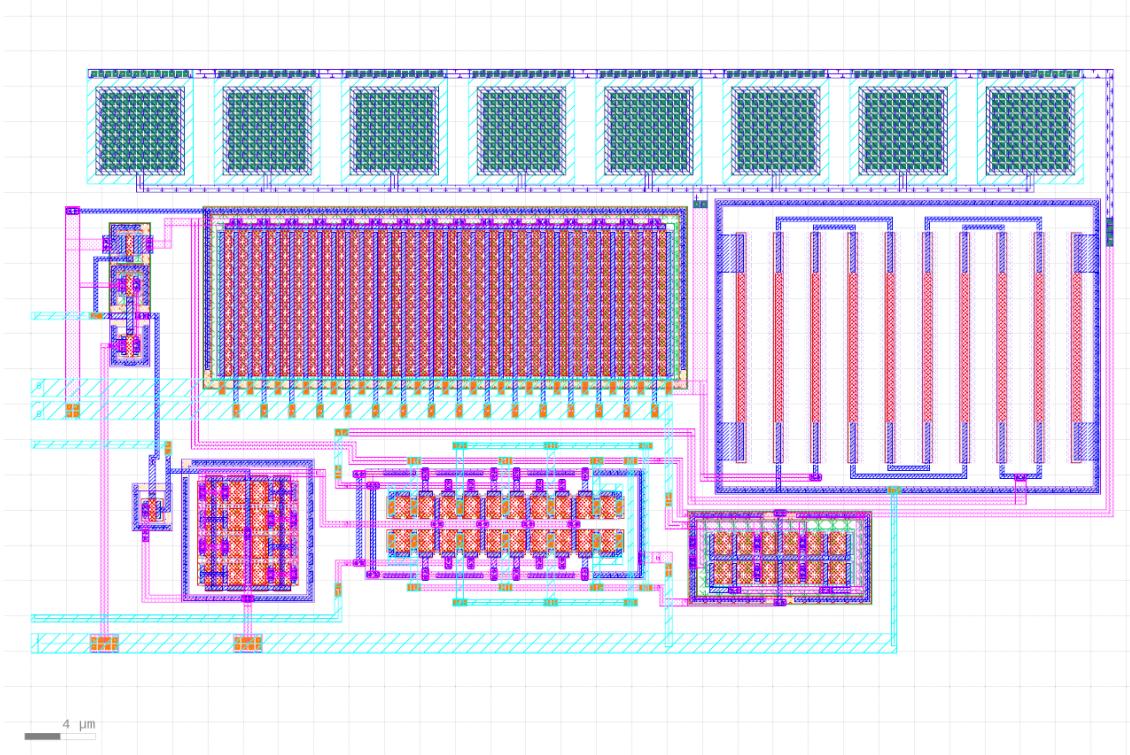


Figure 15: LDO layout

To follow measurement switches the 1.5V output on and off. The measurement is observed through the TB.

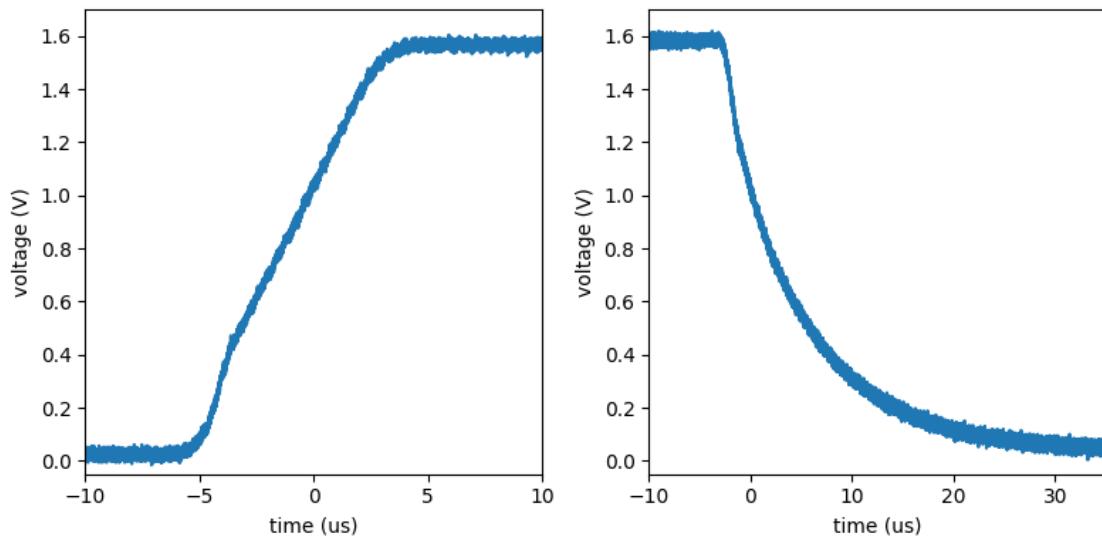
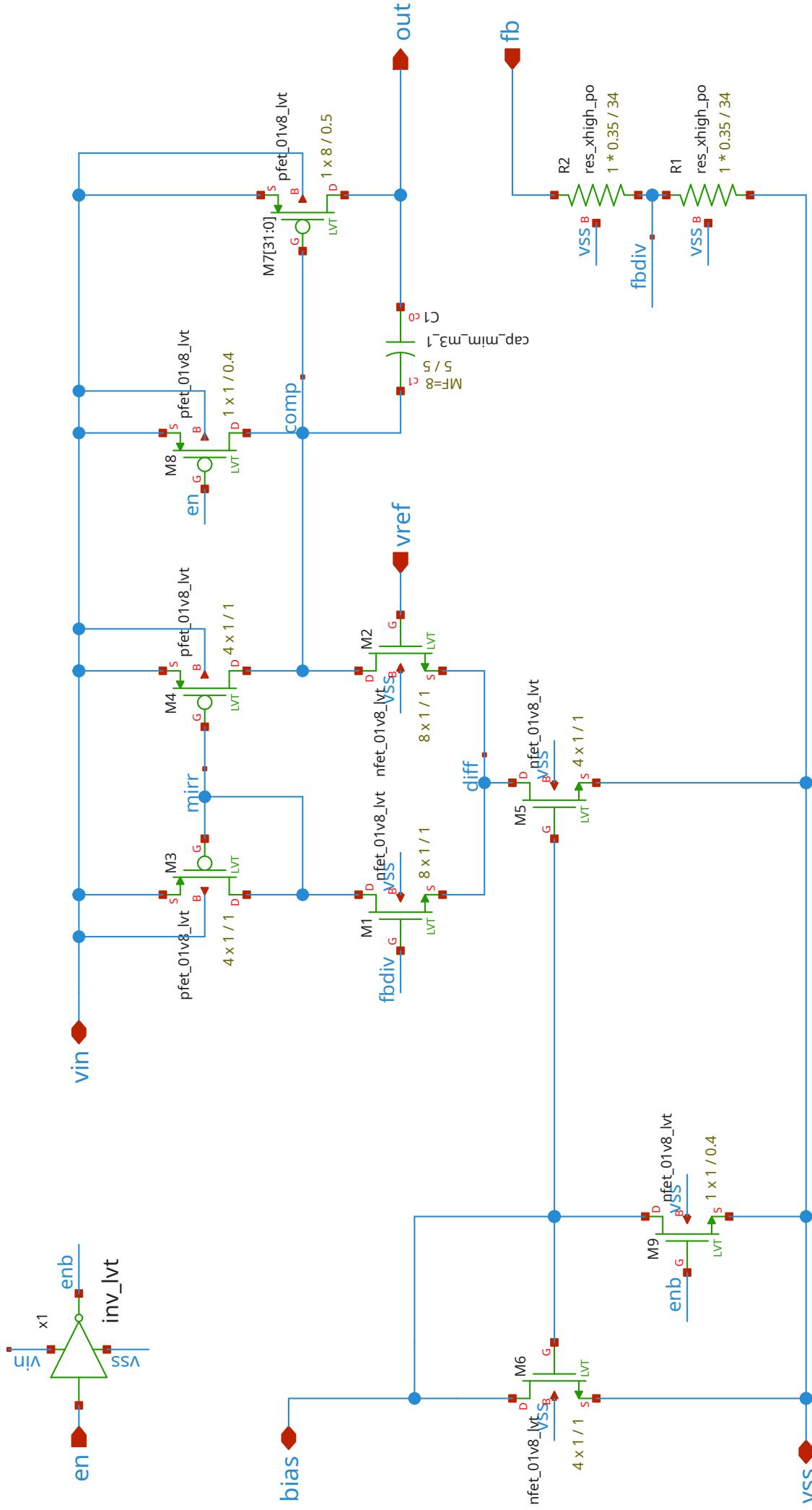


Figure 16: Analog LDO Rise and Fall edges

As we have seen from the measurements of the BIAG block there was a offset that can be seen here again, but multiplied by 2. Hence why the output rises higher than 1.5V. Note also that the switching happens so fast that the TB will be operating close to its maximum bandwidth on the rising edge.



1.6 Current Starved Oscillator (OSC)

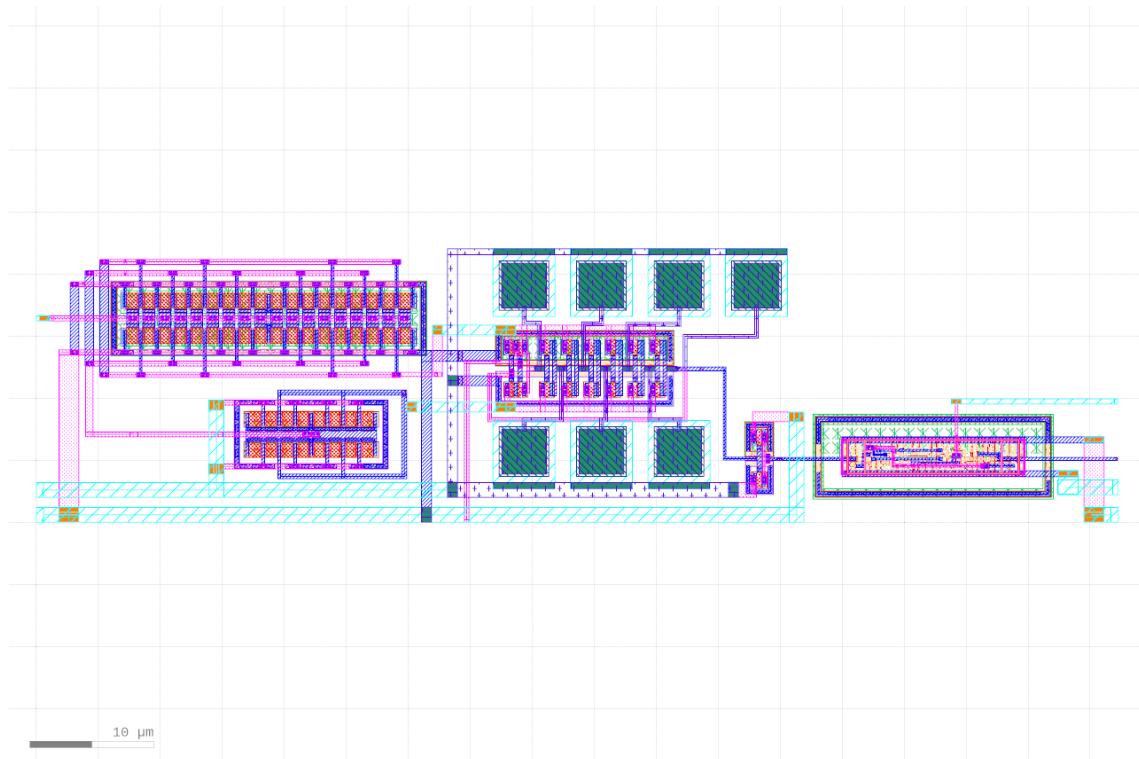
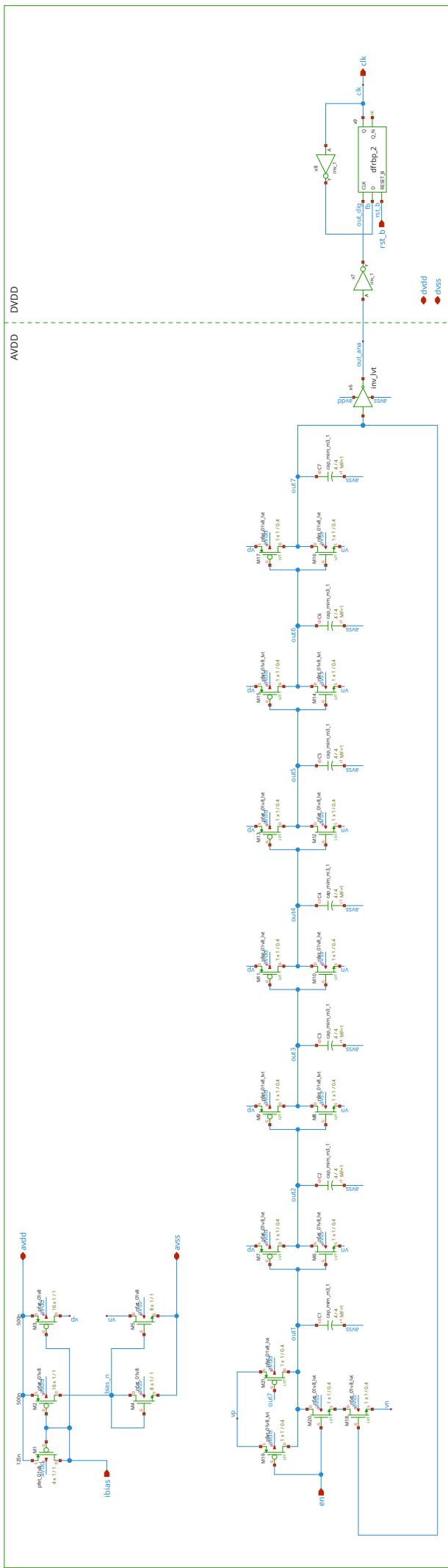


Figure 17: Oscillator Layout



2 SAR

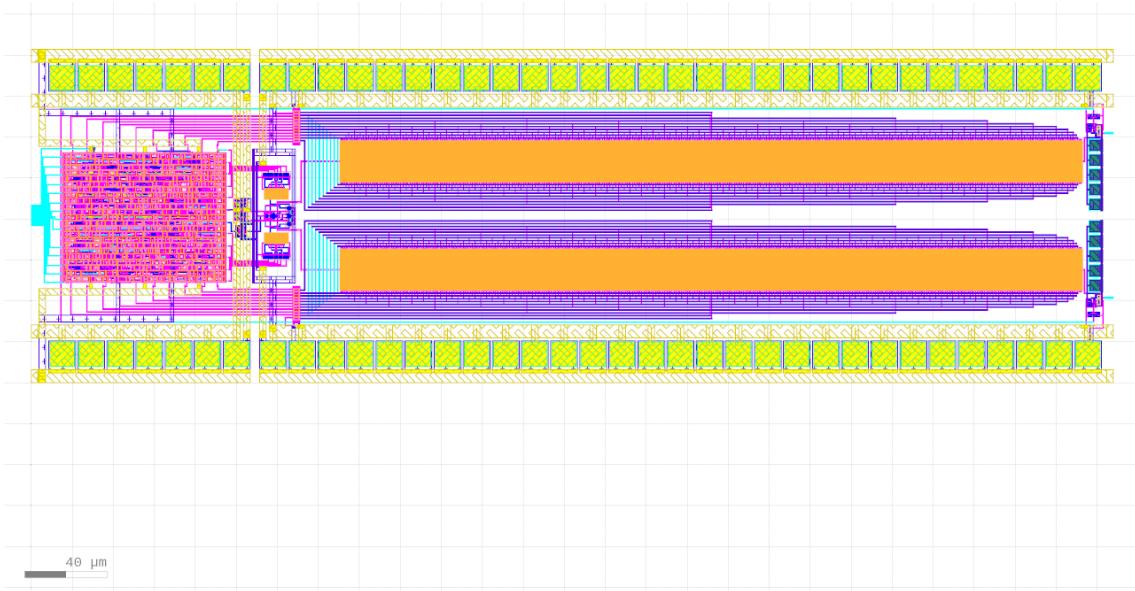
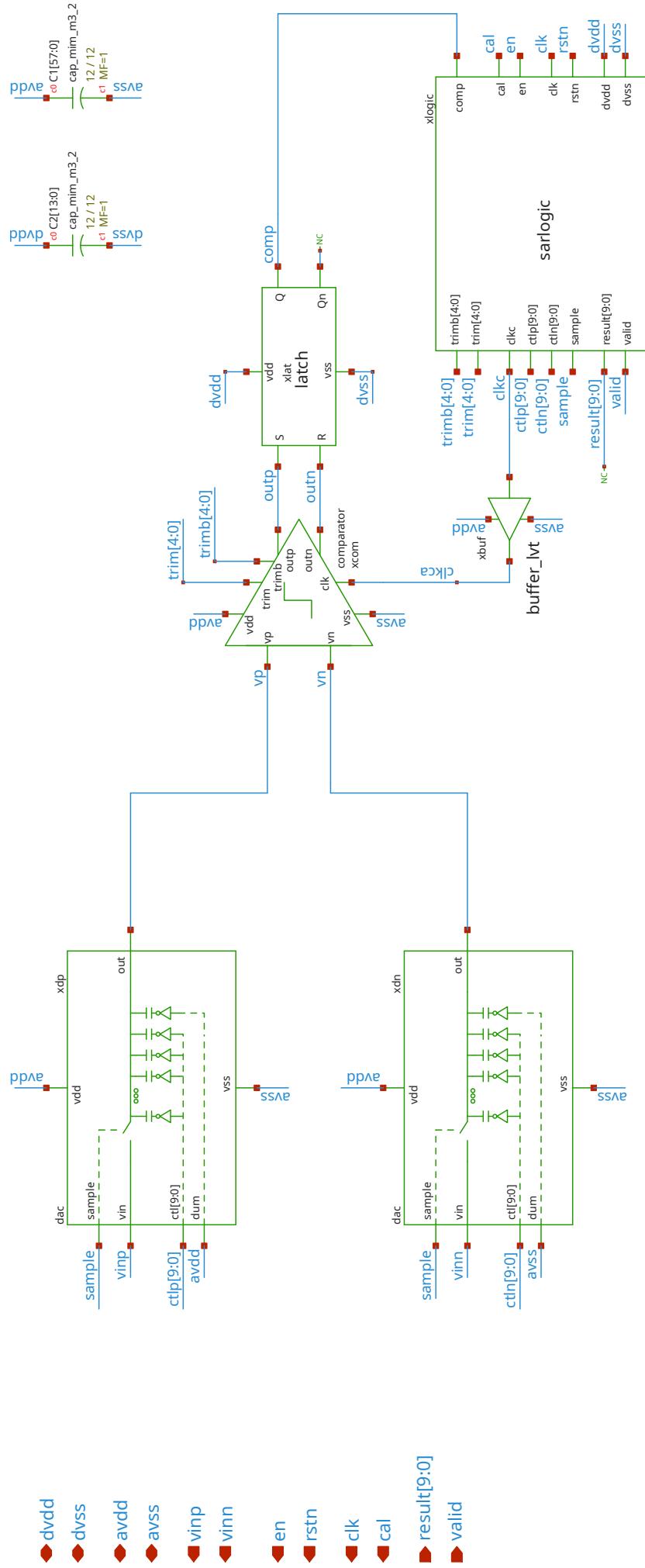


Figure 18: Layout of the SAR-ADC



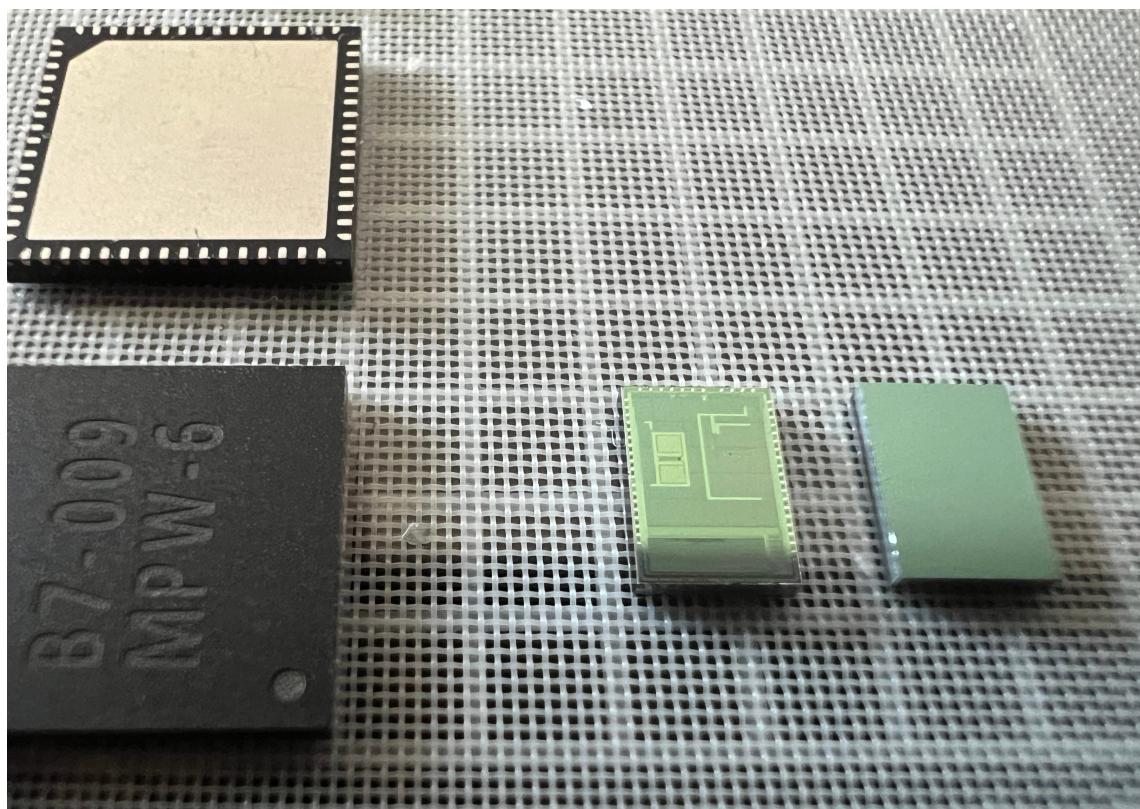


Figure 19: MPW-6 Parts