Measurement Report

MPW-6 B7, SLOT-013

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1 Main

This section concerns itself with the verification of the main analog block mostly referred to as the main block.

The main block consists of:

- Basis Current Source. (BCS)
- Bandgap Reference Voltage. (BGR)
- Bias Generator. (BIAG)
- Two Low Dropout Regulators. (LDO)
- Testbuffer. (TB)
- Current Starved Ring Oscillator. (OSC)

Each of the parts above will be discussed in detail in the following sections.

Figure 1: Main layout

vdd
ibp[0]
vss
xtb
vdd
bias
vss
vbg,vss,dvdd,vb[4],vb[3],vb[2],avdd
inp[6:0]
tbout
tbctl[2:0]
ctl[2:0]
testbuffer
rstn
vdd
vss
1 * 9.6 / 4
res_generic_m4
R1
dvss
dvss
vss
avss
avss
1 * 9.6 / 4
res_generic_m4
R3
regulator
xrd
vdd
vin
out
ibp[2]
bias
vb[3]
vref
fb
en_ldo_dig
en
vss
vss
1.2V
dvdd
regulator
xra
vdd
vin
out
ibp[1]
bias
vb[2]
vref
fb
en_ldo_ana
en
vss
vss
1.5V
avdd
vdd
bias_basis_current
xbc
vdd
ibp
ibpbas
vss
vss
ibn
ibnbas
bandgap
xbg
vdd
vdd
vbg
vbg_int
bgtrim[15:0]
trim
bias
vss
vss
vdd
bias
xbb
iamp
vdd
vb[6:0]
vb[6:0]
vbg
ibp[3:0]
ibp[3:0]
ibn[1:0]
ibn[1:0]
vss
vss
vdd
spdt
xsw
vss
refsel
vbg_ext
vbg
rstn
rosc
rst_b
avdd
dvdd
xro
clkint
en_clk_int
en
clk
ibn[0]
ibias
avss
dvss
avss
dvss
clksel
xcs
dvdd
dvss
dvss
rstn
rst_b
clkext
clk_out
clksys
clk_sel
en_div
clksel
en_clkdiv

1.1 Basis Current Source (BCS)

There is no direct measurement that can confirm the operation of the BCS. However the indirect verification of this block can be done by checking the BGR and BIAG, as these blocks directly depend on the BCS to provide a bias current for their respective amplifiers.

Figure 2: BCS layout

Startup
Current Source
vdd
vss
R1
res_xhigh_po
1 * 0.35 / 17
M10
pfet_01v8_lvt
1 x 0.5 / 1
M9
pfet_01v8_lvt
1 x 0.5 / 1
vsu
M7
nfet_01v8_lvt
1 x 1 / 0.3
M8
nfet_01v8_lvt
1 x 1 / 0.3
M4
pfet_01v8_lvt
8 x 1 / 1
M5
pfet_01v8_lvt
8 x 1 / 1
M6
pfet_01v8_lvt
2 x 1 / 1
vbp
ibp
ibn
M1
nfet_01v8_lvt
8 x 1 / 0.5
M2
nfet_01v8_lvt
32 x 1 / 0.5
M3
nfet_01v8_lvt
2 x 1 / 0.5
vbn
vres
R2
res_xhigh_po
1 * 0.35 / 14

1.2 Bandgap Reference Voltage (BGR)

The bandgap reference voltage is designed to nominal 1.214V at room temperature with a trim value: 8 out of 16. The trim value was intended to give suffient room for inacccuracies in both directions for the first tapeout.

Figure 3: BGR layout

The following plot shows a itteration through the trim range. Due to the physical arangement of the logic analyzer pins controling the trimvalues the stepping order in decimal is: 1,3,5,7,9,11,13,15,14,12,10,8,6,4,2,0

Figure 4: BGR Voltage during trimming

The value closest to target at is actually the highest trimable value! Luckily it does overreach slightly so the trim circuit is able to reach close to the target value of 1.214V at

room temperature.

Note that the measurement is made using the TB which depends on the BCS, BGR and BIAG. So offset, drift and noise is subject to all other parts of the verification chain as much at the BGR itself. This does therefore imply that those circuits are in fact operational and working at least to some degree as intended.

For the purpose of all following measurements it can be assumed that the BGR is trimmed with a value of 15 resulting in vbg to be close to the measured: 1.2184V.

1.2.1 TODO

- Measure the bandgap voltage over temperature
- Measure the bandgap voltage over supply variations

Bandgap
Startup
vdd
vss
vbg
gate
comp
M1
M2
pfet_01v8
2 x 4 / 1
bg_res
xres
vp
vn
inp
inn
out
bias
xamp
se_folded_cascode_p
R1
res_xhigh_po
1 * 0.69 / 13
C1
cap_mim_m3_1
10 / 10
MF=8
xtr
trim[15:0]
ctl[15:0]
Q1
Q2
pnp05v5
body
M5
M6
M4
M7
M3
nfet_01v8
1 x 1 / 1
vs1
vs2
C2
MF=3

1.3 Bias Generator (BIAG)

The BIAG provides bias currents and voltages. several of the voltages can be measured using the TB.

Figure 5: BIAG layout

With the input provided by the BGR that we have verified working, we have some expectation for the voltages at the vb[6:0] output. Of those we can directly measure some fraction of the Bandgap voltage.:

$$vb[2] = V_{bg} \cdot \frac{10R_u}{10R_u + 6R_u} = \frac{5}{8}V_{bg} \approx 750mV \tag{1}$$

$$vb[3] = V_{bg} \cdot \frac{8R_u}{8R_u + 8R_u} = \frac{1}{2}V_{bg} \approx 600mV \tag{2}$$

$$vb[4] = V_{bg} \cdot \frac{6R_u}{10R_u + 6R_u} = \frac{3}{8}V_{bg} \approx 450mV \tag{3}$$

The results of the measurement is shown below. The testbuffer switches between the 3 voltages.

Figure 6: vb[4:2] voltages

The voltages are somewhat off from the ideal values. Interestingly though is the delta between the values is 150mV suggesting a good matching in the resistor array. This lets us conclude that the observed voltage difference to the ideal voltage (21mV) is the input offset voltage of the amplifer inside the BIAG.

1.3.1 TODO

- Measure the current consumption of the circuit with a voltage of 0V applied to the vbg_ext input switched to the external voltage using refsel. LDO should be disabled and the testbuffer switched to vdd i.e. 0 no setting.

  The current is then measured to get the nominal consumption of the BGR and the BCS. Then a voltage of 1.2V is applied to vbg_ext. The current consumption increase should now be related to the bias currents generated and consumed by the circuit. A total of 1.625uA is expected.

  From this a figure of the resistor chain can be derived and therefore the absolute value of the unit resistor.

- Measure multiple devices to establish if the offset voltag of 21mV is random or systematic mismatch.

- redo mesurement using multimeter instead of oscilloscope for better accuracy.

vdd
1uA
125nA
250nA
iamp
fb
vbg
inp
inn
bias
out
x1
bias_amp
gate
M1
nfet_01v8_lvt
8 x 0.5 / 2
C1
cap_mim_m3_1
5 / 5
MF=8
MPS2[1:0]
MP2[1:0]
MPS3[3:0]
MP3[3:0]
MPS4[1:0]
MP4[1:0]
MPS5[1:0]
MP5[1:0]
MPS6[1:0]
MP6[1:0]
1 x 0.5 / 2
ibp[0]
ibp[1]
ibp[2]
ibp[3]
vb[1]
vb[0]
vb[2]
vb[3]
vb[5]
vb[4]
vb[6]
900mV
1.05V
750mV
600mV
300mV
450mV
150mV
R4
R3
R2
R1
R6
R5
R8
R7
R12
R11
R10
R9
R14
R13
R16
R15
res_xhigh_po
1 * 0.69 / 25.8
vss
MN2[3:0]
MNS2[3:0]
MN3[3:0]
MNS3[3:0]
MN4[3:0]
MNS4[3:0]
nfet_01v8_lvt
1 x 1 / 2
gate_cas
gate_n
ibn[0]
ibn[1]
vb[6:0]
ibp[3:0]
ibn[1:0]
R17[1:0]
MDUM3[3:0]
MP1
24 x 0.5 / 2
MDUM1[3:0]
MDUM2[3:0]
MDUM_1[3:0]
MDUM[7:0]
Dummies

1.4 Testbuffer (TB)

In the previous section it was already established that the testbuffer is operational, as it was used to measure both the BGR voltage and the output voltages the BIAG.

Figure 7: TB layout

The testbuffer has a multiplexer in front of it which lets us select one of 8 input singnals. It defaults to vdd for 0 as the input code. Below is a measurement where the testbuffer is cycled through all of its inputs. The inputs are switched in a gray-code manner to provide a clear picture of all inputs and transistions.

Figure 8: TB cycling through its inputs

Since the testbuffer can switch between vdd and vss as inputs it is possible to measure the slewrate of the amplifier directly. The resulting measurement can be seen in the picture below, where the measurement is overlayed by the results from the typical corner SPICE simulation.

Figure 9: TB transitions

Finally the testbuffer is set to measure vbg.
The measurement bandwith of the oscilloscope is set to 20MHz. The observed output can be seen below.

Figure 10: TB 20MHz BW noise measurment

vdd
vss
inp[6:0]
ctl[2:0]
inp[6:0],vdd
mux
7
vss
vdd
xmux
vss
vdd
ctl[2:0]
mux_out
bias
inp
bias
out
inn
xamp
vdd
vss
se_folded_cascode_np_ab
out

vdd
vss
bias
inn
inp
out
vbp1
vbp2
vbn1
diffa
diffb
outa1n
outa1p
outb1p
outb1n
mirr
outs1
MB1
MB2
MB3
MB4
MB5
M1P1
M1P2
M1P3
M1N1
M1N2
M1N3
M4
M5
M6
M7
M8
M9
M10
M11
M0P
M0N
C1[19]
cap_mim_m3_1

vdd
mirr
outs1
diffa
vss
diffb
vbn1
Dummies

1.5 Low Dropout Regulator (LDO)

There are two seperate LDO providing 1.2V and 1.5V respectively. The reference voltage is provided by the BIAG and is multiplied by 2 inside the LDO.

Figure 11: LDO layout

To follwing measurement switches the 1.5V output on and off. The measurement is observed through the TB.

Figure 12: Analog LDO Rise and Fall edges

As we have seen from the measurements of the BIAG block there was a offset that can be seen here again, but multiplied by 2. Hence why the output rises higher than 1.5V. Note also that the switching happens so fast that the TB will be operating close to its maximum bandwidth on the rising edge.

en
vin
x1
enb
vss
inv_lvt
vin
pfet_01v8_lvt
M3
4 x 1 / 1
mirr
M4
pfet_01v8_lvt
4 x 1 / 1
en
M8
pfet_01v8_lvt
1 x 1 / 0.4
M7[31:0]
pfet_01v8_lvt
1 x 8 / 0.5
bias
comp
M1
pfet_01v8_lvt
fbdiv
vss
8 x 1 / 1
nfet_01v8_lvt
M2
vss
8 x 1 / 1
vref
out
MF=8
5 / 5
cap_mim_m3_1
C1
diff
fb
nfet_01v8_lvt
M6
vss
4 x 1 / 1
M5
nfet_01v8_lvt
vss
4 x 1 / 1
R2
res_xhigh_po
1 * 0.35 / 34
vss
fbdiv
R1
res_xhigh_po
1 * 0.35 / 34
vss
M9
nfet_01v8_lvt
enb
vss
1 x 1 / 0.4
vss

vss
R3[1:0]
res_xhigh_po
1 * 0.35 / 8.5
mirr
M15
pfet_01v8_lvt
vin
2 x 1 / 1
comp
M16
pfet_01v8_lvt
mirr
vin
2 x 1 / 1
mirr
nfet_01v8_lvt
M13
vss
2 x 1 / 1
comp
nfet_01v8_lvt
M12
vss
2 x 1 / 1
diff
nfet_01v8_lvt
M11
vss
bias
4 x 1 / 1
bias
nfet_01v8_lvt
M10
vss
4 x 1 / 1
Dummies

1.6 Current Starved Oscillator (OSC)

Figure 13: Oscillator Layout

AVDD
DVDD
avdd
avss
ibias
bias_n
vp
vn
en
out1
out2
out3
out4
out5
out6
out7
out_ana
out_dig
fb
rst_b
clk
inv_lvt
dfrbp_2
inv_1
dvdd
dvss

2 SAR

Figure 14: Layout of the SAR-ADC

dvdd
dvss
avdd
avss
vinp
vinn
en
rstn
clk
cal
result[9:0]
valid
dac
xdp
vdd
sample
vinp
ctlp[9:0]
avdd
vin
out
ctl[9:0]
dum
vss
xdn
vinn
ctln[9:0]
avss
vp
vn
trim[4:0]
trimb[4:0]
trim
trimb
outp
outn
clk
comparator
xcom
clkca
xbuf
buffer_lvt
latch
xlat
S
R
Q
Qn
comp
NC
C2[13:0]
C1[57:0]
cap_mim_m3_2
12 / 12
MF=1
sarlogic
xlogic
clkc
ctlp[9:0]
ctln[9:0]
result[9:0]
valid
cal
en
clk
rstn
dvdd
dvss

Figure 15: MPW-6 Parts