ECE 176 – Computer Aided Engineering in Digital Design
Fall 2014

Design a FSM Sequence Detector
Assignment 11

Objectives:

1. Design and development of a sequential Moore Machine
2. Synthesis the design and check the code for correctness
3. Perform an RTL simulation

Step 1: Design a Moore FSM Machine

1. Go through the sequential design process to design and implement a Moore machine detecting the "11010" sequence. This Moore machine has an input x, asynchronous reset input, clk input, and output w. Use D-FF to implement the circuit.
2. Develop Verilog code and testbench for the sequence detector

Step 2: Using Quartus II synthesize the design and check the code for correctness

1. Synthesize and compile the design.
2. Correct any warning and errors. Repeat compile and synthesis and error checking until the Quartus II software reports that the "**Compile Analysis & Synthesis is Successful**".

Step 3: Perform an RTL Simulation

Develop a Verilog **testbench** file using the ModelSim-Altera Starter Edition simulation tool. Follow the process as we did in class to develop your **testbench** and use corresponding generated design files (.VO and .SDO) to simulate your design. Use simulation generated signals to verify the Verilog code is functioning correctly. Examine the waveform for analysis and behavior of your sequence detector to be integrated into your report.