SORRY IT WAS A LITTLE LATE, WE HAD OUR GRADUATION CEREMONY TODAY.

Fabrication of Solar Cell

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I. Abstract

In this experiment, two silicon-based solar cells were fabricated. The first solar cell was a "control" where the mask was provided. The second solar cell was an "experimental" where the mask was modified to evaluate the effects of front-side contact geometry. Our "experimental" design involved wider and more fingers. The goal of the "experimental" solar cell was to increase the efficiency. Solar cells are important because they provide a renewable energy source without emitting greenhouse gases. Currently, the Earth's climate is worsening, and solar cells will alleviate this problem. The p-type silicon wafer underwent phosphorus spin-on dopant, drive-in anneal, photolithography, and aluminum deposition. Photolithography allowed us to define the front contact pattern. Thermal evaporation was used to deposit the aluminum. These procedures were done in the UCLA Engineering V Semiconductor Laboratory. The "control" silicon-based solar cell had an efficiency of 3.07% whereas the "experimental" silicon-based solar cell had an efficiency of 2.99%. This proved to be unexpected because we believed the efficiency would have increased due to a larger light collecting area. We have attributed the decline in efficiency to fabrication issues, such as overexposure and improper metal lift-off. Although our "experimental" solar cell had a lower efficiency, both devices proved to be functional.

II. Introduction

The purpose of this experiment was to fabricate a silicon-based solar cell and examine its change in efficiency upon changing the mask design. Solar cells consist of a shallow p-n

junction. a front ohmic contact stripe and fingers, a back ohmic contact, and an antireflective coating. Under illumination, photons that have energy greater than E_g will contribute E_g amount of energy which creates electron-hole pairs in the depletion layer [1]. These pairs are separated by the built-in electric field which in turn generates a photocurrent. The schematic of Figure 1 showcases a solar cell with antireflection coating, front contact stripe, fingers, and the p-n junction.

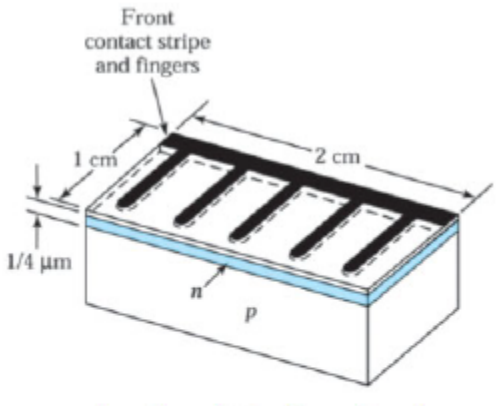


Figure 1. Representation of a p-n junction solar cell [1].

A key portion of this experiment was to identify ways to enhance the efficiency of solar cells. Three ways to increase the efficiency of a solar cell is to (1) increase the light collected, (2) increase the carriers, and (3) to extract the light with minimum resistive loss [2]. To successfully increase the light collected, antireflective coatings and surface texturing must be applied. Antireflective coatings are thin layers of dielectric material with a specific thickness to create destructive interference so there are no reflected waves, as shown in Figure 2 [2].

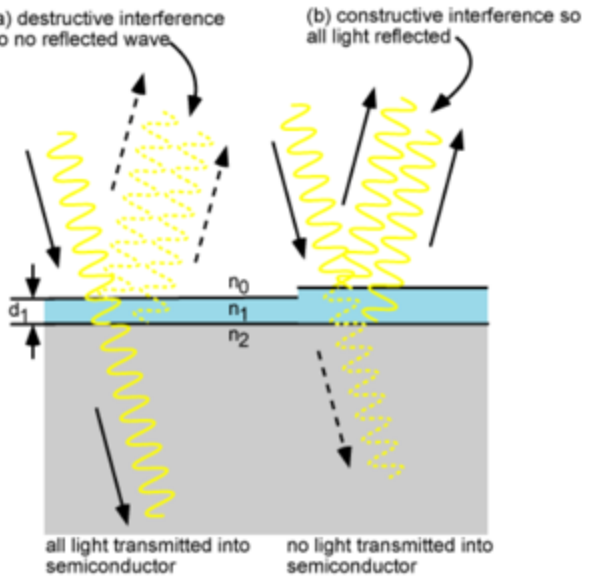


Figure 2. Comparison between reflected waves interacting destructively versus constructively [2].

Surface texturing can be applied to silicon through etching, which allows reflected light to hit another surface, as seen in Figure 3.

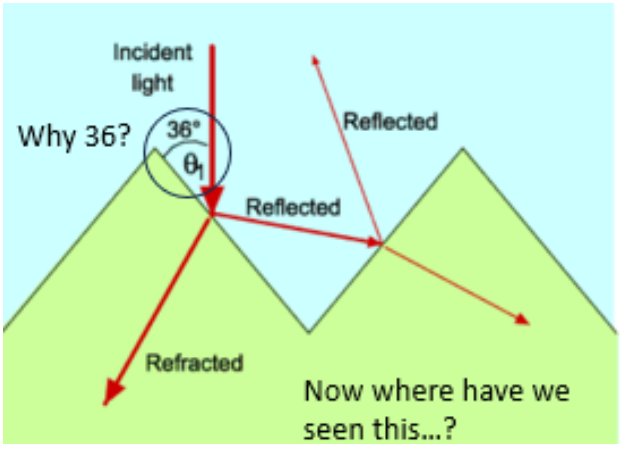


Figure 3. Textured surface after etching silicon, which creates a 36°. This is the angle between the (100) plane and the etched (111) surface [2].

Instead of the incident light soley escaping, with the textured surface it can reflect into nearby surfaces and increase the efficiency of the solar cell. To increase the number of carriers in a solar cell, recombination must be reduced. Recombination can be classified as radiative,

Shockley-Read-Hall, or Auger. Shockley-Read-Hall and Auger are dominant in silicon solar cells. To minimize recombination, heavy doping under the solar cell's contacts and its rear is essential [2]. This process can be visualized in Figure 4.

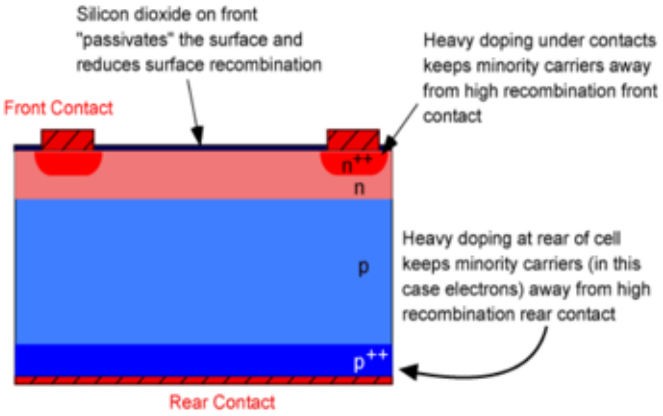


Figure 4. To reduce recombination, heavy doping and surface passivation can be used [2].

As stated in Figure 4, doping at these regions keeps carriers away from these high recombination areas. Additionally, using a thin oxide layer allows for surface passivation which minimizes the number of broken silicon bonds and reduces recombination [2]. To minimize the resistive losses, the solar cell must be designed with certain things in mind. Key design considerations are to use narrow fingers and busbars to collect current.

The spin-on dopant method uses a non-hygroscopic solution that is spun onto the wafer and then baked [3]. The benefits of the spin-on dopant process are there is precise control of the dopant concentrations, cost-effectiveness, and combined furnace processes. The soft bake is used to prepare the device for drive-in anneal. This process is important because it allows the user to control the depth and distribution of dopants [3]. The diffusion profile can be from an unlimited source or a limited source. The equation representing the diffusion from an unlimited source is

$$N(x,t) = N_s[1 - erf(\frac{x}{2\sqrt{Dt}}) \quad (1)$$

where N is concentration, N_S is the surface impurity concentration, D is diffusivity, x is depth, t is time [4]. For the purposes of this lab, diffusion from an unlimited source will be applied. The equation representing the diffusion from a limited source is

$$N(x,t) = \frac{Q}{\sqrt{\pi Dt}} exp(-\frac{x^2}{4Dt}) \quad (2)$$

where the variables are the same as equation (1) but Q is dose [4]. Equation (1) uses the error function to describe how the dopant concentration decreases with depth. Equation (2) implies that the surface concentration drops over time. The difference between each process is outlined in Figure 5.

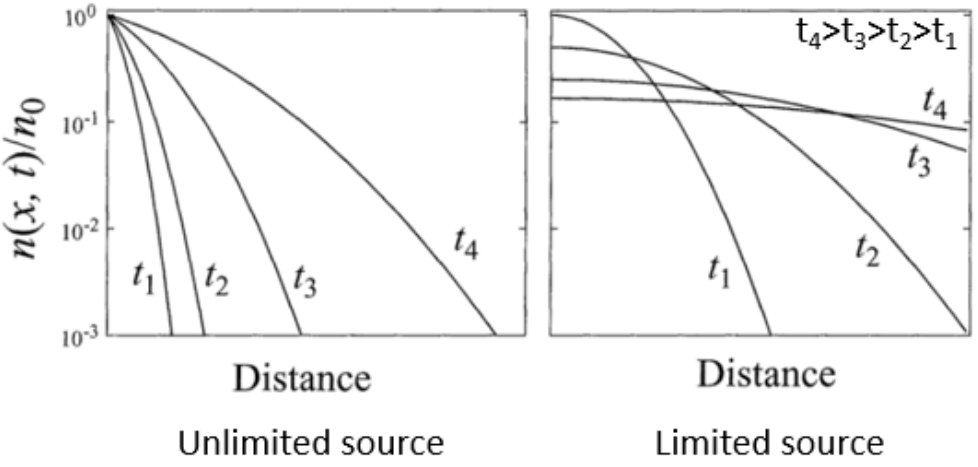


Figure 5. Unlimited source versus limited source [5].

In Figure 5, the dopants diffuse deeper into the silicon wafer as time increases when under an unlimited source.

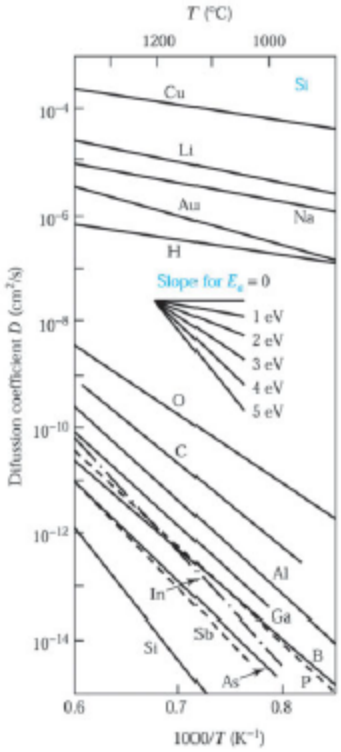


Figure 6. Diffusion coefficient as function of 1/T for silicon [1].

Figure 6 shows the diffusion coefficient profile for silicon, which will be used later in this report. When the wafer is under a limited source, the concentration of the surface decreases as time increases. The results of spin-on dopant diffusion, soft bake, and drive-in anneal are shown in Figure 7.

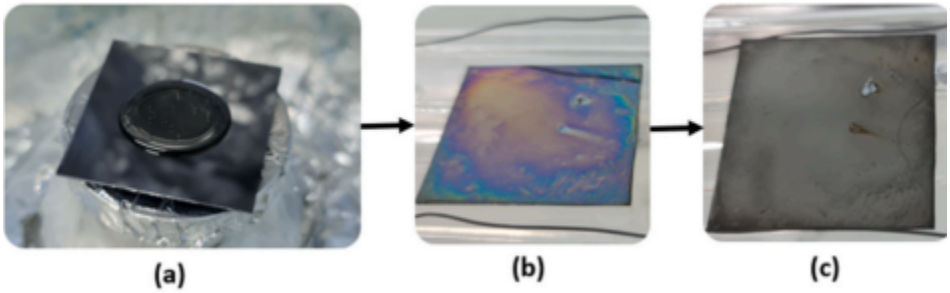


Figure 7. (a) Spin-on dopant deposition on silicon wafer. (b) Soft-bake of wafer. (c) Wafer after undergoing drive-in anneal [3].

Photolithography is the process of transferring patterns of a mask to a photoresist located on a wafer. There are two types of photoresists, positive and negative. Their differences are shown in Figure 8.

Figure 8. (a) Positive photoresist. (b) Negative photoresist [1].

A positive photoresist is composed of lower molecular weight structures and has weaker links whereas a negative photoresist has long structural chains [6]. This experiment uses a positive photoresist, and the mechanism is shown in Figure 9 below.

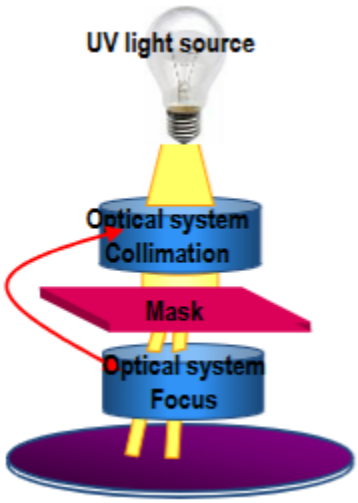


Figure 9. Schematic representation of photolithography [6].

The purpose of this procedure is to define where the metal contacts will later be deposited. As discussed in later sections, this step is vital to the efficiency of solar cells because metal deposition and lift-off are dependent on PR.

Once photolithography has been achieved, physical vapor deposition (PVD) is used to deposit aluminum onto both sides of the silicon wafer. The most common methods of PVD are evaporation, e-beam evaporation, plasma spray deposition, and sputtering. For the purposes of

this lab, only evaporation is used. To perform this specific type of PVD, a Denton vacuum is required. Figure 10 below is a schematic representation of evaporation.

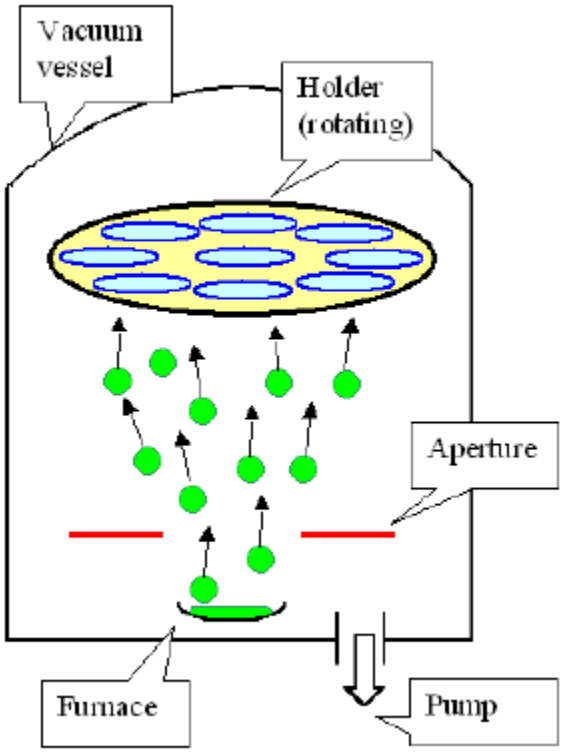


Figure 10. Schematic representation of evaporation [6].

From Figure 10, a metal is heated in the chamber until it evaporates and it will travel upwards onto the rotating wafers located on the holder. The rate at which the metal atoms evaporate can be described by the following equation

$$N = N_0 exp(\frac{-\Phi}{kT}) \quad (3)$$

where N is the number of molecules leaving a unit area of evaporation per second, Φ is the activation energy to evaporate one molecule, k is the Boltzmann constant, and T is the temperature [6]. To diffuse the aluminum into the silicon wafer, rapid thermal annealing (RTA) was used. RTA is performed with a transient lamp shown in Figure 11.

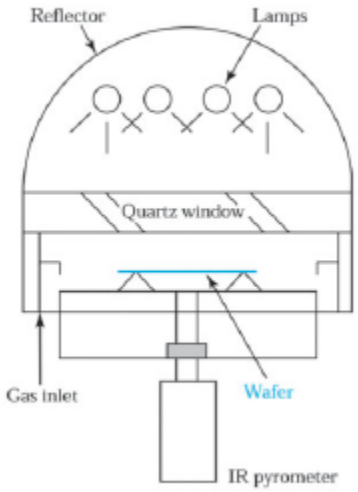


Figure 11. Schematic representation of RTA system [1].

In Figure 11, the RTA system is shown, where the wafer is heated quickly at low pressures. The rapid heating and cooling of the wafer is created because the lamps are hotter than the wafer while the chamber is cooler than it [1].

To evaluate the performance of solar cells, IV characterization must be performed under dark and light conditions. It is important to test the solar cell under both conditions because each provides different insights into its performance. Obtaining the IV curve in the dark is used to examine the diode properties because electrically generated carriers are injected into the circuit [7]. Under illumination, light generated carriers are injected into the circuit and the standardized conditions for IV characterization under light are AM 1.5 for terrestrial cells, 100 mW/cm^2 for illumination, and 25℃ for cell temperature [7]. A comparison between a dark and illuminated IV curve is seen in Figure 11.

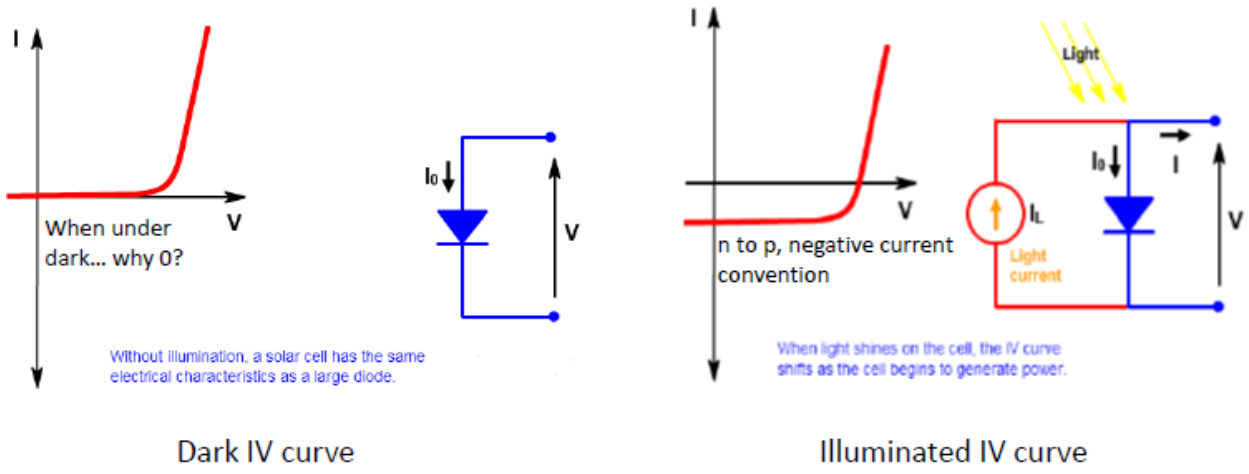


Figure 12. Dark versus illumination IV curve [7].

The dark IV curve of Figure 12 shows regular diode behavior and goes through the origin because there are no electron-hole pairs being generated. The illuminated light curve of Figure 12 shows a shift downwards which signals the generation of power. The mechanism behind these electron-hole pairs is explained earlier in this report's section.

To obtain the efficiency of the solar cell, the following equation must be used

$$\eta = \frac{V_{OC} I_{SC} FF}{P_{in}} \tag{4}$$

where V_{OC} is the max voltage at zero current, I_{SC} is the short circuit current, FF is the fill factor, and P_{in} is the incident power [7]. An example IV curve highlighting these components is shown in Figure 13.

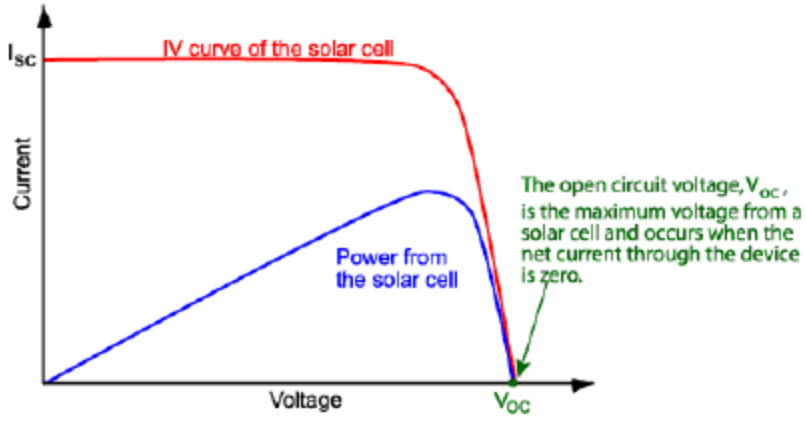


Figure 13. I_{SC} and V_{OC} shown on this plot [7].

From Figure 13, it can be seen that I_{SC} occurs when the voltage across the device is zero, or at the y-intercept. From Figure 13, it can be seen that V_{OC} occurs when the current through device is zero, or at the x-intercept. Fill factor can be calculated using the following equation

$$FF = \frac{I_{mp}V_{mp}}{I_{sc}V_{oc}} \tag{5}$$

where I_{mp} is the current at max power and V_{mp} is the voltage of max power. Fill factor can also be thought of as the area of the largest square under the curve [7]. Further testing using a four-point probe can be done to measure the resistivity of the top layer, shown in Figure 14.

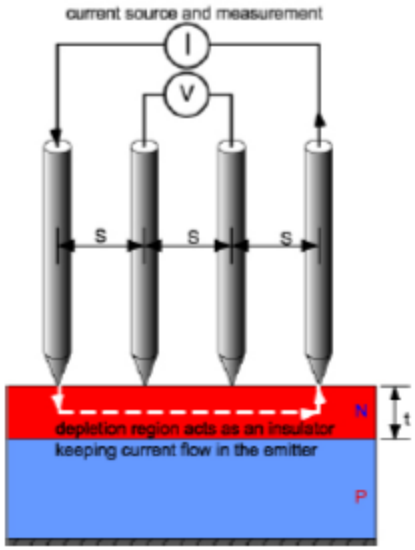


Figure 14. Diagram of four-point probe [7].

The four point probe calculates resistivity with the following equations

$$\rho = \frac{\pi V}{ln(2) I} \tag{6}$$

$$\rho = \frac{V}{I} = \frac{\pi t}{ln(\frac{sinh(t/s)}{sinh(t/2s)})} \tag{7}$$

where equation (7) is used for wafers that are thicker [7].

III. Experimental Procedure

The fabrication process of the solar cell began with the application of a spin-on dopant onto a quarter of a wafer that was p-type silicon (doped with boron), had a 2-inch diameter, and had a thickness of 100 nm. The spinner used was a Laurell Technologies Corp Model WS-406B-6NPP/LITE spinner, the spin-on dopant was P-SOD (P-509 Filmtronics Phosphorous), and the spin program was set to 3000 rpm for 30 seconds. The wafer was then baked at 250°C for 10 minutes in order to evaporate residual solvent. Next, dopant diffusion was initiated by annealing the wafer using a Lindberg Tube Furnace. The temperature was first ramped from

750°C to 1000°C, then held at 1000°C for 30 minutes, and lastly ramped back down to 750°C. Then, a HF etch was performed for 1 minute in order to remove residual spin-on dopant.

The phosphorus doping was followed by photolithographic patterning using a positive photoresist. The process began with spin coating on a Laurell Technologies Corp. Model WS-406B-6NPP/LITE spinner. A dropper was used to apply AZ 5214-EIR positive photoresist to the center of the wafer. The spin program consisted of 300 rpm for 10 seconds followed by 3000 rpm for 30 seconds to evenly spread the photoresist. The wafer was then soft-baked at 90°C for one minute to evaporate residual solvent. After the photolithographic patterning was complete, UV exposure was performed using a Myriad Semiconductor Aligner. The photomask shown Figure M1 was mounted onto the mask holder and tilt holder while the wafer was carefully placed on the sample stage and the vacuum chuck was turned on. The mask was then lowered slowly onto the sample and exposed with UV light for 16 seconds. Then, the wafer was developed in a dilute developer solution for approximately one minute, which exposed the desired pattern on the wafer. The developer solution used was AZ 400K, diluted 1:5 with deionized water. Next, the wafer was rinsed with deionized water and dried with nitrogen gas. Lastly, the wafer underwent a hard bake at 120°C for one minute to solidify and set the photoresist.

Figure 15. Photomask used for “control” solar cell IV measurements.

After development, aluminum was deposited on both sides of the wafer. First, a ~250 nm-thick aluminum layer was deposited on the front side using physical vapor deposition via evaporation with a Denton Vacuum DV-502A system. Metal lift-off was carried out by

immersing the wafer in acetone in an ultrasonic bath. A second ~250 nm aluminum layer was then deposited on the back side using the same equipment.

Cells were then isolated as needed via cleaving (wire saw cutting). The aluminum contacts were annealed through diffusion into the silicon using Rapid Thermal Annealing with a Modular Process Technology Corp. RTP 610 system at 450°C for 10 minutes with a ramp rate of 75°C/s. Finally, IV measurements were performed in both dark and illuminated conditions using a four-point probe. Figure 16 illustrates the entire procedure in a flow chart.

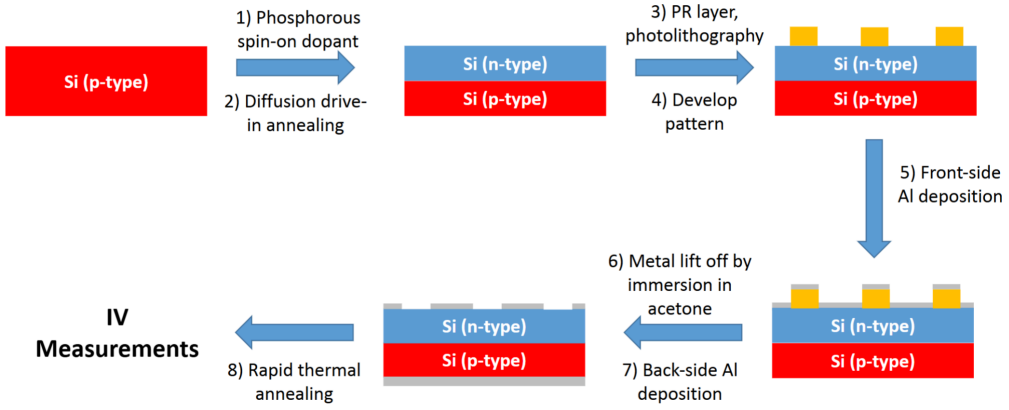


Figure 16. Lab procedure flow chart showing the solar cell fabrication process [4].

This process produced our "control" solar cell and accompanying IV measurements. The same procedure was then repeated, with the only change being the use of the photomask shown in Figure 17 instead of the one shown in Figure 15. The annealing time and temperature were kept constant to isolate the effects of the photomask design change. This resulted in our "experimental" solar cell and its corresponding IV measurements.

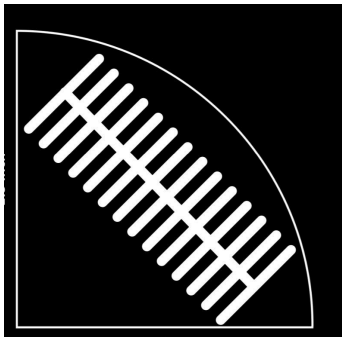


Figure 17. Photomask used for "experimental" solar cell IV measurements.

IV. Results and Discussion

The "control" solar cell created from the photomask shown in Figure 15 is shown in Figure 18. The IV measurements were used to create IV curves for our solar cells under both dark and illuminated conditions. Figure 19 shows the IV curves for the "control" solar cell under dark and illuminated conditions.

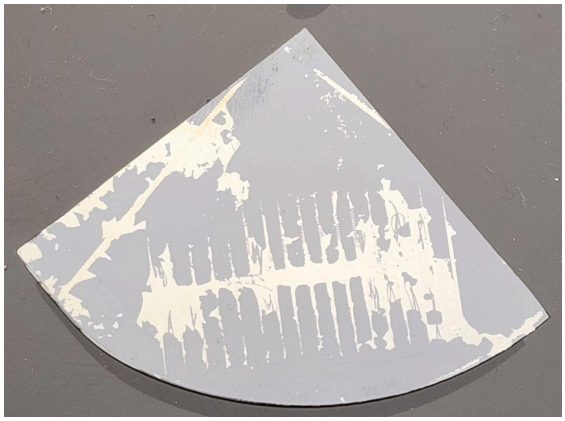
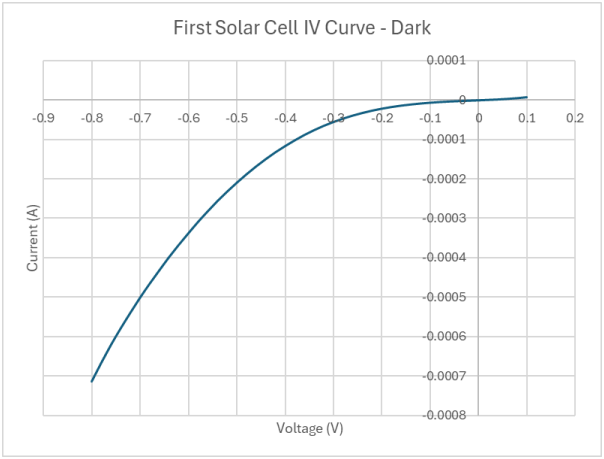
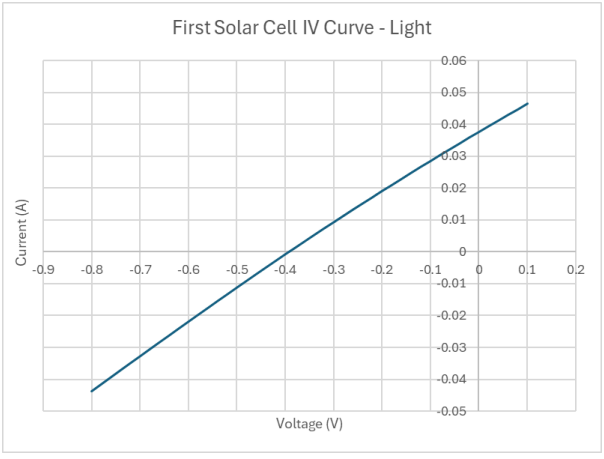


Figure 18. "Control" solar cell.



(a)



(b)

Figure 19. "Control" solar cell IV curves. **(a)** Under dark conditions. **(b)** Under illuminated conditions.

The "experimental" solar cell created from the photomask shown in Figure 17 is shown in Figure 20. Figure 21 shows the IV curves for the "experimental" solar cell under dark and illuminated conditions.

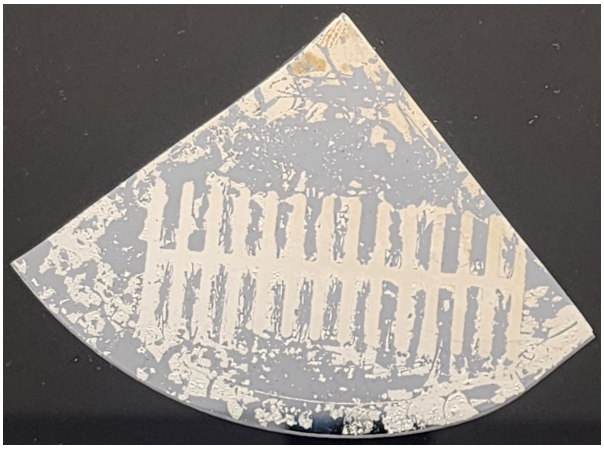
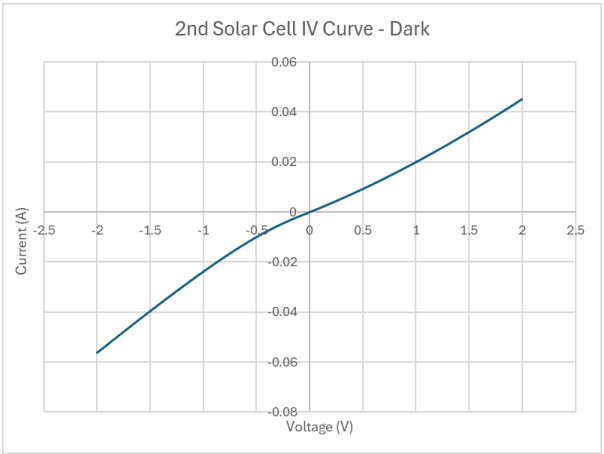
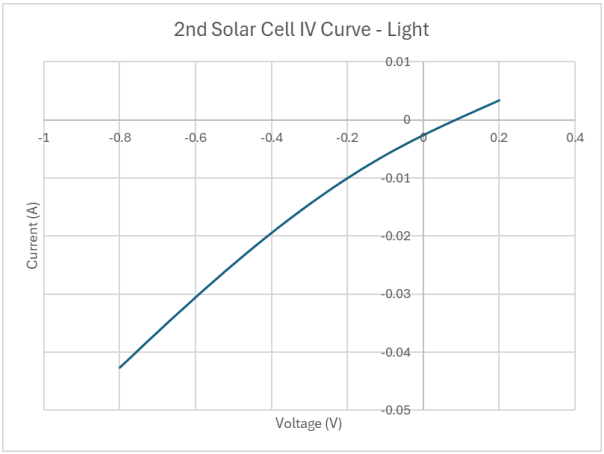


Figure 20. "Experimental" solar cell.

Figure 21. "Experimental" solar cell IV curves. **(a)** Under dark conditions. **(b)** Under illuminated conditions.



(a)



(b)

Once the IV curves were generated, Equation (5) was used to calculate the FF for each cell under illuminated conditions. The calculated FF values were then used in Equation (4) to determine the efficiency of both solar cells. Table 1 shows the short circuit current (I_{SC}), the open circuit voltage (V_{OC}), and the efficiency (η) values of both solar cells.

Table 1. Short circuit current (I_{SC}), open circuit voltage (V_{OC}), and efficiency (η) values of the "control" and "experimental" solar cells.

	"Control" Solar Cell	**"Experimental" Solar Cell**
I_{SC} **(A)**	0.037584	0.000262
V_{OC} **(V)**	0.392	0.090
η	3.07%	2.99%

Finally, we used Equation (1) to calculate the p-n junction depth, assuming that the B-doped Si wafer was doped with a concentration of $2 * 10^{15}\ cm^{-3}$ and a P surface concentration equal to the solid solubility of P in Si at 1000°C, $10^{21}\ cm^{-3}$. Here, N_s corresponds to the solid solubility of P in Si, and $N(x, t)$ corresponds to the background doping level because by definition, the junction depth is where the P donor concentration equals the B acceptor background. The diffusion coefficient D was extracted from Figure 6 as approximately $3 * 10^{-14}\ cm^2/s$, and the diffusion time *t* used for our solar cells was 30 minutes (1800 seconds). Substituting these values into Equation (3) and solving for *x* yielded a junction depth of 0.494 μm.

The IV curve in Figure 19a exhibited diode-like behavior, as expected. It also passed through the origin (0, 0), which is consistent with the absence of photocurrent under dark conditions. In contrast, the IV curve in Figure 19b had a positive short circuit current, which is

not conventional. A working solar cell should exhibit a negative short circuit current under standard IV plotting conventions, indicating current generation at zero applied voltage. The deviation suggests that our device was not delivering its maximum photocurrent, likely due to insufficient light-collecting area. Furthermore, the calculated efficiency of 3.07% supports this conclusion, as it is significantly lower than the reported efficiency of 25-25.6% for Si solar cells in the literature [8]. To address this, we modified the photomask design from Figure 15 by increasing the number and width of the fingers on the bus bar. We hypothesized that this change would improve efficiency by increasing light transmission to the active area of the cell, specifically the non-contact regions not obstructed by metal fingers. Additionally, inspection of the "control" solar cell in Figure 18 suggests an issue with underexposure during photolithography. This is indicated by excessive metal lift-off, which resulted in the bus bar and fingers appearing significantly narrower than intended based on the photomask design in Figure M1.

The IV curve in Figure 21 lacked the exponential rise characteristic of diode behavior. Instead, it appeared approximately linear, passing through the origin (0, 0) and spanning both negative and positive voltages and currents. This suggests the device was not functioning as a proper p–n junction diode. This interpretation is supported by Figure 20, which shows a failure in the metal lift-off process. There are large areas of unintended Al coverage around the bus bar and fingers, which are regions that should be completely contact-free according to the photomask design. In contrast, the IV curve in Figure 21b demonstrated a negative short circuit current, as expected for a functioning solar cell under illumination. Although the open circuit voltage was lower than that of commercial silicon cells, it still indicated some junction activity [9]. Overall, the "experimental" solar cell was functioning and exhibiting expected photovoltaic behavior, but its performance was suboptimal. The calculated efficiency was 2.99%, representing a 2.61% decrease from the "control" solar cell's efficiency of 3.07%.

Several factors could explain the improper metal lift-off and reduced performance. First, overexposure of the photomask may have caused UV light to leak into regions that should have remained unexposed. This would result in unintentional development of photoresist in non-contact areas, allowing metal to adhere directly to the wafer. Second, the use of only two stacked photomasks in this experiment, as opposed to three in the previous lab, may have allowed more UV light penetration, reducing masking effectiveness. Third, the photoresist layer

may have been too thin to support proper lift-off. A thinner resist increases the likelihood that metal remains adhered to unintended regions during deposition. Increasing the photoresist thickness could therefore be a potential improvement in future iterations to enhance device efficiency. Together, these factors underscore the critical role of photolithographic exposure control, mask integrity, and resist thickness in ensuring effective metal lift-off and achieving high-performance solar cell fabrication.

V. Conclusions

This laboratory experiment achieved the fabrication of a silicon-based solar cell. Various laboratory techniques, such as spin-on dopant diffusion, photolithography, contact deposition, and IV characterization, were applied throughout this experiment. Specifically, this lab resulted in the fabrication of a controlled design and a modified design solar cell. The controlled design for the solar cell can be seen in Figure _ and the design for the modified solar cell can be seen in Figure _. The IV curve of the “control” solar cell passed through the origin and displayed diode-like behavior in the dark, which was expected. Under illumination, the “control” solar cell had an efficiency of 3.07%. Although the efficiency of the “control” solar cell is not as high as a commercial one would be, we were still able to successfully create a functioning solar cell. After this, our “experimental” solar cell featured a modified mask print with wider and increased number of fingers. The IV curve of the “experiment” solar cell did not display diode-like behavior because the plot was linear. Under illumination, the “experimental” solar cell had an efficiency of 2.99%, which is a 0.08 difference compared to the “control”. Various factors, such as overexposure, inconsistent number of mask prints, thin photoresist layer, could have contributed to the decrease in solar cell efficiency. Although our second solar cell did not perform as well as the first, we were still able to make it functional. To improve our solar cell performance, we would have improved control of the photolithography conditions to ensure proper metal lift off. Overall, this lab was an invaluable experience because it provided us with the necessary tools to apply for industry positions within this industry.

VI. References

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