

# Fabrication of TEM Sample Holder

Christopher Santiago Garcia  
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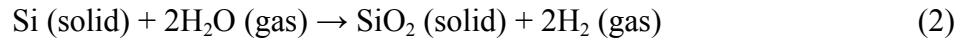
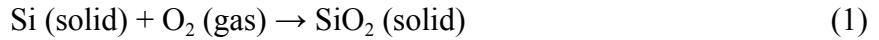
## I. Abstract

In this experiment, a transmission electron microscope (TEM) sample holder was fabricated using a 2 inch silicon wafer as the substrate. Sample holders are important because they provide a secure support for samples during electron beam interaction. The wafer underwent low pressure chemical vapor deposition (LPCVD), photoresist spin coating, UV exposure, dry etching, and wet etching. These procedures were done in the UCLA Engineering V Semiconductor Laboratory and the UCLA NanoLab. The yield % across the entire wafer ranges from 94% to 132%. The inconsistent % yield value resulted from improper cleaning procedures, inconsistent etching times, and poor mask print quality. An unexpected result from this experiment is the % yield. The wide range of % yield values puts into perspective how careful semiconductor companies must be when fabricating their products. Specifically, these companies have to ensure they have the best machinery and work environments.

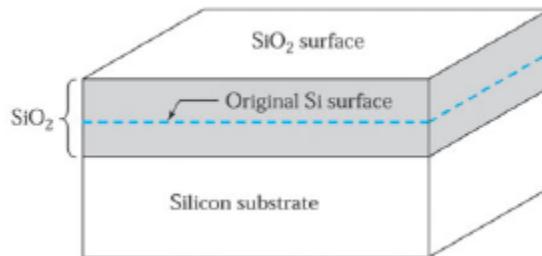
## II. Introduction

The purpose of this experiment was to fabricate a Transmission Electron Microscope (TEM) sample holder using various techniques such as film deposition, PR and lithography, dry etching, and wet etching. These techniques are crucial towards the production of Micro-Electro-Mechanical Systems (MEMS) devices. MEMS devices are miniaturized devices and structures whose elements have mechanical functionality [1]. The components of MEMS devices are miniaturized structures, sensors, actuators, and electronics. Of these components, the most important are the microsensors and microactuators because they convert energy from one form to another [1]. The performances of these devices can surpass that of the macroscale devices. TEM sample holders provide a secure support for the sample during electron beam interaction. The different holders allow the user to modify the number of grids, imaging temperature, tilt, and rotation of the grid [2].

The fabrication of TEM sample holders and MEMS devices relies on deposition. Thin films are deposited onto the wafer surface and are essential to creating layers needed to build these devices. These thin films can be classified into four groups: thermal oxides, dielectric layers, polycrystalline silicon, and metal films. For this report, the main deposition processes that will be discussed are thermal oxidation to form  $\text{SiO}_2$ , metallization, and chemical vapor deposition. Thermal oxidation uses silicon as the base material for devices because it is abundant and when it is exposed to room temperature conditions, a 20 $\text{\AA}$  native oxide layer forms on the surface [3]. The two kinds of oxidation methods are shown in the following equations:



Equation (1) depicts the dry oxidation of silicon which produces high quality  $\text{SiO}_2$  for gate oxides and equation (2) depicts the wet oxidation of silicon which has a faster growth rate and is often used for masks [3].

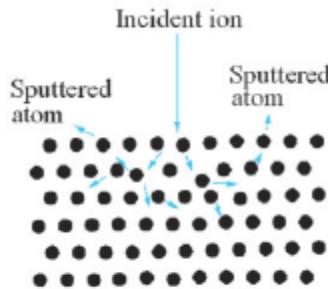


**Figure 1.** Thermal oxidation of  $\text{SiO}_2$  on Silicon [4].

The schematic diagram of Figure 1 showcases that growing an oxide with thickness  $x$  consumes 44% of the original silicon [4]. Thickness measurement can be calculated using the following equation

$$\Delta\Theta = \lambda/2d \quad (3)$$

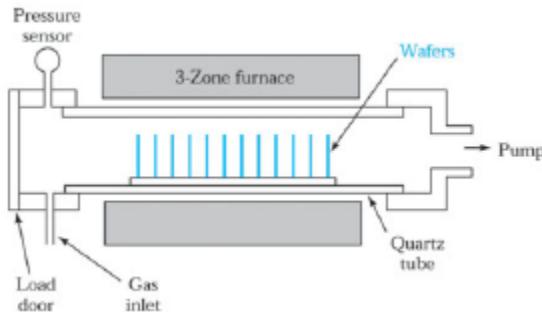
where  $\Delta\Theta$  is fringe spacing,  $\lambda$  is x-ray wavelength, and  $d$  is thickness [3]. The fringe spacing is the angular distance between two adjacent peaks in an XRR curve. This equation will be manipulated to isolate  $d$  to find the thickness of nitride in the Results section of this report. Physical vapor deposition (PVD), a method used for metallization, transfers metals or compounds onto Si wafer surfaces. The process of physical vapor deposition consists of evaporation, e-beam evaporation, plasma spray deposition, and sputtering. For the purpose of this report, only evaporation and sputtering will be considered. Evaporation, such as molecular beam epitaxy, occurs when the source material is heated above its melting point in a chamber [4]. To perform this process, a Denton vacuum can be used. In sputtering, the target surface is bombarded with Argon gas ions to transport the material from a target to a substrate [4].



**Figure 2.** Schematic representation of sputtering process [4].

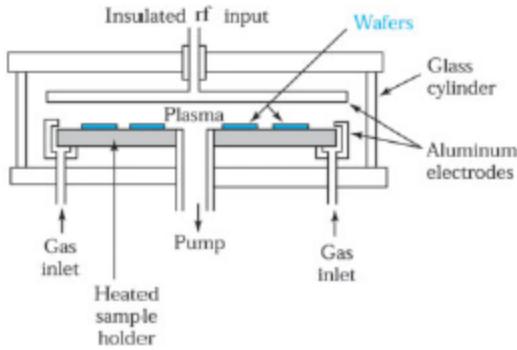
In Figure 2, the Argon ion is accelerated towards the target material and it will cause the particles to eject. When compared to evaporation, sputtering works with a wider range of materials, has better step coverage, and improved adhesion but it has a low target material utilization and non-uniform thickness [3].

The process of chemical vapor deposition (CVD) is used to deposit conformal thin films onto semiconductor devices. There are three types of chemical vapor deposition: atmospheric-pressure CVD, low-pressure CVD (LPCVD), and plasma-enhanced chemical vapor deposition (PECVD). For the purpose of this report, only LPCVD and PECVD will be discussed. LPCVD occurs at reduced atmospheric pressure and temperature range of 500-900°C to reduce gas-phase reactions and improve film uniformity [3, 4].



**Figure 3.** A schematic diagram of a LPCVD reactor [4].

In Figure 3, the reactor used for the LPCVD process is shown, which includes a pressure sensor, load dock, gas inlet, quartz tube, and a pump. In PECVD, plasma energy (typically 13.56MHz) is added to the CVD system [3].



**Figure 4.** A schematic diagram of a PECVD reactor [4].

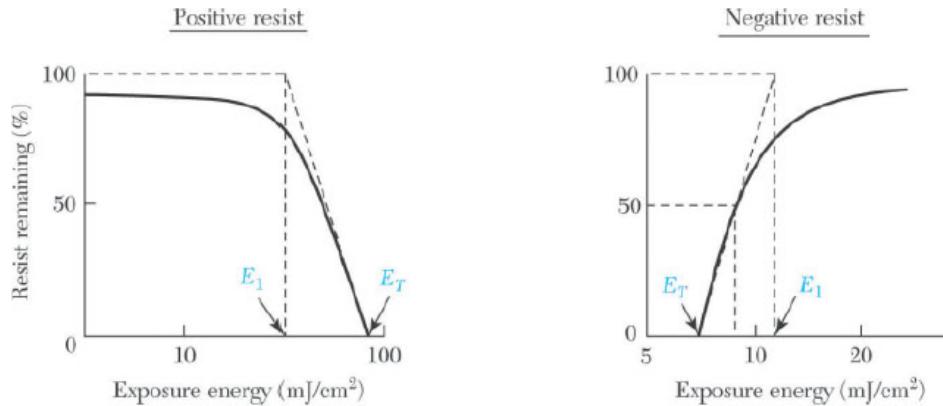
In Figure 4, the reactor used for the PECVD process is shown, which includes a glass cylinder, aluminum electrodes, gas inlets, plasma, sample holders, insulated rf inputs, and a pump. In this process, the wafers are heated to between 100°C and 400°C [3].

Following deposition processes, photolithography is used to transfer patterns of a mask to a thin layer of resist which covers a wafer.



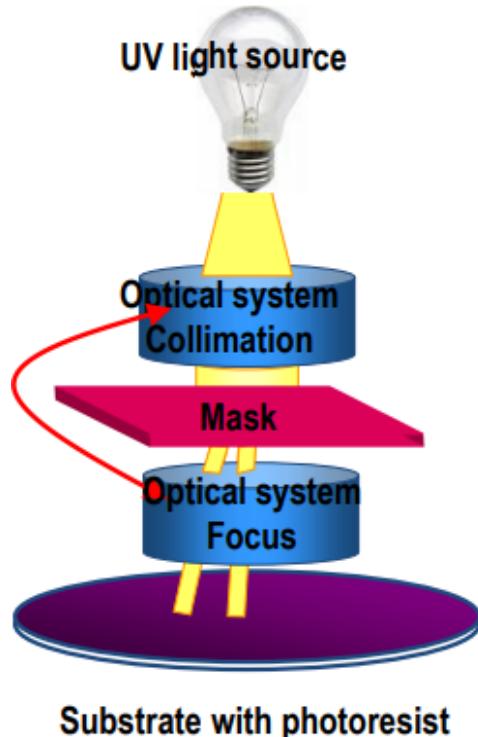
**Figure 5.** (a) Schematic diagram of a positive photoresist. (b) Schematic diagram of a negative photoresist [4].

Photoresists are radiation-sensitive compounds, and can be classified as either positive or negative. As seen in Figure 5(a), the exposed regions of a positive photoresist are removed. This occurs because the exposed regions become more soluble [4]. The opposite occurs in negative photoresists.



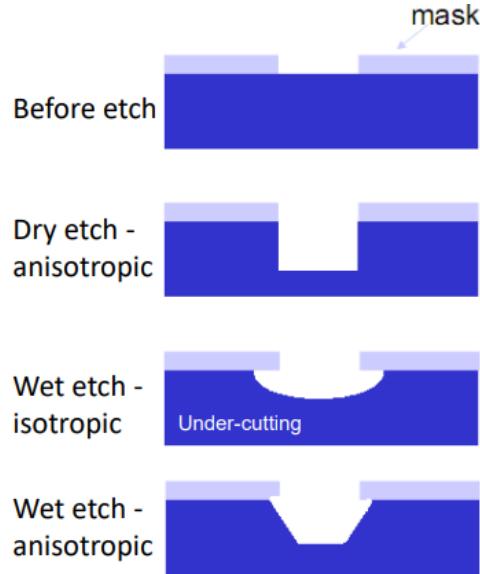
**Figure 6.** (left) Resist remaining (%) vs exposure energy ( $\text{mJ}/\text{cm}^2$ ) of positive photoresist. (right) Resist remaining (%) vs exposure energy ( $\text{mJ}/\text{cm}^2$ ) of negative photoresist [4].

In the left plot of Figure 6, as the resist remaining decreases the exposure energy decreases, signifying a positive photoresist. The opposite relationship can be seen in the right plot of Figure 6. In the processing of semiconductor devices, wet and dry etching are used to remove material from the wafer's surface.



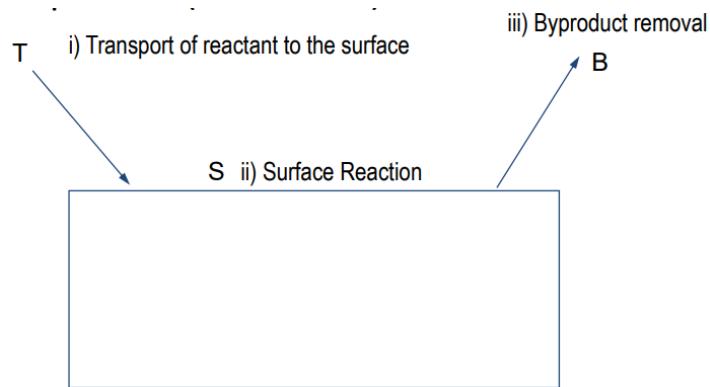
**Figure 7.** Schematic representation of lithographic process [3].

Lithography uses a UV light source to expose a pattern through a mask to print onto a photoresist. Figure 7 shows that the mask prevents the entire range of light from getting through and reaching the photoresist.



**Figure 8.** Diagram showing the mechanism behind each type of etching [5].

Anisotropic etching has varying etch rates for different crystal planes and the etch shape is dependent on the mask geometry and crystal orientation whereas isotropic etching has a constant etch rate regardless of direction or mask geometry [5]. In Figure 8, the anisotropic dry etch has vertical sidewalls, the isotropic wet etch has under-cutting leading to a curved floor, and the anisotropic wet etch has diagonal sidewalls.



**Figure 9.** Diagram showing the steps for wet etching [5].

The mechanism behind wet etching is (1) reactant transport to the surface, (2) surface reaction, and (3) byproduct removal, as shown in Figure 9. Unlike isotropic wet etching, anisotropic wet

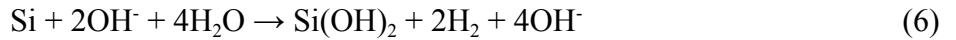
etching has etch rates of  $(100) > (110) > (111)$ , where (111) planes act as a stop plane [5]. The formula to calculate  $t_{\text{si}}$  is

$$t_{\text{si}} = ((W_{\text{mask}} - W_{\text{window}})/2) * \tan(\Theta) \quad (4)$$

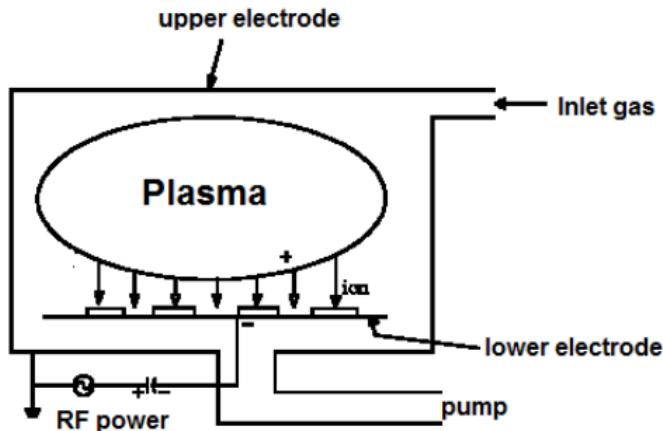
where  $W_{\text{mask}}$  is width of mask,  $W_{\text{window}}$  is width of window, and  $\Theta$  is  $54.74^\circ$  [6]. To wet etch silicon materials,  $\text{HNO}_3$  and HF are the most commonly used etchants and represented by the following chemical equation



Wet etching Si with KOH is also viable and can be represented with the following chemical equation



where the (111) plane acts as the stop plane. In dry etching, the mechanism is (1) generation of reactive species, (2) transport to wafer surface, (3) reaction, and (4) byproduct removal and falls under one of three types: physical, chemical, or Reactive Ion Etching (RIE) [5].

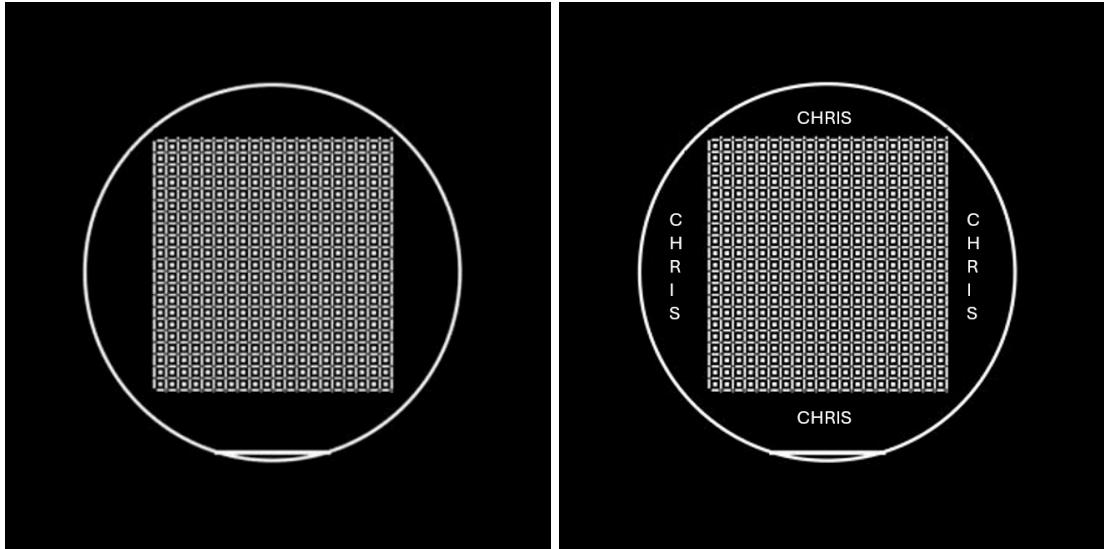


**Figure 10.** Schematic representation of RIE setup [5].

The RIE chamber setup is depicted in Figure 10, which includes an upper electrode, lower electrode, RF power, pump, and inlet gas. The mechanism behind RIE is that ions and neutral radicals are accumulated onto the material surface in an anisotropic manner [4]. Advantages of this method include improved safety, anisotropic process, and cleanliness although it has high equipment costs and toxic gas [5].

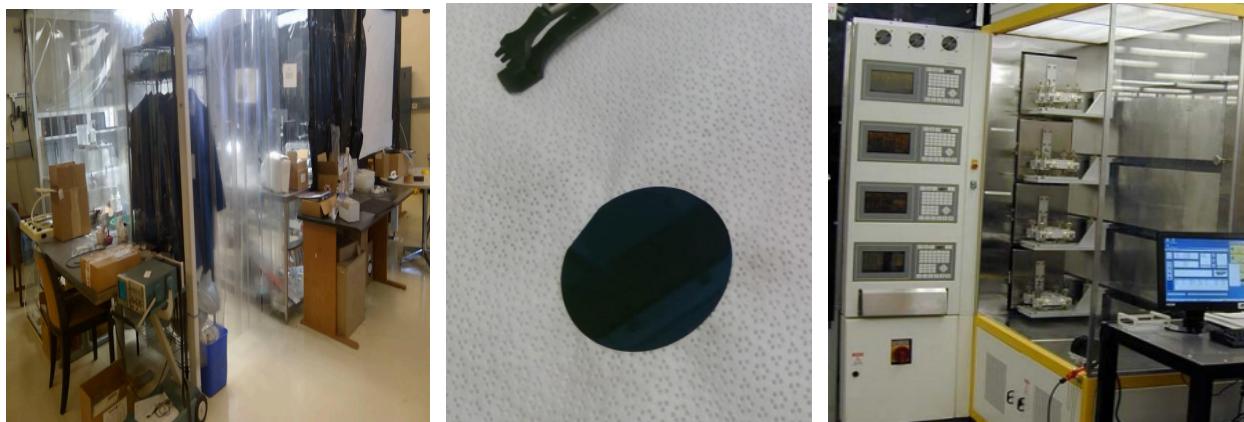
### III. Experimental Procedure

Week 1 of this experiment consisted of adding designs to the blank regions of the mask.



**Figure 11.** (left) Blank mask. (right) Student, Christopher Santiago Garcia's completed mask.

The design on each blank region was required to stay within the outline of the wafer but outside of the device area, as shown in Figure 11. Microsoft Powerpoint software was used to add text. Three copies of the mask were printed out, aligned, and attached to each other with tape to prepare for UV lithography.



**Figure 12.** (left) Cleanroom in the Engineering V building at UCLA. (middle) Picture of the wafer used in this experiment. (right) LPCVD machine found in NanoLab at UCLA [3].

Starting in Week 2, the remaining portions of the experiment were conducted in the cleanroom where proper PPE was used. Proper PPE included gloves, cleanroom boots, face mask, coverall, hood, and goggles. The 280-micron boron-doped silicon wafers with LPCVD-grown silicon nitride layers are shown in Figure 12. These 2 inch diameter wafers were required to be cleaned to prevent any contaminants from outside sources. The wafers were rinsed with acetone and DI

$\text{H}_2\text{O}$ , and then dried with  $\text{N}_2$  using the  $\text{N}_2$  gun. The drying mechanism involves slowly rotating in a circular direction starting at the center of the wafer. Then, the wafer underwent a dehydration bake at  $120^\circ\text{C}$  for 1-2 minutes. This was done to make sure there is no water left on the surface.

After the dehydration bake, the wafer was placed on the Laurell Technologies Corp Model WS-406B-6NPP/LITE branded spin-coater. The wafer was locked onto the stand, to make sure it did not fly off when the spin-coating took place. One dropper-full of AZ 5214-EIR positive photoresist was placed into the center of the wafer. It was ensured that the spin-coater machine was placed level on the table. Program A (300 rpm for 10s, 3000rpm for 30s) was selected and ran. This is done to uniformly spread the photoresist across the entire wafer's surface. Once the spin-coating was completed, the wafer was soft baked at  $90^\circ\text{C}$  for 1 minute to solidify the photoresist.



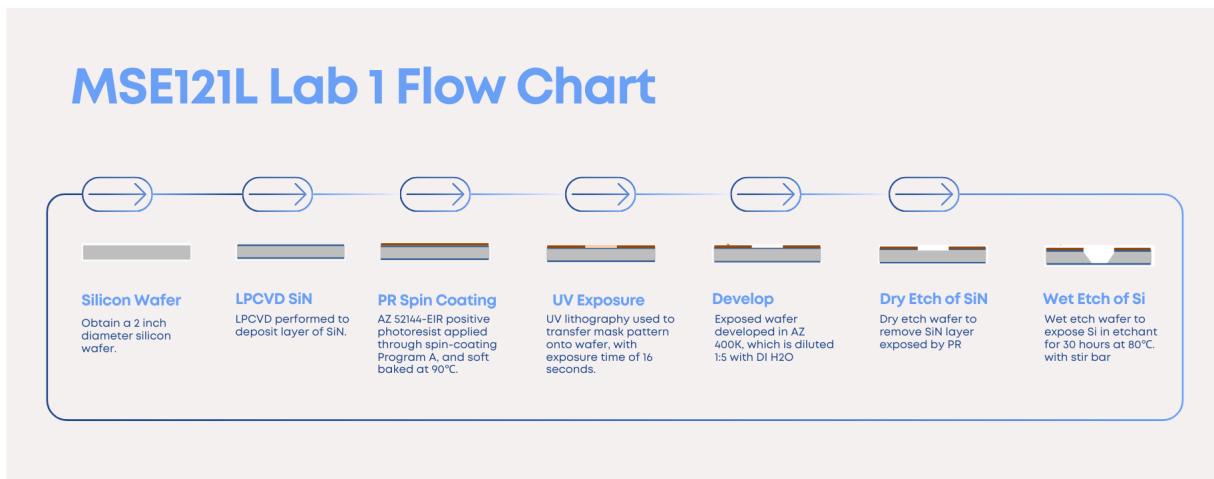
**Figure 13.** Image of the UV lithography machine found in the Engineering V building at UCLA [3].

Once the spin-coating process was completed, UV lithography was the next step. The Myriad Semiconductor Aligner machine is shown in Figure 13. The 3 masks that were taped together earlier in the experiment were placed into the mask holder. The wafer is then placed onto the sample stage and the vacuum is turned on. Lastly, lower the mask to the wafer and have a 16 second exposure time. Remove the wafer once it has been exposed to the UV for 16 seconds. It is important to not stare into the UV light because it can damage the user's eyes. The exposed wafer is then developed in AZ 400K, diluted 1:5 with DI  $\text{H}_2\text{O}$  for ~1 minute to reveal the nitride at the bottom. Next, rinse the wafer with DI water to stop the development process. Using the  $\text{N}_2$  gun, dry the wafer again with the same circular motion as before. To prepare the photoresist for etching procedures, the wafer must undergo another hardbake at  $120^\circ\text{C}$  for 1 minute.

Week 3 of this experiment was completed in the NanoLab located in Engineering IV. This week consisted of etching procedures, both dry and wet etching. Dry etching was done first using a Technics RIE 800 which is shown in Figure 14.



**Figure 14.** Image of the Technics RIE 800 machine found in the UCLA NanoLab [3]. The parameters for the dry etching was 200 watt power, 20 mTorr O<sub>2</sub>, 100 mTorr CF<sub>4</sub>, and an etch duration of 2 minutes. Once the dry etching was completed, the wet etching was performed to remove silicon. The etchant solution is 250g of NaOH, 200g of propanol, and 800g of H<sub>2</sub>O at 80°C with continuous agitation using a stir bar for 30 hours.

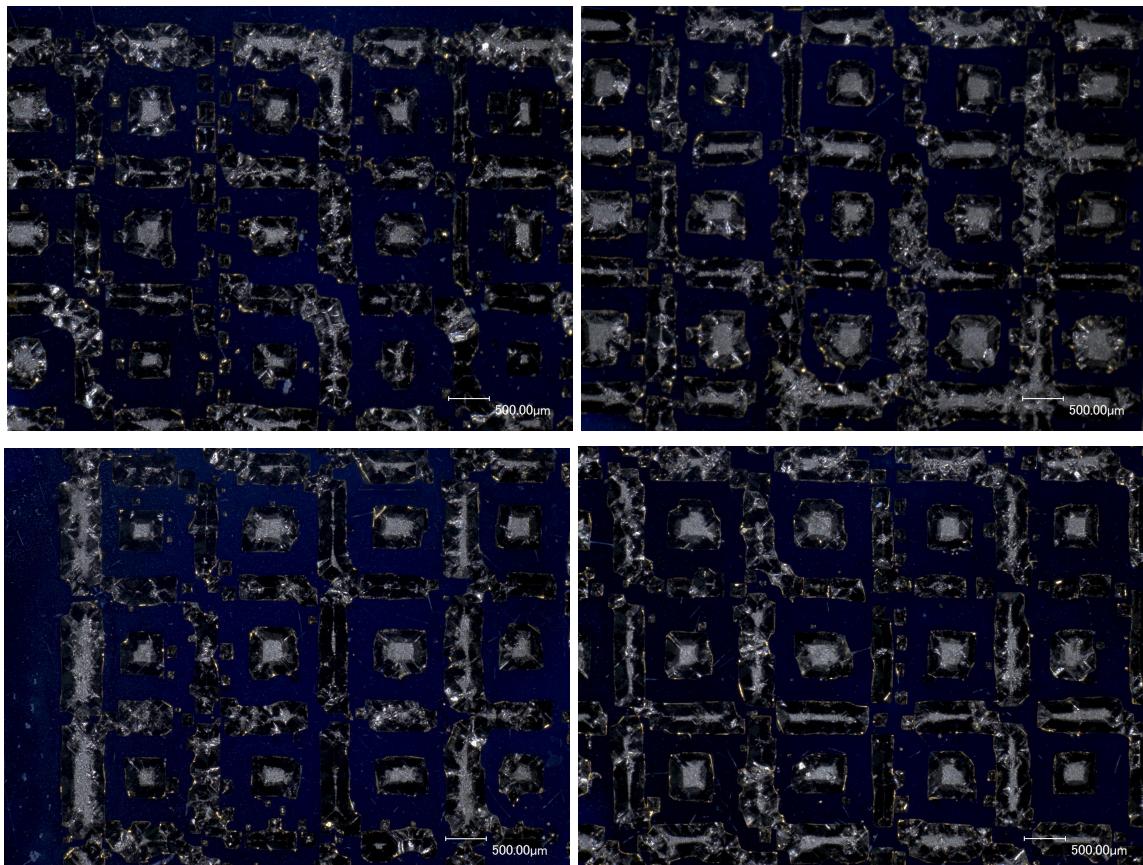


**Figure 15.** Process flow chart for development of TEM sample holder [3].

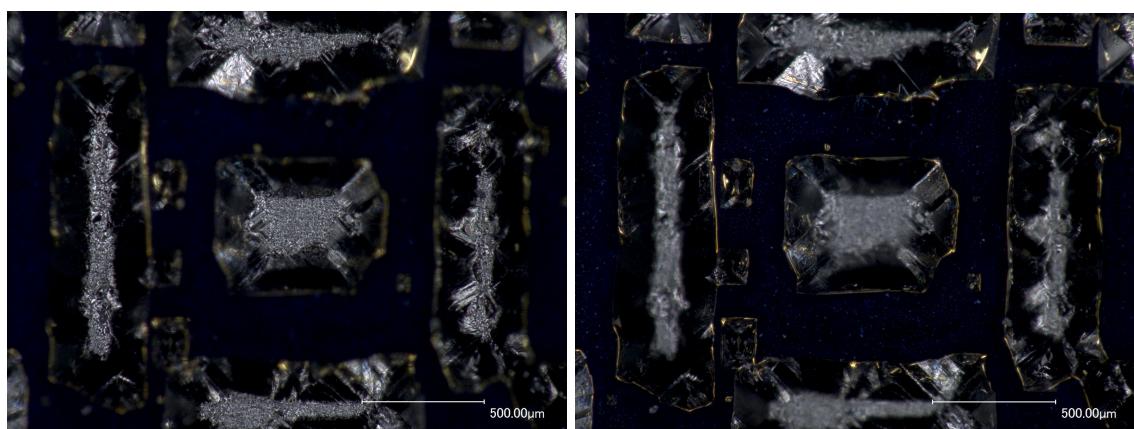
Figure 15 shows a general outline of the procedure to manufacture a TEM sample holder.

#### IV. Results and Discussion

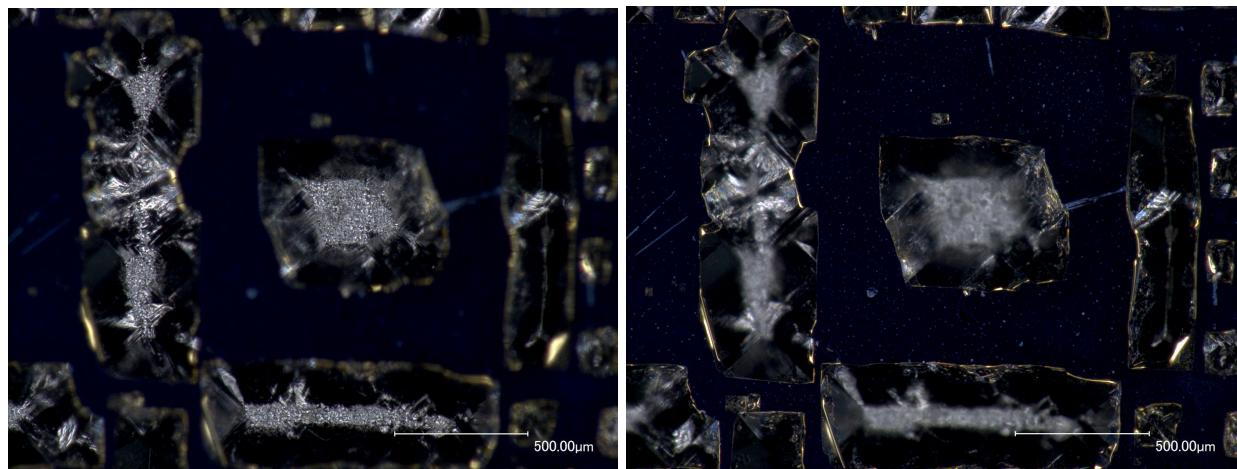
The silicon wafers were observed under an optical microscope after all the processing techniques were conducted. The following figures showcase these images.



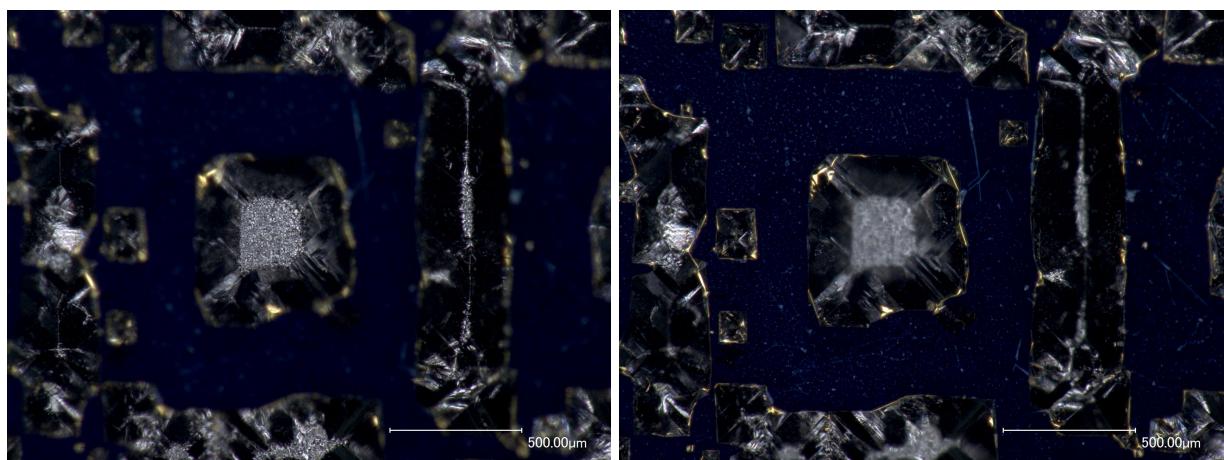
**Figure 16.** (top left) Top 50x. (top right) Right 50x. (bottom left) Left 50x. (bottom right) Bottom 50x.



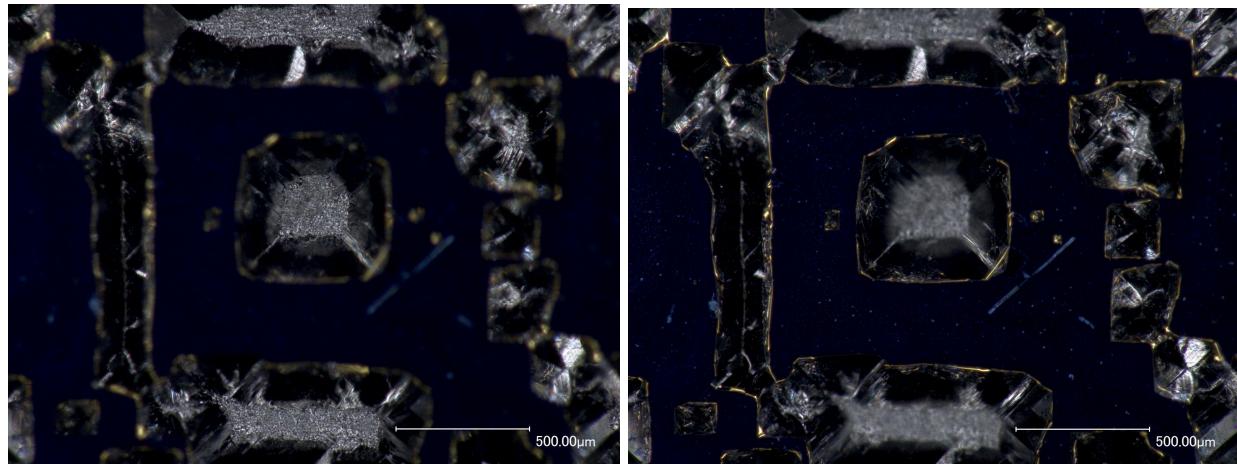
**Figure 17.** (left) 150x bottom window focus. (right) 150x bottom mask focus.



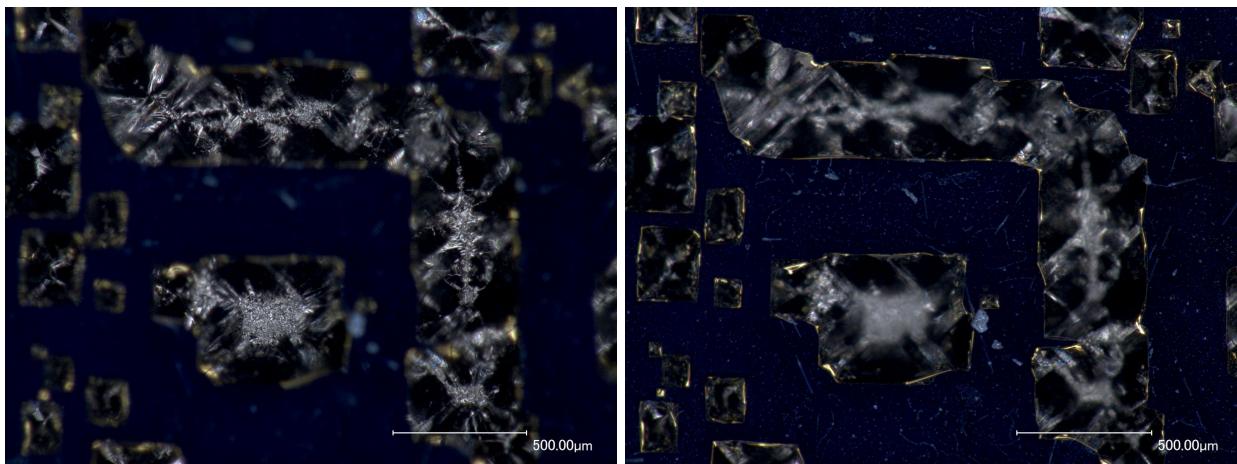
**Figure 18.** (left) 150x center window focus. (right) 150x center mask focus.



**Figure 19.** (left) 150x left window focus. (right) 150x right mask focus.

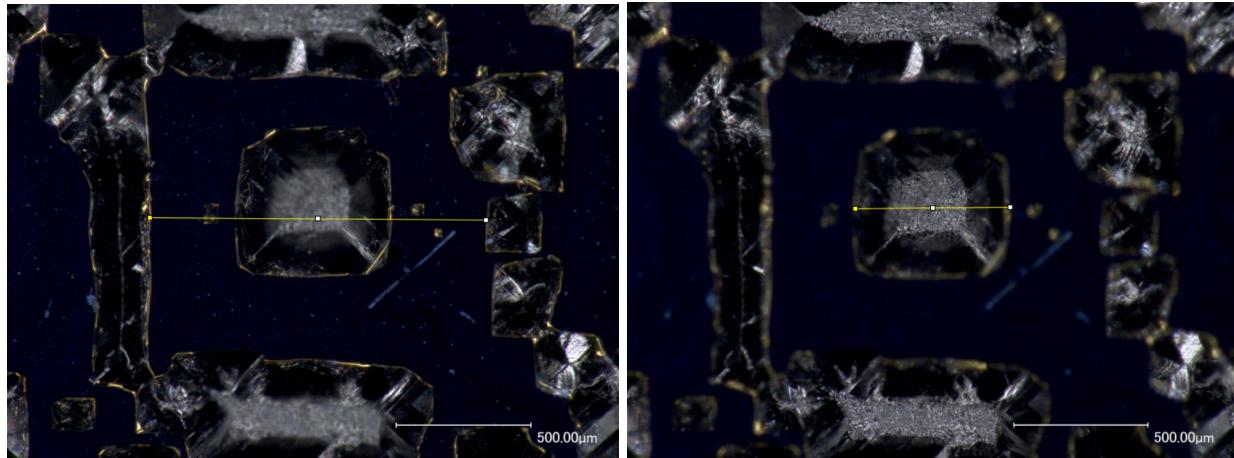


**Figure 20.** (left) 150x right window focus. (right) 150x right mask focus.



**Figure 21.** (left) 150x top window focus. (right) 150x top mask focus.

The images of the wafers under a phone camera lens are shown below. To measure the  $W_{\text{mask}}$  and  $W_{\text{window}}$ , ImageJ software was used.



**Figure 22.** (left) ImageJ 150x right mask focus measurement for  $W_{\text{mask}}$ . (right) ImageJ 150x right window focus measurement for  $W_{\text{window}}$ .

Figure 22 depicts how  $W_{\text{mask}}$  and  $W_{\text{window}}$  was measured on ImageJ for the 150x images. This procedure was used to collect 3 measurements of  $W_{\text{mask}}$  and  $W_{\text{window}}$  from each location on the wafer. Table 1 shows the  $W_{\text{mask}}$  and  $W_{\text{window}}$  measurements and  $t_{\text{si}}$  value which was calculated using the formula from equation (4).

**Table 1.** Measurement values for 150x top, bottom, left, and right images in ( $\mu\text{m}$ ). The silicon etch depth for the wafer is based on the fact that the etch stop plane is (111), and the wafer is (100) orientated.  $\Theta$  as  $54.74^\circ$  [7].

Region	Measurement #	$W_{\text{mask}} (\mu\text{m})$	$W_{\text{window}} (\mu\text{m})$	$W_{\text{mask}} - W_{\text{window}} (\mu\text{m})$	$t_{\text{Si}} (\mu\text{m})$
Top	1	1126.528	557.141	284.6935	402.6829
	2	1094.963	535.712	279.6255	395.5145
	3	1074.728	544.283	265.2225	375.1422
Bottom	1	1196.016	695.119	250.4485	354.2452
	2	1184.437	697.403	243.517	344.441
	3	1219.015	703.173	257.921	364.8147
Left	1	1217.302	567.789	324.7565	459.3497
	2	1211.437	582.589	314.424	444.735
	3	1222.855	541.787	340.534	481.6661
Right	1	1057.083	532.746	262.1685	370.8225
	2	1179.06	554.597	312.2315	441.6338
	3	1100.426	594.025	253.2005	358.1378

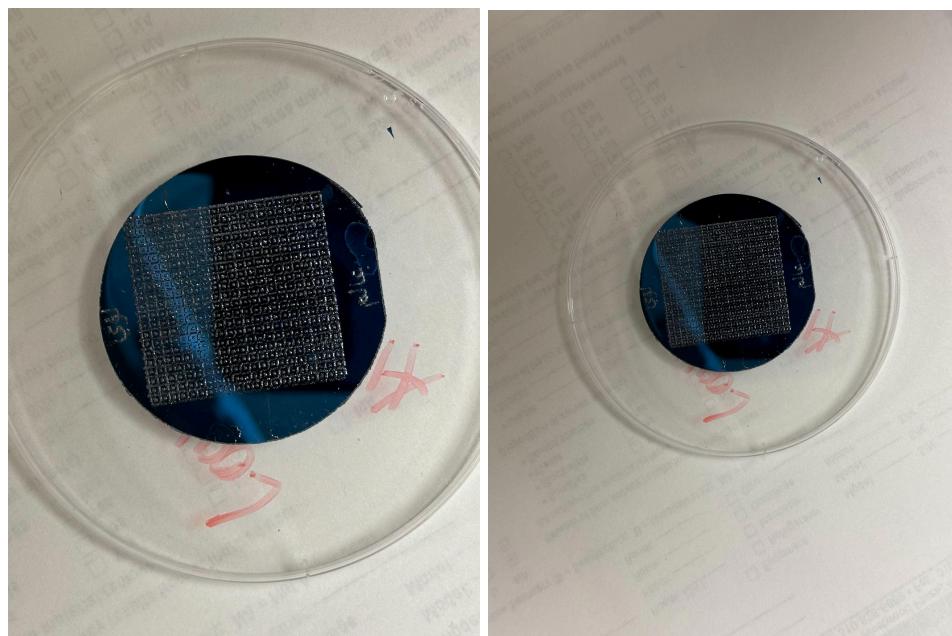
To determine the percent yield, the formula  $t_{\text{Si}}/280 * 100\%$  will be used.

**Table 2.** Percent Yield Calculations for  $t_{\text{Si}}$ .

Region	$t_{\text{Si}} (\mu\text{m})$	% yield (%)
Top	402.6829	110.6272
	395.5145	108.6578
	375.1422	103.0611
Bottom	354.2452	97.32012
	344.441	94.62665
	364.8147	100.2238

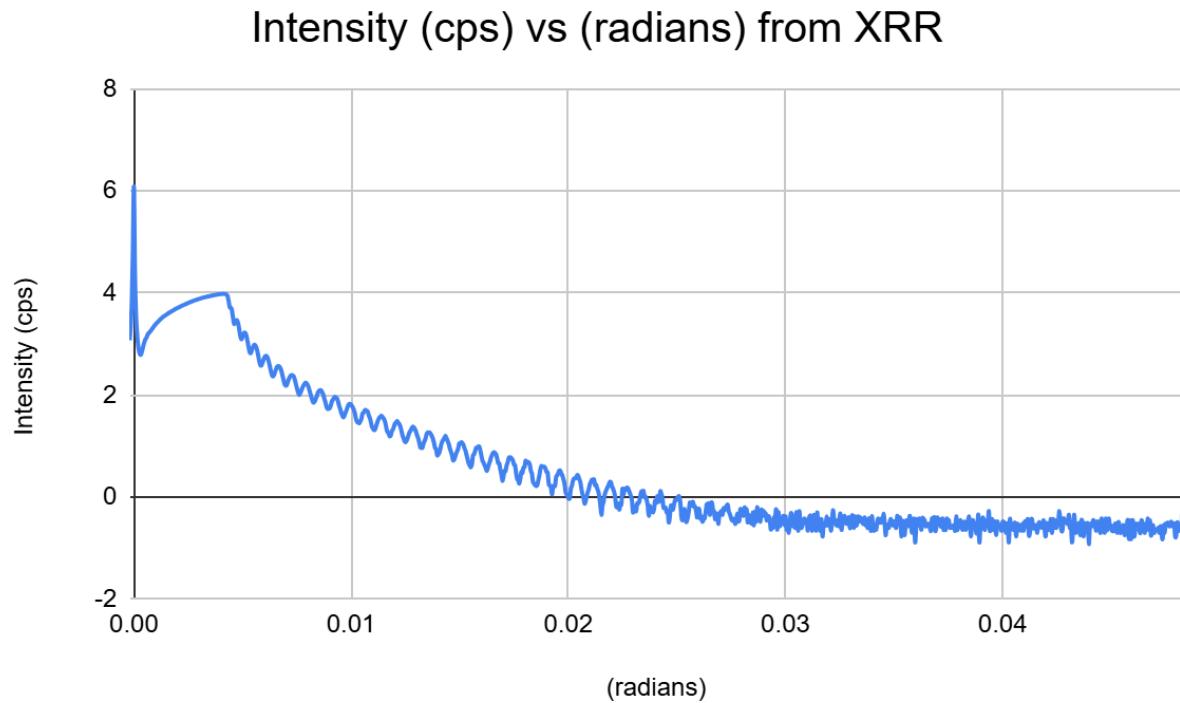
<b>Left</b>	459.3497	126.195
	444.735	122.1799
	481.6661	132.3258
<b>Right</b>	370.8225	101.8743
	441.6338	121.328
	358.1378	98.3895

From Table 2, the percent yield of most samples is over 100%, except 3. In Figure 23 below, without observing the pattern under an optical microscope, it looks good. Once observing under the optical microscope and calculating the % yield, it is clear that the number of successful etches was extremely low.



**Figure 23.** Silicon wafer images taken on an iPhone 14 Pro camera.

To calculate the thickness of the nitride layer, equation (3) from the Introduction section must be used.



**Figure 24.** XRR data plotted to confirm nitride thickness.

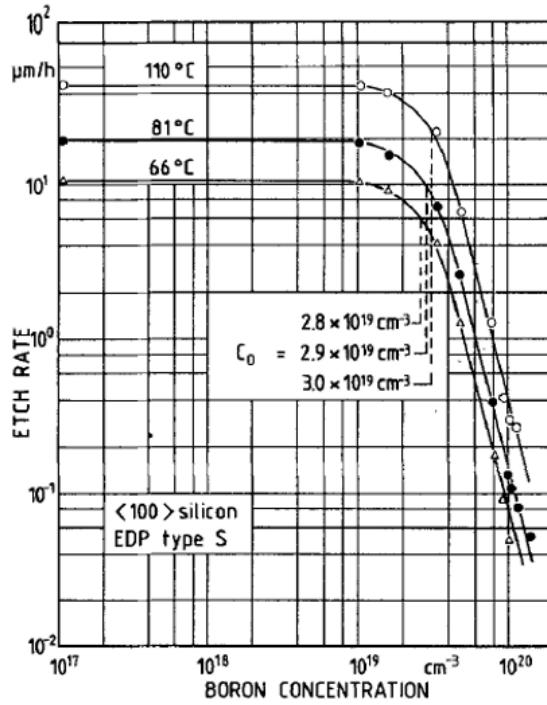
The XRR data was plotted in (radians) vs Intensity (cps) to obtain the fringe spacing ( $\Delta\Theta$ ). The peaks that were selected were found at  $\Theta_1 = 0.01284756255$  radians and  $\Theta_2 = 0.012112034203$ . Using the new formula that isolates  $d$ , thickness:

$$d = \lambda/\Delta\Theta \quad (4)$$

where  $\lambda$  is  $1.5406 \text{ \AA}$  due to Copper K-alpha1 radiation and  $\Delta\Theta$  is  $0.000735528347$  radians [4]. Plugging these values into equation (4), results in nitride thickness,  $d = 1047.27 \text{ \AA}$  or  $d = 104.727 \text{ nm}$ .

Overall, the results in this experiment were fairly poor. In Figures 16 to 22, it is clear that the windows are extremely uneven. Moreover, there appears to be dust particles littered throughout the wafer. These dust particles are white. The % yield for all but 3 etch profiles were over 100%. This means that the samples were over-etched, and more material was removed than planned. The inconsistency in the % yield and  $t_{Si}$  signifies that the etching was inconsistent. The samples may have been overetched because the etching time was 30 hours. The original etching time was 5 hours, but when silicon is p-doped with levels greater than  $1 \times 10^{19} \text{ cm}^{-3}$ , there is a narrow-space charge region which causes recombination and a passive layer spontaneously forms [8]. This

results in the etch rate to decrease, meaning it would take longer to etch a sample. The irregular jump from 5 to 30 hours likely caused over-etching.



**Figure 25.** Plot of etch rate versus boron concentration [9].

Figure 25 shows that the etch rate decreases significantly once the boron concentration surpasses  $1 \times 10^{19} \text{ cm}^{-3}$  regardless of the temperature. The printer used to produce the mask designs may lack the necessary precision to ensure dimensional accuracy. Additionally, the wafers should be properly cleaned and handled to ensure there are no particles leftover. The etching time should be fixed to ensure that the sample is not under or over etched. The printer quality should be improved to ensure that the masks prints are precise.

## V. Conclusions

This lab achieved the fabrication of a TEM sample holder. Various laboratory techniques, such as film deposition, lithography, dry etching, and wet etching, were applied throughout the experiment. Analytical techniques were applied as well. Specifically, in the calculation of silicon etch depth and the % yield. The % yield achieved in this experiment ranged from 94%-132%, which signifies the etching profile was inconsistent. Wafer contamination, inconsistencies in the wet etching process, and inaccurate mask prints contributed to the large range of % yield. Moving forward, these issues must be addressed to obtain a more consistent % yield. To achieve a consistent % yield, the samples must be properly cleaned with the N<sub>2</sub> gun, etched with consistent times, and obtain high quality prints for the mask. Although a high quality structure was not obtained, the experimental skills obtained through this lab were invaluable. As an

undergraduate student, the exposure to semiconductor practices is extremely beneficial. These skills are a topic of conversation for industry positions in the field.

## VI. Citations

- [1] "What is MEMS Technology?," Mems-exchange.org, 2019.  
<https://www.mems-exchange.org/MEMS/what-is.html>
- [2] "TEM Holders," Electron Microscopy Center.  
<https://iubemcenter.indiana.edu/equipment/tem-holders/index.html>
- [3] M. Goorsky (2025). Lab 1 TEM Sample Holder [PowerPoint Slides]. Available:  
<https://bruinlearn.ucla.edu/>
- [4] S. M. Sze and M. K. Lee, Semiconductor Devices: Physics and Technology, 3rd ed. Hoboken, NJ: Wiley, 2012.
- [5] M. Goorsky (2025). TEM Sample Holder Lab Etching Week 3 [PowerPoint Slides]. Available: <https://bruinlearn.ucla.edu/>
- [6] M. Goorsky (2025). Lab 1 Membrane Inspection Week 4 [PowerPoint Slides]. Available: <https://bruinlearn.ucla.edu/>
- [7] "Crystal Planes in Silicon/Miller Index/Angle between Planes/Wafer Flat/Crystallography," cleanroom.groups.et.byu.net. [https://cleanroom.groups.et.byu.net/EW\\_orientation.phtml](https://cleanroom.groups.et.byu.net/EW_orientation.phtml)
- [8] The Effects of Process-Induced Defects on the Chemical Selectivity of Highly Doped Boron Etch Stops in Silicon, <https://iopscience.iop.org/article/10.1149/1.2054680>.
- [9] Seidel, Helmut & Csepregi, L. & Heuberger, A. & Baumgaertel, H.. (1990). Anisotropic etching of crystalline silicon in alkaline solutions. II. Influence of dopants. Journal of the Electrochemical Society. 137. 3626-3632.