AN0002: Hardware Design Considerations

This application note details hardware design considerations for EFM32 Series 1 and 2 Gecko, EZR32, and EFR32 Wireless Gecko devices.

Topics specifically covered are supported power supply configurations, supply filtering considerations, debug interface connections, and external clock sources. In addition, reference designs for the EFM32 Series 1 Gecko microcontrollers are included.

For simplicity, EFM32 Series 1 Gecko is used throughout this document to represent the EFM32 Wonder Gecko, Gecko, Giant Gecko, Leopard Gecko, Tiny Gecko, Zero Gecko, or Happy Gecko MCU series, EZR32 is used to represent the EZR32 Wireless MCUs, EFR32 Wireless Gecko is used to represent the EFR32 Wireless Gecko portfolio devices, and EFM32 Series 2 Gecko is used to represent the EFM32 Pearl Gecko and Jade Gecko (and future devices).

For more information on hardware design and layout considerations for the DC-DC converter on EFM32 Series 2 and EFR32 Wireless Gecko devices, see *AN0948: Power Configurations and DC-DC*.

For more information on hardware layout considerations for the radio portion of EFR32 Wireless Gecko devices, see *AN930: EFR32 2.4 GHz Matching Guide*, *AN933: EFR32 2.4 GHz Minimal BOM*, and *AN928: EFR32 Layout Design Guide*.

For more information on hardware layout considerations for the radio portion of EZR32 devices, see *AN629: Si4460/61/63/64/67/68 RF ICs Layout Design Guide*.

KEY POINTS

- Decoupling capacitors are crucial to ensuring the integrity of the device's power supplies.
- The debug interface consists of two communication pins (SWCLK and SWDIO).
- External clock sources must be connected to the device correctly for proper operation.
- This application note includes:
  - This PDF document
  - Reference Design (zip)
    - OrCAD schematic design files
    - PDF Schematics
    - Symbol libraries (OrCAD, CSV, and Edif formats)

1. Power Supply Overview

1.1 Introduction

Although the EFM32 Series 1 and 2 Gecko, EZR32, and EFR32 Wireless Gecko devices have an exceptionally small average current consumption, proper decoupling is crucial. As for all digital circuits, current is drawn in short pulses corresponding to the clock edges. Particularly when several I/O lines are switching simultaneously, transient current pulses on the power supply can be in the order of several hundred mA for a few nanoseconds, even though the average current consumption is quite small.

These kinds of transient currents cannot be properly delivered over high impedance power supply lines without introducing considerable noise in the supply voltage. To reduce this noise, decoupling capacitors are employed to supplement the current during these short transients.

1.2 Decoupling Capacitors

Decoupling capacitors make the current loop between supply, MCU, and ground as short as possible for high frequency transients. Therefore, all decoupling capacitors should be placed as close as possible to each of their respective power supply pin, ground pin, and PCB (Printed Circuit Board) ground plane.

All external decoupling capacitors should have a temperature range reflecting the environment in which the application will be used. For example, a suitable choice might be X5R ceramic capacitors with a change in capacitance of ±15% over the temperature range -55 °C – +85°C (standard temperature range devices) or -55 °C – +125°C (extended temperature range devices).

1.3 Power Supply Pin Overview

Note that not all supply pins exist on all devices. The table below describes the supply pins and where it appears.

Table 1.1. Power Supply Pin Overview

Pin Name	Product Family	Description
VDD_VREG	EFM32 Series 1 Gecko and EZR32 only	Input to the internal Digital LDO
AVDD	All devices	Supply to analog peripherals
DECOUPLE	All devices	Output of the internal Digital LDO & Digital logic power supply
IOVDD	All devices	GPIO supply voltage
USB_VREGI	All USB-enabled devices	Input to the internal 3.3 V LDO. Typically connected to the USB 5V supply.
USB_VREGO	All USB-enabled devices	Output of the internal 3.3 V LDO.
VREGVDD	EFM32 Series 2 and EFR32 Wireless Gecko only	Input to the DC-DC converter
VREGSW	EFM32 Series 2 and EFR32 Wireless Gecko only	DC-DC powertrain switching node
VREGVSS	EFM32 Series 2 and EFR32 Wireless Gecko only	DC-DC ground
DVDD	EFM32 Series 2 and EFR32 Wireless Gecko only	DC-DC feedback node and input to the internal Digital LDO
RFVDD	EZR32 and EFR32 Wireless Gecko only	Supply to radio analog. Note, on EZR32, RFVDD also supplies the radio power amplifier.
PAVDD	EFR32 Wireless Gecko only	Supply to radio power amplifier

1.4 Power Supply Requirements

An important consideration for all devices is the voltage requirements and dependencies between the power supply pins. The system designer needs to ensure that these power supply requirements are met, regardless of power configuration or topology. Please see the device data sheet for absolute maximum rating and additional details regarding relative system voltage constraints.

EFM32 Series 1 Gecko Power Supply Requirements

- VDD_DREG = AVDD = IOVDD

EFM32 Series 2 Gecko Power Supply Requirements

- VREGVDD = AVDD (Must be the highest voltage in the system)
- VREGVDD >= DVDD
- VREGVDD >= IOVDD
- DVDD >= DECOUPLE

EZR32 Power Supply Requirements

- VDD_DREG = AVDD = IOVDD = RFVDD

EFR32 Wireless Gecko Power Supply Requirements

- VREGVDD = AVDD (Must be the highest voltage in the system)
- VREGVDD >= DVDD
- VREGVDD >= PAVDD
- VREGVDD >= RFVDD
- VREGVDD >= IOVDD
- DVDD >= DECOUPLE

1.5 DECOUPLE

All EFM32 Series 1 and 2 Gecko, EZR32, and EFR32 Wireless Geckodevices include an internal linear regulator that powers the core and digital logic. The DECOUPLE pin is the the output of the Digital LDO, and requires a 1 uF capacitor. The input to the Digital LDO depends on the device family, as shown below.

1.5.1 DECOUPLE Pin — EFM32 Series 1 Gecko and EZR32

On EFM32 Series 1 Gecko and EZR32 devices, the Digital LDO is sourced by the VDD_DREG pin. DECOUPLE is the output of the LDO.

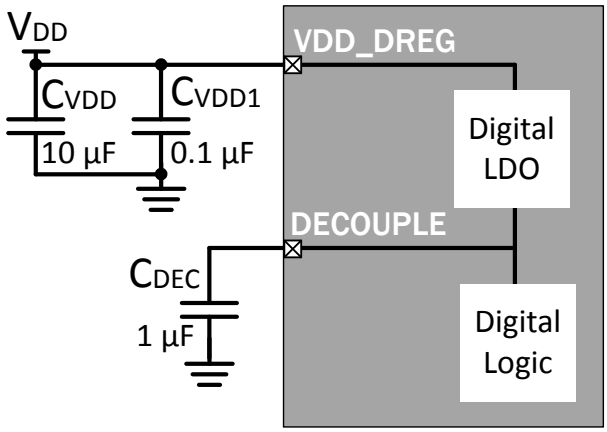


Figure 1.1. VDD_DREG and DECOUPLE on EFM32 Series 1 Gecko and EZR32 devices

1.5.2 DECOUPLE Pin — EFM32 Series 2 and EFR32 Wireless Gecko

On EFM32 Series 2 and EFR32 Wireless Gecko devices, the DVDD pin is the input supply to the Digital LDO, with the DECOUPLE pin the output of the LDO.

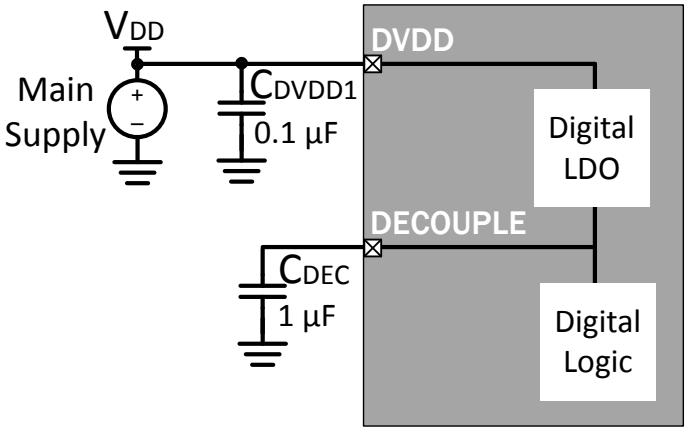


Figure 1.2. DVDD and DECOUPLE on EFM32 Series 2 and EFR32 Wireless Gecko devices

1.6 IOVDD

The IOVDD pin(s) provide decoupling for all of the GPIO pins on the device. A 0.1 uF capacitor per IOVDD pin is recommend, along with a 10 uF bulk capacitor. The bulk capacitor value may safely be reduced if there are other large bulk capacitors on the same supply (e.g., if IOVDD=AVDD=VDD_VREG, and both VDD_VREG and AVDD both have a 10uF capacitor already).

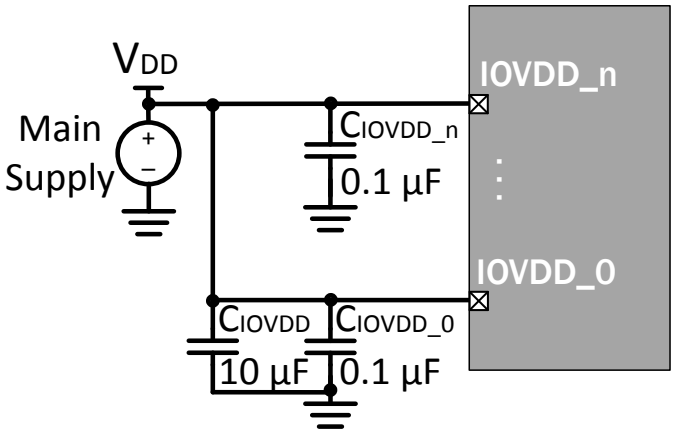


Figure 1.3. IOVDD Decoupling

1.7 AVDD

The analog peripheral performance of the device is impacted by the quality of the AVDD power supply. For applications with less demanding analog performance, a simpler decoupling scheme for AVDD may be acceptable. For applications requiring the highest quality analog performance, more robust decoupling and filtering is required.

Note that the number of AVDD analog power pins may vary by device and package.

1.7.1 AVDD Standard Decoupling

The figure below illustrates a standard approach for decoupling the AVDD pin(s). In general, the application should include one bulk capacitor (C_{AVDD}) of 10 µF, as well as one 10 nF capacitor per each AVDD pin (C_{AVDD_0} through C_{AVDD_n}).

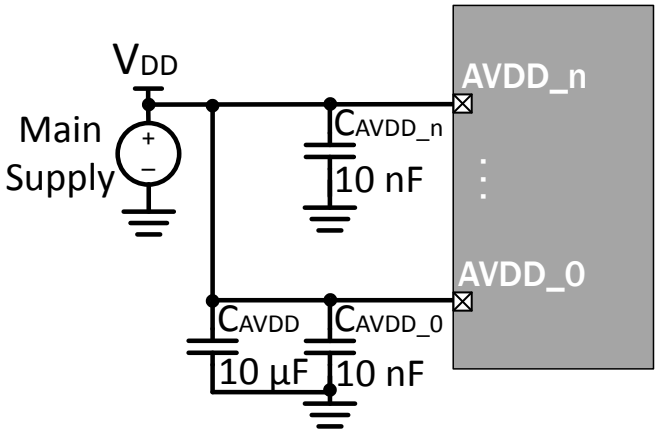


Figure 1.4. AVDD Standard Decoupling

1.7.2 AVDD Improved Decoupling

The figure below illustrates an improved approach for decoupling and filtering the AVDD pin(s). In general, the application should include one bulk capacitor (C_{AVDD}) of 10 µF, as well as one 10 nF capacitor per each AVDD pin (C_{AVDD_0} through C_{AVDD_n}). In addition, a ferrite bead and series 1 Ω resistor provide additional power supply filtering and isolation.

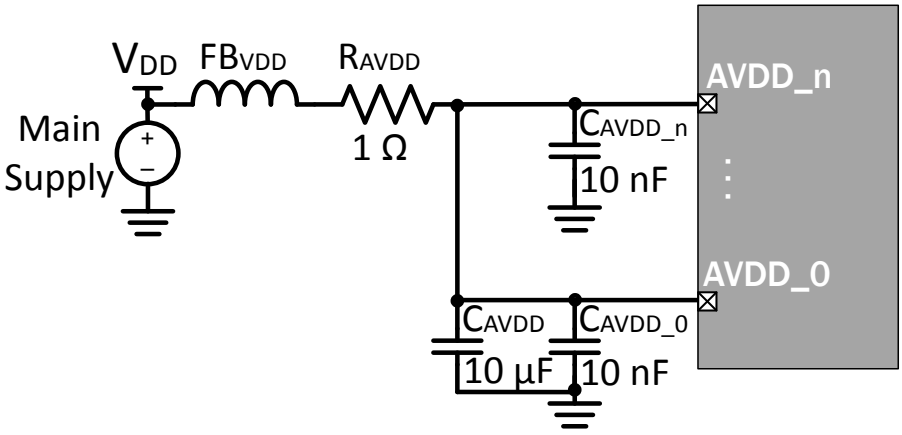


Figure 1.5. AVDD Improved Decoupling

The table below lists some recommended ferrite bead part numbers suitable for AVDD filtering.

Table 1.2. Recommended Ferrite Beads

Manufacturer	Part Number	Impedance	I_{MAX} (mA)	DCR (Ω)	Operating Temperature (°C)	Package
Würth Electronics	74279266	1 kΩ @ 100 MHz	200	0.600	-55 to +125	0603/1608
Murata	BLM21BD102SN1D	1 kΩ @ 100 MHz	200	0.400	-55 to +125	0805/2012

1.8 USB (USB_VREGI & USB_VREGO)

Some Gecko devices integrate a USB controller and a 3.3V LDO. The figure below illustrates a standard approach for connecting and decoupling the USB_VREGI, and USB_VREGO pins. In addition, the USB5V sense line (USB_VBUS) is shown connected directly to V_{USB}.

To avoid violating the USB specification, the total capacitance on V_{USB} should not exceed 10 µF. Consult *AN0046: USB Hardware Design Guide* for detailed hardware guidance for USB applications.

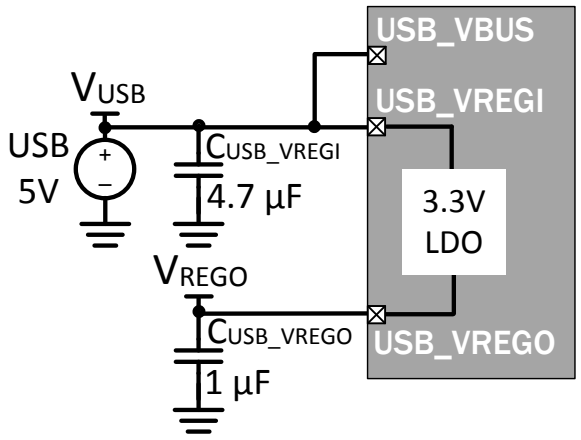


Figure 1.6. USB_VREGI and USB_VREGO Decoupling

1.9 DC-DC— EFM32 Series 2 and EFR32 Wireless Gecko

EFM32 Series 2 and EFR32 Wireless Gecko devices may take advantage of an onboard DC-DC converter for improved power efficiency. However, due to additional switching noise present on the DC-DC converter output (V_{DCDC}), some additional filtering components may be required.

1.9.1 DC-DC — Unused

When the DC-DC converter isn't used, the DVDD pin should be shorted to the VREGVDD pin. VREGSW must be left floating, and VREGVSS should be grounded.

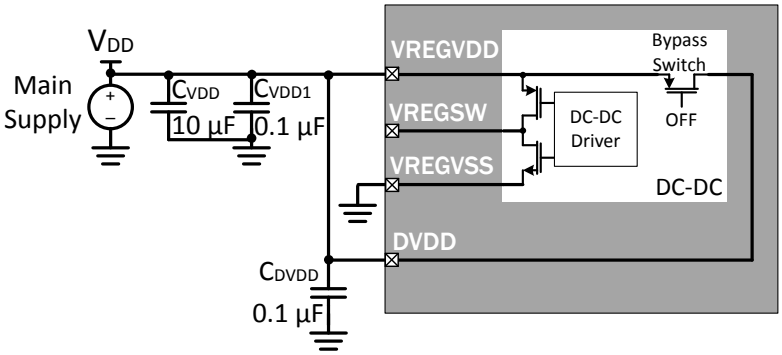


Figure 1.7. Configuration when the DC-DC converter is unused

1.9.2 DC-DC — Powering DVDD

For the lowest power applications, the DC-DC converter can be used to power the DVDD supply (as well as RFVDD and PAVDD on EFR32 Wireless Gecko) as shown in the figure below. In this configuration, the DC-DC Output (V_{DCDC}) is connected to DVDD. In addition to being the DC-DC converter feedback path, the DVDD pin powers the internal Digital LDO which in turn powers the digital circuits.

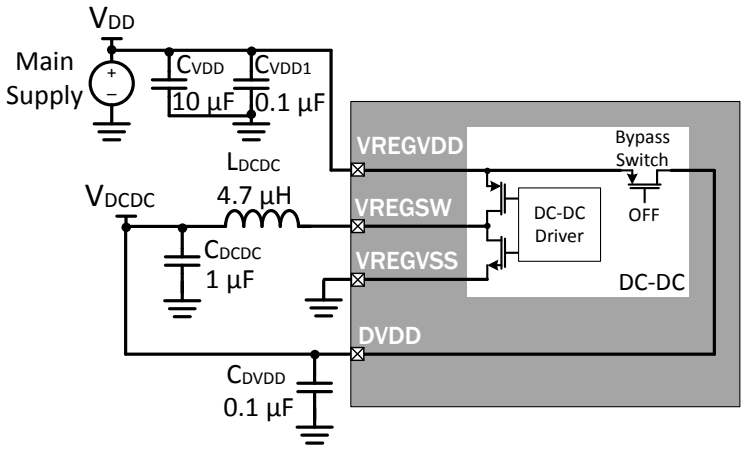


Figure 1.8. DC-DC Converter Powering DVDD

1.10 Radio (RFVDD & PAVDD) — EFR32 Wireless Gecko

On EFR32 Wireless Gecko devices, the radio power supplies (PAVDD and RFVDD) will typically be powered from one of two sources:

1. The integrated DC-DC converter. This option provides improved power efficiency, although it only supports up to 13 dBm transmit power. And due to additional switching noise present on the DC-DC converter output (V_{DCDC}), some additional filtering components may be required.
2. The main supply. This option is less efficient, but requires less filtering components and supports > 13 dBm transmit power.

1.10.1 RFVDD and PAVDD — Powered from DC-DC

Both RFVDD and PAVDD may be powered from the DC-DC converter output (V_{DCDC}) for lowest power operation. Note, however, that the maximum transmit power is limited to 13 dBm when PAVDD is powered from V_{DCDC}. If higher power is required, PAVDD should be powered from the main supply instead of the DC-DC output.

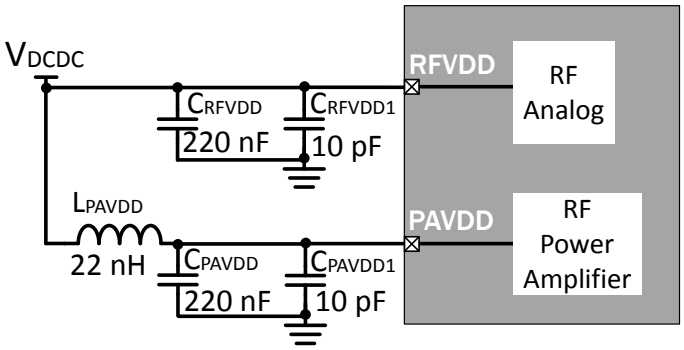


Figure 1.9. RFVDD and PAVDD Decoupling (2.4 GHz Application, both supplies powered from DC-DC output)

The minimal BOM option eliminates C_{RFVDD1} and C_{PAVDD1}, which may allow acceptable RF performance at lower power levels. For more complete details on the minimal BOM option, along with performance comparisons, refer to *AN933: EFR32 2.4 GHz Minimal BOM*.

Table 1.3. RFVDD & PAVDD Decoupling Values, Powered from DC-DC Converter

Application	C_{RFVDD}	C_{RFVDD1}	L_{PAVDD}	C_{PAVDD}	C_{PAVDD1}
2.4 GHz	220 nF	10 pF	22 nH	220 nF	10 pF
2.4 GHz (minimal BOM)	220 nF	-	22 nH	220 nF	-
sub-GHz	220 nF	56-270 pF	100-270 nH	220 nF	56 - 270 pF
sub-GHz (minimal BOM)	220 nF	-	100-270 nH	220 nF	-

Table 1.4. Recommended L_{PAVDD} 22 nH Inductor

Manufacturer	Part Number	Inductance (nH)	I_{MAX} (mA)	DCR (Ω)	Operating Temperature (°C)	Package
Murata	LQG15HS22NJ02D	22±5%	300	0.420	-55 to +125	0402/1005

1.10.2 RFVDD and PAVDD — Powered from Main Supply

When greater than 13 dBm transmit power is required, PAVDD should be powered directly from the main supply, and RFVDD may be powered from either the main supply or the DC-DC output (V_{DCDC}). Note that in this configuration, the L_{PAVDD} filter inductor is not shown on the PAVDD input, because the main supply is presumed to be less noisy than V_{DCDC}.

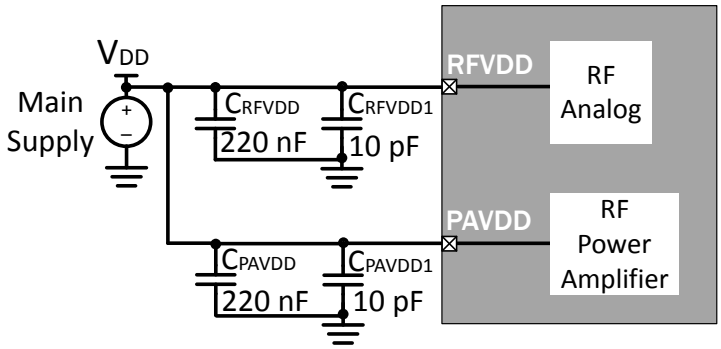


Figure 1.10. RFVDD and PAVDD Decoupling (2.4 GHz Application, both supplies powered from Main Supply)

The minimal BOM option eliminates C_{RFVDD1} and C_{PAVDD1}, which may allow acceptable RF performance at lower power levels. For more complete details on the minimal BOM option, along with performance comparisons, refer to *AN933: EFR32 2.4 GHz Minimal BOM*.

Table 1.5. RFVDD & PAVDD Decoupling Values, Powered from Main Supply

Application	C_{RFVDD}	C_{RFVDD1}	L_{PAVDD}	C_{PAVDD}	C_{PAVDD1}
2.4 GHz	220 nF	10 pF	-	220 nF	10 pF
2.4 GHz (minimal BOM)	220 nF	-	-	220 nF	-
sub-GHz	220 nF	56-270 pF	-	220 nF	56 - 270 pF
sub-GHz (minimal BOM)	220 nF	-	-	220 nF	-

2. Example Power Supply Configurations

2.1 EFM32 Series 1 Gecko and EZR32 Example Power Supply Configurations

Several EFM32 Series 1 Gecko and EZR32 example power supply configurations are shown below.

2.1.1 EFM32 Series 1 and 2 Gecko — Standard Decoupling Example

The figure below illustrates a standard approach for decoupling. This configuration is simple and uses minimal components, while providing sufficient noise suppression for many typical applications.

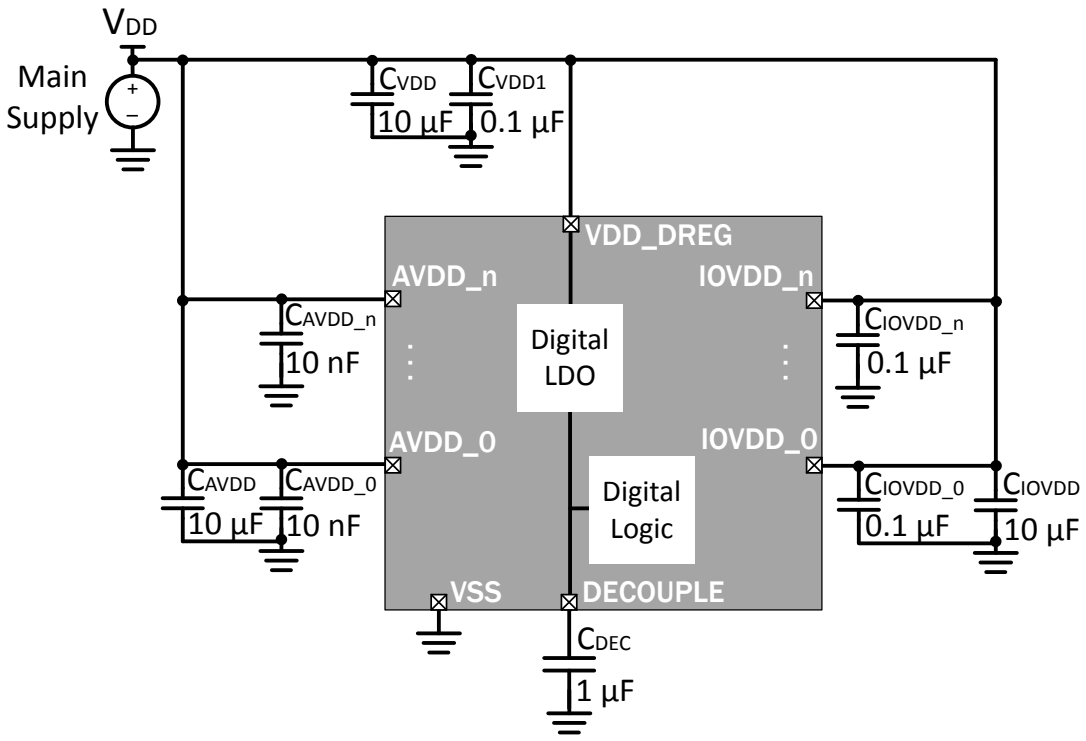


Figure 2.1. EFM32 Series 1 and 2 Gecko Standard Decoupling Example

2.1.2 EFM32 Series 1 and 2 Gecko — Improved AVDD Filtering Example

In the following figure, a decoupling approach providing better noise suppression and isolation between the digital and analog power pins using a ferrite bead and a resistor is illustrated. This configuration is preferred when higher ADC accuracy is required. Refer to Table 1.2 Recommended Ferrite Beads on page 5 for recommended ferrite bead part numbers.

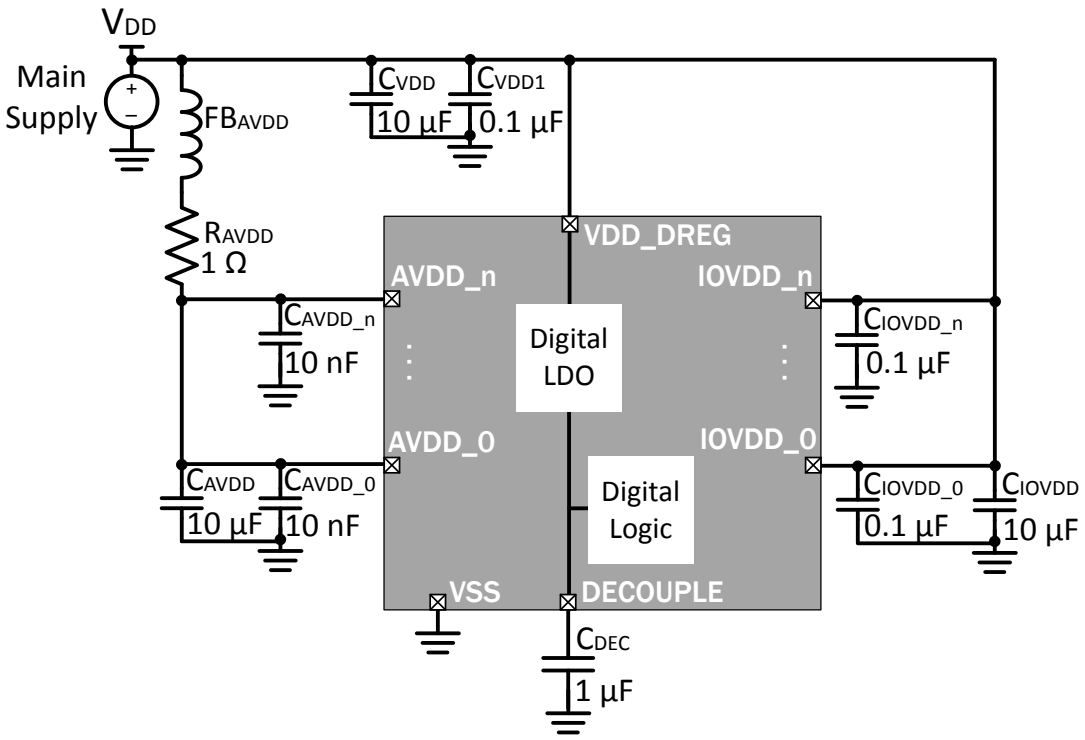


Figure 2.2. EFM32 Series 1 and 2 Gecko Improved AVDD Filtering Example

Note: Note that during power-on for EFM32GG and EFM32G Gecko devices, the AVDD_x pins must not be powered up after the IOVDD_x and VDD_DREG pins. If the rise time of the power supply is short, the filter in Figure 2.2 EFM32 Series 1 and 2 Gecko Improved AVDD Filtering Example on page 10 can cause a significant delay on the AVDD_x pins. For improved AVDD filtering for EFM32GG and EFM32G Gecko devices, refer to section 2.1.3 EFM32GG and EFM32G Gecko Only — Improved AVDD Filtering Example

2.1.3 EFM32GG and EFM32G Gecko Only — Improved AVDD Filtering Example

Similar to section 2.1.2 EFM32 Series 1 and 2 Gecko — Improved AVDD Filtering Example, the figure below shows improved noise suppression and isolation between the digital and analog power pins for high ADC accuracy. Refer to Table 1.2 Recommended Ferrite Beads on page 5 for recommended ferrite bead part numbers.

There is a unique restriction on EFM32GG and EFM32G Gecko devices that at power on, the AVDD_x pins must not be powered up after the IOVDD_x and VDD_DREG pins. If the rise time of the power supply is short, the AVDD filter can cause a significant delay on the AVDD_x pins. Therefore, for EFM32GG and EFM32G Gecko devices, an additional 1 Ω resistor should also be added to the VDD_DREG supply path, as shown in the figure below.

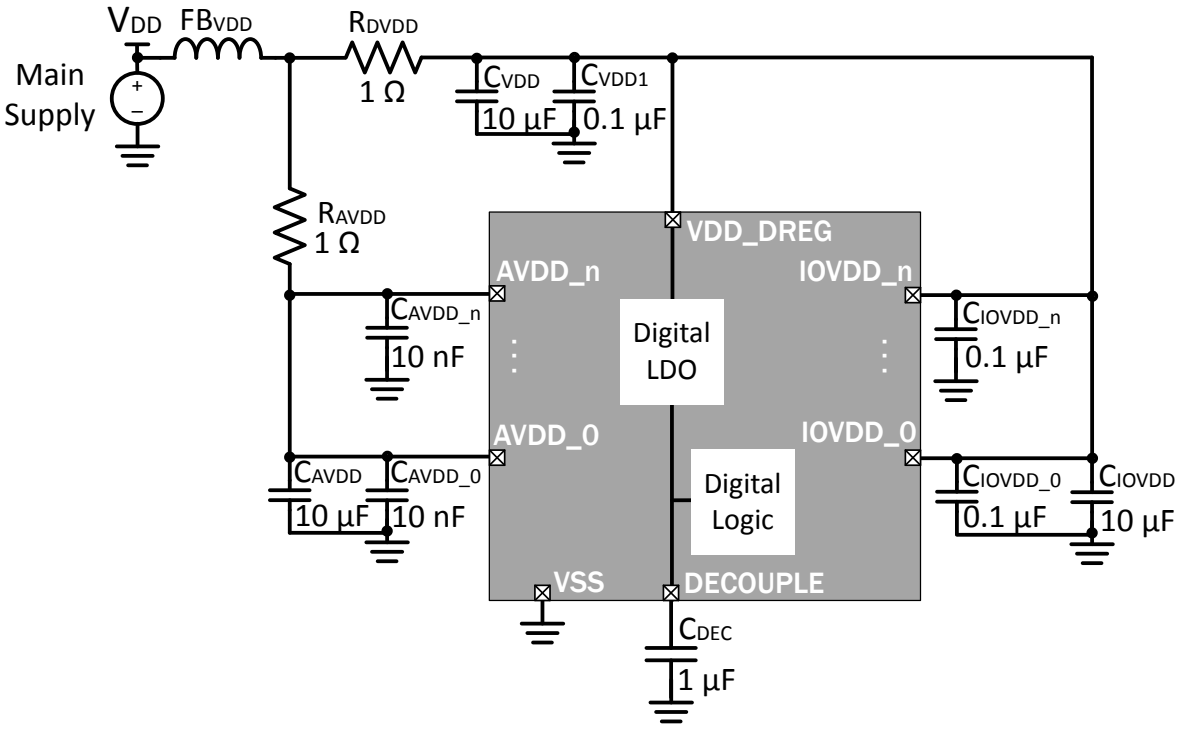


Figure 2.3. EFM32 Series 1 and 2 Gecko Improved AVDD Filtering Example

2.1.4 EZR32 — Standard Decoupling Example

The figure below illustrates a standard approach for decoupling a EZR32 device.

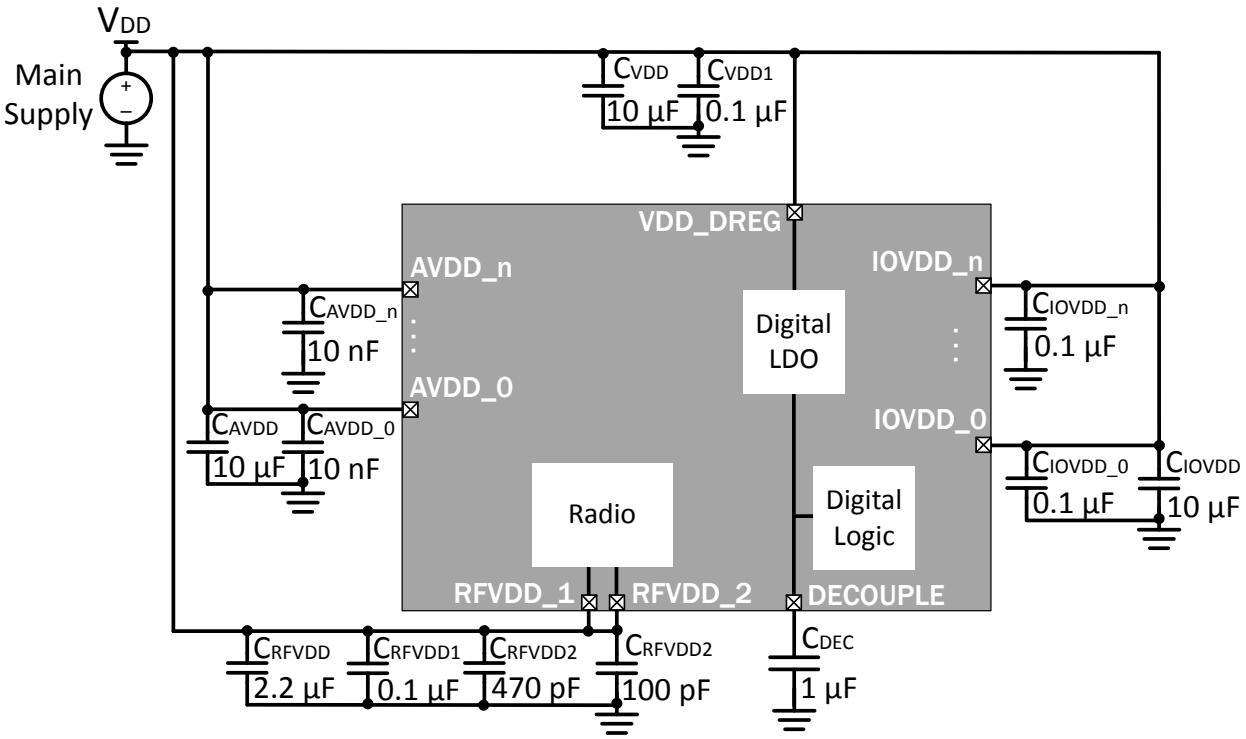


Figure 2.4. EZR32 Standard Decoupling Example

2.2 EFM32 Series 2 and EFR32 Wireless Gecko Example Power Supply Configurations

EFM32 Series 2 and EFR32 Wireless Gecko applications can enable the DC-DC converter to maximize power savings in embedded applications. The DC-DC converter requires an external inductor and capacitor, in addition to the standard decoupling capacitors on each power net. For detailed information on the DC-DC converter operation, emlib programming, recommended DC-DC components, and supported power configurations, see application note *AN0948: Power Configurations and DC-DC*.

At power on, the EFM32 Series 2 and EFR32 Wireless Gecko devices boot into an initial power configuration with the DC-DC module bypassed internally (i.e, the VREGVDD pin is shorted internally to the DVDD pin). After startup, software must change the power configuration settings to configure the DC-DC and any associated external components as described in the following subsections.

Note: Figure 2.5 EFM32 Series 2 and EFR32 Wireless Gecko Startup Configuration on page 13 is only provided to show the device startup default supply configuration, and is not a usable application configuration.

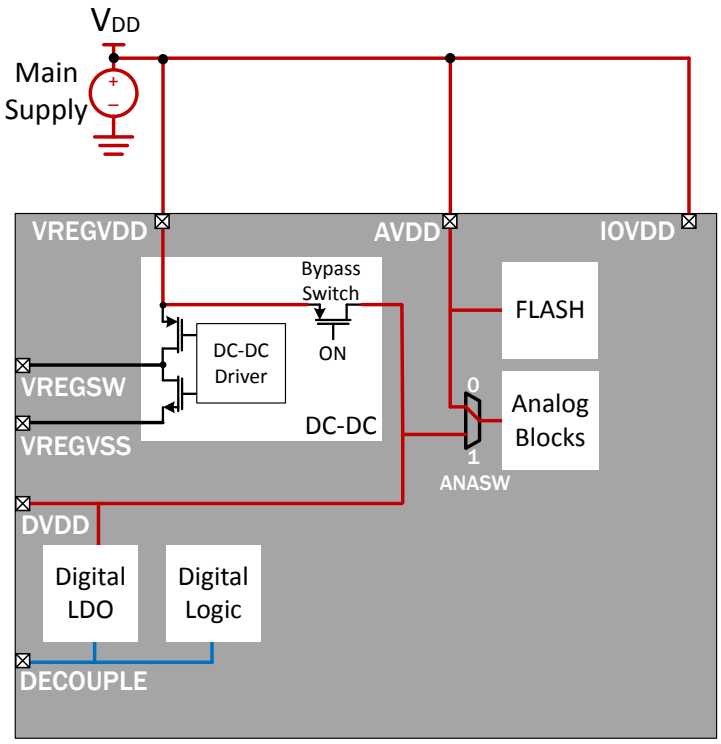


Figure 2.5. EFM32 Series 2 and EFR32 Wireless Gecko Startup Configuration

2.2.1 EFR32 Wireless Gecko — No DC-DC, 2.4 GHz, <= 13 dBm Example

For space-sensitive or cost-sensitive applications, or when power efficiency isn't important, the DC-DC converter may be unused. In this configuration:

- The DC-DC converter is programmed in Off mode, and the Bypass switch is Off.
- The DVDD pin must be powered externally - typically, it is shorted to the main supply.
- In addition, RFVDD, PAVDD, IOVDD, and AVDD are all connected to the main supply.
- VREGSW should be left disconnected.

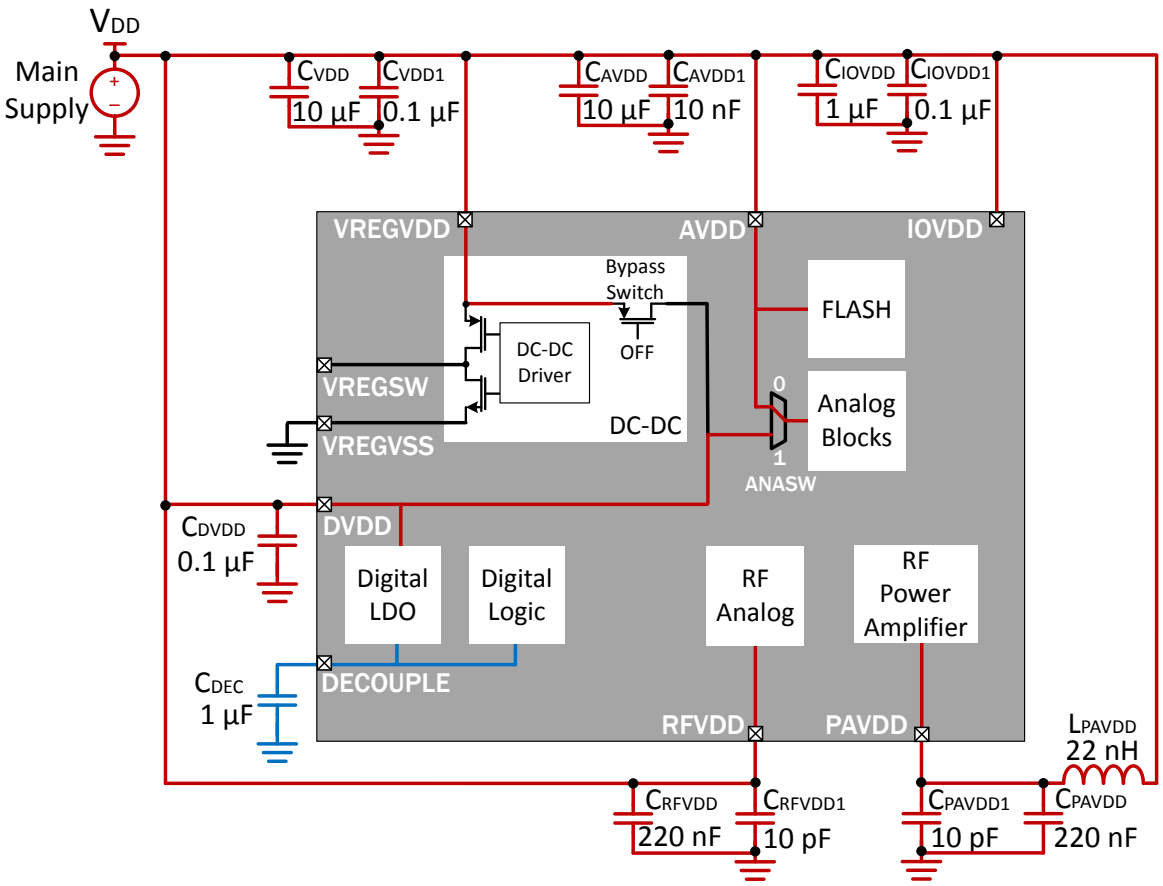


Figure 2.6. EFR32 Wireless Gecko No DC-DC, 2.4 GHz, <= 13 dBm Example

2.2.2 EFR32 Wireless Gecko — DC-DC, 2.4 GHz, <= 13 dBm Example

For the lowest power radio applications, the DC-DC converter can be used to power the DVDD supply, as well as RFVDD and PAVDD. In this configuration:

- The DC-DC Output (V_{DCDC}) is connected to DVDD. DVDD powers the internal Digital LDO which powers the digital circuits.
- Both radio power supplies (RFVDD and PAVDD) are also powered from the DC-DC Output.
- AVDD is connected to the main supply voltage. The internal analog blocks may be powered from AVDD or DVDD, depending on the ANASW configuration. Flash is always powered from the AVDD pin.
- IOVDD could be connected to either the main supply (as shown below) or to V_{DCDC}, depending on the system IO requirements.

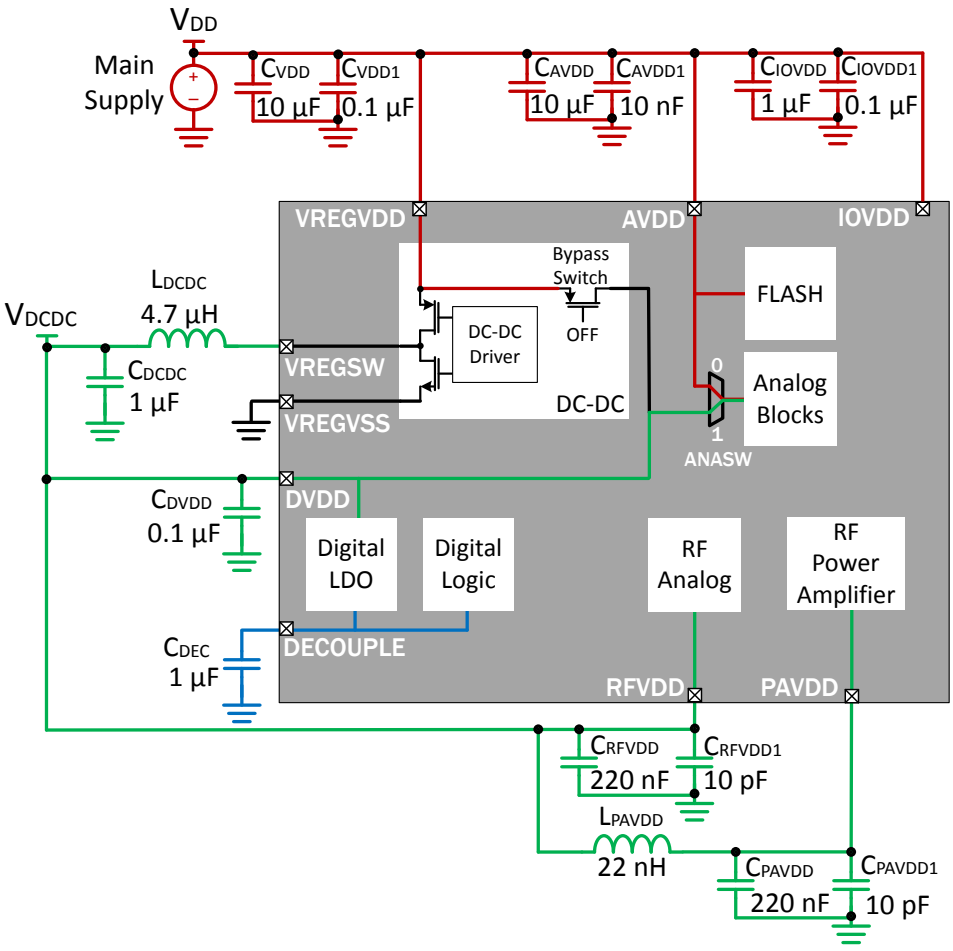


Figure 2.7. EFR32 Wireless Gecko DC-DC, 2.4 GHz, <= 13 dBm Example

2.2.3 EFR32 Wireless Gecko — DC-DC, 2.4 GHz, > 13 dBm Example

When high power (>13 dBm) radio output power is required, PAVDD should be connected to the main supply. The DC-DC converter can continue to power DVDD, IOVDD, and RFVDD. This power configuration is illustrated below.

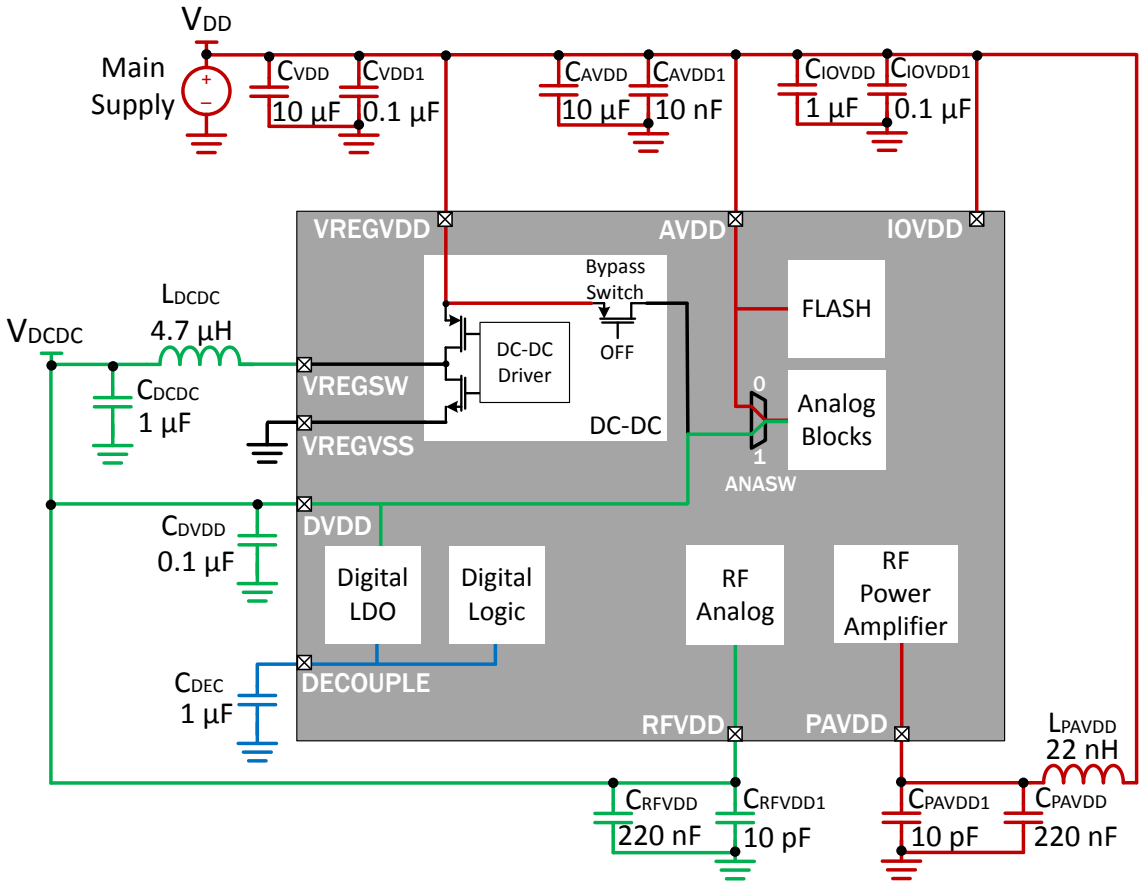


Figure 2.8. EFR32 Wireless Gecko DC-DC, 2.4 GHz, > 13 dBm Example

2.2.4 EFM32 Series 2 Gecko — DC-DC Example

The diagram below illustrates a typical connection configuration for a EFM32 Series 2 Gecko device using the DC-DC converter.

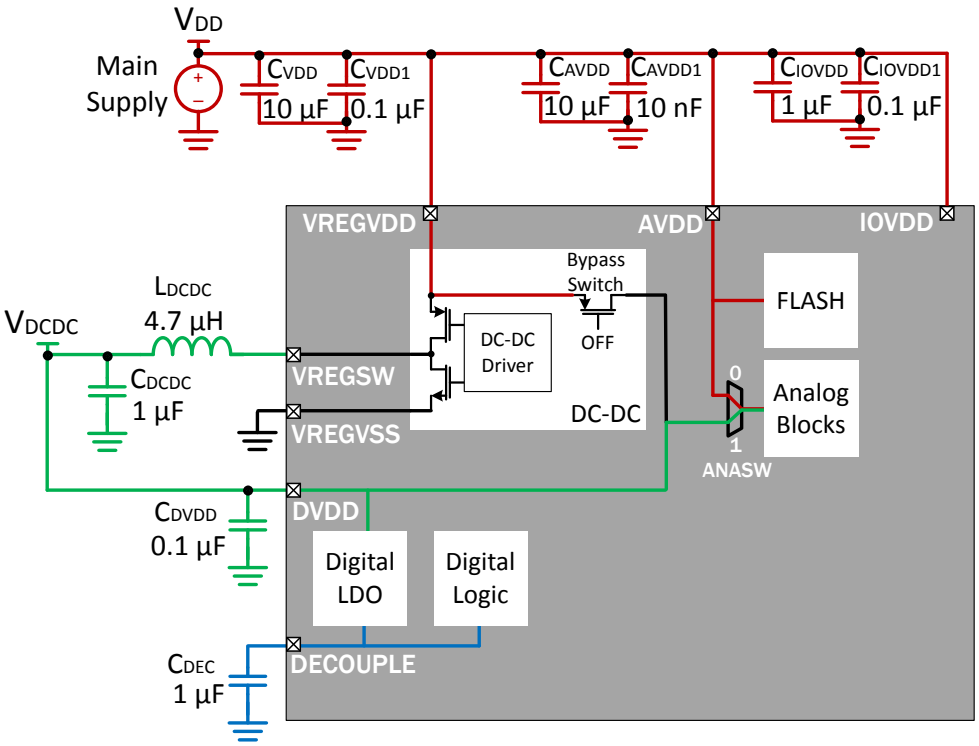


Figure 2.9. EFM32 Series 2 Gecko DC-DC Example

3. Debug Interface and External Reset Pin

3.1 Serial Wire Debug

The Serial Wire (SWD) interface is supported by all EFM32 Series 1 and 2 Gecko, EZR32, and EFR32 Wireless Gecko devices. The SWD debug interface consists of the SWCLK (clock input) and SWDIO (data in/out) lines, in addition to the optional SWO (serial wire output). The SWO line is used for instrumentation trace and program counter sampling, and is not needed for programming and normal debugging. However, it can be valuable in advanced debugging scenarios, and it is therefore recommended to include this line in a design.

The connection to an ARM 20-pin debug connector is shown in the following figure. Pins with no connection should be left unconnected.

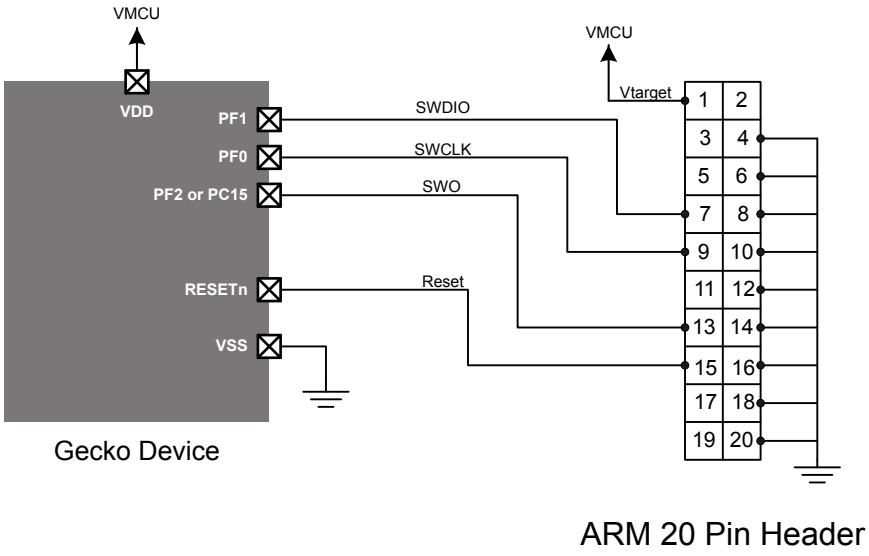


Figure 3.1. Connecting the Gecko Device to an ARM 20-pin Debug Header

Note: The V_{target} connection is not for supplying power. The debugger uses V_{target} as a reference voltage for the debugger's level translators.

3.2 JTAG Debug — EFM32 Series 2 and EFR32 Wireless Gecko

The JTAG debug interface is supported by the EFM32 Series 2 and EFR32 Wireless Gecko devices and consists of the TDI (data input), TDO (data output), TCLK (clock), and TMS (input mode select) lines. TDI carries input data, and is sampled on the rising edge of TCLK. TDO carries output data and is shifted out on the falling edge of TCLK. TCLK is the debug clock line. Finally, TMS is the input mode select signal, and is used to navigate through the Test Access Port state machine.

The connection to an ARM 20-pin debug connector is shown in the following figure. Pins with no connection should be left unconnected.

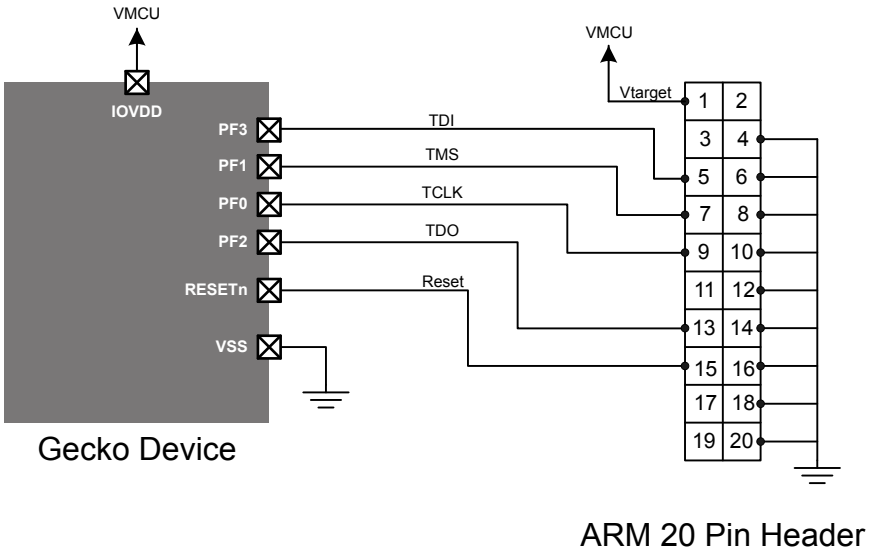


Figure 3.2. Connecting the EFM32 Series 2 and EFR32 Wireless Gecko Device to an ARM 20-pin Debug Header

Note: The V_{target} connection is not for supplying power, only sensing the target voltage.

3.3 External Reset Pin (RESETn)

Forcing the RESETn pin low generates a reset of the EFM32 Series 1 and 2 Gecko, EZR32, and EFR32 Wireless Gecko device. The RESETn pin includes an internal pull-up resistor and can therefore be left unconnected if no external reset source is required. Also connected to the RESETn line is a low-pass filter which prevents noise glitches from causing unintended resets. The characteristics of the pullup and input filter is identical to the corresponding characteristic of a GPIO pin, which is found in the device data sheet.

Note: To apply an external reset source to this pin, drive this pin low during reset. The internal pull-up ensures that the reset is released. This pin should not be connected to an external pull-up or driven high while the device is unpowered, as this could damage the device. This is also important when using back-up power mode, as the internal pull-up automatically switches to the back-up power rail, which could end up back-powering the entire system through the external pull up.

4. External Clock Sources

4.1 Introduction

The EFM32 Series 1 and 2 Gecko, EZR32, and EFR32 Wireless Gecko devices support different external clock sources to generate the low and high frequency clocks in addition to the internal LF and HF RC oscillators. The possible external clock sources for both the LF and HF domains are external oscillators (square or sine wave) or crystals/ceramic resonators. This section describes how the external clock sources should be connected.

For additional information on the external oscillators, refer to the application note *AN0016: Oscillator Design Considerations*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or in Simplicity Studio using the [**Application Notes**] tile.

4.2 Low Frequency Clock Sources

The external low frequency clock can be generated from a crystal/ceramic resonator or from an external clock source.

4.2.1 Low Frequency Crystals and Ceramic Resonators — EFM32 Series 1 Gecko and EZR32

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 4.1 Low Frequency Crystal on page 20. The crystal is to be connected across the LFXTAL_N and LFXTAL_P pins of the EFM32 Series 1 Gecko and EZR32.

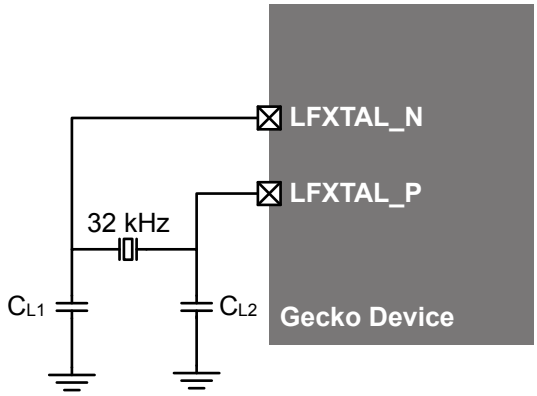


Figure 4.1. Low Frequency Crystal

The crystals/ceramic resonators oscillate mechanically and have an electrical equivalent circuit as shown in Figure 4.2 Equivalent Circuit of a Crystal/Ceramic Resonator on page 20. In the electrical circuit, C_S represents the motional capacitance, L_S the motional inductance, R_S the mechanical losses during oscillation, and C_0 the parasitic capacitance of the package and pins. C_{L1} and C_{L2} represent the load capacitance. This circuit is valid for both crystals and ceramic resonators.

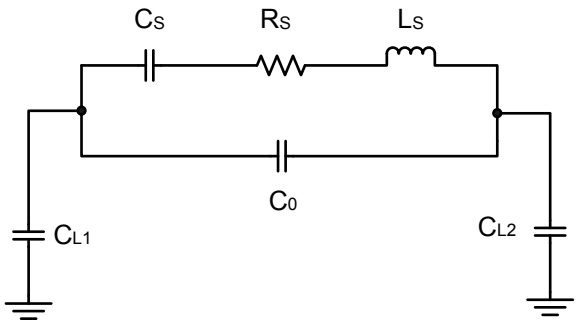


Figure 4.2. Equivalent Circuit of a Crystal/Ceramic Resonator

4.2.2 Low Frequency Crystals and Ceramic Resonators — EFM32 Series 2 and EFR32 Wireless Gecko

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 4.3 Low Frequency Crystal - EFM32 Series 2 and EFR32 Wireless Gecko on page 21. The crystal is to be connected across the LFXTAL_N and LFXTAL_P pins of the EFM32 Series 2 and EFR32 Wireless Gecko. This circuit is valid for both crystals and ceramic resonators.

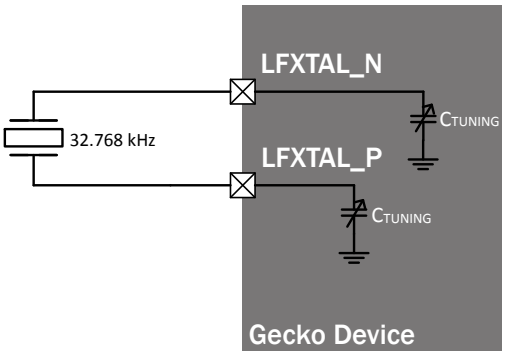


Figure 4.3. Low Frequency Crystal - EFM32 Series 2 and EFR32 Wireless Gecko

The difference between this crystal configuration and that of the EFM32 Series 1 Gecko and EZR32 is that the need for external load capacitors C_{L1} and C_{L2} have been eliminated. These load capacitors are now on-chip and can be tuned by software. The EFM32 Series 2 and EFR32 Wireless Gecko devices support low frequency crystals with load capacitance in the range of 6 pF to 18 pF. Check device specific data sheets and reference manuals for load capacitance values and instructions for tuning the internal load capacitances.

4.2.3 Low Frequency External Clocks

The EFM32 Series 1 and 2 Gecko, EZR32, and EFR32 Wireless Gecko devices can also be clocked by an LF external clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle, and signal levels. The external clock signal can either be a square wave or sine signal with a frequency of 32.768 kHz. The external clock source must be connected as indicated in Figure 4.4 Low Frequency External Clock on page 21.

When a square wave source is used, the LFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%, as specified in the device data sheet. When a sine source is used, the amplitude must be in accordance with the device data sheet. The sine signal is buffered through the LFXO buffer, whose input is ac-coupled.

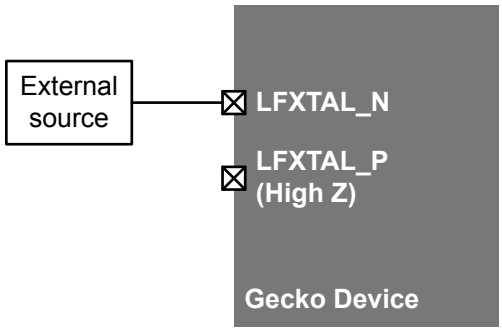


Figure 4.4. Low Frequency External Clock

4.3 High Frequency Clock Sources

The external high frequency clock can be generated from a crystal/ceramic resonator or from an external square or sine wave source.

4.3.1 High Frequency Crystals and Ceramic Resonators — EFM32 Series 1 Gecko and EZR32

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 4.5 High Frequency Crystal Oscillator on page 22. The crystal should be connected across the HFXTAL_N and HFXTAL_P pins.

The electrical equivalent circuit of the HF crystal/ceramic resonators is equal to the one for LF crystals/ceramic resonators in the figure below.

Placement of C_L is important for proper operating frequency.

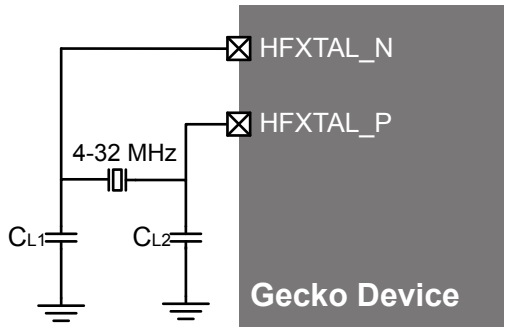


Figure 4.5. High Frequency Crystal Oscillator

4.3.2 High Frequency Crystals and Ceramic Resonators — EFM32 Series 2 and EFR32 Wireless Gecko

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 4.6 High Frequency Crystal Oscillator - EFM32 Series 2 and EFR32 Wireless Gecko on page 22. The crystal should be connected across the HFXTAL_N and HFXTAL_P pins.

The difference between this crystal configuration and that of the EFM32 Series 1 Gecko and EZR32 is that the need for external load capacitors C_{L1} and C_{L2} have been eliminated. These load capacitors are now on-chip and can be tuned by software. The EFM32 Series 2 and EFR32 Wireless Gecko devices support high frequency crystals with load capacitance in the range of 6 pF to 12 pF. Check device specific data sheets and reference manuals for load capacitance values and instructions for tuning the internal load capacitances.

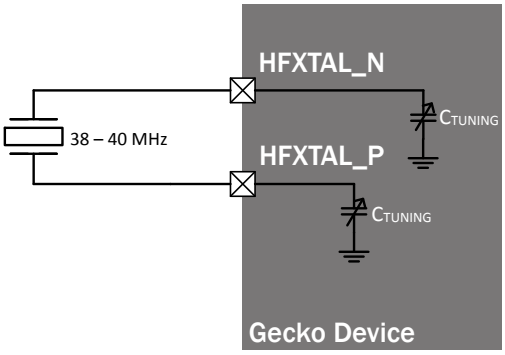


Figure 4.6. High Frequency Crystal Oscillator - EFM32 Series 2 and EFR32 Wireless Gecko

Note: Some devices are subject to the 38 - 40 MHz frequency limit for the high frequency crystal oscillator, whereas other devices will have a wider frequency range. Please consult the device-specific data sheet for more information.

4.3.3 High Frequency External Clocks

The EFM32 Series 1 and 2 Gecko, EZR32, and EFR32 Wireless Gecko devices can also be clocked by an external HF clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle and signal levels. The external clock signal can either be square wave or a sine signal with a frequency in accordance with the device data sheet. The external clock source must be connected as indicated in Figure 4.7 External High Frequency Clock on page 23.

When a square wave source is used, the HFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%. Refer to the device data sheet for further details. When a sine source is used, the sine amplitude must be in accordance with what is specified in the device data sheet. The sine signal is buffered through the HFXO buffer, whose input is ac-coupled.

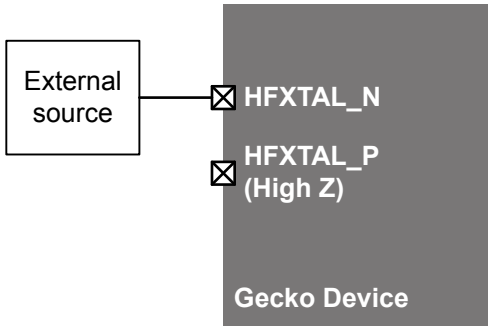


Figure 4.7. External High Frequency Clock

5. Reference Design

When starting a new EFM32 Series 1 Gecko and EZR32 design, some parts of the layout are almost always required regardless of the application. Attached to this application note are example schematics for power decoupling, reset, external clocks, and debug interface. Using this reference design as a template can improve development speed in the early stages of a new design. The reference design and included symbols are compatible with Cadence OrCAD 9.0 and later versions.

This application note does not include footprints for the devices, but these can be found in `*.bxl` format on http://www.silabs.com.

5.1 Contents

The application note folder includes several zip files with the following contents:

- CSV pin list files
- Edif symbols
- OrCAD OLB symbols
- OrCAD DSN example schematics
- PDF example schematics

The schematics and symbols are included for the following device families:

- EFM32ZG
- EFM32HG
- EFM32TG
- EFM32G
- EFM32LG
- EFM32WG
- EFM32GG

A generic symbol is included for the EZR32 family.

5.2 Comments on the Schematics

5.2.1 Power Supply Decoupling

The decouple pin uses a 1 µF capacitor to filter transients in the power domain for the internal voltage regulator.

Each power pin has a 100 nF decoupling capacitor in addition to the common 10 µF decoupling capacitor, as described in 2.1 EFM32 Series 1 Gecko and EZR32 Example Power Supply Configurations. The digital power supply is separated from the analog power supply to reduce EMI. To further improve the switching noise of the analog power, an EMI suppressor is put in series between V_{MCU} and the analog power pins.

The active low reset pin is connected to ground through a normally open switch, as well as to the debug interface connector.

5.2.2 Debug Interface

A standard ARM 20-pin debug connector is connected to the EFM32 Series 1 Gecko and EZR32 device debug pins.

5.2.3 High/Low Frequency Clock

Both the high and low frequency clock pins are connected to crystal oscillators using two of the recommended crystals from the *AN0016: Oscillator Design Considerations* application note.

6. Revision History

6.1 Revision 1.45

2016-6-15

Added note about ceramic capacitor selection for extended temperature range devices (i.e., -55 °C – +125°C)

Added power supply pin overview

Added section on USB power pins

Updated all the power supply connection diagrams

Added EZR32 power supply diagram

6.2 Revision 1.44

2015-11-13

Added power configuration and crystal resonator info for EFR32 Wireless Gecko portfolio devices.

6.3 Revision 1.43

2015-10-21

Added power configuration and crystal resonator info for EFM32 Series 2 Gecko devices.

Added symbols and schematics for EFM32JG and EZR32PG devices.

6.4 Revision 1.42

2015-03-04

Added symbols and schematics for EFM32HG and EZR32LG devices.

6.5 Revision 1.41

2015-02-13

Added EZR32 devices.

Updated format.

6.6 Revision 1.40

2014-05-07

Added symbols and schematics for EFM32WG and EFM32ZG devices.

Corrected numbering for EM4WU pins for EFM32TG devices in symbols and schematics.

6.7 Revision 1.36

2013-10-14

New cover layout

6.8 Revision 1.35

2013-08-14

Updated section on power supply decoupling

6.9 Revision 1.34

2013-05-08

Added note about decoupling capacitor purpose.

Added new design files for new packages and devices.

6.10 Revision 1.33

2012-03-21

Added CSV and Edif formats for schematic symbols.

6.11 Revision 1.32

2012-03-16

Added OrCAD reference designs and OrCAD symbols for more parts.

6.12 Revision 1.31

November 23th, 2010.

Corrected schematic values.

Added information on power sequencing considerations.

6.13 Revision 1.30

November 17th, 2010.

Added information on alternate schematic recommendations.

6.14 Revision 1.20

September 13th, 2010.

Merged sections on PCB design considerations and external clock sources.

Modified chapter on external clock sources to correspond with *AN0016: EFM32 Oscillator Design Considerations*.

Added OrCAD and PDF reference designs.

6.15 Revision 1.10

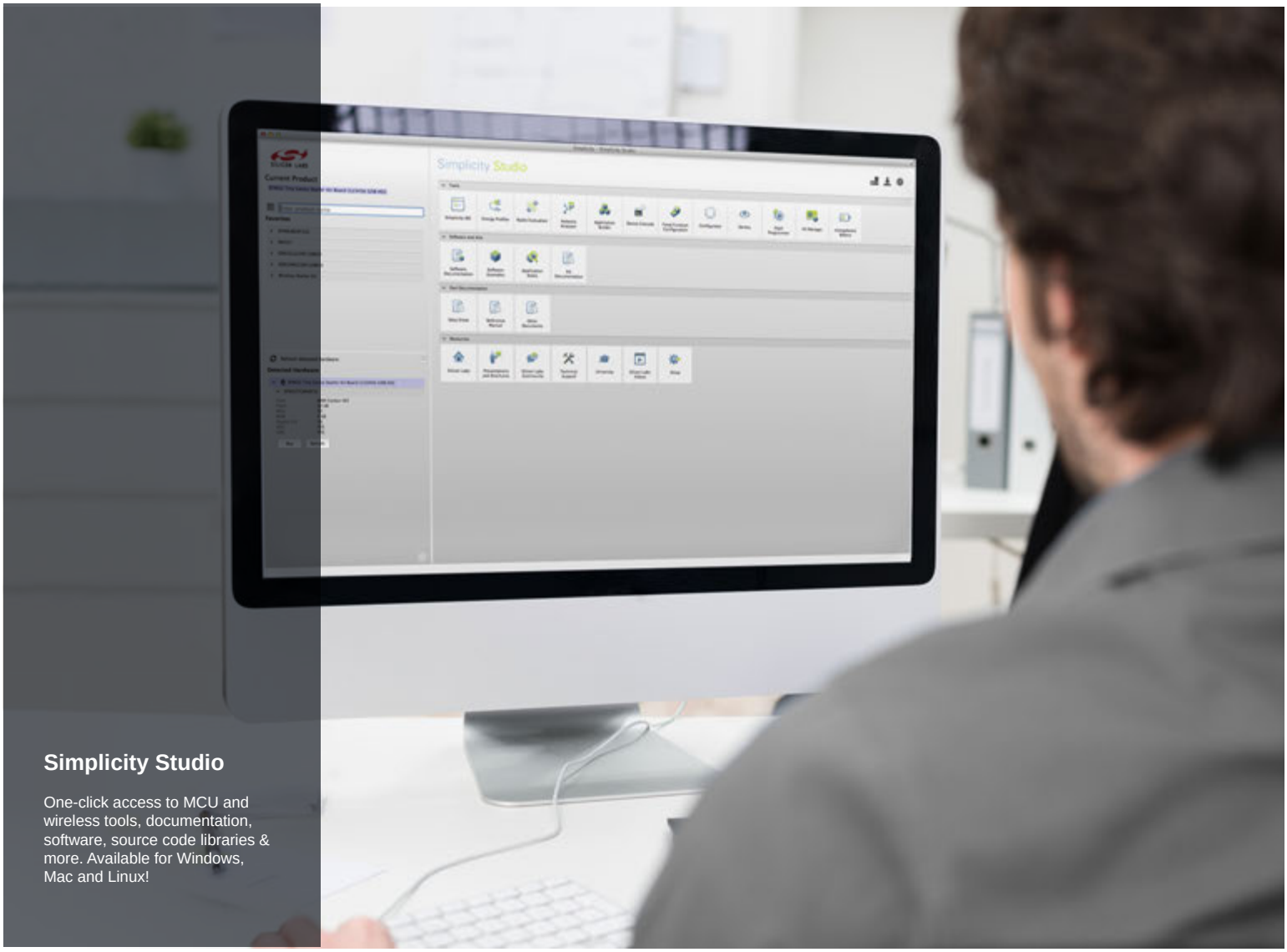
May 6th, 2010.

Added debug interface section.

6.16 Revision 1.00

October 21th, 2009.

Initial revision.



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