Signal Integrity

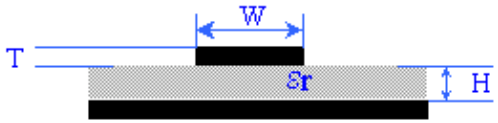
From IBIS2Spice

This example shows how to use a converted IBIS model to perform an analysis on the signal integrity of a PCB trace at high frequencies. In this simplified example, we'll use the 74VHC04 (http://www.fairchildsemi.com/pf/74/74VHC04.html) hex inverter chip from Fairchild Semiconductor. The chip model (http://www.fairchildsemi.com/models/email_model_file.jsp?file=vhc04tm0.inc) we'll use is typical with an SOIC-14 package.

Problem

Let's say that two 74VHC04s are being used to buffer a clock signal from one side of a PCB to another. The two chips are connected via a straight line, 4 inch long, 6 mil (0.006 inch) copper trace on 62 mil thick FR4 substrate using 1oz copper. Below the trace, on the other side of the PCB, is a ground plane. This is a the type of construction that a normal board house, such as PCB Fab Express (http://www.pcbfabexpress.com) . Using their board specifications to calculate the impedance characteristics of the PCB trace, we have:

- Er = 4.2 - This is the permeability of the FR4 substrate.
- H = 62 mils - This is the thickness of the FR4 substrate.
- W = 6 mils - This is the width of the PCB trace.
- T = 1 oz - This is the thickness of the copper trace.



Characterizing the PCB Trace

We can then plug in these values to a Microstrip Trace Impedance Calculator (http://www.pcb123.com/help/calculators/microstrip.html) and we see that the PCB trace has the following characteristics:

$Zo = 150.6Ohms$ - This is the characteristic impedance of the PCB 'transmission line'

$Lo = \frac{20.79nH}{in}$ - The distributed inductance of the trace.

$Co = \frac{0.917pF}{1in}$ - The distributed capacitance of the trace.

Distributed over 4 inches, the line has a total capacitance and inductance of:

$$L = \frac{20.79nH}{1in} * 4in = 83.16nH$$

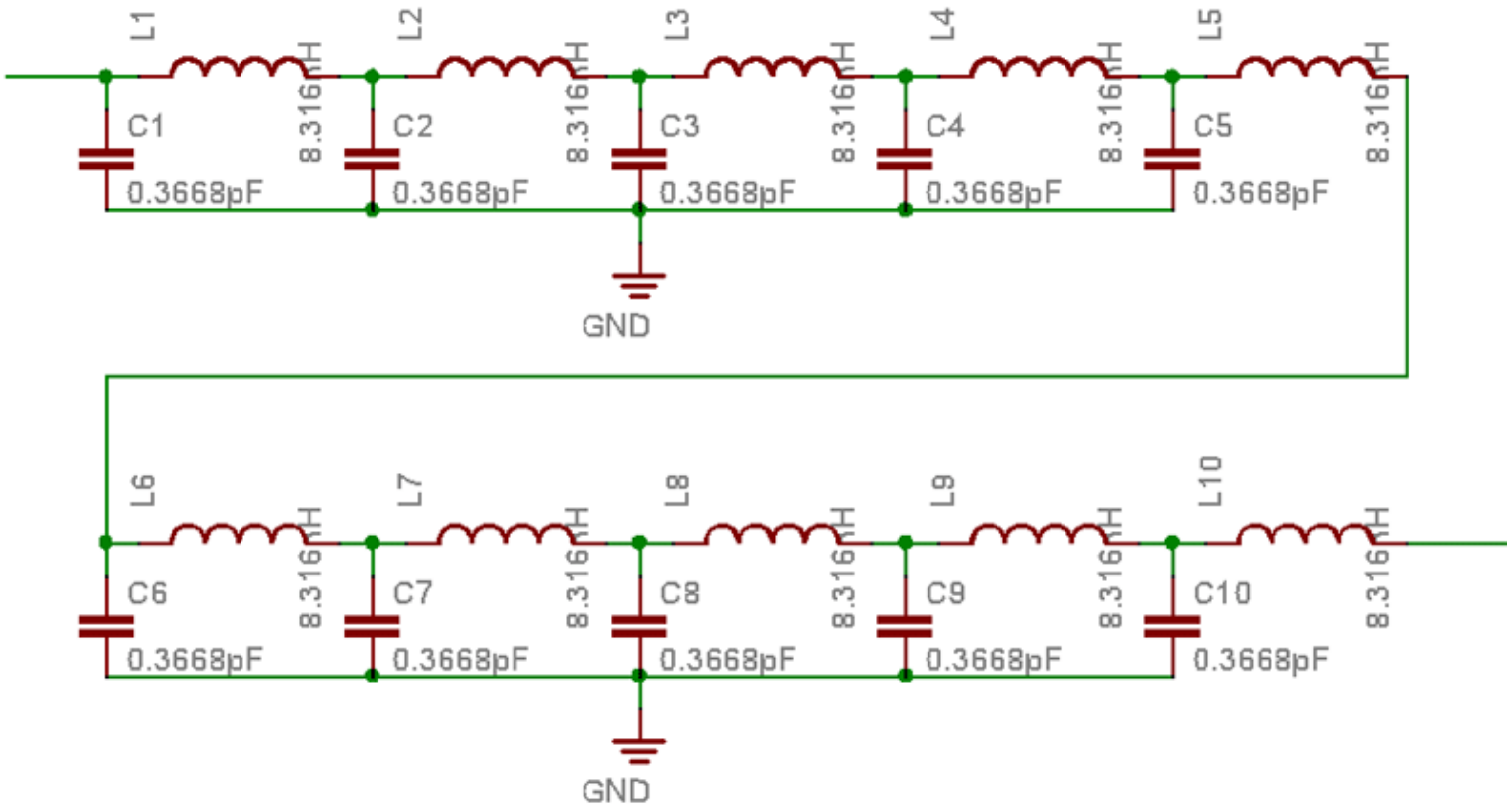
$$C = \frac{0.917pF}{1in} * 4in = 3.668nH$$

This capacitance and inductance is distributed evenly along the line. For simulation purposes, we could schematically represent the transmission line as 10 inductors and 10 capacitors whose values are:

$$L_d = \frac{83.16nH}{10} = 8.316nH$$

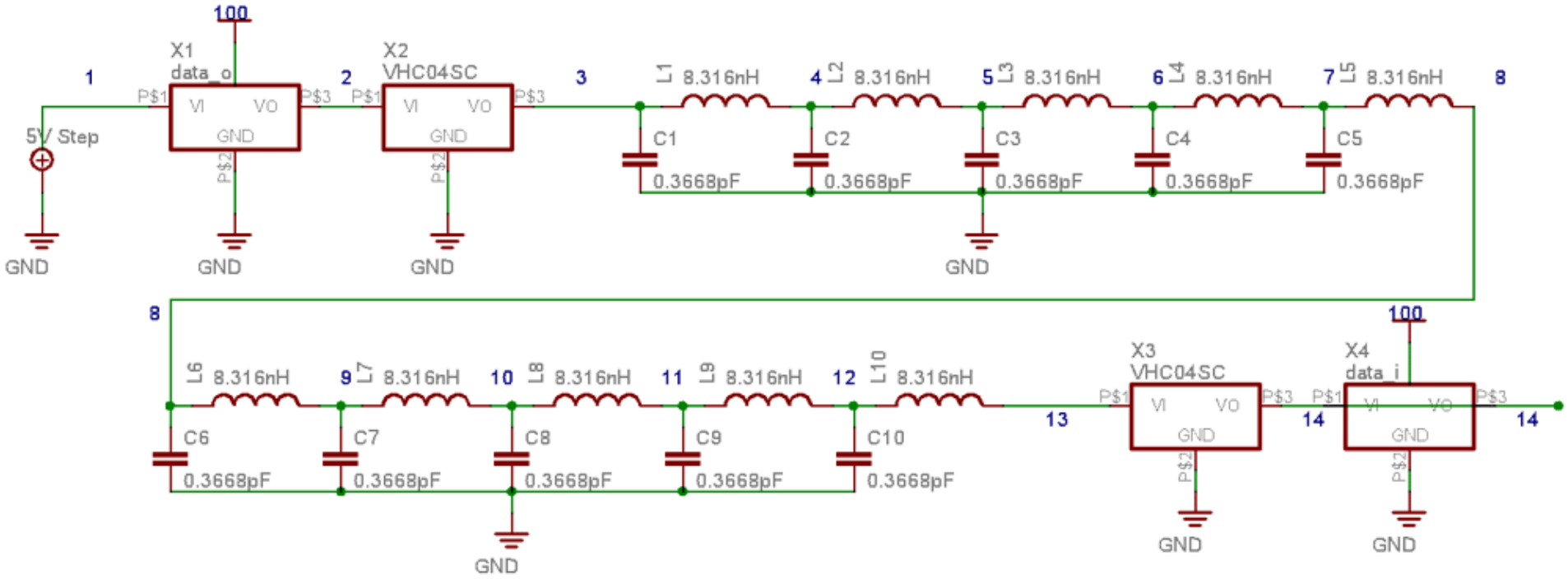
$$C_d = \frac{3.668nH}{10} = 0.3668nH$$

Schematically, it looks like this:



Creating a Net List

The schematic below was used to construct the following LTSpice (http://www.linear.com/designtools/software/) net list. The blue numbers in the schematic are the net list nodes. X1 through X4 come from the converted IBIS model. X1 is the model for the 74VHC04 output, X2 and X3 is the SOIC-14 package model, and X4 is the 74VHC04 input model.



Now that you have an accurate model of the system, you can simulate the circuit and review the Analysis of SI Example Waveforms.

Note to self:
At the end of the example, include links to Mentor Graphics software and other expensive IBIS PCB analysis software and point out that they got to do the same thing that expensive software does for the price of a conversion - $1.

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Analysis of SI Example Waveforms

From IBIS2Spice

Contents

Uncompensated Signals Analysis

First, let's look at our uncompensated system at different frequencies. What we're really trying to do with this analysis is answer the question: "At what frequencies do the transmission line effects of the PCB trace begin to affect the integrity of the clock signal?"

Figured 1 through 3 all show three waveforms. If you refer back to the schematic on the Signal Integrity page, you'll see that V(1) corresponds to the input signal (at node 1) - i.e. the clock signal we are attempting to buffer, V(3) is the output signal of the driving 74VHC04 chip at the pin, and V(14) is the signal that the receiving 74VHC04 chip 'see's when the signal get's through its package and to the actual silicon.

100 KHz Clock

Even at 100 KHz, a relatively slow signal by today’s standards, there is significant distortion of the signal by the time it reaches the receiving 74VHC04 chip. You can see in Figure 1 that as the first 74VHC chips tries to drive a logic high on the line, the reactance of the PCB trace forces the signal to oscillate as low as 3.709 Volts. Since a 5V CMOS part has a very consistent logic threshold of 2.5V, the signal is still about 1.2V above where it may be considered a logic 0. The integrity of our signal is pretty good and the trace probably does not need to be compensated.

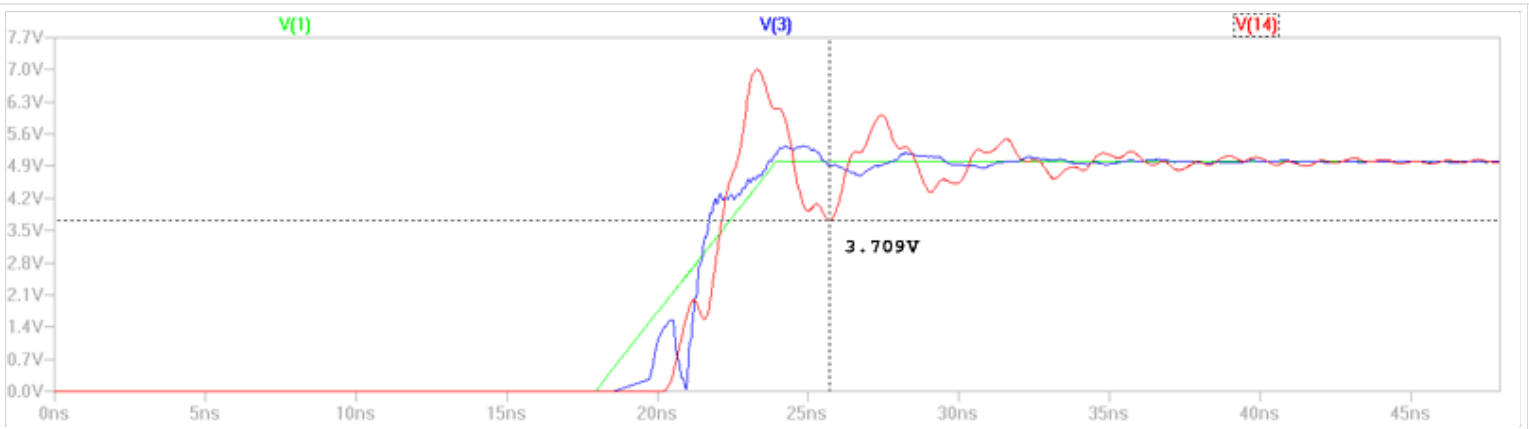

Fig. 1 - 100KHz Signal Analysis

1 MHz Clock

You can see from Figure 2 that there are no degrading effects on the signal by increasing the frequency from 100 KHz to 1MHz. The frequency effects do not create any appreciable distortion of our signal from the change in frequency. Therefore, weather the system is compensated or not, the system can run a 1 MHz signal just as 'cleanly' as a 100 KHz signal.

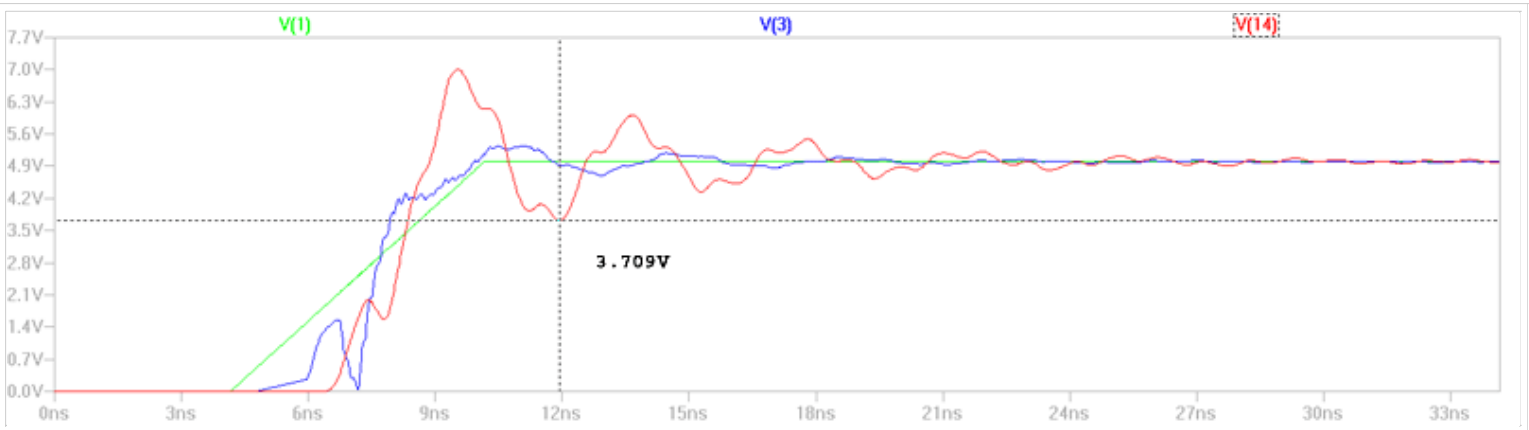

Fig. 2 - 1MHz Signal Analysis

10 MHz Clock

At 10 MHz we begin to see additional signal degradation due to frequency effects. At this frequency the oscillation of the signal reaches a minimum of 3.092V - only about 0.6V above the logic threshold of 2.5V. At this and higher frequencies, the high-frequency transmission lines effe cts of the PCB begin to seriously affect the integrity of the clock signal.

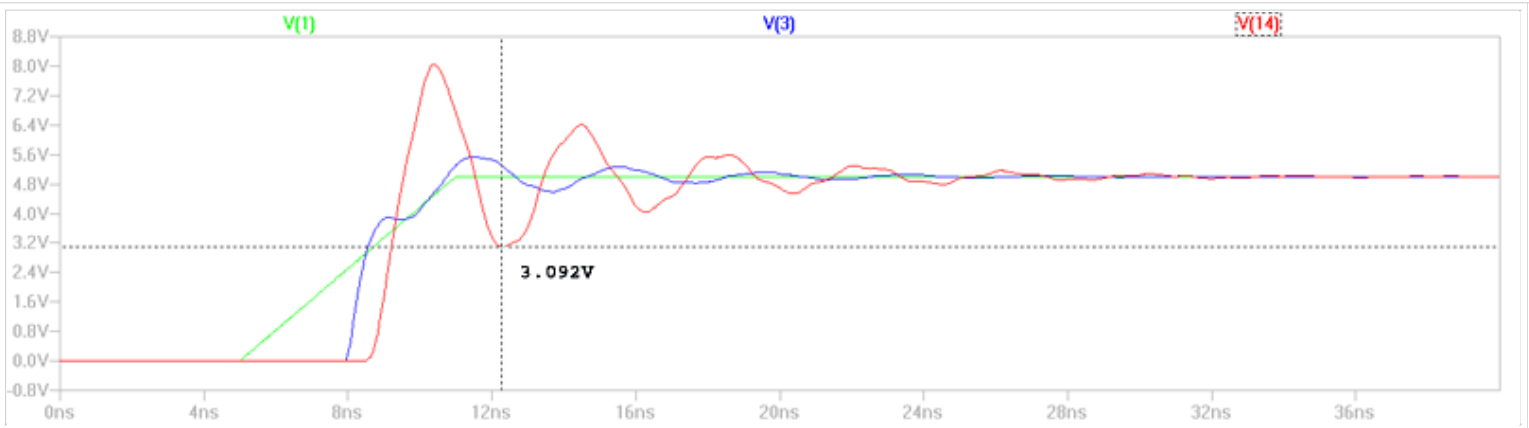

Fig. 3 - 10MHz Signal Analysis

Compensated Signal Analysis

Since the real world is always noisier than a simulation, any circuit should use capacitors or inductors to compensate a PCB trace whenever a simulation shows that high-frequency effects will drop the signal to within 1 volt of the respective logic threshold. For our example, we can compensate the trace by placing a capacitor as physically close as possible to the receiving 74VHC04 chip - shown in the layout below:

Fig. 4 - Compensated Circuit Layout

This is the equivalent of adding a capacitor between node 13 and ground in our simulation schematic (http://www.ibis2spice.com/mw/index.php/Image:PCB_strip_full_schematic.gif) . In Figure 5, you can see that at 10 MHz an added capacitance of 47pF minimizes the distortion so well that our signal reaches a minimum of only 4.865V - that's 2.365V above the logic threshold!

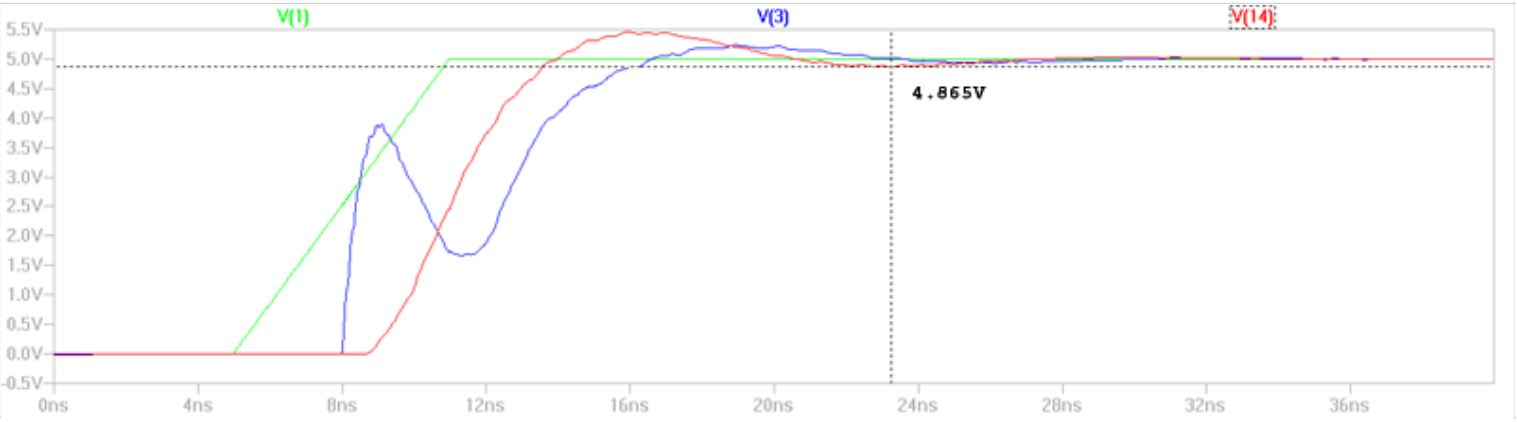

Fig. 4 - Compensated Circuit Layout

The value of 47pF was not chosen arbitrarily. Using the LTSpice simulator and creating a net list based on the converted IBIS model, we can simulate with different capacitance values. Through trial and error, 47pF was shown to be an optimal value for compensating the signal. 47pF is also a readily available value for a 1206 surface mount part. Note: at different frequencies, the optimal value of a compensation capacitor will be different.

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