2EI4: Project #4

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Christy Joseph-Anton, josepc11, 400325365]**

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Circuit Schematic

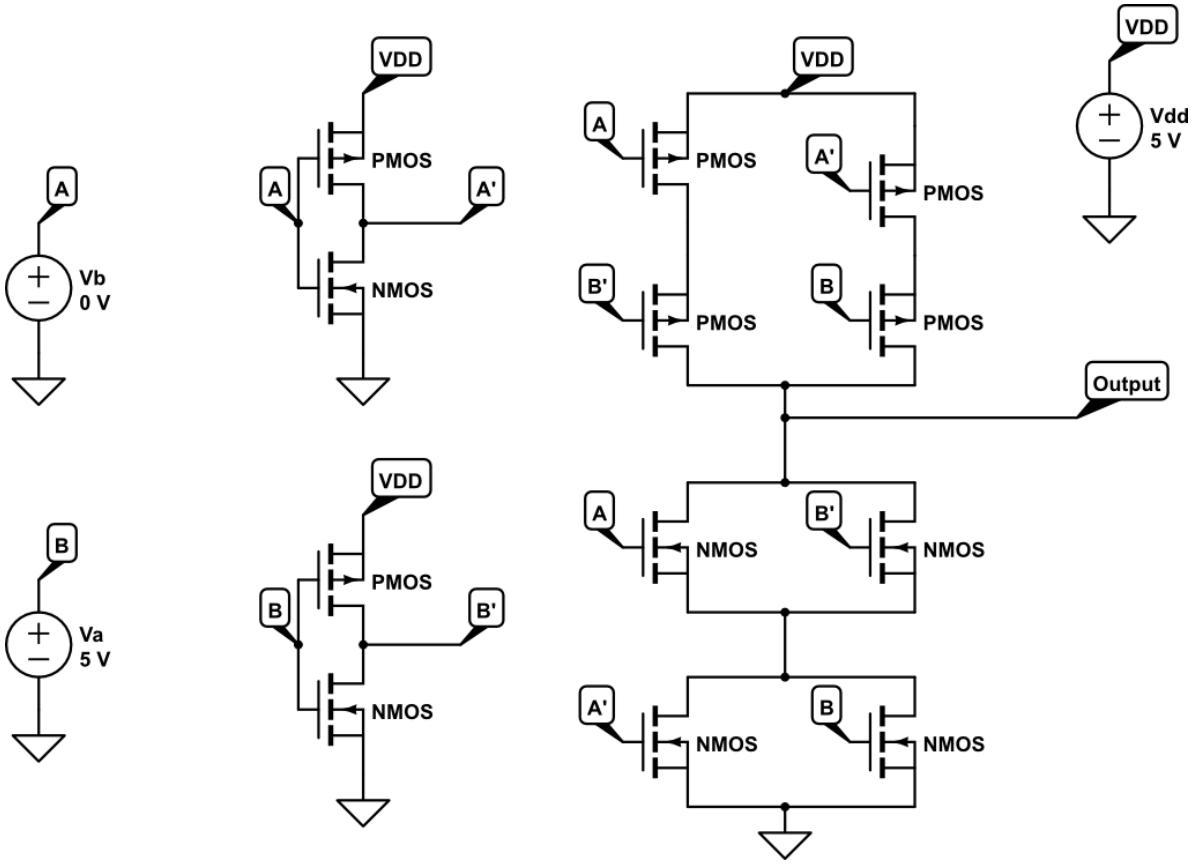


Figure 1: MOSFET based XOR gate, modeled in CircuitLab

The function for the XOR between A and B is:

$$= A'B + AB'$$

This is then converted into the negative function, as CMOS logic is inherently inverted:

$$= ((A'B)'(AB')')'$$
$$= ((A + B')(A' + B))'$$

$$\overline{(\boldsymbol{A} + \overline{\boldsymbol{B}})(\overline{\boldsymbol{A}} + \boldsymbol{B})}$$

Using the design methodology learned in lecture, the circuit schematic was created using the function above.

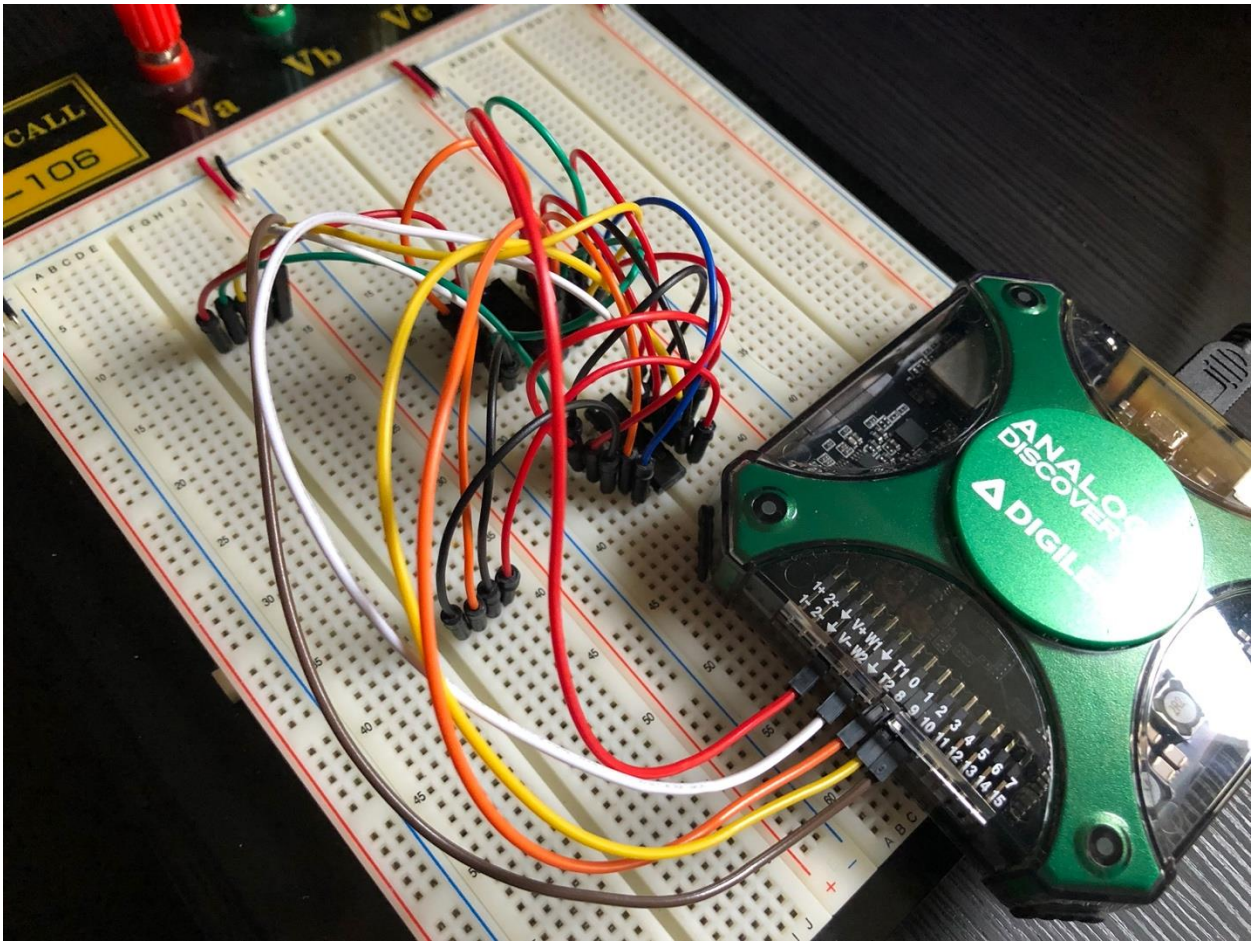
Ideal Sizing

In order to achieve symmetry and have the P-MOSFETS and N-MOSFETS switch at the same time, each of the MOSFETs must be sized such that in the worst case, its switching time is equal to the switching time of the reference inverter. For this course, (W/L)N = 2/1 and (W/L)P = 5/1, therefore all the transistors need to be sized using this reference. For this circuit, all the N-

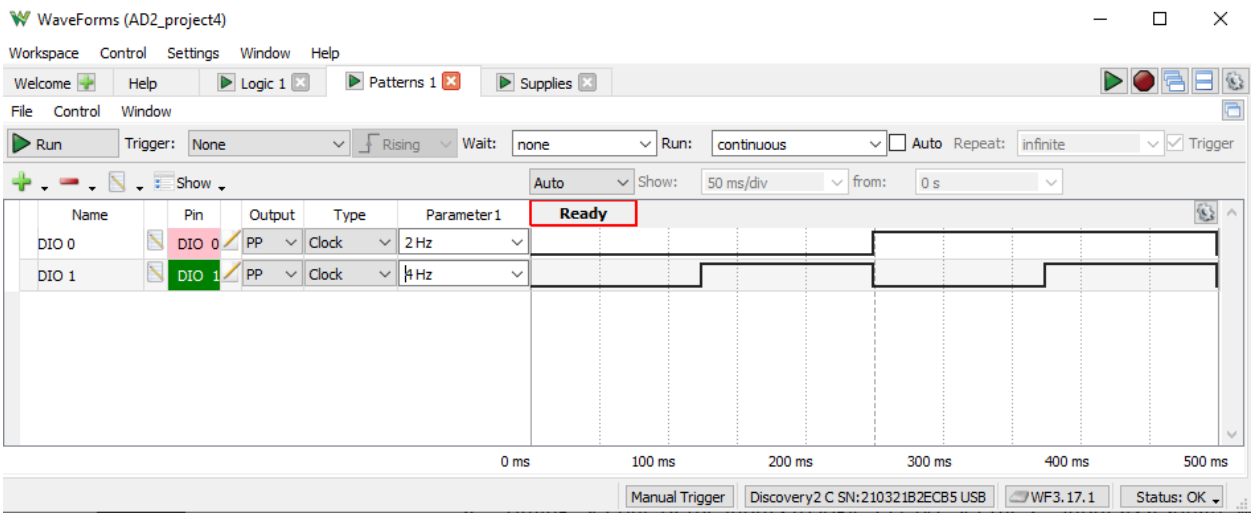
MOSFETs need sizing of 2n, where n is the N-MOSFET reference. The P-MOSFETs need sizing of 2p, where p is the P-MOSFET reference.

The ideal sizing cannot be implemented in the hardware design. In order to realize ideal results, the sizing of each transistor must be changed based on the circuit configuration. This is done to ensure the resistance of each transistor is as close as possible to the reference transistor so delays while switching is reduced. However, in this circuit, all the transistors are roughly the same size, with (W/L)N = 2/1 and (W/L)P = 5/1. We cannot simply change the physical properties of the transistors we are given. Due to the nonideality, there will be notable timing delays with switching inputs in relation to the output. This can be seen using the AD2.

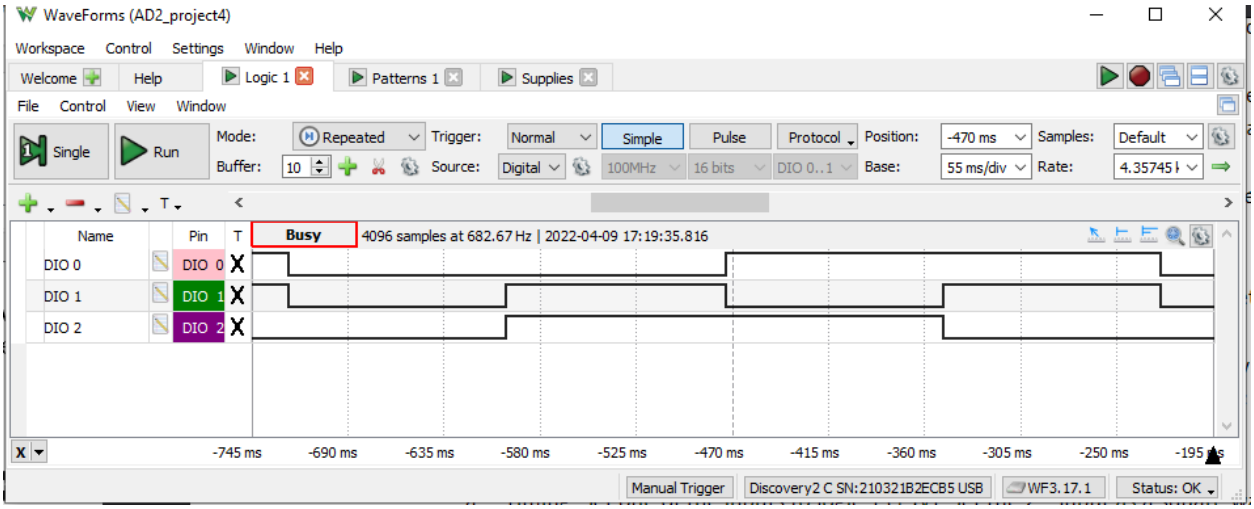
Functional Testing



Using the pattern generator, and logic analyzer, the functionality of the XOR gate was tested. A 2Hz pulsing pattern was used for input A and a 4Hz pulsing pattern was used for input 4. This ensured all logic combinations were tested: 00,01,10,11.



Then, A(DIO 0), B(DIO 1), Y(output)(DIO 2) were displayed using the logic analyzer. This display was zoomed in so only the 4 logic combinations are seen.

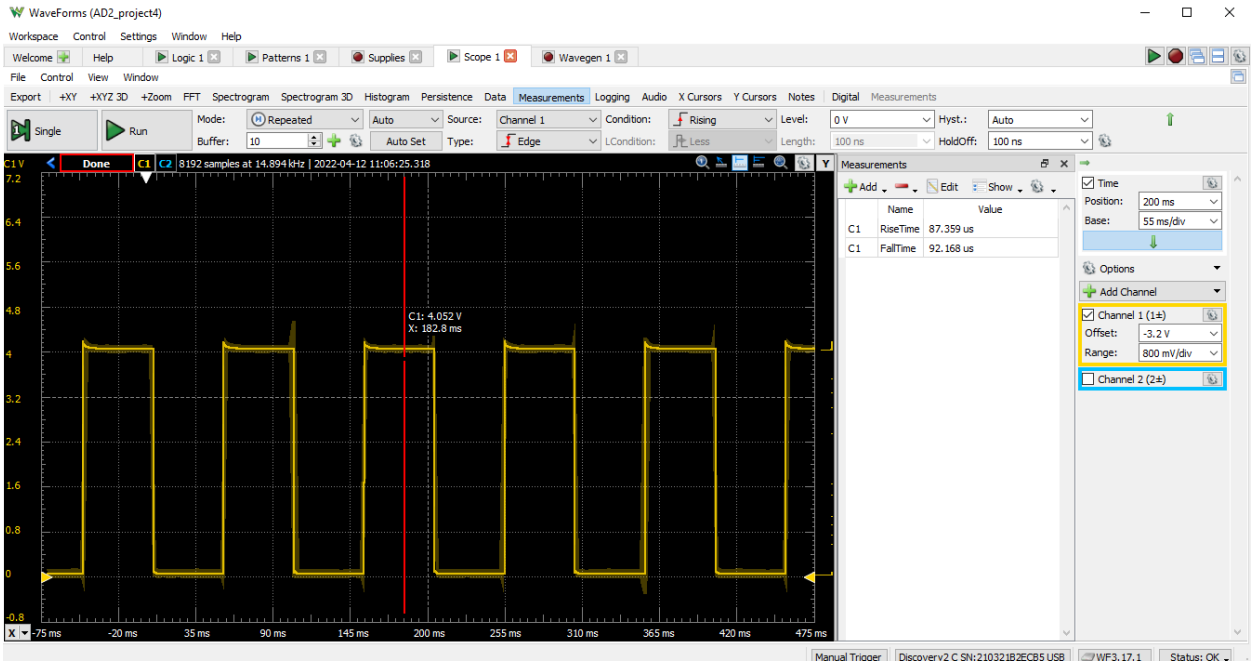


Looking at the screenshot above, the circuit is HIGH only when A and B are not the same. When they are the same, the circuit outputs LOW. This is the functionality of a XOR gate; therefore, the circuit is functioning as expected.

Static level Testing

To find VL and VH of the circuit, input A was set to HIGH (5V), and input B was set to a square wave that ranges from 0V-5V.

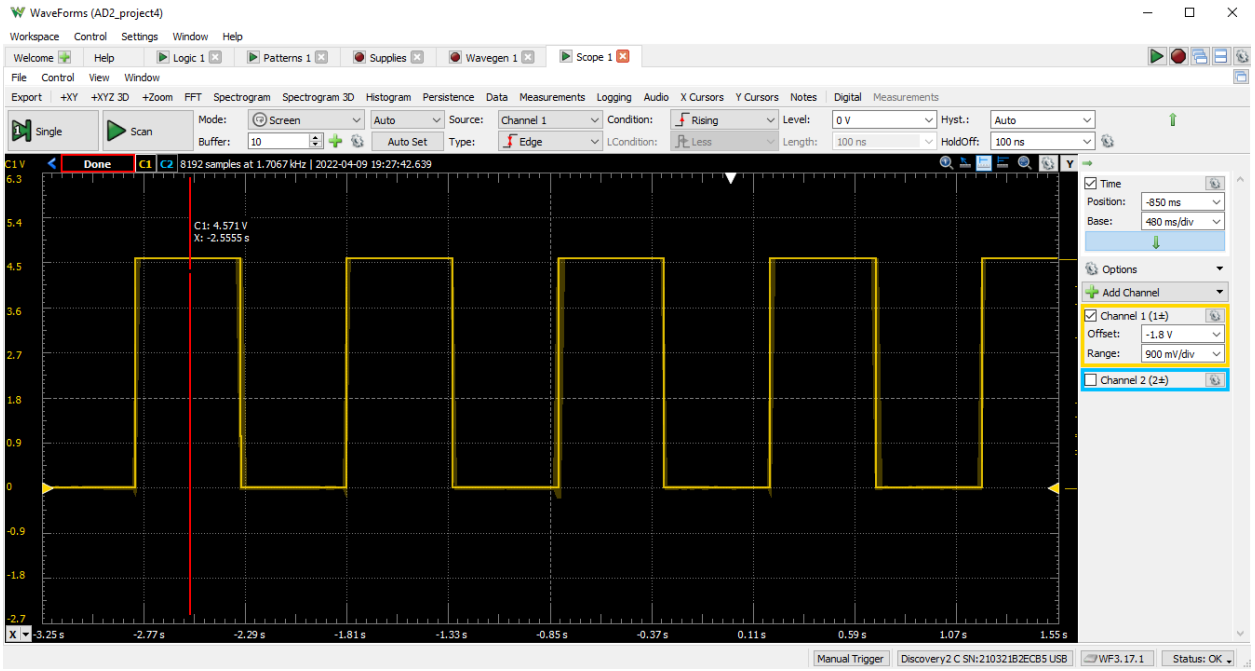
Next, the output Y was displayed on the scope. This will show VL and VH.



According to the scope:

$$VH = 4.052V$$
$$VL = 54.43mV$$

Next, the same test is performed with the inputs switched:



With the inputs switched the results are:

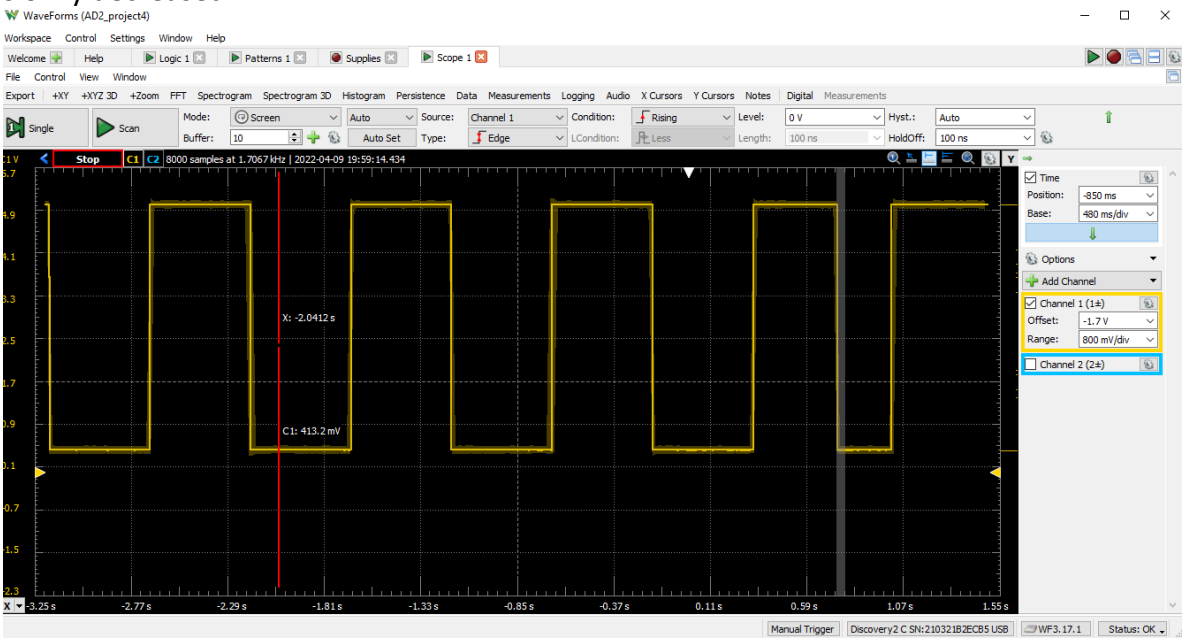
$$VH = 4.571V$$
$$VL = 4.14mV$$

When the inputs are switched, VH and VL are slightly different, however, they should be nearly the same. This could be due to internal resistance within the wires used. In order to construct

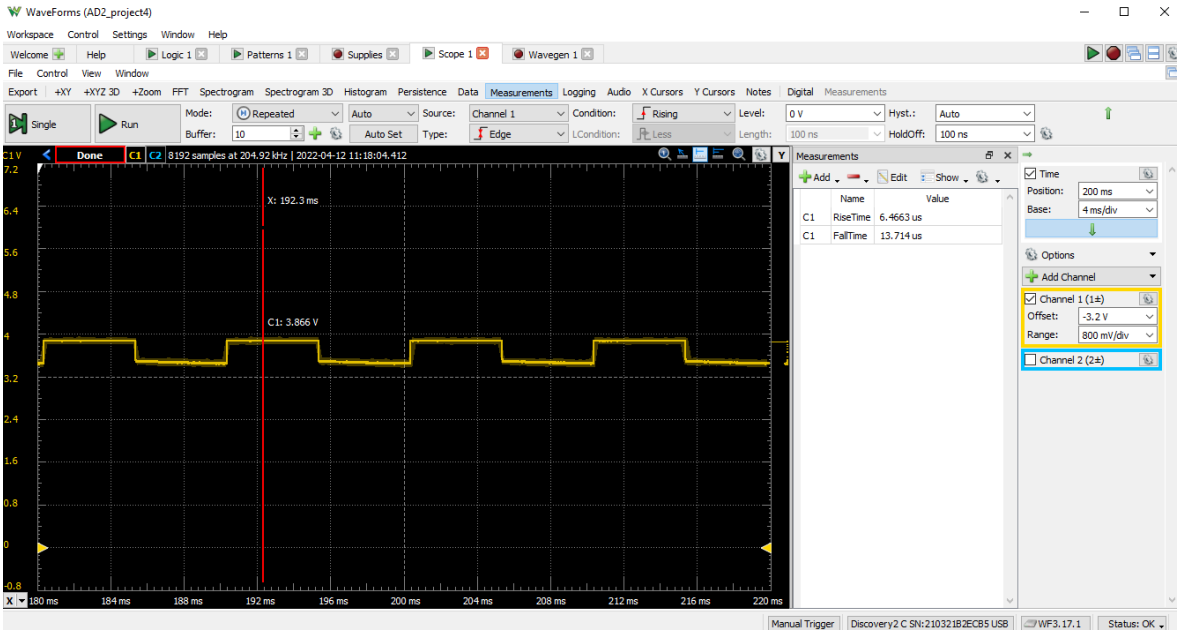
this circuit, a lot of wires needed to be used, so there is a greater chance one or more of those wires have higher internal resistance unaccounted for.

Next, VIL and VIH are found. This will be a very rough approximation of the actual values.

Input B was set to a logic HIGH (5V), and the amplitude of input A (2.5V offset square wave) was slowly decreased.



Through trial and error, it was found that a approximate 100mV amplitude is the smallest amplitude that will result in a functional logic circuit. After 100mV, the logic does not work. Below is a screenshot of the waveform with an input amplitude of 50mV:

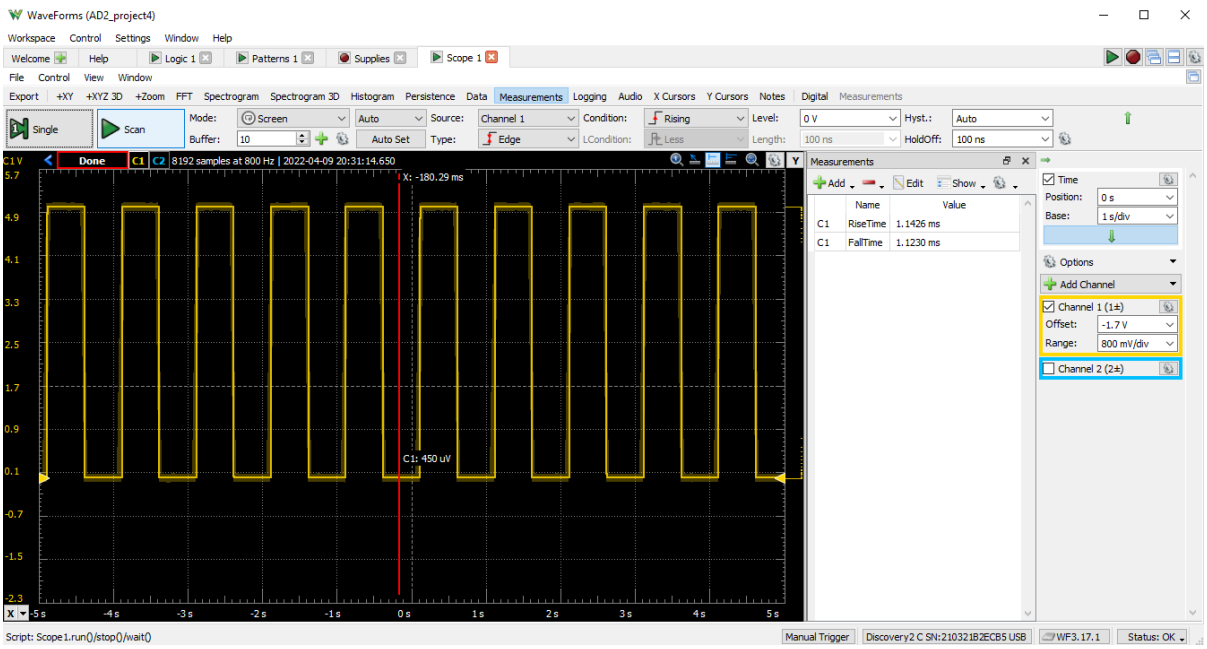


Therefore, VIH and VIL are equal to 2.5+/- 0.1 V:

$$VIH \approx 2.6V$$
$$VIL \approx 2.4V$$

Timing

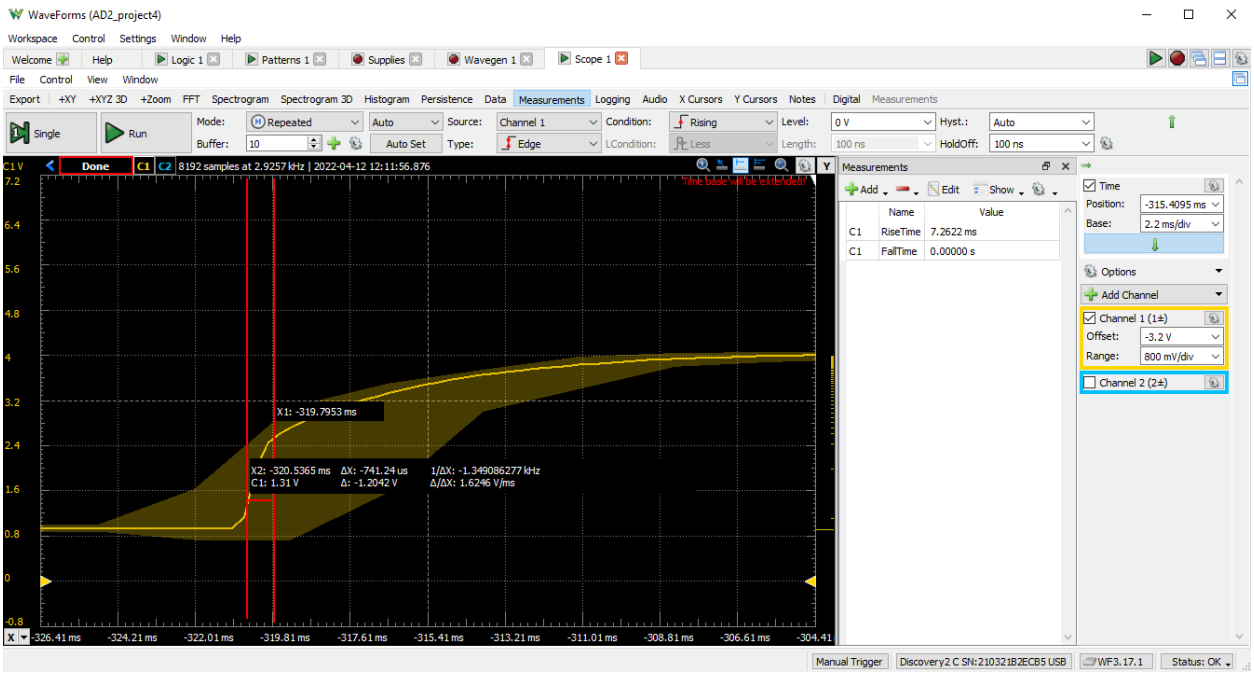
The rise and fall times of the output wave with the capacitor was found using the measurement tools within wave forms. The scope was zoomed out, so more data is included, therefore more accurate results.



According to the screen above, the results are as follows:

$$Rise\ time = 1.426ms$$
$$Fall\ time = 1.1230ms$$

To find τ_{PLH}, the time it took for the output to go from 10% low to 50% was measured. This was done with a 100nF capacitor connected.



This was also done to obtain τ_{PHL} using the same methodology but with the 90% and 50% marks.

The results obtained were:

$$\tau_{PLH} = 741.24us$$
$$\tau_{PHL} = 425.90us$$

Ideally, these values should be similar, however, I found the time to switch from high to low was significantly faster than the time to switch from low to high.

To find τ_P, the average of both values above was found:

$$\tau_p = \frac{\tau_{PLH} + \tau_{PHL}}{2}$$
$$\tau_p = \frac{741.24\text{us} + 425.90\text{us}}{2}$$
$$\tau_p = 583.57us$$