Micropipeline: Delay

```
    room.audience.map(p => self.greet(p))
```

Package: delayPack

```
package delayPack is
    COMPONENT n_delay
              GENERIC (n : positive := 10);
              PORT (   n_del_in : IN  std_logic;
                       n_del_out : OUT std_logic);
    end COMPONENT;

    COMPONENT delay
              PORT (   del_in : IN  std_logic;
                       del_out : OUT std_logic);
    end COMPONENT;

    CONSTANT delayTime: time;
end delayPack;

package body delayPack is
    CONSTANT delayTime : time := 1 ns;
end delayPack;
```

Entity

```
ENTITY n_delay IS
GENERIC (n : positive := 10);
   PORT (n_del_in :      IN    std_logic;
         n_del_out :     OUT   std_logic);
END n_delay;
```

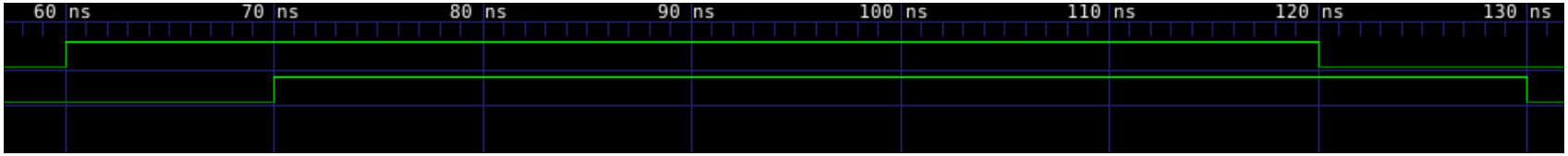
Architektur: Funktionale Simulation

```
ARCHITECTURE timesim OF n_delay IS

SIGNAL intsig_delay : std_logic_vector(
    n DOWNTO 0);

begin
    gen_delays:
     FOR i IN (n) DOWNTO 1 GENERATE
    delay_instance: delay
      PORT MAP (
          del_in => intsig_delay(i),
          del_out => intsig_delay(i-1)
          );
    end generate gen_delays;
    intsig_delay(n) <= n_del_in;
    n_del_out <= intsig_delay(0);
end timesim;
```

Architektur: Funktionale Simulation

```
ENTITY delay IS
    PORT (   del_in  : IN  std_logic;
             del_out : OUT std_logic);
end delay;

ARCHITECTURE arch OF delay IS
begin
    del_out <= del_in AFTER delayTime;
END arch;
```

Testbench




```
ARCHITECTURE arch of func_tb is
SIGNAL in_sig, out_sig : std_logic;

BEGIN
  delay_instance : n_delay
    PORT MAP (in_sig, out_sig);

    in_sig <= '0',
              '1' after 60 ns,
              '0' after 120 ns;
END arch;
```

Synthetisierbare Architektur

Problem!

- Verzögerung mit `after` wird wegoptimiert!

Idee!

- Verwende anstatt dem für die funktionale Simulation erstellten `delay` eine Lookup-Table (LUT).
- Wähle die Funktion `Buffer`, welche nach kurzer Verzögerung das Eingabe - Signal weiterleitet.

Synthetisierbare Architektur

Es funktioniert!

- Verzögerung wird nicht mehr optimiert.

Aber!

- Jeder Synthetisierungsvorgang erzeugt andere Verzögerungszeiten! $\rightarrow$ PFUI!
- Die Platzierung der Lookup-Tables auf dem Board ist nicht deterministisch.
- Unterschiede in der Länge der Verbindungsleitungen erzeugen unterschiedliche Verzögerungszeiten.

Lösung!

- Relative Location Constraints (`RLOC`)!
- Erzwinge relative Lage der Komponenten.

Synthetisierbare Architektur

```
ARCHITECTURE deterministic OF n_delay IS

SIGNAL intsig_delay : std_logic_vector(
    n DOWNTO 0);
ATTRIBUTE RLOC : string;

ATTRIBUTE syn_hier : string;
ATTRIBUTE syn_hier OF deterministic :
    ARCHITECTURE IS "hard";

ATTRIBUTE xc_use_xmodule: boolean;
ATTRIBUTE xc_use_keep_hierarchy OF deterministic :
    ARCHITECTURE IS true;
```

Synthetisierbare Architektur

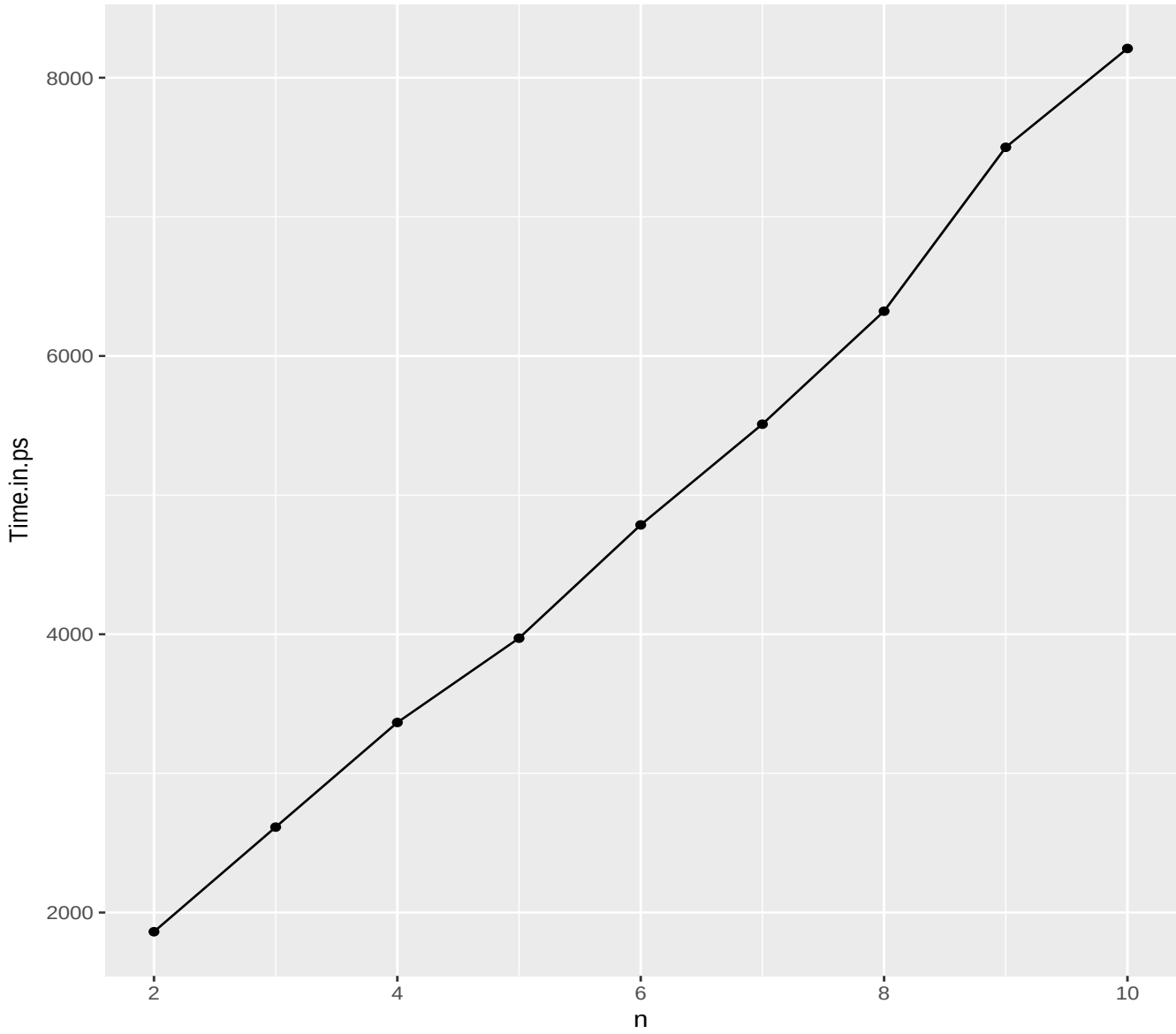
```
BEGIN n_delay:
FOR i IN (n) DOWNTO 1 GENERATE
  CONSTANT param : natural :=
      ((n-i)) mod 2;
  CONSTANT row : natural  :=
      ((n-i)/4) mod 2;
  CONSTANT column : natural :=
      (n-i)/4 + (param - row);
  CONSTANT rloc_str : string :=
      "X" & itoa(row) & "Y" & itoa(column);

  ATTRIBUTE RLOC of lut_instance :
      LABEL IS rloc_str;
```

rloc_str: X0Y0,X0Y1,X0Y0,X0Y1,X1Y0,X1Y1,...

Synthetisierbare Architektur

```
BEGIN

  lut_instance: LUT1
    GENERIC MAP (
      INIT => "0000000000000010"
      )   -- Buffer 10

    PORT MAP (
      O  => intsig_delay(i),
      I0 => intsig_delay(i-1)
      );

END GENERATE;
intsig_delay(0) <= n_del_in;
n_del_out <= intsig_delay(n);
END deterministic;
```

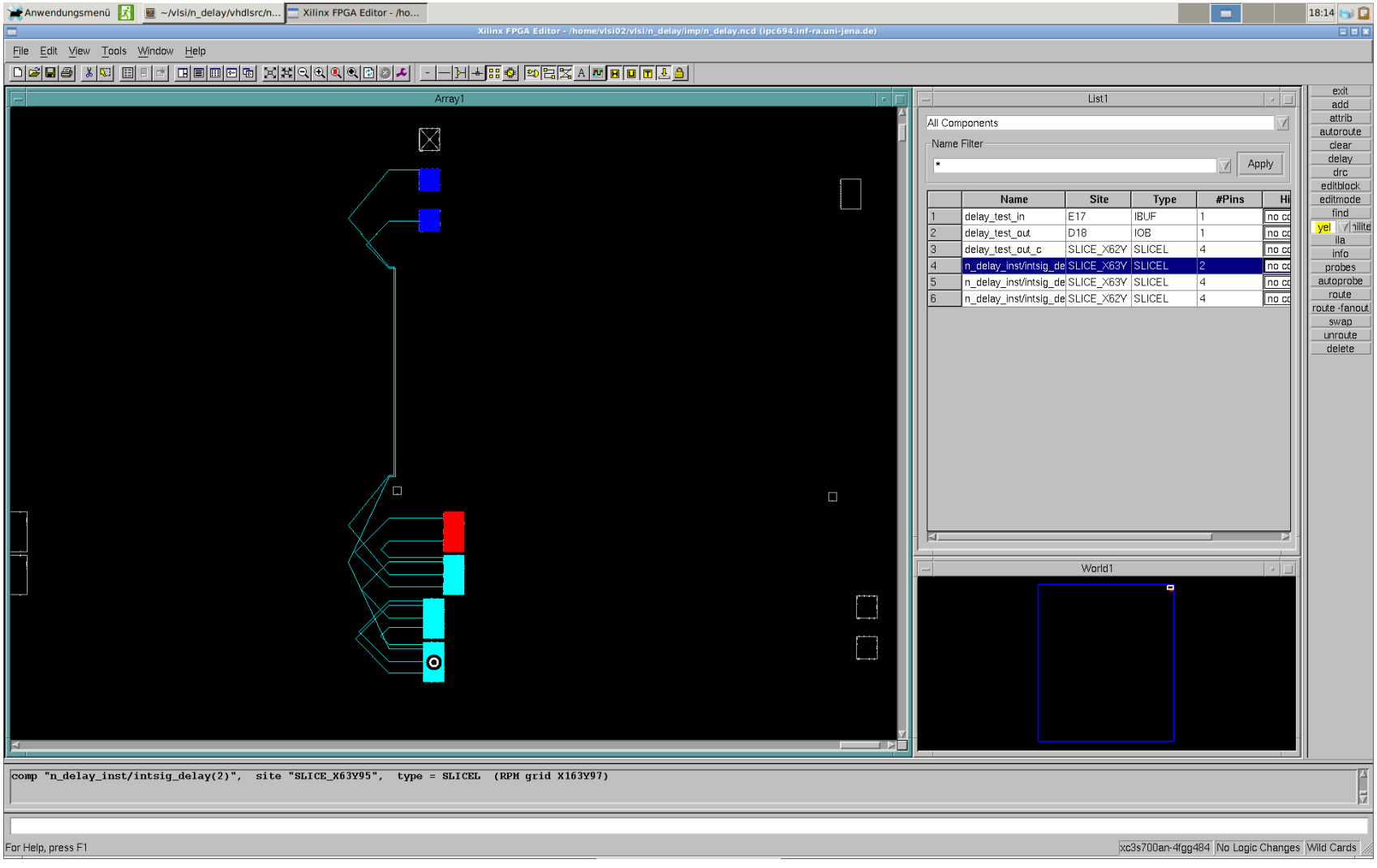
Timing - Simulation



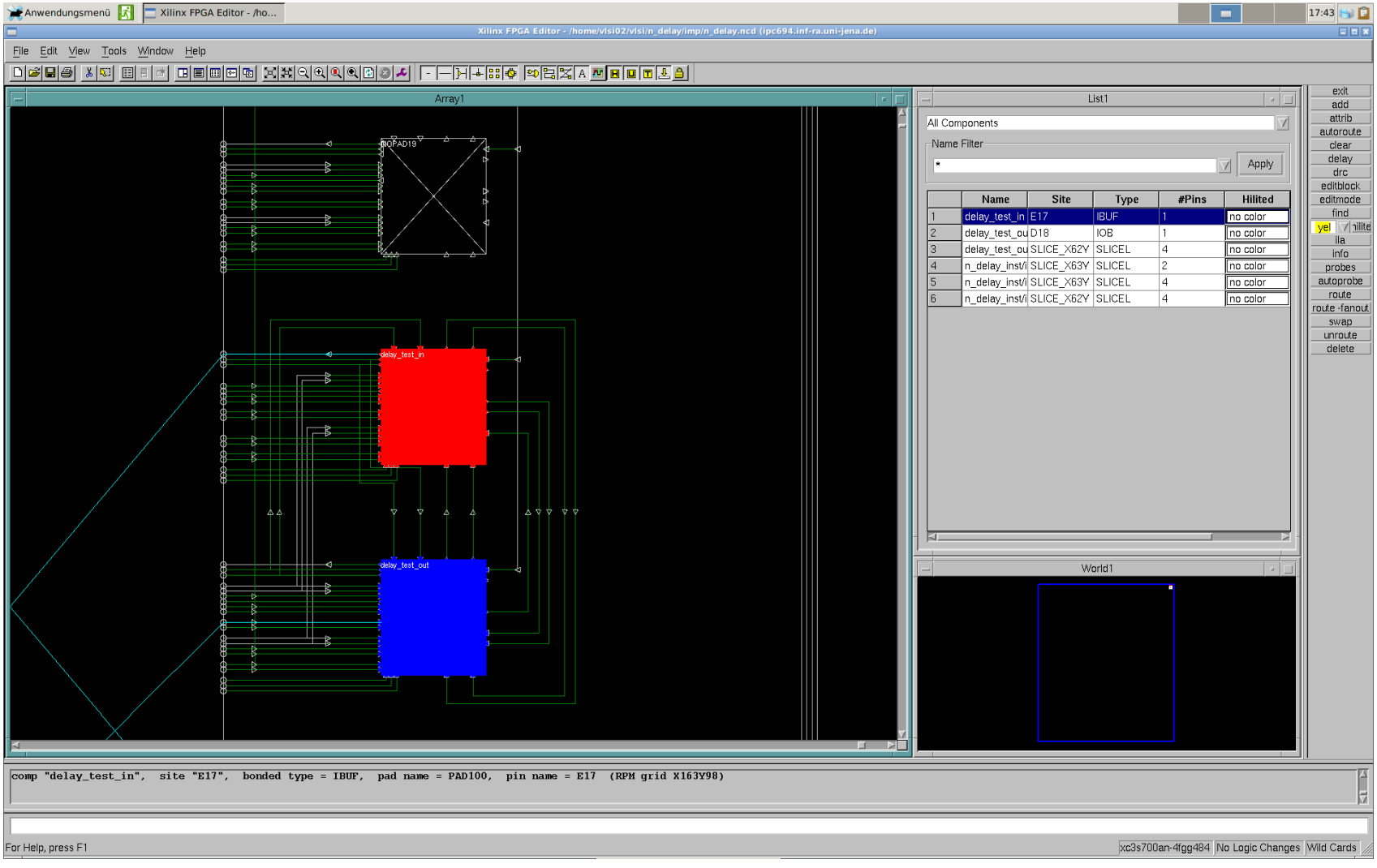
FPGA-Editor

1. Manuelles Platzieren und Verbinden von Elementen
2. Sondieren von internen Zuständen an beliebigen Stellen der Schaltung
3. Downloaden von generierten Bit-Dateien auf das Gerät
4. Kompletter Designvorgang von Hand möglich.

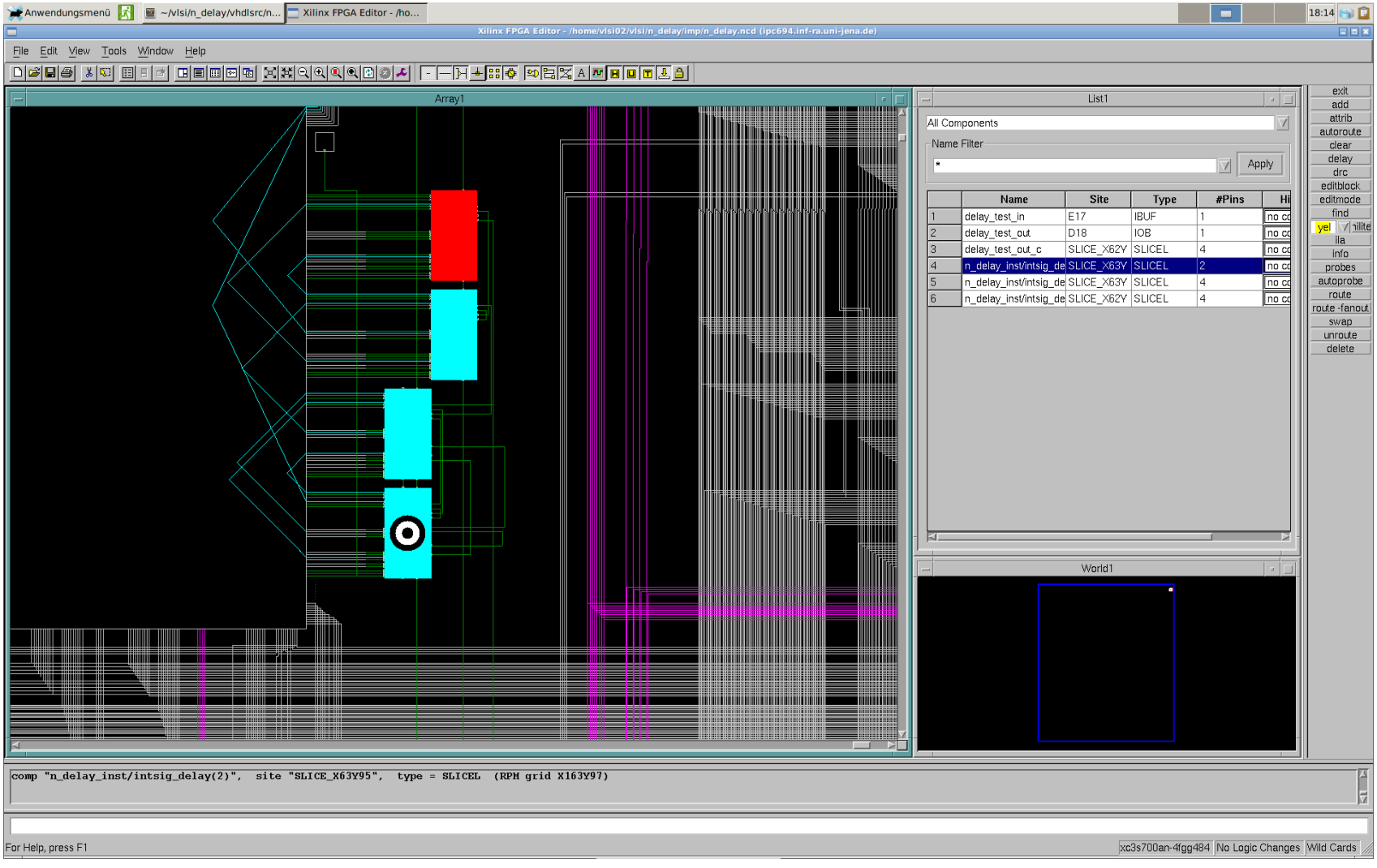
FPGA-Editor


Anwendungsmenü
~/vlsi/n_delay/vhdlsrc/n...
Xilinx FPGA Editor - /ho...
18:14
Xilinx FPGA Editor - /home/vlsi02/vlsi/n_delay/imp/n_delay.ncd (ipc694.inf-ra.uni-jena.de)
File Edit View Tools Window Help
Array1
List1
All Components
Name Filter
*
Apply
Name Site Type #Pins
1 delay_test_in E17 IBUF 1
2 delay_test_out D18 IOB 1
3 delay_test_out_c SLICE_X62Y SLICEL 4
4 n_delay_inst/intsig_de SLICE_X63Y SLICEL 2
5 n_delay_inst/intsig_de SLICE_X63Y SLICEL 4
6 n_delay_inst/intsig_de SLICE_X62Y SLICEL 4
exit
add
attrib
autoroute
clear
delay
drc
editblock
editmode
find
ila
info
probes
autoprobe
route
route -fanout
swap
unroute
delete
World1
comp "n_delay_inst/intsig_delay(2)", site "SLICE_X63Y95", type = SLICEL (RPM grid X163Y97)
For Help, press F1
xc3s700an-4fgg484
No Logic Changes
Wild Cards

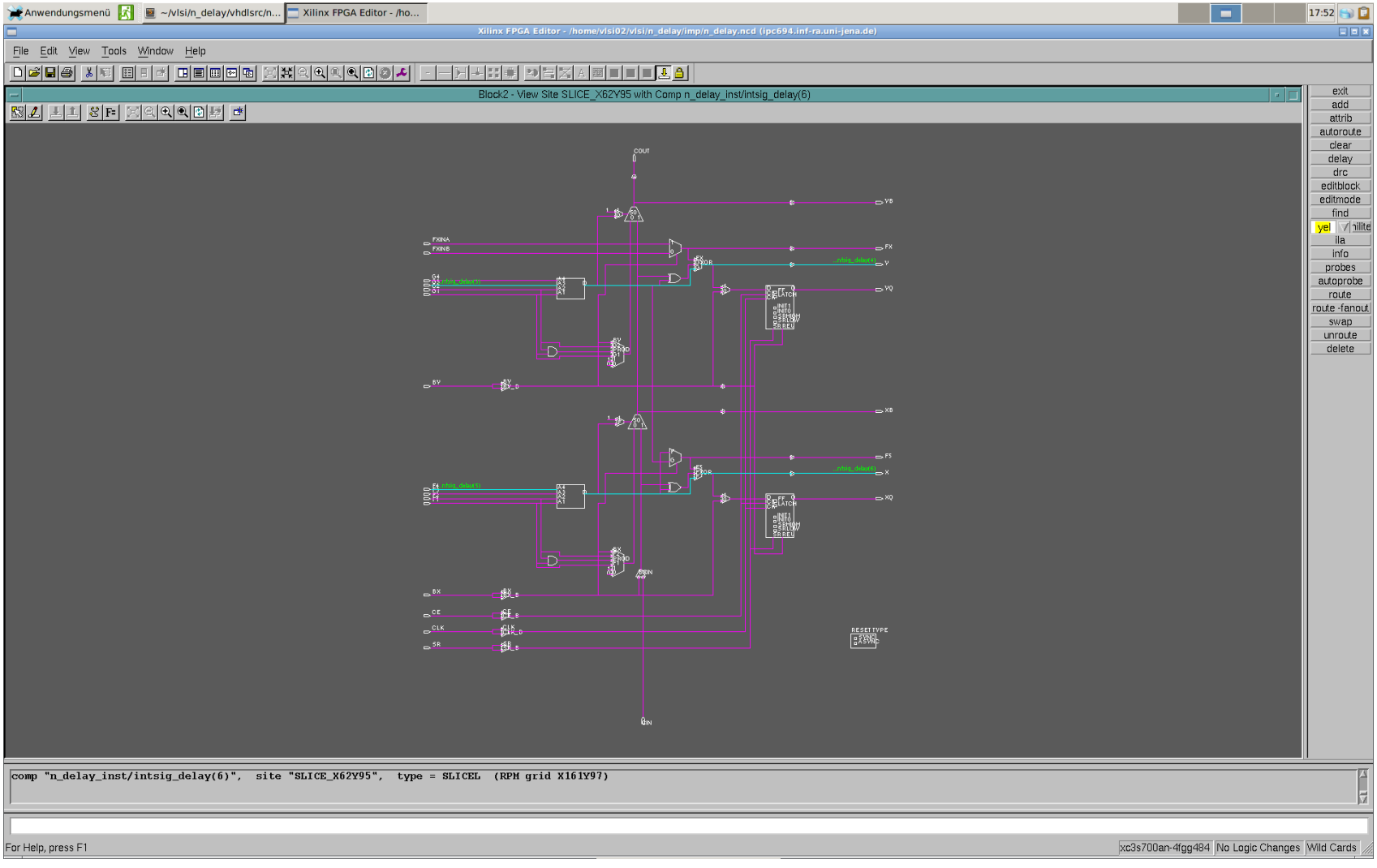
FPGA-Editor


Anwendungsmenü
Xilinx FPGA Editor - /ho...
17:43
Xilinx FPGA Editor - /home/vlsi02/vlsi/n_delay/imp/n_delay.ncd (ipc694.inf-ra.uni-jena.de)
File Edit View Tools Window Help
Array1
IOPAD19
delay_test_in
delay_test_out
List1
All Components
Name Filter
*
Apply
Name Site Type #Pins Hilited
1 delay_test_in E17 IBUF 1 no color
2 delay_test_ou D18 IOB 1 no color
3 delay_test_ou SLICE_X62Y SLICEL 4 no color
4 n_delay_inst/i SLICE_X63Y SLICEL 2 no color
5 n_delay_inst/i SLICE_X63Y SLICEL 4 no color
6 n_delay_inst/i SLICE_X62Y SLICEL 4 no color
World1
exit
add
attrib
autoroute
clear
delay
drc
editblock
editmode
find
yel
lla
info
probes
autoprobe
route
route -fanout
swap
unroute
delete
comp "delay_test_in", site "E17", bonded type = IBUF, pad name = PAD100, pin name = E17 (RPM grid X163Y98)
For Help, press F1
xc3s700an-4fgg484
No Logic Changes
Wild Cards

FPGA-Editor


Anwendungsmenü
~/vlsi/n_delay/vhdlsrc/n...
Xilinx FPGA Editor - /ho...
18:14
Xilinx FPGA Editor - /home/vlsi02/vlsi/n_delay/imp/n_delay.ncd (ipc694.inf-ra.uni-jena.de)
File Edit View Tools Window Help
Array1
List1
All Components
Name Filter
*
Apply
Name Site Type #Pins
1 delay_test_in E17 IBUF 1
2 delay_test_out D18 IOB 1
3 delay_test_out_c SLICE_X62Y SLICEL 4
4 n_delay_inst/intsig_de SLICE_X63Y SLICEL 2
5 n_delay_inst/intsig_de SLICE_X63Y SLICEL 4
6 n_delay_inst/intsig_de SLICE_X62Y SLICEL 4
World1
exit
add
attrib
autoroute
clear
delay
drc
editblock
editmode
find
ila
info
probes
autoprobe
route
route -fanout
swap
unroute
delete
comp "n_delay_inst/intsig_delay(2)", site "SLICE_X63Y95", type = SLICEL (RPM grid X163Y97)
For Help, press F1
xc3s700an-4fgg484
No Logic Changes
Wild Cards

FPGA-Editor


Anwendungsmenü
~/vlsi/n_delay/vhdlsrc/n...
Xilinx FPGA Editor - /ho...
17:52
Xilinx FPGA Editor - /home/vlsi02/vlsi/n_delay/imp/n_delay.ncd (ipc694.inf-ra.uni-jena.de)
File Edit View Tools Window Help
Block2 - View Site SLICE_X62Y95 with Comp n_delay_inst/intsig_delay(6)
exit
add
attrib
autoroute
clear
delay
drc
editblock
editmode
find
ila
info
probes
autoprobe
route
route -fanout
swap
unroute
delete
COUT
FXINA
FXINB
BY
BX
CE
CLK
SR
YB
FX
YQ
XB
F5
X
XQ
RESETTYPE
comp "n_delay_inst/intsig_delay(6)", site "SLICE_X62Y95", type = SLICEL (RPM grid X161Y97)
For Help, press F1
xc3s700an-4fgg484
No Logic Changes
Wild Cards