Table 1: Power consumption and area usage for fastest achieved designs for respective architectures

Design	Clock Freq (Mhz)	Area (mm^2)	Area (Eqv. NAND2)	Power (mW)
BRISC	35.71	17.05	26641.75	37.4
Cached RISC-V	35.71	36.81	57520.75	63.1
SERV	52.63	1.519	2373.5	9.61

Table 2: Cell type distribution for respective architectures

Architecture	**Type**	**Instances**	**Area (Equivalent NAND2)**	**Area (%)**
BRISC	sequential	1472	6,359,040	37.3
	inverter	1988	637,760	3.7
	buffer	386	248,480	1.5
	logic	11,851	9,805,440	57.5
	physical_cells	0	0	0.0
Cached RISC-V	sequential	4083	19,305,280	52.4
	inverter	2508	808,640	2.2
	buffer	269	178,720	0.5
	logic	20,766	16,520,640	44.9
	physical_cells	0	0	0.0
SERV	sequential	182	786,240	51.8
	inverter	172	55,040	3.6
	buffer	92	58,880	3.9
	logic	697	618,880	40.7
	physical_cells	0	0	0.0

Table 3: Critical path of respective architectures shown in ps

Architecture	Period	clk-2-Q	Comb. Delay	Setup	Uncert.	Slack	Total
BRISC	28000	2814	23147	1738	300	1	25961
Cached RISC-V	28000	2620	23805	1275	300	0	26425
SERV	19000	2626	14756	1267	300	51	17382