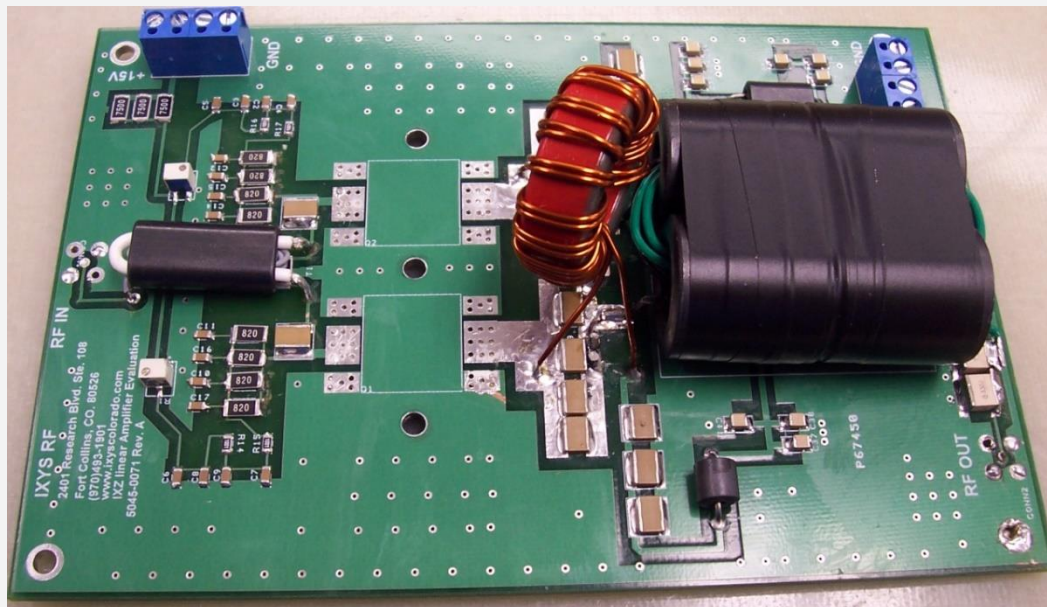


**Reference Design for
13.56 MHz Push-Pull
600 W RF Amplifier
IXZ318N50L**



*Martin Jones
R&D/Application Engineering*

Introduction

The following is an evaluation circuit for the IXZ318N50L Ultra Fast RF MOSFET in a class AB topology producing 600 watts CW at a frequency of 13.56 MHz. These devices are available in our low-inductance RF package. The efficiency is $\geq 70\%$ at 600 W output into a $50\ \Omega$ load with a minimum power gain of 23 dB as seen in Table 1 and Chart 1. This reference design and application note is designed for component evaluation, a demonstration of the functionality of IXYSRF MOSFETs, for industrial, commercial, and scientific RF amplifier applications.

This reference design will demonstrate the advantages of using the IXZ318N50L in the DE series surface mount plastic package. This component is designed to operate at high drain voltages depending on the output load and class of operation. Operating at high drain voltages requires less DC current and a less complicated output matching circuit. DE series components have a thermal resistance that matches or exceeds that of standard RF ceramic and BeO packages, and have a lower profile.

These components provide many advantages, such as having a simple output matching to the load, less DC current, higher gain, lower component count, and lower thermal resistance. This circuit provides a starting point for high power applications in the ISM band and HF RF communications. The economical advantage of these components is second to none with a cost of $\leq \$0.14$ per watt.

Power Input W	Power Out W	Power DC In W	Eff%	Gain dB
1.0	310	556	55.8	24.91
1.3	400	625	64.0	24.88
2.0	500	716	69.8	23.98
2.9	600	800	75.0	23.16
4.3	650	850	76.4	21.79

Table 1

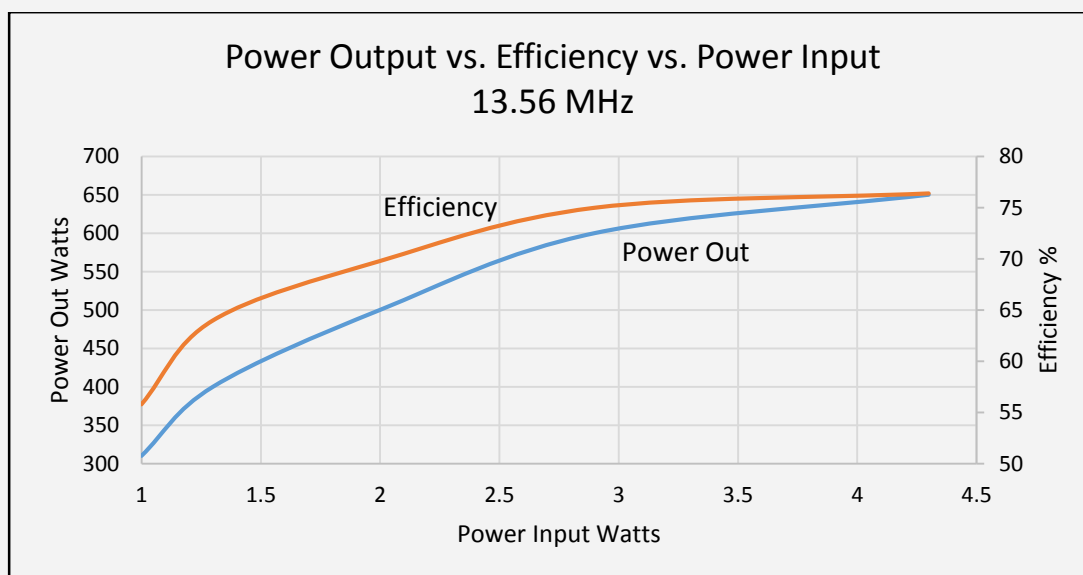


Chart 1

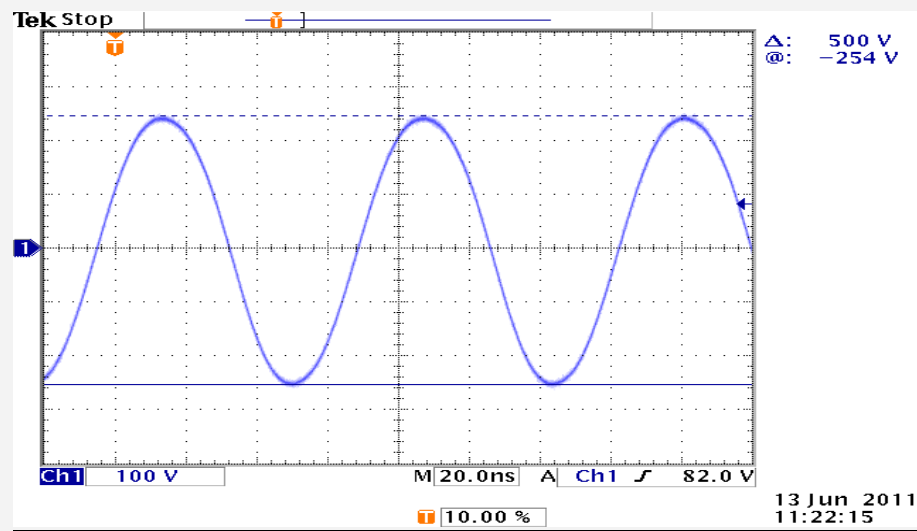


Fig. 2 13.56 MHz 600 W into a 50 Ω Load

DE-Series Package

“The DE-Series Fast Power™ MOSFETs are a class of unique, high-power devices designed from the ground up as a circuit element for high-speed, high-frequency, and high-power applications. DEI's Fast Power™ technology features low insertion inductance (≤ 1.5 nH) and a low-profile, low-cost plastic package with a $R_{\theta JC}$ as low as 0.10°C/W, which provides exceptional switching speeds and power handling capabilities.”^[3]

“For high power applications, the DE-SERIES incorporates several design features that provide excellent thermal dissipation and high power handling capability while offering a less cumbersome mounting technique than conventional devices. By minimizing layer thickness, and selecting materials with a low thermal impedance with a TCE near silicon, a multi-layer configuration is assembled that not only provides low thermal impedance and low die stress but also allows for electrically-isolated elements (gate, drain and source).”^[3]

Support

The following support documentation is available:

- Bill of materials
- Schematic
- Gerber files
- Test procedure
- Proper mounting procedures^[4]

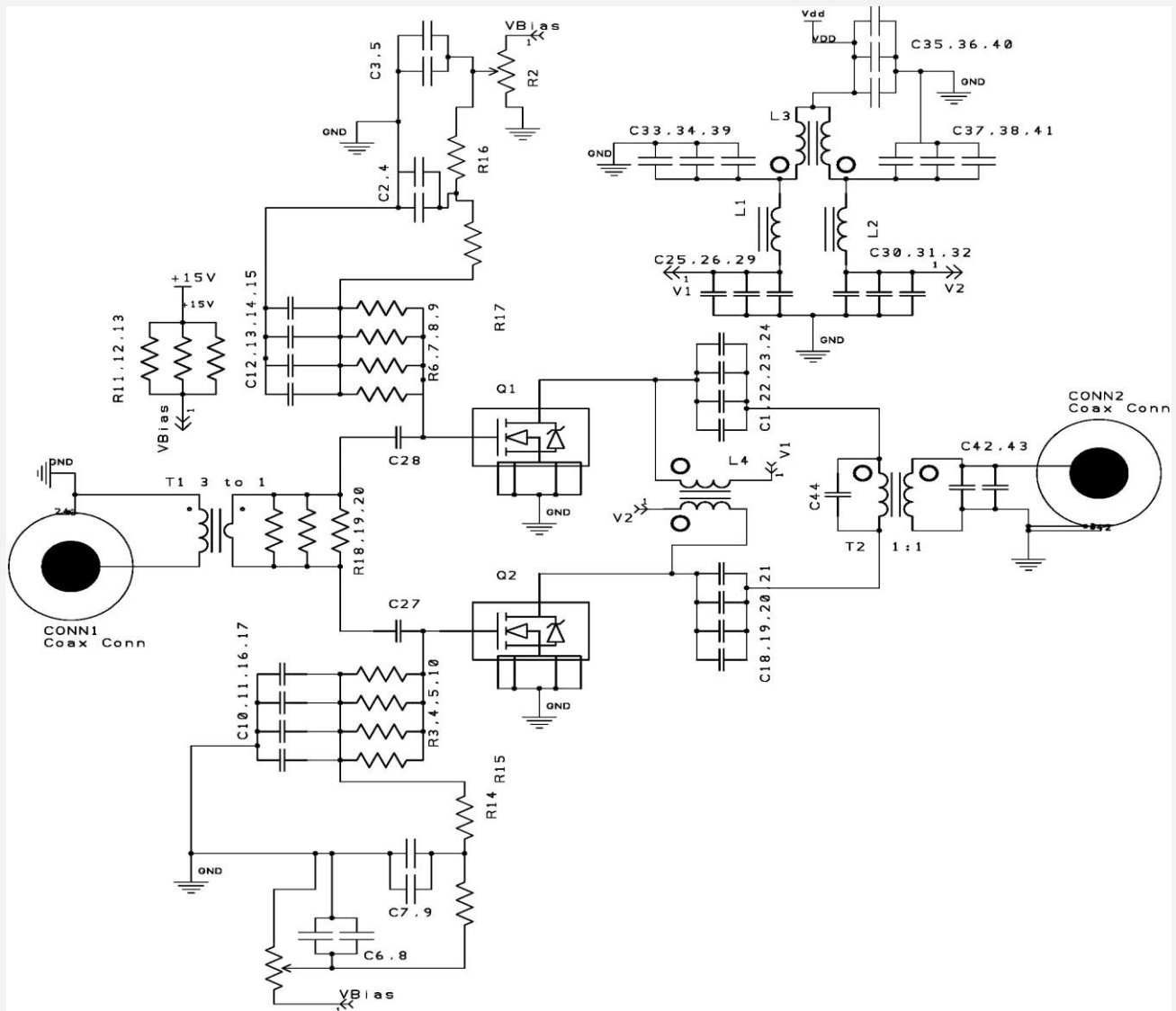
Testing was performed at IXYSRF with a Wakefield Thermal Solutions XX6274 heat sink and an air flow of 120 CFM across the fins. This heat sink has a ϕ_{sa} of 0.80 °C / W / 3". Gerber files are provided for those who wish to arrange for PCB fabrication.

The basic equipment needed to properly test this application is listed below. The equipment that was used at IXYSRF is listed later in this paper.

- RF signal generator (12 MHz to 15 MHz)
- RF power meters capable of measuring both forward and reflected power
- 50 Ω RF power load capable of handling a minimum of 1000 W
- 15 V DC power supply for bias voltage
- 150 V 12 A adjustable DC power supply for the drain voltage
- Voltmeter
- 100 MHz Oscilloscope

Description

The following schematic shown in figure 1 is a Class AB amplifier topology, which is defined as having a conduction angle that is greater than 180° but less than 360° . In other words, DC bias and drive level are adjusted so device output current flows during appreciably more than half the drive cycle but less than the whole drive cycle. This is done by setting V_{GS} to a value greater than $V_{GS(th)}$. Efficiency is much better than Class A, typically reaching 50-65% or greater at maximum output power levels, with a theoretical maximum of 78.5% in an ideal situation. Figure 1 shows the amplifier circuit at 13.56 MHz.



Design

As stated in the description this amplifier operates at 13.56 MHz with a bandwidth of 2 MHz. Having such a large input capacitance, the MOSFETs have a large swing of input impedance at these frequencies. The input impedance (Z) ranges from approximately 39.9 Ω at 2 MHz to 2.7 Ω at 30 MHz. These values can be measured using a Vector Network Analyzer. This option can be time consuming and complicated. A simpler method can be used to get these values. Since the input capacitance is very large with respect to the gate inductance and resistance, $X_{C_{ISS}}$ can be used as the approximate input impedance. The C_{ISS} for the components used is approximately 2000 pF with 125 V drain bias. This now results an approximate input impedance of 5.87 Ω . In order to accomplish a good match to keep the SWR on the input to a minimum, the input impedance to the gates of the MOSFETs must be kept relatively constant.

The first thing to be determined is the ratio of the input impedance transformer. This transformer will need to take our 50 Ω input and transform it to the 5.87 Ω impedance of our component's gate. To do this we just divide 50 Ω by the Z_{IN} value. Now we have a value that would be a perfect impedance transform of 8.5 to 1. Since this type of transformer would be impractical and difficult to use we will need to choose a more practical value. The closest and more practical value is a 9:1 impedance transformer. The transformer is wound on binocular ferrite core #BN43-6802 from Amidon. The turns ratio is 3 turns of #26 insulated wire on the primary and 1 turn of copper braid on the secondary.

Now that our impedance transformer has been chosen, we need to stabilize the input impedance of the MOSFETs at 13.56 MHz to a value that would be close to a 9:1 impedance transformation to 50 Ω . The ideal value would be 5.55 Ω . We will need to place a shunt resistance across each MOSFET gate to source, to decrease the effective input impedance the transformer will see. To achieve a 2:1 SWR or less the effective input Z needs to have a value between 3 Ω to 8 Ω across the entire bandwidth. The value of the total shunt resistance then would need to be 17 Ω across each gate for the best results. This value was derived from the value of resistance that would be needed at the frequency of interest to be used. The formula used to determine this is:

$$R = \frac{X_{ciss} * Z_{in}}{\sqrt{X_{ciss}^2 - Z_{in}^2}}$$

Formula 1_[1]

$X_{C_{ISS}}$ is the input capacitive reactance, Z_{IN} is the desired input impedance, and R is the shunt resistance

This formula is derived from the following formula for calculating impedance from resistance and reactance in parallel.

$$Z = (R * X) / (\sqrt{R^2 + X^2})$$

Formula 2_[1]

The value can be changed depending on where the frequency is set as long as the $X_{C_{ISS}}$ remains greater than 5.55 Ω or the input impedance transformer will need to be changed. These resistors are marked R3 through R10 on the schematic with a generic value of 82 Ω . The resistors across the secondary of the transformer are 150 Ω each given a total resistance of 50 Ω . The purpose of this resistance is to provide balance and stability to the secondary winding.

Now that the input of the amplifier is completed, we need to focus on the output. The first item is to determine the proper load impedance for the amplifier. This is done by using the following formula 3.

$$R_L = \frac{(0.85 * V_{dd})^2}{2 * P_{out}}$$

Formula 3_[1, 2]

This amplifier will be designed to operate at 125 V on the drain with 600 W CW output power. The P_{out} is the power out of a single MOSFET which in this case is 300 W. When we use these values in the R_L formula the results are 26 Ω for each MOSFET. Since in a push-pull configuration this R_L is in series, we now have 52 Ω for our output load resistance. The output matching section is now straight forward; a 1:1 impedance transformer will be the best choice needed to match the 52 Ω to the 50 Ω output load. This transformer is wound on four 2643102002 cores with 4 windings of #18 AWG magnet wire on the primary and 4 windings of #18 AWG magnet wire for the secondary.

To properly supply the drains of the MOSFETs and to isolate the supply voltage from the RF voltage an RF choke inductor must be added. In the schematic shown for this amplifier this is labeled T2. The choke is wound on a single toroidal core T-130-2 from Amidon with 15 turns each of #18 AWG magnet wire. In this amplifier we have wound both chokes on a single core to save space and component count. Note, however, that the two windings on T2 are wound opposite from each other to cancel the flux in the core and therefore prevent heating and component failure.

Operating Conditions:

NOTE: MOSFET packages must be properly heat sunk. Water cooled is preferred but a heat sink with a very low thermal resistance and forced air cooled will be adequate for intermittent use.

Topology- Class AB

Supply voltage- $V_{dd} = 125 \text{ V} \pm 5 \text{ V}$ (this is also the drain to source voltage V_{ds})

Quiescent Idle current- $I_{dq} = 200 \text{ mA} \pm 10 \text{ mA}$ after warm up

Input power requirements- 1.0 W to 5 W depending on desired output power

Output Load - 50 $\Omega \pm 2 \text{ } \Omega$ capable of dissipating 1000 W

Equipment used at IXYSRF for testing-

Rohde & Schwarz model SML01 9 KHz to 1.1 GHz signal generator

ENI model 5100L-NMR RF power amplifier used at input for drive power

Bird model 4421 RF power meter with model 4024 power sensor to measure input power

Bird 43 RF power meter with 2 MHz to 30 MHz 1000 W slug to measure output power

Xantrex XFR150-18 DC power supply, 0-150 V 0-18 A

Bird Termaline Coaxial Resistor 1500 W 50 Ω

Agilent Model 54641A Oscilloscope

Vizatek DC power supply used as bias supply

Fluke 87V DMM digital voltmeter

Operation Instructions:

1. Insure the circuit board is mounted to a water cooled cold plate or a heat sink with a small thermal impedance that is capable of dissipating 500 W of power with forced air.
2. Check 50 Ω RF load resistor. Ensure that the load is capable of dissipating 1000 W and measures 50 Ω $\pm 5\%$.
3. Connect power supply and set to 15 V to the **Vbias** input connectors.
4. Connect power supply and set to 100 V to the **Vdrain** connectors. **Supply should be rated at 150 V 8 A minimum.**
5. Connect a 20 W (minimum) power meter that is capable of measuring both forward and reflected power to the RF input. The RF input connector is labeled and is centered at one end of board. Connect a 1000 W (minimum) power meter that is capable of measuring both forward and reflected power to the RF output. The RF output connector is labeled and positioned at one corner of board.
6. Connect the 50 Ω 1000 W RF load to the output of the 1000 W power meter.
7. Connect an adjustable 2 MHz to 30 MHz low power RF amplifier to the input of the 20 W power meter. Input drive power was produced by the ENI model 5100L amplifier and driven by the Rohde & Schwarz signal generator set to 13.56 MHz at IXYSRF.
8. Turn on Vbias, measure and note the voltage on each gate of the MOSFETs. This voltage was preset at IXYSRF during testing.
9. Turn off Vbias.
10. Ensure the evaluation board is adequately heat sunk.
11. Turn on the Vdrain supply and ensure the voltage is 125 V.
12. Turn on Vbias and monitor the 125 V supply (drain) current. This current should be 200 mA. If the Idrain is too low or high adjust the Vgs at R1 and R2 equally to ensure the Idrain on both MOSFETs remains equal.
If the drain current continues to rise the component is not adequately heat sunk.
13. Adjust signal generator at the input of driving RF amp for the desired frequency and 2 W of drive power.
14. Apply the RF signal at the input and adjust input power level until desired output power is achieved.
15. To calculate the efficiency use this formula where $(P_{out} / P_{in}) * 100 = \text{efficiency in \%}$, **$P_{in} = V_{drain} * I_{drain}$.**
16. To calculate gain = $10 * \log_{10}(RF P_{out} / RF P_{in})$, **$RF P_{in} = RF \text{ input forward power} - RF \text{ input reflected power}$.**
17. To power down, turn off RF signal generator, 125 V drain supply voltage, and bias voltage.

Conclusion

The preceding evaluation circuit demonstrates the advantages the IXYSRF components have with a higher operating voltage with a very simple design. These advantages are simple output matching to the load, less DC current, higher gain, lower component count, and lower thermal resistance. This circuit is a starting point for applications in the ISM band and HF RF communications. The economical advantage of these components is second to none with a cost of $\leq \$0.14$ per watt.

Bill of Materials

Item	Qty	Reference	Part	Vendor	Vendor Part #
1	16	C2 thru C17	0.1 μ f 50 V X7R	Kemet	C1206C104K5RACTU
2	16	C1, C18 thru C32	0.056 μ F 1 KV X7R	Vishay/Vitramon	VJ1825Y563KXGAT
3	9	C33 thru C41	0.1 μ F 500 V X7R	SYFER	1210Y5000104KXT
4	1	C42	68 pF	ATC	ATC700C680JTN2500X
5	1	C44	100 pF	ATC	ATC700C101JTN2500X
6	1	C43	33 pF	ATC	ATC700C330JTN2500X
7	2	CONN1, 2	BNC Jack, Right Angle PCB	Tyco Electronics	5413631-1
8	2	CONN3, 4	4 pos. Terminal Block (Not Loaded)	ON-Shore Technology	OSTTA04161
9	2	L1, L2	Ferrite bead	Fair-Rite	26430008010
10	2	Q1,Q2	IXZ318N50L MOSFET	IXYSRF	IXZ318N50L
11	2	R1, R2	10 K Ω 11 turn	Bourns	3224W-1-103E
12	8	R3 thru R10	82 Ω 1W 2512	Panasonic-ECG	ERJ-1TNF82R0U
13	3	R11, R12, R13	750 Ω 1W 2512	Panasonic-ECG	ERJ-1TNF7500U
14	4	R14 thru R17	1 K Ω 1/4W 1206	Panasonic-ECG	ERJ-8ENF1001V
15	3	R18, R19, R20	150 Ω 1W 2512	Panasonic-ECG	ERJ-1TYJ151U
16	1	T1	3:1 Transformer on BN43-6802 Core Primary 3 turns #24AWG, Secondary 1 Turn copper braid	Amidon	BN-43-6802
17	1	T2	15 turns Bifilar #18 AWG on T106-2 Toriod	Amidon	T130-2
18	1	T3	1:1 600 Ω 4 Turns of #18AWG on Four Fair-Rite 2643102002 Cores	Amidon	2643102002
19	1	PCB	5045-0071	IXYSRF	

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