**架構圖 test bench**

**Signal**

**(6-bits)**

**Testbench**

**Output**

**(32bits)**

**clk**

**DataB**

**(32-bits)**

**DataA**

**(32-bits)**

**ALU Control**

**Shifter**

**HI**

**LO**

**Multiplier**

**M**

**U**

**X**

**ALU**

**FULL ADDER(FA)**

SUM

A

A

B

Cin

COUT

Signal

Ci

**1bit ALU**

0 MUX

1

2

3

control

Ci

Ai

FA Si

Bi

Ci+1

Ai

Bi

Lessi

Ci+1 Set(MSB only)

**32bit ALU**

Signal

SUM1 SUM0

control

SUM31

A0 B0

A0 B0

0 A1 B1

0 A1 B1

0 A31 B31

0 A31 B31

LESS Ai Bi

Ci+1 Ci

SEL

control

ALU0

SUMi

LESS Ai Bi

Ci+1 Ci

SEL

control

ALU1

SUMi

LESS Ai Bi

Ci+1 Ci

SEL

control

ALU31

SUMi

**MUX**

ALU 0 MUX

HI 1

LO 2

Shifter 3

Output

**乘法器**

被乘數MCND(64bits)

左移

乘數MPY(32bits)



LSB 右移

CONTROL

WRITE

PRODUCT(64bits)

**移位器**

A0

A31 A30 A29 A28 A3 A2 A1

0

補16個0

補8個0

S4

S3

S2

S1

S0

0

0

0

0

0

0

0

0

0

0

0

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