IP Generation

This task generates a Vivado IP from the produced HLS output.

The VivadoHLS Script Template

```
# Create project
open_project -reset PRJ_NAME
set_top TOP_LEVEL_FUNCTION

# Add design files
add_files BIN_DIR/HLS_SOURCE_FILE -cflags "-I CLOCKWORK_SRC_DIR -std=c++11"

# Open and configure a new solution
open_solution PRJ_NAME
set_part PART_NUMBER
create_clock -period CLOCK_PERIOD -name default

# Configure build
config_schedule -effort medium -relax_ii_for_timing=0
config_export \
  -format ip_catalog \
  -rtl verilog \
  -description IP_DESCRIPTION \
  -display_name IP_DISPLAY_NAME
  -ipname IP_NAME \
  -library IP_LIBRARY \
  -vendor IP_VENDOR \
  -version IP_VERSION

# Synthesize design (generate HDL)
csynth_design

# Export IP
export_design
```

Automation Script Interface

The automation script should be able to accept a configuration file that provides all the necessary

information.

The configuration file is a JSON file of the form:

```
{
  "config" : {
    "version"             : "config schema version in the form x.y",
    "name"                : "configuration name. Use as prefix for project name in Xi
    "xcel_ip_vlnv"        : "VLNV used for IP instantiation in Vivado",
    "xcel_top_fn"         : "top-level HLS function for IP",
    "xcel_clock_period"   : "implementation timing info for IP",
    "xcel_ip_inputs"      : [
      { "name" : "name of input port 0", "width" : W_IN_0 },
      { "name" : "name of input port 1", "width" : W_IN_1 },
      ...
      { "name" : "name of input port N", "width" : W_IN_N },
    ],
    "xcel_ip_output"      : { "name" : "name of output port", "width" : W_OUT },
    "xcel_rdai_vlnv"      : "VLNV used for RDAI tagging",
    "xlnx_chip_part"      : "part number for the FPGA chip",
    "xlnx_board_part"     : "board part number",
    "vivado_user_ip_repo" : "path to user IP repo",
    "vivado_version"      : "some_version",
    "vivado_handoff_dir"  : "path for directory where to put output collateral",
  }
}
```