## Microprocessor System Design Considerations

## SoC Technology Roadmap and Trend

1. A portable Audio/Video Media player is designed based on the specification given below.
    - Li-Polymer Battery.
    - Audio Playtime 24hr, Video Play-time 10hr, Voice Recording 10hr.
    - USB3 slave connectivity
    - Standby time 7 days.
    - 1920x1080 LCD with Capacitive Touch Screen (SPI interface)
    - 8 user input buttons
    - System wakeup from standby via any button and SPI activity within 10µs
    - Software
        - Main system overhead: 20MIPS (Million Instruction per second)
        - MP3 decoding: 15 MIPS
        - MP4 decoding: 50 MIPS
        - Voice recording: 5 MIPS
        - Total program code size: 240KByte
        - Total program data size: 128Kbyte
        - Total data buffer size: 256MByte
    - Processor power consumption
        - System Overhead: 5mA/MIPS
        - Active (Audio/Voice functions): 5mA/MIPS
        - Active (Audio+Video functions): 10mA/MIPS
        - Standby: 3mA
    - Processor internal memory
        - 256 KByte SRAM, 512 KByte Flash

    (a) What external storage and system memory is suitable for this product? Or are they required?
    - Program Code of 240Kbyte < 512 KByte Flash
    - Program Data of 128Kbyte < 256 KByte RAM
    - => all can fit into the internal memory of the processor
    - 256Mbyte data buffer needs to be resided in external SDRAM, volatile memory chosen since large amount read/write operations is expected.
    - External NAND Flash used for storing Audio/Video media files. ‘Portable’ points to need for small form factor, hence NAND flash chosen for its size as well as cost/bit advantage.

(b) Does the processor require any special internal peripheral to interface to the memories listed above?

- SDRAM requires special controller logic to manage the various complex SDRAM commands/operation, and to enable code to be executed directly from there.
- NAND could use standard SRAM memory interface (with software drivers for NAND flash management) or a NAND Flash controller module.

(c) Calculate the power consumption when performing the following function and calculate the battery capacity required (in mAh) to meet the requirement specified. MP4 includes audio and video. Assume system overhead is the same for all activities. Ignore power consumed by other components on the player.

- Audio Decode
- 20*5 +15*5 = 175mA => 24*175 = 4200mAh
- MP4 Decode
- 20*5 + 50*10 = 600mA => 10*600 = 6000mAh
- Voice Record
- 20*5 +5*5 = 125mA => 10*125 = 1250mAh
- Standby (System Sleeping)
- 3mA*7*24 = 504mAh

Video recording require the most battery capacity. Hence a 6000mAh battery is required to meet the specifications.

(d) What could be done to reduce the battery capacity but still able to meet the various product function requirement?

- Put the processor to sleep whenever possible, e.g. after performing the audio/video decoding, voice recording/playback.

(e) What could be done if we want to increase the standby time?

- Reduce the standby power. E.g. Have a separate controller to manage the system during standby. Small MCU typically has smaller standby current, some can achieve down to uA standby.

(f) Audio codec typically requires a special clock frequency that is a multiple of the sampling frequency. Assuming that the sampling frequency, fs=44.1Khz, one of the common clock frequencies used is 256fs. How can this frequency be generated for this system? External Crystal used by the Processor has a frequency of 48Mhz.

- Not possible to generate multiples of 44.1Khz with a base frequency of 48Mhz. Will need an external clock generator or separate crystal/oscillator with frequency at multiple of 44.1Khz.

(g) Name one important reason why the processor needs a 48MHz crystal.

- USB controller needs a very accurate 48Mhz base clock transfer data over USB interface.

2. With reference to the information derived in Q1, some questions below

- Based on the very fast wakeup time requirement of 10µs, should a crystal be used during standby or an on-chip oscillator?
- What other points should be considered where pin connection and termination are concerned?

- The wakeup time when using external crystal should be tested to see if the 10us could be met. In general, crystal oscillation requires some time to stablise so an on-chip oscillator should be use or the external crystal oscillation shouldn't be shut down during standby (power consumption permit)
- Ensure all input pins are terminated to avoid excessive current drawn due to I/O pad's transistors being held at Vcc/2 level. Some pins have multiple functions mux'ed together, check that these functions are not used simultaneously.

3. Further to the system in Q1, what are the power supply design considerations given the following?
   - The processor selected has separate voltage rails for its core and I/O.
   - The system includes mixed signal components such as audio codec, video codec, ADC etc.
   - Any other additional power management considerations.
   - Check if there are any requirement on Processor Power supply sequencing, may need a separate power management IC.
   - Separate digital and analog voltage rails to isolate digital noise from the analog voltage supply. This will increase the accuracy of the ADCs and CODECs.
   - Apply Dynamic Voltage Frequency Scaling (DVFS), take note of the proper sequencing requirement of changing CPU frequency vs Core Voltage levels.

4. What is value proposition of the heterogeneous processing architecture that ARM proposed? How does ARM's big.LITTLE™ processor architecture managed to fulfill the these value proposition?

Value Proposition

- To use "just sufficient" resources to perform a particular function to achieve maximum power efficiency
- To be able to adapt dynamically and efficiently to changing application loading

"Just sufficient" resource deployment

- ARM big.LITTLE™ technology is a heterogeneous processing architecture which uses two types of processor core.
  - "LITTLE" processors are designed for maximum power efficiency
  - "big" processors are designed to provide maximum compute performance.
  - Processor vendor is allowed to mix and match different number of big and LITTLE cores to suit their targeted application's loading.
- When the application loading is light, the LITTLE processor will be used to save power. When the loading when beyond that of the LITTLE processor, the big processor will be switched in to carry the heavier load.

Dynamic and efficient adaption to application load

- One of the main issues with heterogeneous processing, or in fact, that of multi-processing are the data paths between processing cores. It is usually slower than the processor core speed so tends to be the bottleneck. Especially if one of the main features is to be able to dynamically move program around the system.
- ARM build a special interconnect known as the "Cache Coherent Interconnect" (CCI-400 ) enable the seamless data transfer between clusters, particularly between cache of each processors, without having to go through the relatively slower external memory
- Employment of Global Task Scheduling allows full flexibility to allocate a particular task to any available processor core.