

# EE4C10 Analog Circuit Design Fundamentals

## Homework Assignment I

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## Problem 1

For  $I_D = 40\mu A$ :

$$I_D = \frac{1.8V - V_D}{R}$$

$$V_D = 1.8V - I_D R$$

$$\underline{V_D} = 1.0V$$

Saturation region:

$$V_{GS} = 1.0V > V_{TH}$$

$$V_{GS} - V_{TH} = 0.4V < V_{DS}$$

1.  $\lambda = 0V^{-1}$

$$I_D = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$L = \frac{\mu_n C_{OX}}{2} \frac{W}{I_D} (V_{GS} - V_{TH})^2$$

$$\underline{L} = 0.39\mu m$$

2.  $\lambda = 0.06V^{-1}$

$$I_D = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

$$L = \frac{\mu_n C_{OX}}{2} \frac{W}{I_D} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

$$\underline{L} = 0.41\mu m$$

## Problem 2

1. Bulk of the transistors are connected to the source,  $V_B = V_S$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\varphi_F + V_{BS}} - \sqrt{|2\varphi_F|})$$

$$V_{TH} = V_{TH0} = 0.33V$$

(a) Transistor M<sub>1</sub>

$$V_{SG} = 2.5V - 1.7V = 0.8V$$

$$I_D = \frac{\mu_p C_{OX}}{2} \frac{W}{L} (V_{SG} - V_{TH})^2$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_1 = 2.72\mu m$$

(b) Transistor M<sub>2</sub>

$$V_{SG} = 1.7V - 1V = 0.7V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_2 = 4.38\mu m$$

(c) Transistor M<sub>3</sub>

$$V_{SG} = 1V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_3 = 1.37\mu m$$

2. Bulk terminals are attached to the V<sub>DD</sub>, V<sub>B</sub> = V<sub>DD</sub>.

(a) Transistor M<sub>1</sub>

$$V_{BS} = 2.5V - 2.5V = 0V$$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\varphi_F + V_{BS}} - \sqrt{|2\varphi_F|})$$

$$V_{TH} = V_{TH0} = 0.33V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_1 = 2.72\mu m$$

(b) Transistor M<sub>2</sub>

$$V_{BS} = 2.5V - 1.7V = 0.8V$$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\varphi_F + V_{BS}} - \sqrt{|2\varphi_F|})$$

$$V_{TH} = V_{TH0} = 0.43V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_2 = 8.23\mu m$$

(c) Transistor M<sub>3</sub>

$$V_{BS} = 2.5V - 1.0V = 1.5V$$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\varphi_F + V_{BS}} - \sqrt{|2\varphi_F|})$$

$$V_{TH} = V_{TH0} = 0.49V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_3 = 2.31\mu m$$

## Problem 3

### 1. Testbench and $I_D$ - $V_{GS}$ characteristics of NMOS and PMOS

#### (a) NMOS

##### i. Testbench

```
.lib 'C:\Program Files\LTC\LTspiceXVII\lib\cmp\log018.l' TT  
.dc VGS 0 1.8 0.001
```

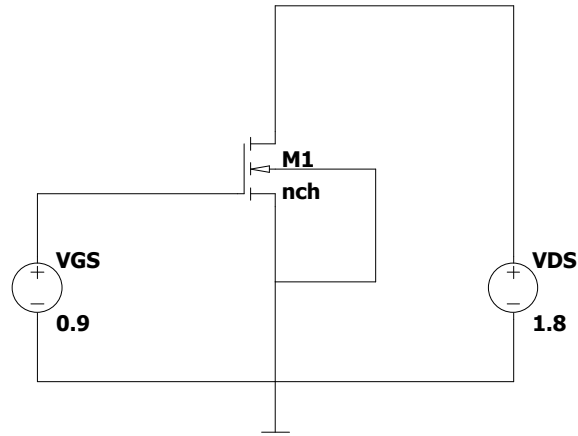


Figure 1: NMOS Testbench

##### ii. $I_D$ - $V_{GS}$

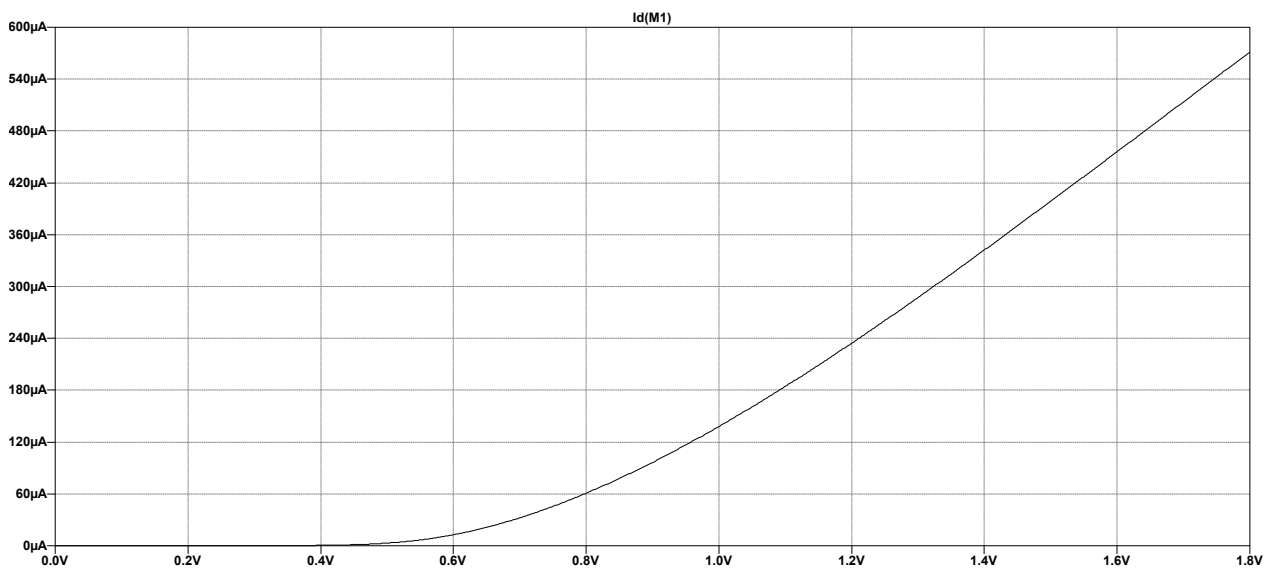


Figure 2: NMOS  $I_D$ - $V_{GS}$

#### (b) PMOS

##### i. Testbench

```
.lib 'C:\Program Files\LTC\LTspiceXVII\lib\cmp\log018.l' TT
.dc VGS -1.8 0 0.001
```

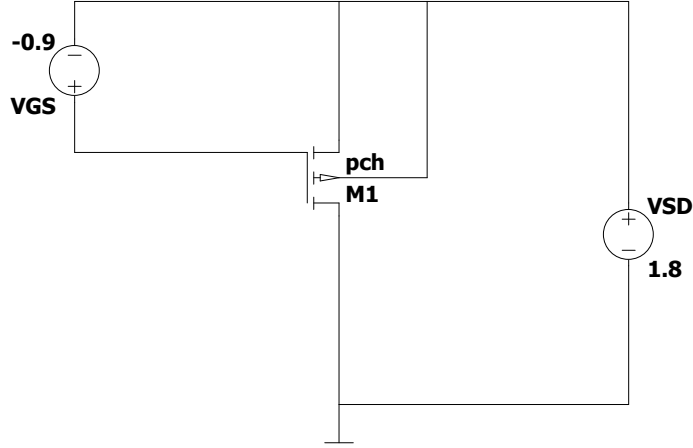


Figure 3: PMOS Testbench

ii.  $I_S$ - $V_{GS}$

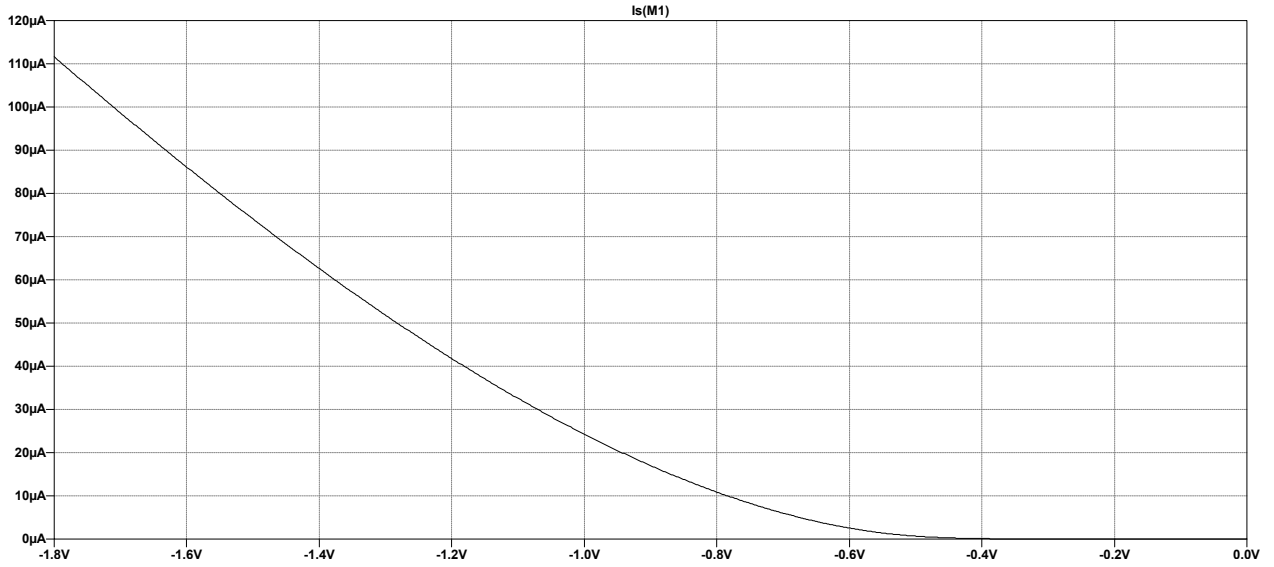


Figure 4: PMOS  $I_S$ - $V_{GS}$

2.  $\mu_{n(p)}C_{OX}$  and  $V_{THn(p)}$

Assuming that channel length modulation is negligible,  $V_{THn}$  for NMOS can be derived from the following relation:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{THn})^2$$

$$\frac{2I_D}{\mu_n C_{ox}} \frac{L}{W} = (V_{GS} - V_{THn})^2$$

$$\sqrt{\frac{2I_D}{\mu_n C_{ox}} \frac{L}{W}} = V_{GS} - V_{THn}$$

$V_{THn}$  is the x-axis intercept when the saturation region is extrapolated. In the case of PMOS, the relation becomes:

$$\sqrt{\frac{2I_S}{\mu_p C_{ox}} \frac{L}{W}} = V_{SG} - V_{THp}$$

For deriving  $\mu_n C_{OX}$ , since  $V_{THn(p)}$  is constant at specific temperatures. Differentiating both sides with respect to

$V_{GS(SG)}$  will give:

$$\begin{aligned}\frac{d}{dV_{GS}} \sqrt{\frac{2I_D}{\mu_n C_{ox}} \frac{L}{W}} &= \frac{d}{dV_{GS}} (V_{GS} - V_{THn}) \\ \frac{1}{2} \frac{dI_D}{dV_{GS}} \sqrt{\frac{2}{I_D \mu_n C_{ox}} \frac{L}{W}} &= 1 \\ \sqrt{\mu_n C_{ox}} &= \frac{1}{2} \frac{dI_D}{dV_{GS}} \sqrt{\frac{2}{I_D} \frac{L}{W}} \\ \mu_n C_{ox} &= \frac{1}{2} \frac{L}{W} \frac{1}{I_D} \left( \frac{dI_D}{dV_{GS}} \right)^2 \\ \mu_n C_{ox} &= \frac{1}{6I_D} \left( \frac{dI_D}{dV_{GS}} \right)^2\end{aligned}$$

In the case for PMOS, the relation becomes:

$$\mu_p C_{ox} = \frac{1}{6I_S} \left( \frac{dI_S}{dV_{SG}} \right)^2$$

(a) NMOS

i.  $\mu_n C_{OX} = 306 \mu A V^{-2}$

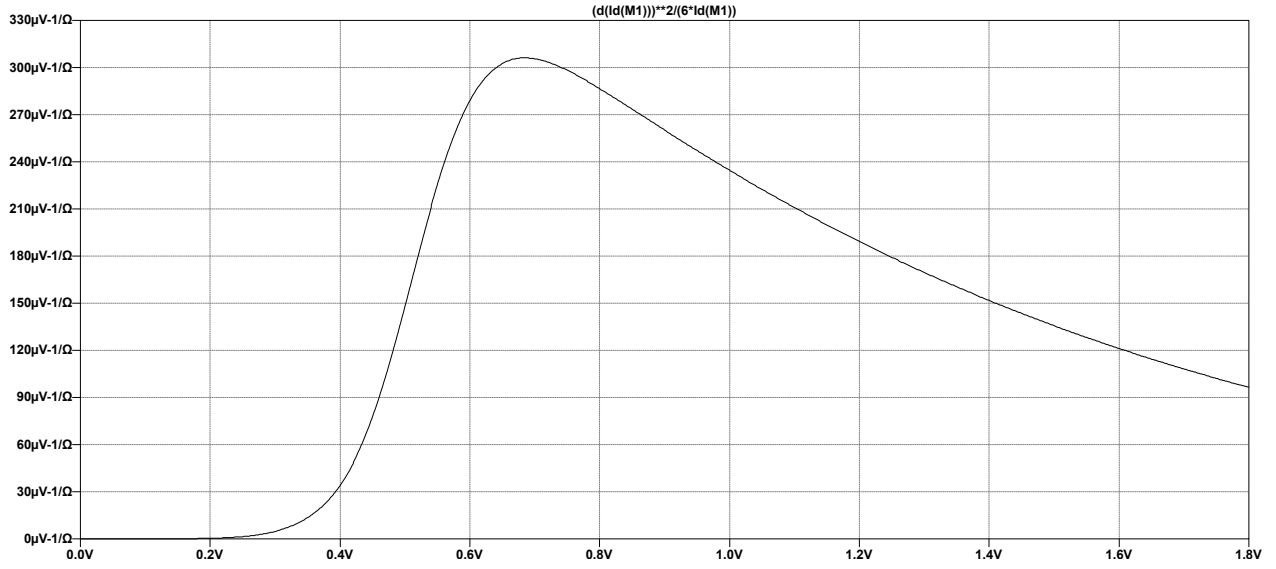


Figure 5: NMOS  $\mu_n C_{OX}$ - $V_{GS}$

ii.  $V_{THn} = 0.44V$

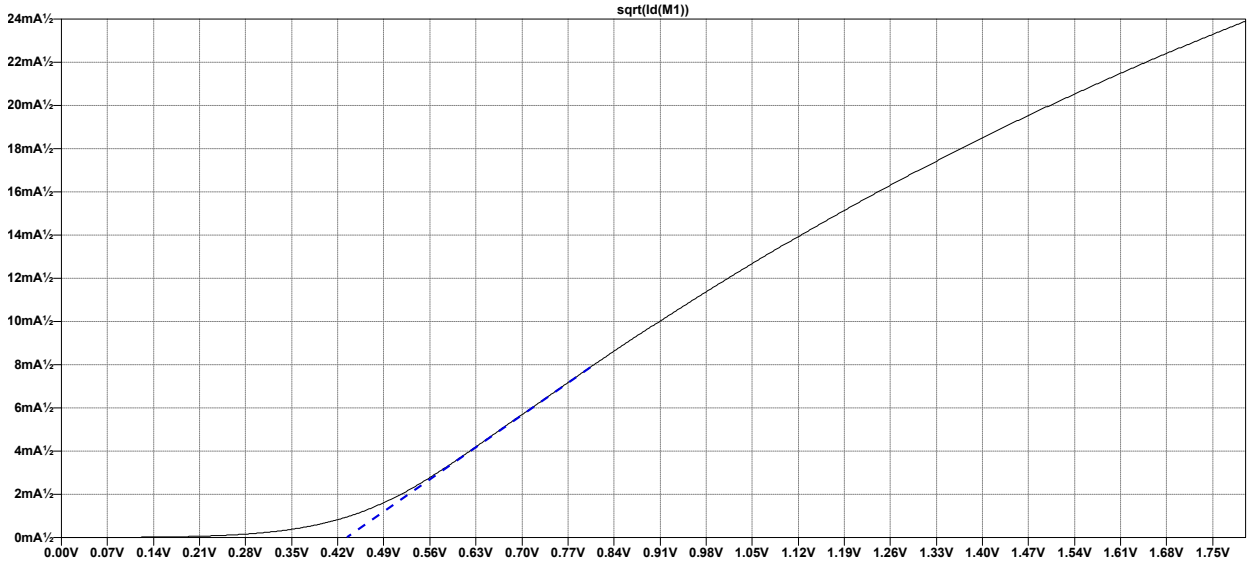


Figure 6: NMOS  $\sqrt{I_D} - V_{GS}$

(b) PMOS

i.  $\mu_p C_{OX} = 294 \mu A V^{-2}$

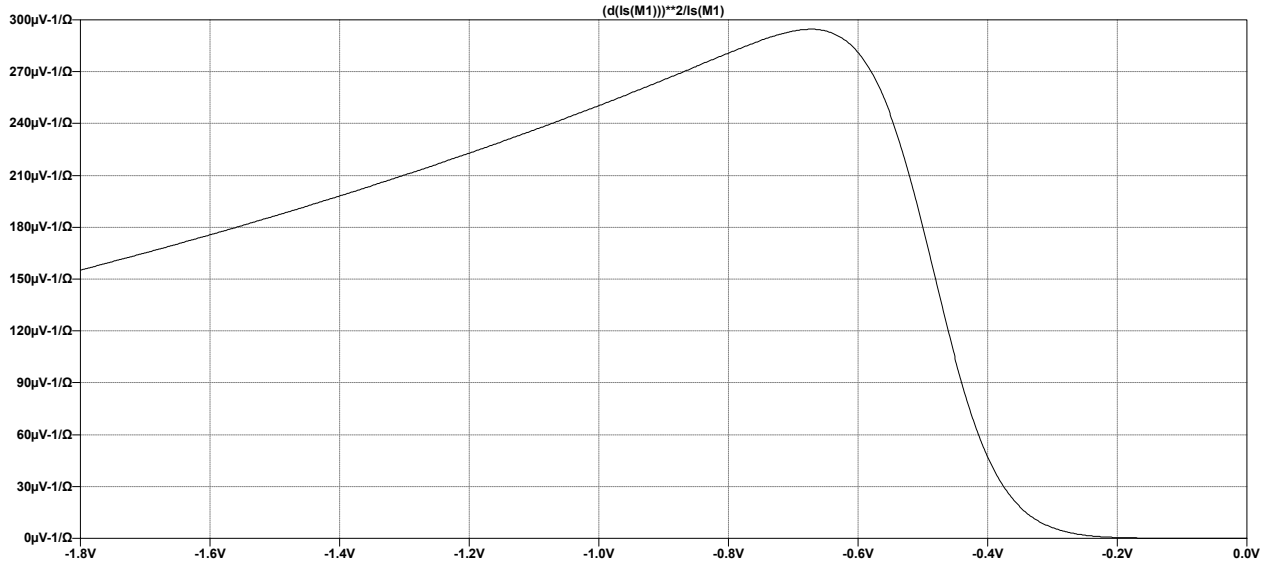


Figure 7: PMOS  $\mu_p C_{OX} - V_{GS}$

ii.  $V_{THp} = -0.42V$

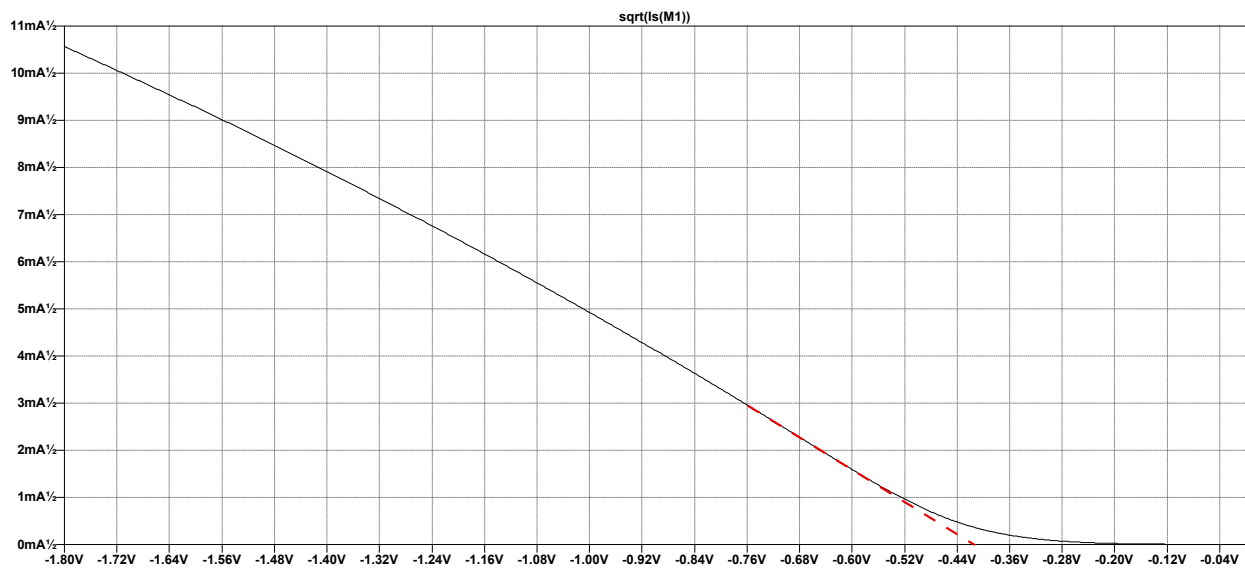


Figure 8: PMOS  $\sqrt{I_S} - V_{GS}$

## Problem 4

1. Testbench and  $I_D - V_{DS}$  characteristics of NMOS and PMOS

(a) NMOS

i. Testbench

```
.lib 'C:\Program Files\LTC\LTspiceXVII\lib\cmp\log018.l' TT
.dc VDS 0 1.8 0.001
```

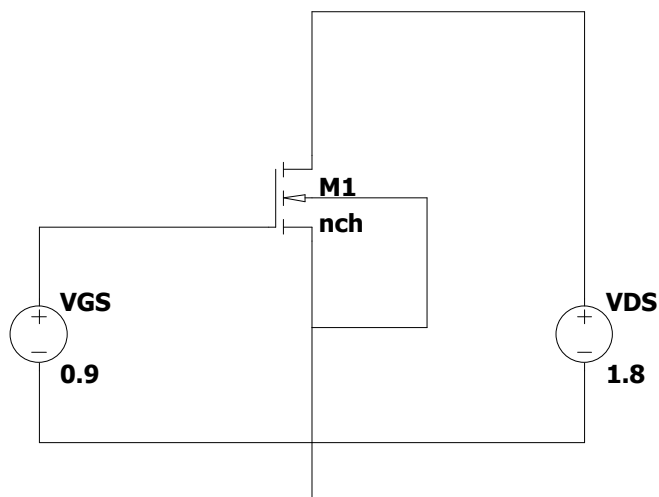


Figure 9: NMOS Testbench

ii.  $I_D - V_{DS}$  characteristics

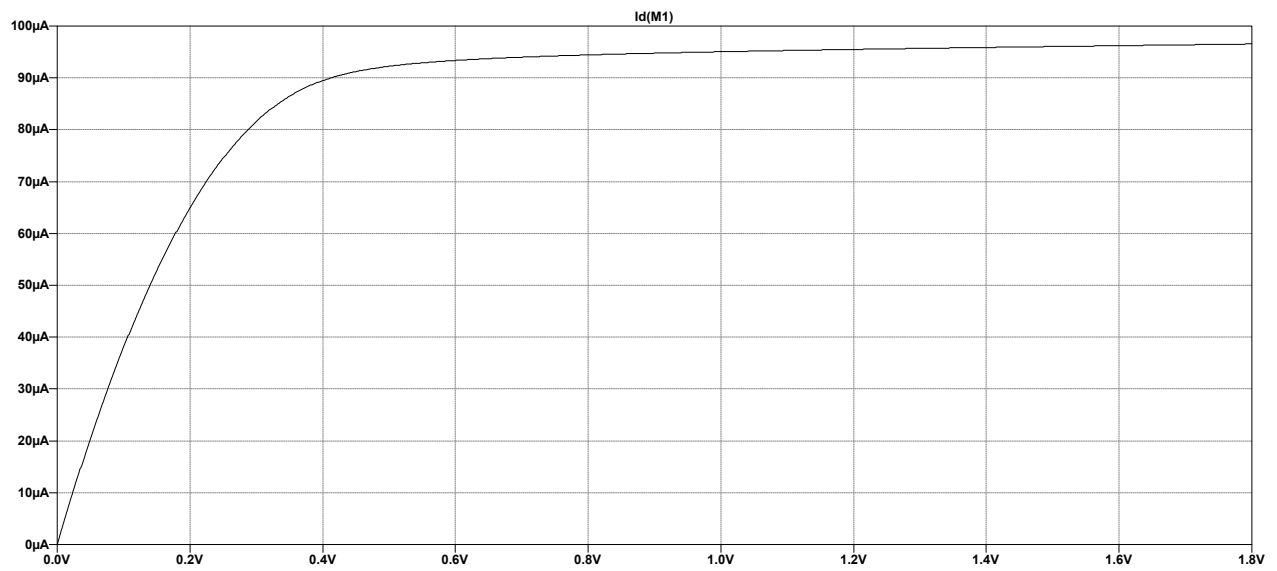


Figure 10: NMOS  $I_D$ - $V_{DS}$

(b) PMOS

i. Testbench

```
.lib 'C:\Program Files\LTC\LTspiceXVII\lib\cmp\log018.l' TT
.dc VDS -1.8 0 0.001
```

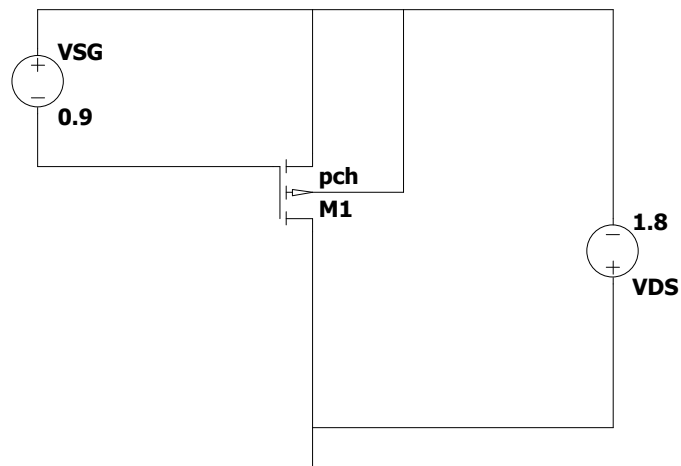


Figure 11: PMOS Testbench

ii.  $I_S$ - $V_{DS}$  characteristics



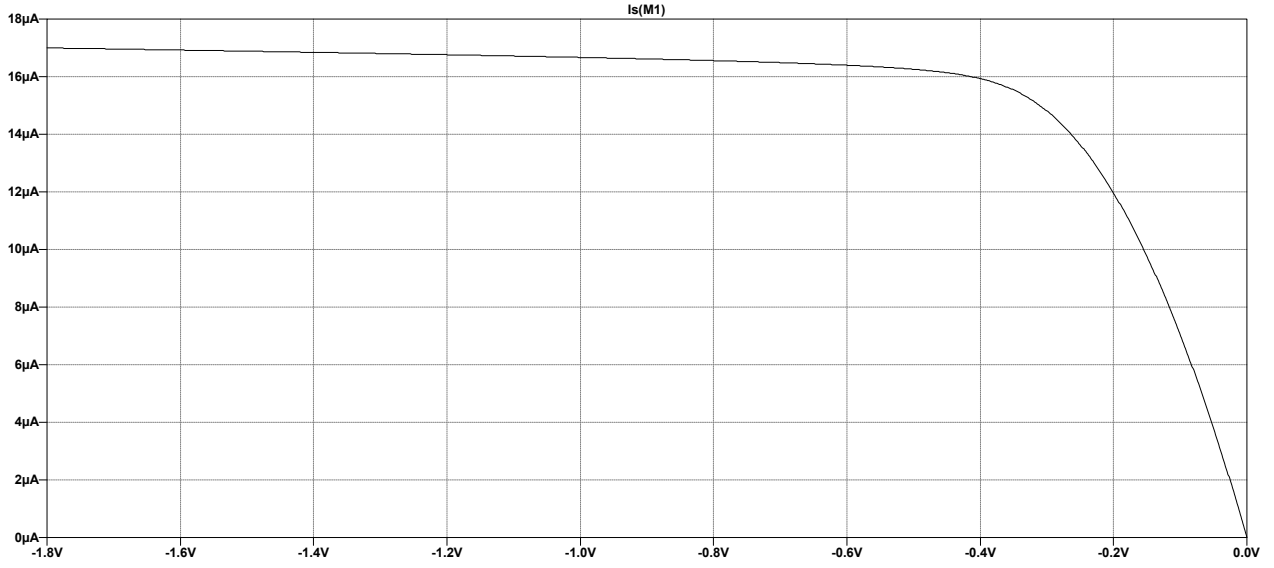


Figure 12: PMOS  $I_S$ - $V_{DS}$

2.  $\lambda_{n(p)}$

Drain current characteristics for NMOS under saturation conditions:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda_n V_{DS})$$

Differentiating both side with respect to  $V_{DS}$ .

$$\begin{aligned} \frac{dI_D}{dV_{DS}} &= \frac{d}{dV_{DS}} \left( \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda_n V_{DS}) \right) \\ \frac{dI_D}{dV_{DS}} &= \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 \lambda_n \end{aligned}$$

Assuming that the body-effect is small:

$$I_D \approx \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$\begin{aligned} \frac{dI_D}{dV_{DS}} &\approx I_D \lambda_n \\ \lambda_n &\approx \frac{1}{I_D} \frac{dI_D}{dV_{DS}} \end{aligned}$$

In the case of PMOS:

$$\lambda_p \approx \frac{1}{I_S} \frac{dI_S}{dV_{SD}}$$

(a)  $\lambda_n = 0.18V^{-1}$

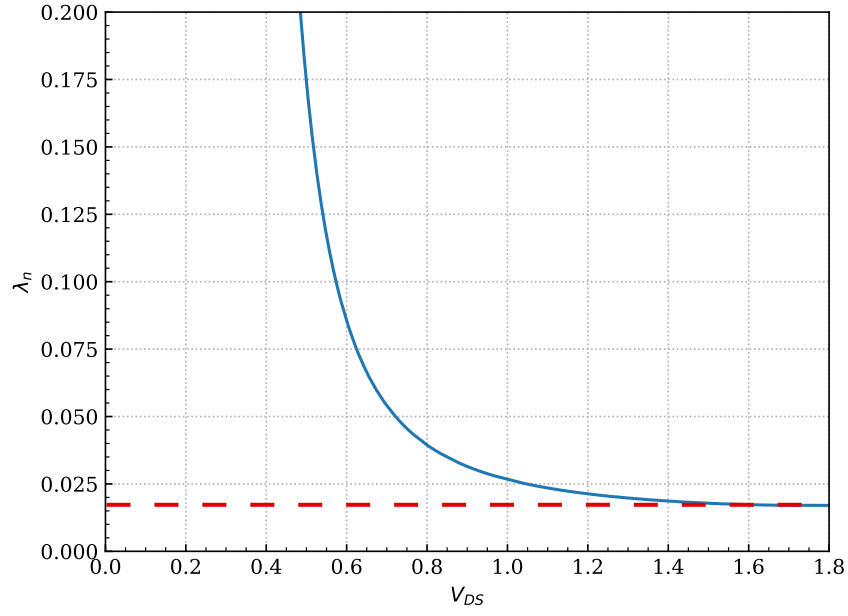


Figure 13: NMOS  $\lambda_n - V_{DS}$

(b)  $\lambda_p = -0.022V^{-1}$

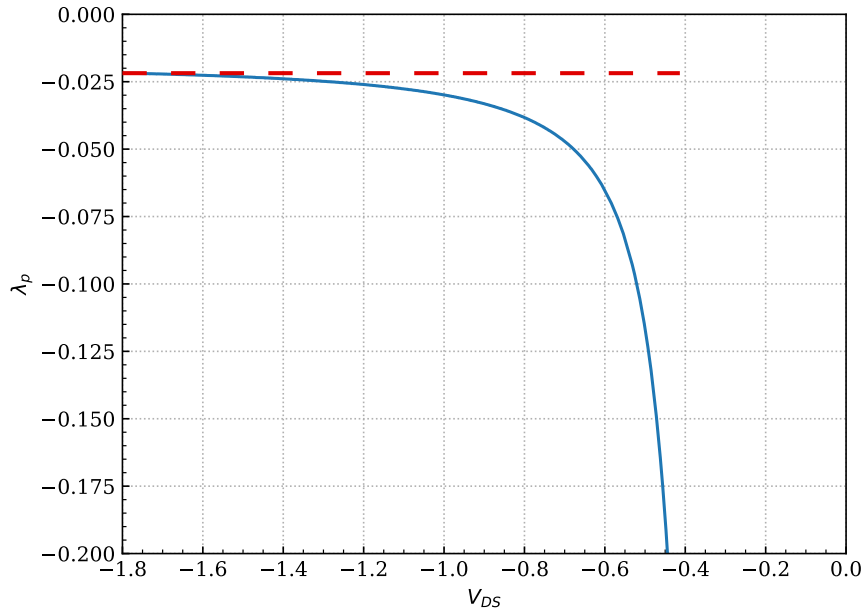


Figure 14: PMOS  $\lambda_p - V_{DS}$

## Problem 5

$g_m$  for NMOS is approximately:

$$g_m \approx \frac{\partial I_D}{\partial V_{GS}}$$

For PMOS:

$$g_m \approx \frac{\partial I_S}{\partial V_{SG}}$$

1.  $\frac{g_m}{I_D} - V_{GS}$

(a) NMOS

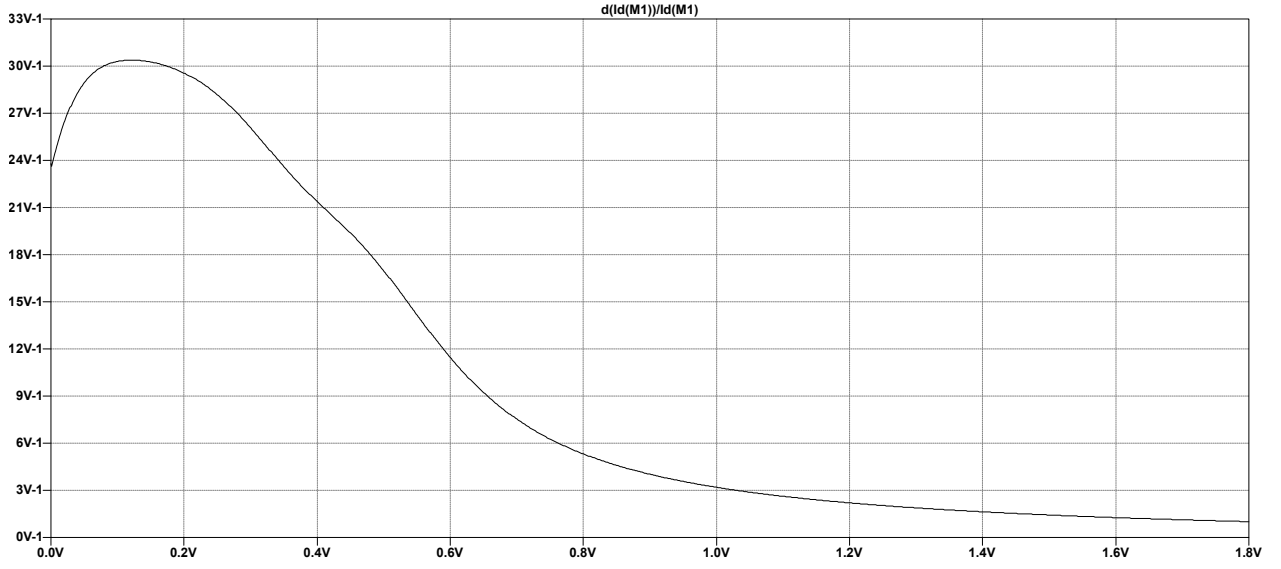


Figure 15: NMOS  $\frac{g_m}{I_D} - V_{GS}$

(b) PMOS

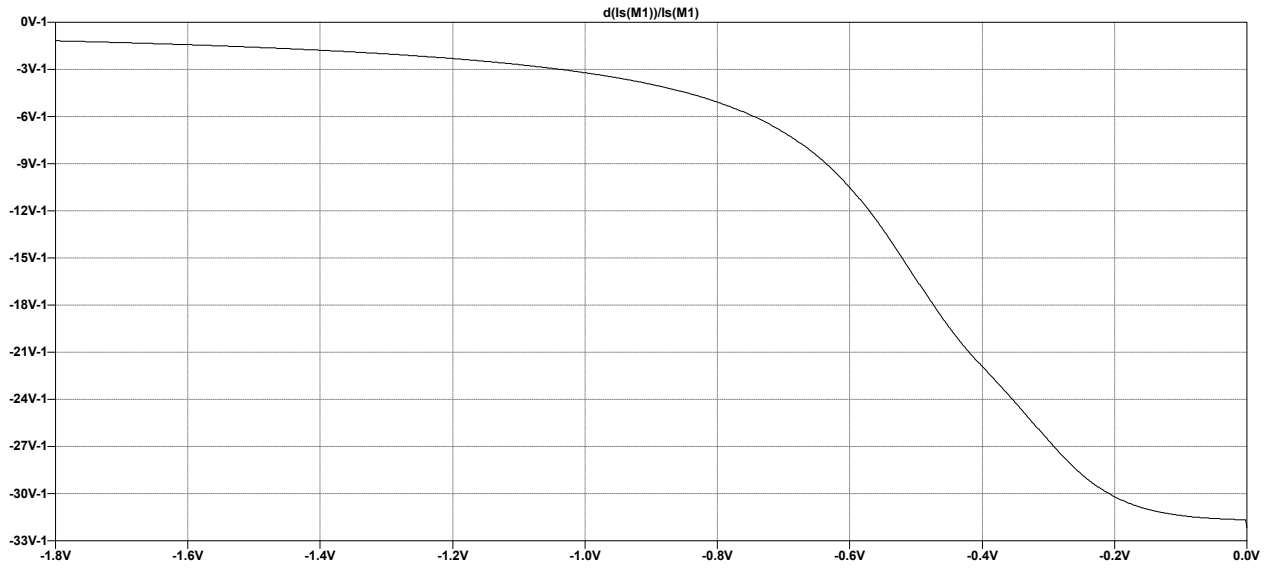


Figure 16: PMOS  $\frac{g_m}{I_S} - V_{GS}$

2.  $\max(|\frac{g_m}{I_{D(S)}}|)$

(a) NMOS

$$\max(|\frac{g_m}{I_D}|) = 30.4V^{-1}$$

(b) PMOS

$$\max(|\frac{g_m}{I_S}|) = 31.7V^{-1}$$

3. Slope factor, n

(a) NMOS

$$\max\left(\frac{g_m}{I_D}\right) = 30.4V^{-1}$$

$$\frac{1}{nV_t} = 30.4V^{-1}$$

$$n = \frac{1}{0.026 \times 30.4}$$

$$n = 1.27$$

(b) PMOS

$$\max\left(\frac{g_m}{I_S}\right) = 31.7V^{-1}$$

$$\frac{1}{nV_t} = 31.7V^{-1}$$

$$n = \frac{1}{0.026 \times 31.7}$$

$$n = 1.21$$

## Problem 6

1. Small-signal Model

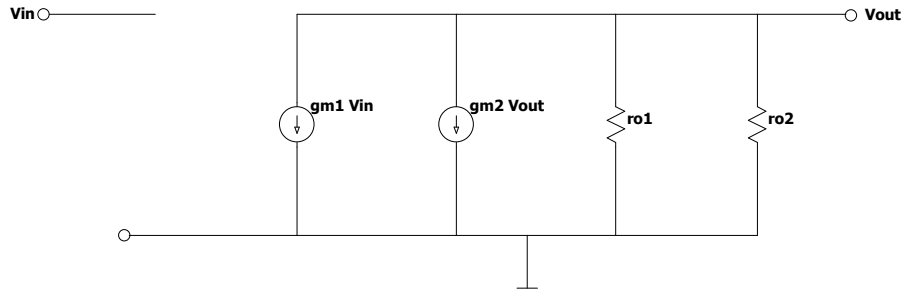


Figure 17: Small signal model

2.  $\lambda = 0V^{-1}$

3.  $\lambda \neq 0V^{-1}$

(a)  $A_V = \frac{v_{out}}{v_{in}}$

$$\begin{aligned} -v_{out} &= (g_{m1}v_{in} + g_{m2}v_{out})(r_{o1}/r_{o2}) \\ -v_{in}g_{m1}(r_{o1}/r_{o2}) &= (1 + g_{m2}(r_{o1}/r_{o2}))v_{out} \\ A_V = \frac{v_{out}}{v_{in}} &= -\frac{g_{m1}}{g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}} \end{aligned}$$

(b)  $R_{out}$

$$R_{out} = \frac{1}{g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}}$$

## Problem 7