EE4C10 Analog Circuit Design Fundamentals

Homework Assignment IV

Tzong Lin Chua

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Simulation Files

Each question with simulation files will have their respective subfolder.

Running the simulation files should be able to directly plot the graphs used (configured in the *.plt file). The folders for each question are arranged as follows after extracting:

$_{ m spice}$		
	q3	
		\mathbf{a}
		b
		\mathbf{c}
		d
	q4	
		\mathbf{a}
		b
		\mathbf{c}

Problem 1

(a) DC gain, $\left| \frac{V_{out}}{V_{in}} \right|$ KCL at drain node,

$$\frac{V_{out}}{R_D} = (g_m + g_{mb})v_s$$
$$\frac{V_{out}}{v_s} = (g_m + g_{mb})R_D$$

KCL at source node,

$$\frac{V_{in} - V_S}{R_S} = (g_m + g_{mb})v_s$$
$$\frac{V_{in}}{v_s} = R_S(g_m + g_{mb}) + 1$$

DC gain,

$$|\frac{V_{out}}{V_{in}}| = \frac{(g_m + g_{mb})R_D}{(g_m + g_{mb})R_S + 1}$$

(b) Pole of output node, $\omega_{p,out}$

$$R_{out} = R_D$$

$$C_{out} = C_{DB} + C_{GD}$$

$$\omega_{p,out} = \frac{1}{R_D(C_{DB} + C_{GD})}$$

(c) Input impedance,

$$Z_{IN} = \frac{1}{g_m + g_{mb} + s(C_{GS} + C_{SB})}$$

(d) Source capacitance, C_S , and input pole, $\omega_{p,in}$,

$$C_S = C_{GS} + C_{SB}$$

$$\omega_{p,in} = \frac{g_m + g_{mb} + R_S^{-1}}{C_S}$$
$$= \frac{g_m + g_{mb} + R_S^{-1}}{C_{GS} + C_{SB}}$$

Problem 2

(a) Transfer function, $\frac{V_{out}(s)}{V_{in}(s)}$, DC gain,

$$\left|\frac{V_{out}(S)}{V_{in}(s)}\right| = 1$$

Poles at gate and source nodes,

$$\omega_{p,G} = \frac{1}{R_S(C_{GB} + G_{GD})}$$

$$\omega_{p,D} = \frac{g_m}{C_{SB}}$$

Transfer function,

$$\frac{V_{out}(S)}{V_{in}(s)} = \frac{1}{1 + sR_S(C_{GB} + G_{GD})} \frac{1}{1 + s\frac{C_{SB}}{g_m}}$$
$$= \frac{1}{(1 + sR_S(C_{GB} + G_{GD}))(1 + \frac{sC_{SB}}{g_m})}$$

(b) Poles at gate and source nodes,

$$\omega_{p,G} = \frac{1}{R_S(C_{GB} + G_{GD})}$$

$$\omega_{p,D} = \frac{g_m}{C_{SB}}$$

(c) Input impedance,

$$Z_{in} = \frac{1}{s(C_{GB} + C_{GD})}$$

Problem 3

(a) Testbench,

.lib 'C:\Program Files\LTC\LTspiceXVII\lib\cmp\log018.l' TT .dc V1 0 1.8 ;ac dec 10 10 1G

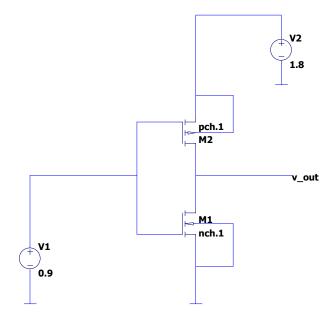


Figure 1: Inverter testbench

DC transfer curve,

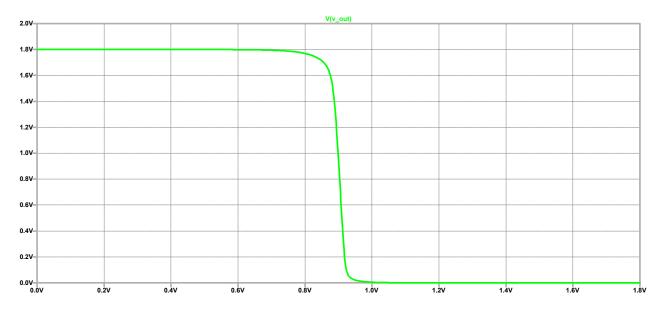


Figure 2: Inverter DC response

(b) Transient response,

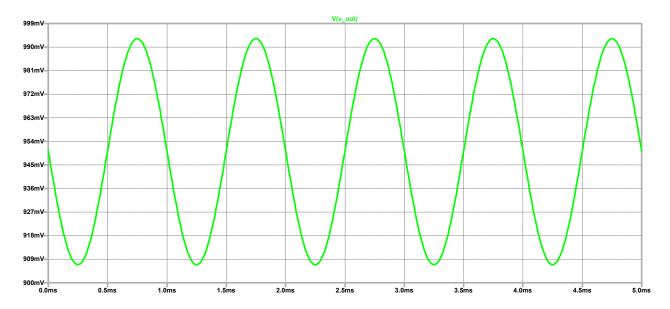


Figure 3: Inverter transient response

(c) AC responce

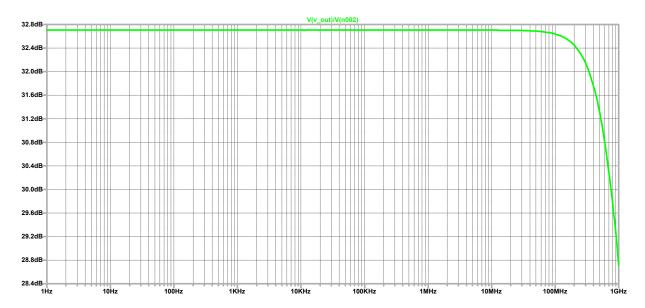


Figure 4: Inverter AC gain

$$|\frac{V_{out}}{V_{in}}| = 32.7dB$$

$$= 43.2$$

$$\omega_p = 2\pi f_{-3dB}$$

$$= 5.136 \times 10^9 rads^{-1}$$

(d) AC Response

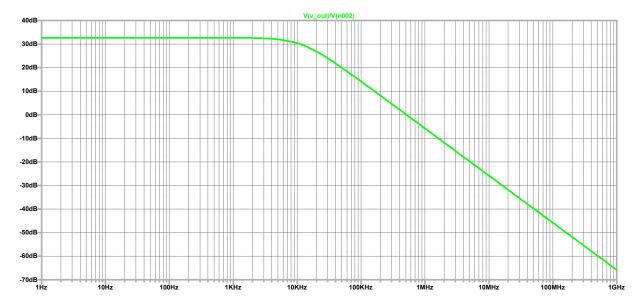


Figure 5: Inverter AC gain with output capacitor

$$|\frac{V_{out}}{V_{in}}| = 32.7dB$$

$$= 43.2$$

$$\omega_p = 2\pi f_{-3dB}$$

$$= 7.42 \times 10^4 rads^{-1}$$

(e) The pole at output node,

$$RC = \frac{1}{2\pi f_c}$$

$$R(C + \Delta C) = \frac{1}{2\pi f_d}$$

$$R = \frac{1}{\Delta C} \left(\frac{1}{2\pi f_d} - \frac{1}{2\pi f_c}\right)$$

$$= \frac{1}{\Delta C} \left(\frac{1}{2\pi f_d} - \frac{1}{2\pi f_c}\right)$$

$$R_{out} = 134.75k\Omega$$

Problem 4

(a) Testbench

.lib 'C:\Program Files\LTC\LTspiceXVII\lib\cmp\log018.l' TT .dc V1 0 1.8 0.01 ;ac dec 10 1 1G

;tran 0 5m 0 0.01 ;1 0 1.8

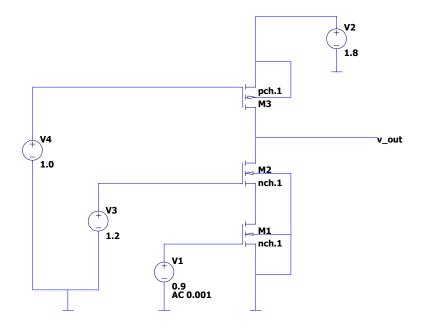


Figure 6: Testbench

DC transfer curve,

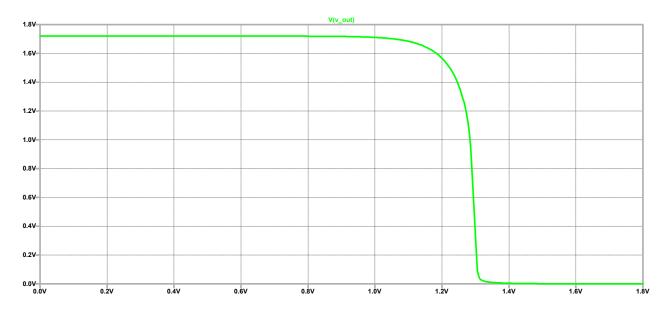


Figure 7: DC response

(b) Transient response,

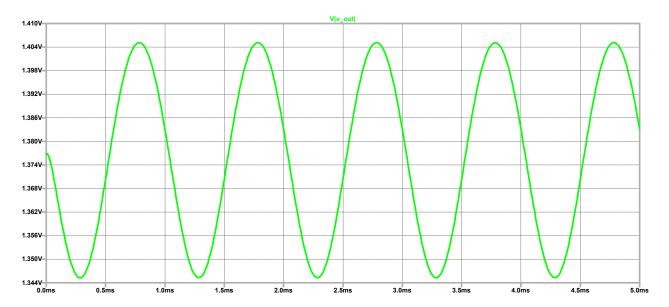


Figure 8: Transient response

(c) AC response

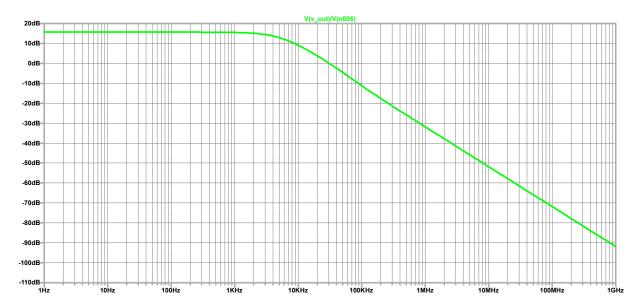


Figure 9: Inverter AC gain

$$|\frac{V_{out}}{V_{in}}| = 15.7dB$$

$$= 6.06$$

$$\omega_p = 2\pi f_{-3dB}$$

$$= 3.35 \times 10^4 rads^{-1}$$

(d) Gain bandwidth product, GBWP

$$|\frac{V_{out}}{V_{in}}| = 6.06$$

$$f_{-3dB} = 5.331kHz$$

$$GBWP = 32.3kHz$$