

EE4C10 Analog Circuit Design Fundamentals

Homework Assignment I

Tzong Lin Chua

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Contents

Problem 1	1
Problem 2	1
Problem 3	3
Problem 4	5
Problem 5	5
Problem 6	5
Problem 7	5

Problem 1

For $I_D = 40\mu A$:

$$I_D = \frac{1.8V - V_D}{R}$$

$$V_D = 1.8V - I_D R$$

$$\underline{V_D} = 1.0V$$

Saturation region:

$$V_{GS} = 1.0V > V_{TH}$$

$$V_{GS} - V_{TH} = 0.4V < V_{DS}$$

1. $\lambda = 0V^{-1}$

$$I_D = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$L = \frac{\mu_n C_{OX}}{2} \frac{W}{I_D} (V_{GS} - V_{TH})^2$$

$$\underline{L} = 0.39\mu m$$

2. $\lambda = 0.06V^{-1}$

$$I_D = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

$$L = \frac{\mu_n C_{OX}}{2} \frac{W}{I_D} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

$$\underline{L} = 0.41\mu m$$

Problem 2

1. Bulk of the transistors are connected to the source, $V_B = V_S$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\varphi_F + V_{BS}} - \sqrt{|2\varphi_F|})$$

$$V_{TH} = V_{TH0} = 0.33V$$

(a) Transistor M₁

$$V_{SG} = 2.5V - 1.7V = 0.8V$$

$$I_D = \frac{\mu_p C_{OX}}{2} \frac{W}{L} (V_{SG} - V_{TH})^2$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_1 = 2.72\mu m$$

(b) Transistor M₂

$$V_{SG} = 1.7V - 1V = 0.7V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_2 = 4.38\mu m$$

(c) Transistor M₃

$$V_{SG} = 1V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_3 = 1.37\mu m$$

2. Bulk terminals are attached to the V_{DD}, V_B = V_{DD}.

(a) Transistor M₁

$$V_{BS} = 2.5V - 2.5V = 0V$$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\varphi_F + V_{BS}} - \sqrt{|2\varphi_F|})$$

$$V_{TH} = V_{TH0} = 0.33V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_1 = 2.72\mu m$$

(b) Transistor M₂

$$V_{BS} = 2.5V - 1.7V = 0.8V$$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\varphi_F + V_{BS}} - \sqrt{|2\varphi_F|})$$

$$V_{TH} = V_{TH0} = 0.43V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_2 = 8.23\mu m$$

(c) Transistor M₃

$$V_{BS} = 2.5V - 1.0V = 1.5V$$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\varphi_F + V_{BS}} - \sqrt{|2\varphi_F|})$$

$$V_{TH} = V_{TH0} = 0.49V$$

$$W = \frac{2LI_D}{\mu_p C_{OX}} \frac{1}{(V_{SG} - V_{TH})^2}$$

$$W_3 = 2.31\mu m$$

Problem 3

1. Testbench and I_D - V_{GS} characteristics of NMOS and PMOS

(a) NMOS

i. Testbench

```
.lib 'C:\Program Files\LTC\LTspiceXVII\lib\cmp\log018.l' TT
.dc VGS 0 1.8 0.001
```

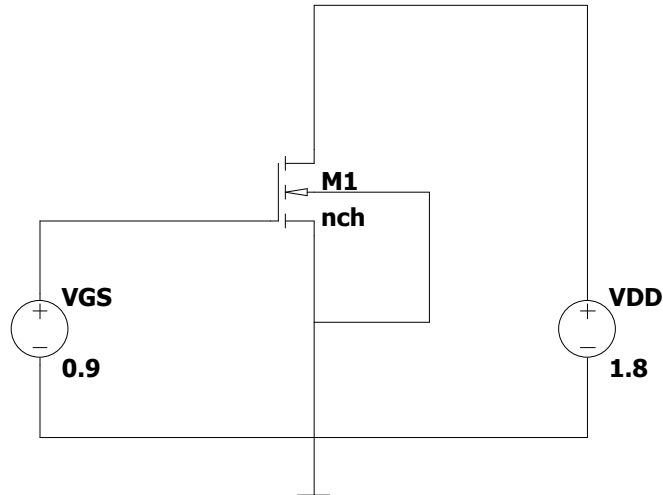


Figure 1: NMOS Testbench

ii. I_D - V_{GS}

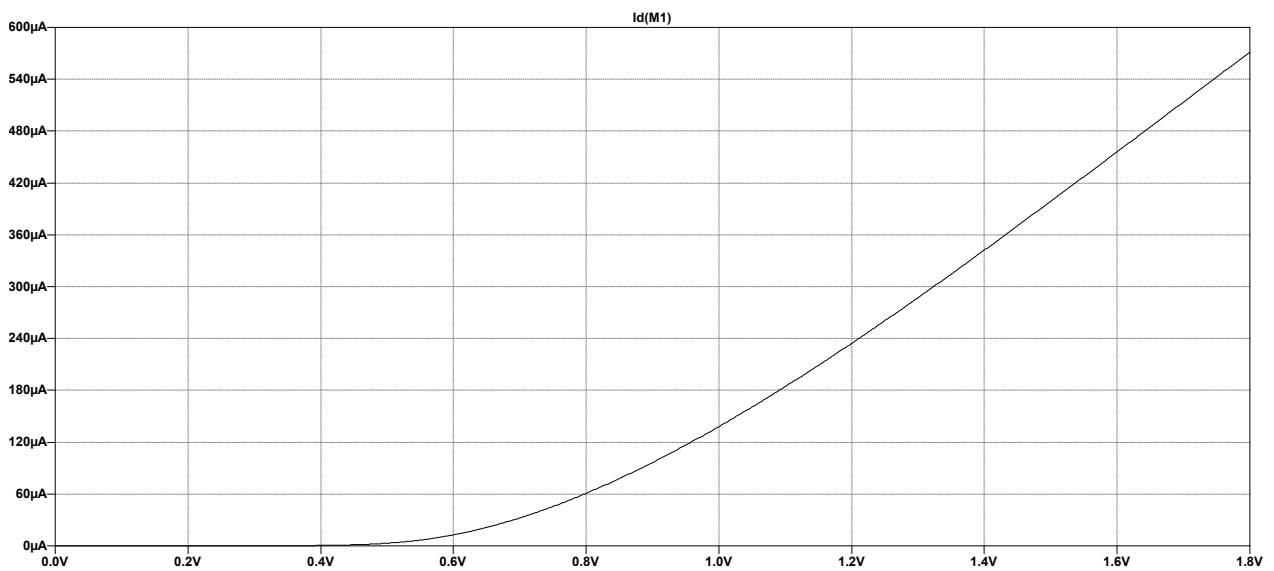


Figure 2: NMOS I_D - V_{GS}

(b) PMOS

i. Testbench

ii. I_D - V_{GS}

2. $\mu_{n(p)}C_{OX}$ and $V_{THn(p)}$

Assuming that channel length modulation is negligible, $\mu_n C_{OX}$ for NMOS can be derived from the following relation:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{THn})^2$$

$$\frac{2I_D}{\mu_n C_{ox}} \frac{L}{W} = (V_{GS} - V_{THn})^2$$

$$\sqrt{\frac{2I_D}{\mu_n C_{ox}} \frac{L}{W}} = V_{GS} - V_{THn}$$

Since V_{THn} is constant at specific temperatures. Differentiating both sides will give:

$$\frac{d}{dV_{GS}} \sqrt{\frac{2I_D}{\mu_n C_{ox}} \frac{L}{W}} = \frac{d}{dV_{GS}} (V_{GS} - V_{THn})$$

$$\frac{1}{2} \frac{dI_D}{dV_{GS}} \sqrt{\frac{2}{I_D \mu_n C_{ox}} \frac{L}{W}} = 1$$

$$\sqrt{\mu_n C_{ox}} = \frac{1}{2} \frac{dI_D}{dV_{GS}} \sqrt{\frac{2}{I_D} \frac{L}{W}}$$

$$\mu_n C_{ox} = \frac{1}{2} \frac{L}{W} \frac{1}{I_D} \left(\frac{dI_D}{dV_{GS}} \right)^2$$

$$\mu_n C_{ox} = \frac{1}{6I_D} \left(\frac{dI_D}{dV_{GS}} \right)^2$$

In the case for PMOS, the relation becomes:

$$\mu_p C_{ox} = \frac{1}{6I_S} \left(\frac{dI_S}{dV_{SG}} \right)^2$$

(a) NMOS

i. $\mu_n C_{OX}$

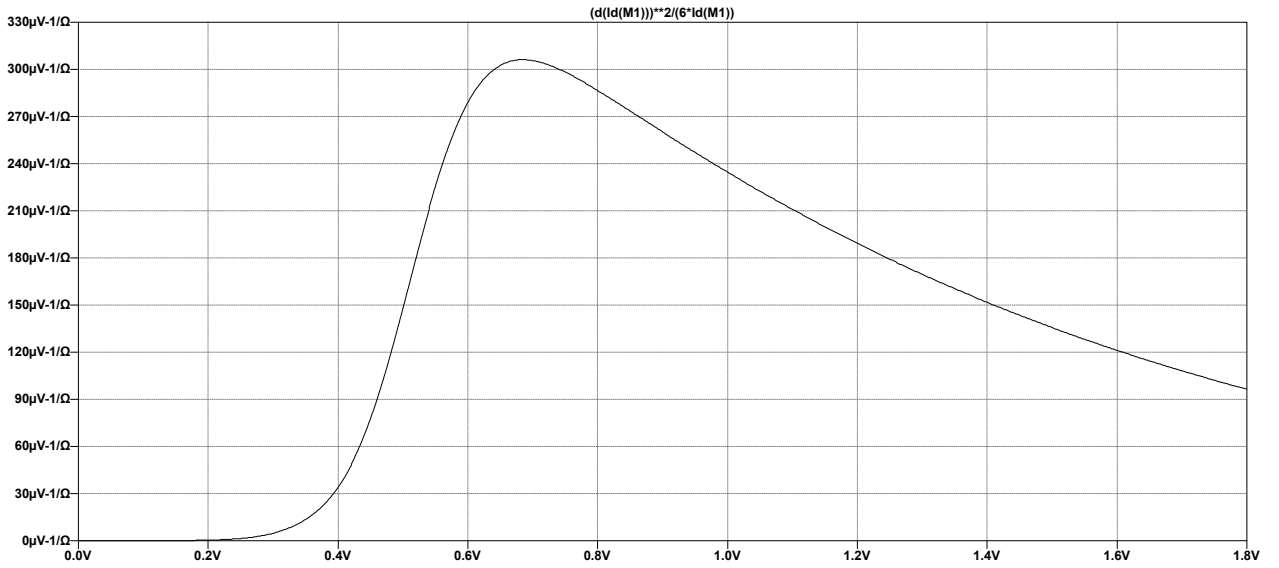


Figure 3: NMOS $\mu_n C_{OX}$ - V_{GS}

ii. V_{THn}

(b) PMOS

i. $\mu_p C_{OX}$

ii. V_{THp}

Problem 4

Problem 5

Problem 6

Problem 7