TU Delft

EE4C10 Analog Circuit Design Fundamentals

Homework Assignment III

Start date: 24/09/2021

Due date: 01/10/2021

Please upload your homework via Brightspace

INSTRUCTIONS

1. Solutions must be submitted in PDF file named "Name_Surname_HW3.pdf". Descriptions of the simulation and simulation results must be included in the PDF file, while schematics used for simulations must be compressed in a single ZIP file named "Name_Surname_HW3.zip" containing the LTspice files. Converted photographs are not accepted. Please avoid hand-written reports and graphs. Simulation waveforms should have a white background.

2. Late submissions would not be accepted.

3. For the simulation's questions, attach a LTspice file used for each question that can be directly simulated.

    1. For all exercises in this question assume, unless otherwise noted: W/L = 15um/1um for the NMOS, μnCox = 100 μA/V^2 for NMOS. Assume that all transistors operate in saturation. Calculate the following quantities for a differential pair with input NMOS devices with an ideal tail current of 150μA.
        a. (1 point) What is the equilibrium overdrive voltage of each transistor, i.e. the overdrive voltage for zero differential input?
        b. (1 point) Calculate the change in current ΔI_D for a change in voltage of $\Delta V_{in} = 30\ mV$
        c. (2 points) What is the equivalent g_m under this condition (question 1b)?

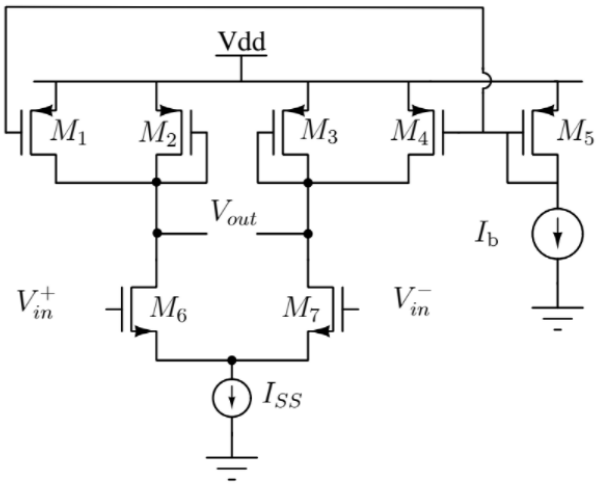

Figure 1 Circuit for question 2

2. In the circuit of Fig.1, assume ISS = 1 mA and W/L = 15/1 for all transistors, μnCox = 300 uA/V^2 for NMOS and μpCox = 150 uA/V^2 for PMOS and threshold voltage of 0.7 V and lambda=0.1 1/V, for all the transistors. The supply voltage is $V_{DD} = 1.8\,V$.

    a. (1 point) Calculate Ib such that ID2=ID3=0.8(ISS/2)
    b. (1 point) Determine the voltage gain, assuming the value of Ib computed in a).
    c. (2 points) Compute the CM-CM gain, the DM-CM gain, the CM-DM gain, and the CMRR.
    d. (2 points) If ISS requires a minimum voltage of 0.4 V, determine the input common-mode range to keep all transistors in saturation.

Simulation exercise:

3. (2 points) Simulate an NMOS differential pair with PMOS current mirror load. Dimensions of input pair: L=1um, W=15um. Dimensions tail transistor: L=1um, W=30um. Dimensions mirror diode: L=1um, W=15um. Bias current: 15 uA. For the setup, see figure 3. For the PMOS mirror on top use 30um wide and 1um long transistors. Unless otherwise noted: input common mode voltage=1.5 V.
    a. Extract differential and common mode gain at low frequencies using an AC simulation

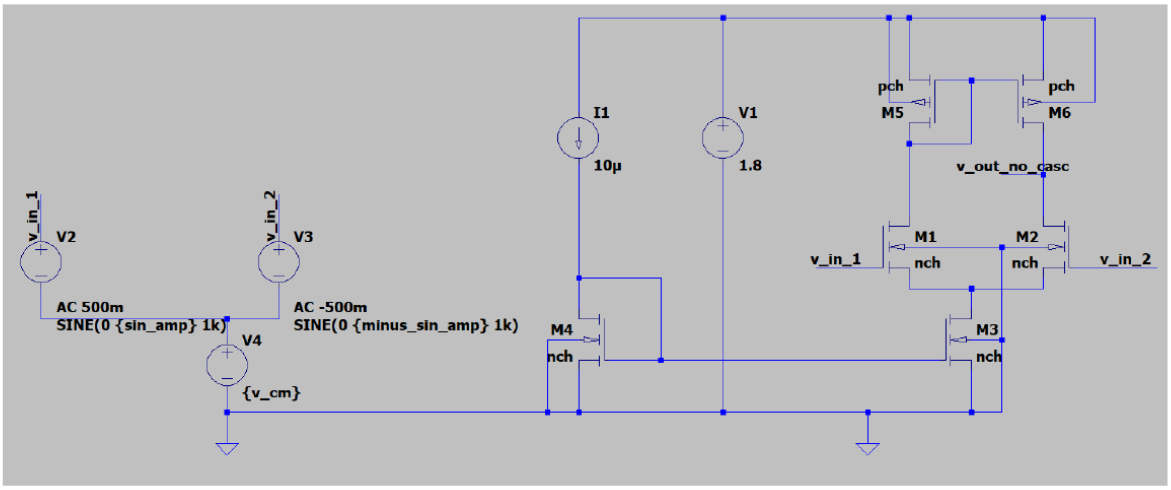

Figure 2 Circuit for simulation exercise 3a

4) (2 points) Add cascodes that are of the same size as the input and mirror transistors, like shown in figure 3. Build a bias network for the cascodes from transistors and resistors, using a single current source as the only ideal source. All transistors must be operating in saturation. Report the obtained DC operating point of all transistors in the biasing circuit. Report the current through all resistors and transistors as well as the bias voltages generated. Also provide a screenshot of your circuit with annotated DC-bias points.

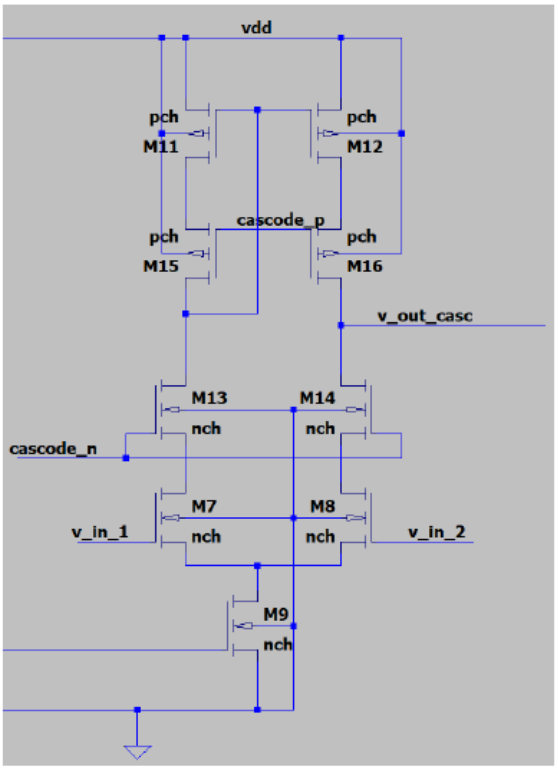

Figure 3 Adding cascode to exercise 3

5) (2 points) Simulate the differential and common mode gain for the structure. If you did not build the bias network use 900 mV for biasing the PMOS and 1400 mV for biasing the NMOS cascode transistors.

---- END OF THE ASSIGNMENT ----