EE4C10 Analog Circuit Design Fundamentals

Homework Assignment III

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Simulation Files

Each question with simulation files will have their respective subfolder. Except for `q4`, the other questions will have separate subfolders for common-mode and differential mode circuits.

Running the simulation files should be able to directly plot the graphs used (configured in the *.plt file) or the operation points. The folders for each question are arranged as follows after extracting:

```
spice
    q3
        cm
        dm
    q4
    q5
        cm
        dm
```

Problem 1

(a) Overdrive voltage of NMOS transistor M1 and M2, V_{OV1} and V_{OV2}.

Drain current of M1 and M2 for 0 differential input,

$$I_{D1} = I_{D2} = \frac{I_{DD}}{2} = 75\mu A$$

$$I_{D1} = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{OV1})^2$$

$$V_{OV1} = \sqrt{\frac{2I_{D1}}{\mu_n C_{OX}}\frac{L}{W}}$$

$$= 0.316V$$

$$V_{OV1} = V_{OV2} = 0.316V$$

(b) ΔI_D when ΔV_{in}

$$\begin{aligned} I_{D1} &= \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{OV1} + \frac{\Delta V_{in}}{2})^2 \\ &= 82.28\mu A \\ \Delta I_{D1} &= I_{D1} - \frac{I_{DD}}{2} \\ &= 7.28\mu A \end{aligned}$$

$$\begin{aligned} I_{D2} &= \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{OV2} - \frac{\Delta V_{in}}{2})^2 \\ &= 68.05\mu A \\ \Delta I_{D2} &= I_{D2} - \frac{I_{DD}}{2} \\ &= -6.95\mu A \\ \Delta I_D &= \Delta I_{D1} + \Delta I_{D2} \\ &= 14.23\mu A \end{aligned}$$

(c) Equivalent g_m.

Since M1 and M2 has the same dimensions,

$$\begin{aligned} g_m &= 2g_{m1} = 2g_{m2} \\ &= 2\frac{\mu_n C_{OX}}{2}\frac{W}{L}V_{OV1} \\ &= 474\mu S \end{aligned}$$

Problem 2

(a) I_b when $I_{D2} = I_{D3} = 0.8(\frac{I_{SS}}{2})$

$$\begin{aligned} I_{D2} = I_{D3} &= 0.8\frac{I_{SS}}{2} \\ &= 0.4mA \end{aligned}$$

$$\begin{aligned} I_{D1} = I_{D4} &= 0.2\frac{I_{SS}}{2} \\ &= 0.1mA \end{aligned}$$

Since transistor M5-M1 and M5-M4 are current mirror pairs,

$$\begin{aligned} I_b &= I_{D5} = I_{D1} = I_{D4} \\ I_b &= 0.1mA \end{aligned}$$

(b) Voltage gain, $A_{\text{DM-DM}}$, is equal to the gain of the half circuit.

$$G_m = g_{m6}$$

$$R_{out} = \frac{1}{g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{1}{r_{o6}}}$$

$$\begin{aligned} A_{DM-DM} &= -G_m R_{out} \\ &= \frac{g_{m6}}{g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{1}{r_{o6}}} \end{aligned}$$

$$\begin{aligned} g_{m2} &\approx \sqrt{2\mu_p C_{OX} \frac{W}{L} I_{D2}} \\ &\approx 1.342mS \end{aligned}$$

$$\begin{aligned} g_{m6} &\approx \sqrt{2\mu_n C_{OX} \frac{W}{L} \frac{I_{SS}}{2}} \\ &\approx 2.121mS \end{aligned}$$

$$\begin{aligned} r_{o1} &= \frac{1}{I_{D1}\lambda} \\ &= 100k\Omega \\ r_{o2} &= \frac{1}{I_{D2}\lambda} \\ &= 25k\Omega \\ r_{o6} &= \frac{1}{I_{D6}\lambda} \\ &= 20k\Omega \end{aligned}$$

$$A_{DM-DM} = -1.471$$

(c) The circuit's:

1. CM-CM gain
   From the lecture slides,

$$A_{CM-CM} = \frac{2g_m \frac{r_o}{2} \frac{R_D}{2}}{\frac{r_o}{2}(1 + 2g_m R_{SS}) + R_{SS} + \frac{R_D}{2}}$$

$$\begin{aligned} g_m &= g_{m6} \\ &= 2.121mS \end{aligned}$$

$$\begin{aligned} r_o &= r_{o6} \\ &= 20k\Omega \end{aligned}$$

$$\begin{aligned} R_D &= \frac{r_{o1} r_{o2}}{g_{m2} r_{o1} r_{o2} + r_{o1} + r_{o2}} \\ &= 718.4\Omega \end{aligned}$$

$$R_{out} = \frac{1}{2g_{m2} + \frac{2}{r_{o1}} + \frac{2}{r_{o2}} + \frac{2}{r_{o6}}}$$

$$A_{CM-CM} = -\frac{15237}{10359 + 43.42R_{SS}}$$

Since resistance of ideal current source is infinite, $A_{CM-CM} = 0$.

2. DM-CM gain
   Since the ideal case is considered, there will be no mismatch in resistance or transconductance $A_{DM-CM} = 0$
3. CM-DM gain
   Since the ideal case is considered, there will be no mismatch in resistance or transconductance $A_{DM-CM} = 0$
4. CMRR

$$CMRR = |\frac{A_{DM-DM}}{A_{CM-DM}}|$$
$$CMRR = \infty$$

(d) Input common-mode range to keep all transistors in saturation.

Range of V_{out},

$$V_{dd} - V_{out} \geq 0.7V$$
$$V_{out} \leq 1.1V$$

Range of V_{in},

$$V_{out} - 0.4V \geq V_{in} - 0.4V - 0.7V$$
$$V_{in} \leq 1.8V$$

$$V_{in} - 0.4V \geq 0.7V$$
$$V_{in} \geq 1.1V$$

$$1.1V \leq V_{in} \leq 1.8V$$

Problem 3

(a) Low frequency

1. Differential gain
   From figure 1, $A_{DM} = 42.0dB$

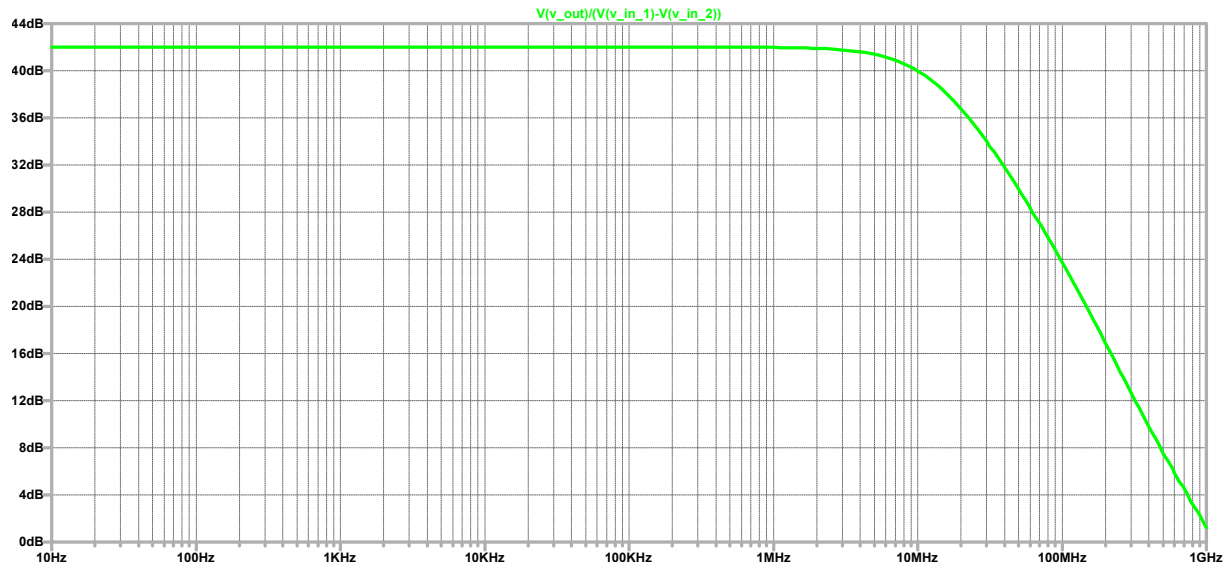

Figure 1: Differential gain of differential pair

2. Common mode gain
   From figure 2, $A_{CM} = -48.4dB$

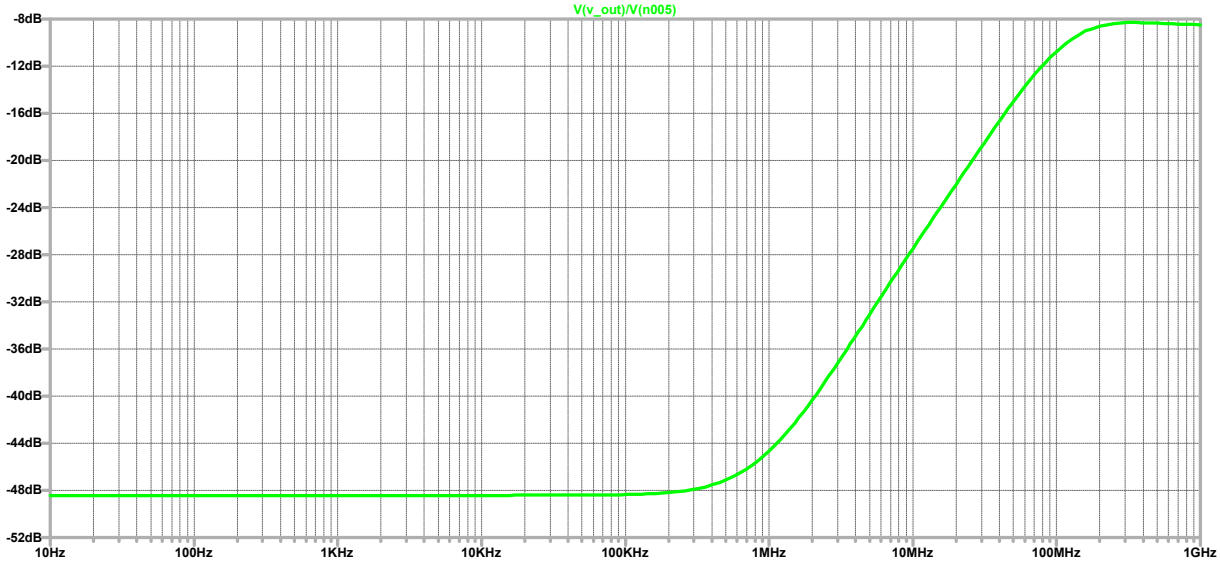

Figure 2: Common mode gain of differential pair

Problem 4

The final circuit NMOS differential pair with PMOS current mirror load and cascode stages are shown in figure 3.

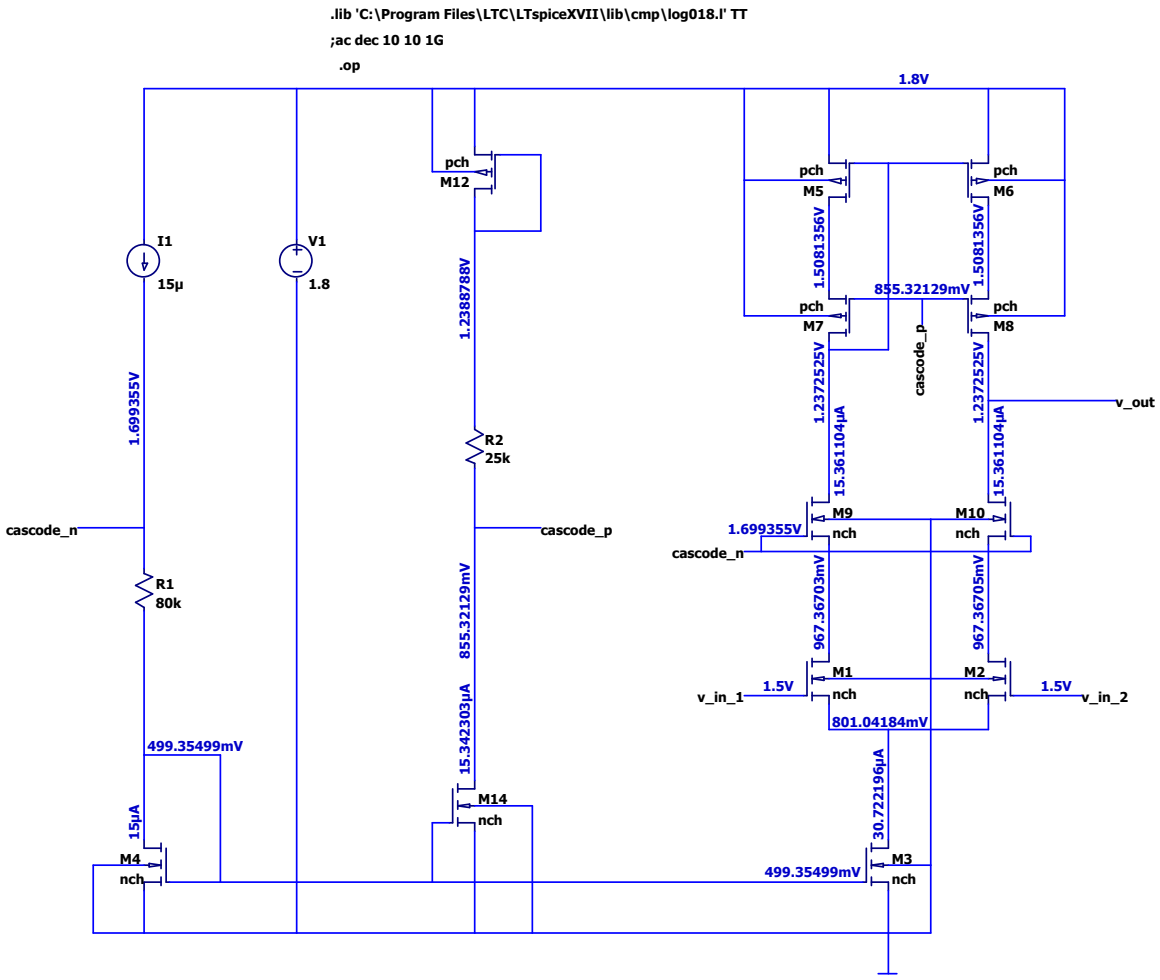

Figure 3: Bias points for NMOS differential pair with PMOS current mirror load and cascode stage

The following images show the device operating points.

Name:	m12	m8	m7	m6	m5
Model:	pch.2	pch.2	pch.2	pch.2	pch.2
Id:	-1.53e-05	-1.54e-05	-1.54e-05	-1.54e-05	-1.54e-05
Vgs:	-5.61e-01	-6.53e-01	-6.53e-01	-5.63e-01	-5.63e-01
Vds:	-5.61e-01	-2.71e-01	-2.71e-01	-2.92e-01	-2.92e-01
Vbs:	0.00e+00	2.92e-01	2.92e-01	0.00e+00	0.00e+00
Vth:	-4.57e-01	-5.45e-01	-5.45e-01	-4.57e-01	-4.57e-01
Vdsat:	-1.28e-01	-1.33e-01	-1.33e-01	-1.29e-01	-1.29e-01
Gm:	1.97e-04	1.94e-04	1.94e-04	1.96e-04	1.96e-04
Gds:	8.96e-07	1.96e-06	1.96e-06	1.66e-06	1.66e-06
Gmb	6.44e-05	5.66e-05	5.66e-05	6.40e-05	6.40e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	9.83e-15	9.83e-15	9.83e-15	9.83e-15	9.83e-15
Cgdov:	9.83e-15	9.83e-15	9.83e-15	9.83e-15	9.83e-15
Cgbov:	2.73e-16	2.73e-16	2.73e-16	2.73e-16	2.73e-16
dQgdVgb:	1.93e-13	1.94e-13	1.94e-13	1.94e-13	1.94e-13
dQgdVdb:	-9.85e-15	-1.03e-14	-1.03e-14	-1.02e-14	-1.02e-14
dQgdVsb:	-1.69e-13	-1.73e-13	-1.73e-13	-1.70e-13	-1.70e-13
dQddVgb:	-1.02e-14	-1.19e-14	-1.19e-14	-1.15e-14	-1.15e-14
dQddVdb:	9.95e-15	1.10e-14	1.10e-14	1.07e-14	1.07e-14
dQddVsb:	3.63e-16	1.42e-15	1.42e-15	1.27e-15	1.27e-15
dQbdVgb:	-2.96e-14	-2.75e-14	-2.75e-14	-2.93e-14	-2.93e-14
dQbdVdb:	-2.27e-17	-2.79e-16	-2.79e-16	-2.18e-16	-2.18e-16
dQbdVsb:	-3.10e-14	-2.50e-14	-2.50e-14	-3.12e-14	-3.12e-14

Figure 4: Spice error log file 1

Name:	m14	m10	m9	m4	m3
Model:	nch.2	nch.2	nch.2	nch.2	nch.2
Id:	1.53e-05	1.54e-05	1.54e-05	1.50e-05	3.07e-05
Vgs:	4.99e-01	7.32e-01	7.32e-01	4.99e-01	4.99e-01
Vds:	8.55e-01	2.70e-01	2.70e-01	4.99e-01	8.01e-01
Vbs:	0.00e+00	-9.67e-01	-9.67e-01	0.00e+00	0.00e+00
Vth:	4.81e-01	7.09e-01	7.09e-01	4.81e-01	4.81e-01
Vdsat:	9.47e-02	1.00e-01	1.00e-01	9.47e-02	9.48e-02
Gm:	2.63e-04	2.65e-04	2.65e-04	2.58e-04	5.27e-04
Gds:	9.01e-07	2.04e-06	2.04e-06	1.07e-06	1.83e-06
Gmb	7.60e-05	5.35e-05	5.35e-05	7.47e-05	1.53e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	5.49e-15	5.49e-15	5.49e-15	5.49e-15	1.10e-14
Cgdov:	5.49e-15	5.49e-15	5.49e-15	5.49e-15	1.10e-14
Cgbov:	1.81e-16	1.81e-16	1.81e-16	1.81e-16	1.81e-16
dQgdVgb:	7.03e-14	7.00e-14	7.00e-14	7.03e-14	1.41e-13
dQgdVdb:	-5.48e-15	-5.55e-15	-5.55e-15	-5.49e-15	-1.10e-14
dQgdVsb:	-4.81e-14	-5.33e-14	-5.33e-14	-4.81e-14	-9.66e-14
dQddVgb:	-5.53e-15	-5.91e-15	-5.91e-15	-5.60e-15	-1.11e-14
dQddVdb:	5.49e-15	5.62e-15	5.62e-15	5.51e-15	1.10e-14
dQddVsb:	4.37e-17	3.76e-16	3.76e-16	1.21e-16	9.99e-17
dQbdVgb:	-1.52e-14	-1.11e-14	-1.11e-14	-1.52e-14	-3.03e-14
dQbdVdb:	1.95e-18	-1.44e-17	-1.44e-17	-4.56e-19	3.69e-18
dQbdVsb:	-1.43e-14	-9.78e-15	-9.78e-15	-1.43e-14	-2.91e-14

Figure 5: Spice error log file 2

Name:	m2	m1
Model:	nch.2	nch.2
Id:	1.54e-05	1.54e-05
Vgs:	6.99e-01	6.99e-01
Vds:	1.66e-01	1.66e-01
Vbs:	-8.01e-01	-8.01e-01
Vth:	6.75e-01	6.75e-01
Vdsat:	1.00e-01	1.00e-01
Gm:	2.61e-04	2.61e-04
Gds:	6.49e-06	6.49e-06
Gmb	5.53e-05	5.53e-05
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	5.49e-15	5.49e-15
Cgdov:	5.49e-15	5.49e-15
Cgbov:	1.81e-16	1.81e-16
dQgdVgb:	7.11e-14	7.11e-14
dQgdVdb:	-5.76e-15	-5.76e-15
dQgdVsb:	-5.38e-14	-5.38e-14
dQddVgb:	-6.63e-15	-6.63e-15
dQddVdb:	6.02e-15	6.02e-15
dQddVsb:	8.49e-16	8.49e-16
dQbdVgb:	-1.13e-14	-1.13e-14
dQbdVdb:	-6.77e-17	-6.77e-17
dQbdVsb:	-1.05e-14	-1.05e-14

Figure 6: Spice error log file 3

The following sections roughly estimates the bias points for saturation.

(a) For biasing $V_{cascode_n}$, the staturation conditions for each transistor starting from the ground.

1. M3

$$V_{D3} \geq V_{G3} - V_{TH3}$$

2. M1

$$\begin{aligned} V_{D1} - V_{S1} &\geq V_{G1} - V_{S1} - V_{TH1} \\ V_{D1} &\geq V_{G1} - V_{TH1} \\ V_{D1} &\geq 1.5V - 0.675V \\ V_{D1} &\geq 0.825V \end{aligned}$$

3. M9

$$\begin{aligned} V_{D9} - V_{S9} &\geq V_{G9} - V_{S9} - V_{TH9} \\ V_{D9} &\geq V_{G9} - V_{TH9} \\ V_{G9} &\leq V_{D9} + V_{TH9} \end{aligned}$$

$$\begin{aligned} V_{G9} - V_{S9} &\geq V_{TH9} \\ V_{G9} &\geq 0.825V + 0.709V \\ V_{G9} &\geq 1.534V \end{aligned}$$

Since only one current source is available and using a NMOS current mirror PMOS diode connected current source will not be able to acheive voltage of 1.534V ($>$ V_{DD} - V_{THp}), the remaining option is to attach a resistor to the current source circuit line.

The required resistance,

$$\begin{aligned} R &\geq \frac{1.5V - V_{D4}}{15\mu A} \\ &\geq 68.93k\Omega \end{aligned}$$

In the simulation, the resistance is increased to 80k to increase the DM gain.

1. For biasing $V_{cascode_p}$, a maximum voltage for keeping the circuit in saturation is desired for maximizing the voltage swing. The saturation for transistor starting from V_{DD}.

(a) M5 Maximum value of V_D

$$\begin{aligned} Max(V_D) &= V_{DD} - |V_{TH5}| \\ &= 1.8V - 0.457V \\ &= 1.343V \end{aligned}$$

(b) M7

$$\begin{aligned} V_{S7} - V_{G7} &\geq V_{TH7} \\ V_{G7} &\leq 1.343V - 0.543V \\ V_{G7} &\leq 0.8V \end{aligned}$$

In this case using a NMOS current mirror PMOS diode connected current source is possible for bias voltage of 0.8V ($<$ V_{DD} - V_{THp}).

The required resistance,

$$\begin{aligned} R &= \frac{1.8V - V_{TH12} - V_{D4}}{15\mu A} \\ &= 27.376k\Omega \end{aligned}$$

Similar to the previous section, the resistance in the simulation is decreased to increase the DM gain.

Problem 5

(a) Differential gain

From figure 7, $A_{DM} = 73.6dB$

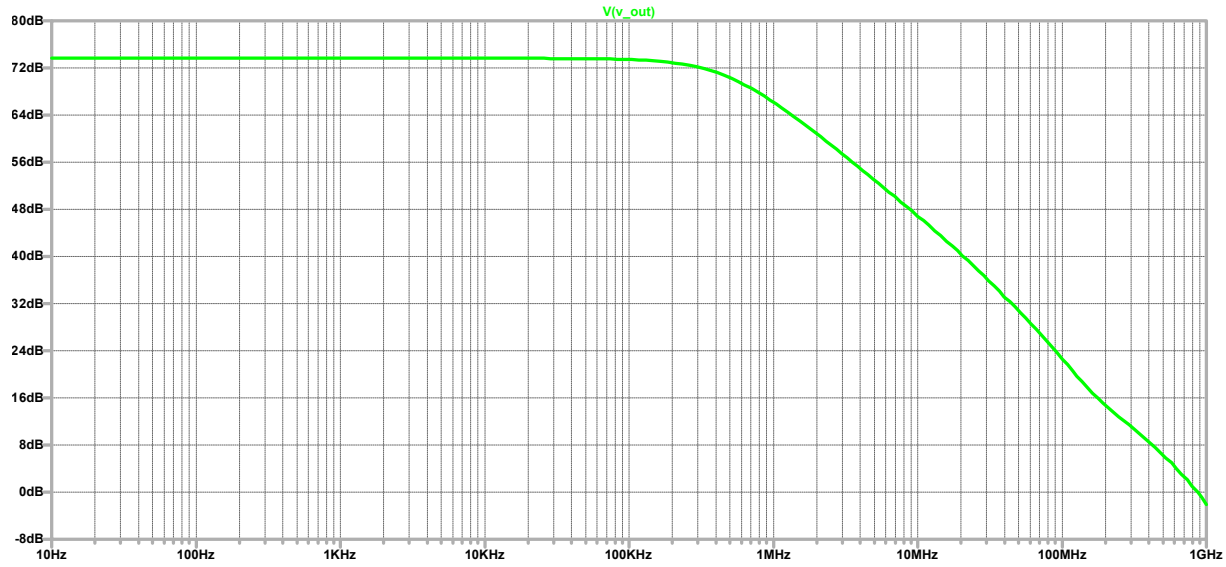

Figure 7: Differential gain of differential pair

(b) Common-mode gain

From figure 8, $A_{CM} = -48.4dB$

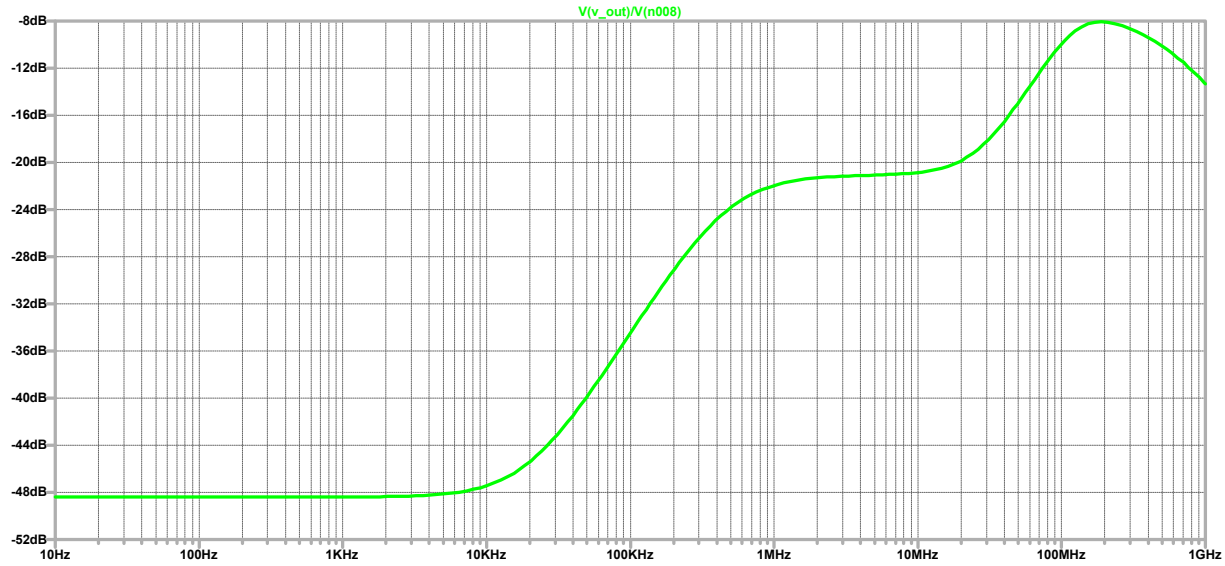

Figure 8: Common mode gain of differential pair