EE4C10 Analog Circuit Design Fundamentals

RF Track

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October 26, 2021

Contents

Simulation Files

Each question with simulation files will have their respective subfolder. The subsubfolder should be self-explainatory depending on the question, (e.g., unmatched => unmatched LNA, r-matched => only resistive matching, matched => fully matched, base => only used for testing (can be ignored, no plots made from this file)).

Running the simulation files should be able to directly plot the graphs used (configured in the *.plt file). The folders for each question are arranged as follows after extracting:

spice		
	q1	
		c
		d
	q2	
		a
		b
	q4	
		ab
		c
		d
	q5	
		a
	q6	
		a
		b
		c
		d

Part 1

Question 1

A. Optimum gate width, W_g, for current budget of $12mA$.

The maximum current,

$$I_{d,max} = \frac{I_{total}}{N_{fingers} \cdot W_g}$$
$$W_g = \frac{I_{total}}{N_{fingers} \cdot I_{d,max}}$$
$$= 200\mu m$$

In the case of 5 fingers,

$$W_{g,f} = \frac{W_g}{N_f} \quad = 40\mu m$$

B. Highest g_m of given current budget.

g_m for long channel devices,

$$g_m = \frac{\partial I_d}{\partial V_{gs}}$$
$$\approx \sqrt{2\mu_{nOX}\frac{W}{L}I_D}$$
$$\approx 0.0833S$$

C. Gate biasing conditions.

Drain current of MOS transistor, using the parameters extracted from LTspice

$$i_{ds} = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{gs} - V_{th})^2(1 + \lambda V_{ds})$$
$$V_{gs} = \sqrt{\frac{2i_{ds}}{\mu_n C_{OX}}\frac{L}{W}\frac{1}{1 + \lambda V_{ds}}} + V_{th}$$
$$= 0.766V$$

Parameter sweep in LTspice in Figure 1, gives a value of

$$V_{gs} = 0.7V$$
$$i_{ds} = 11.9mA$$

g_m in LTspice

$$g_m = 0.0774S$$

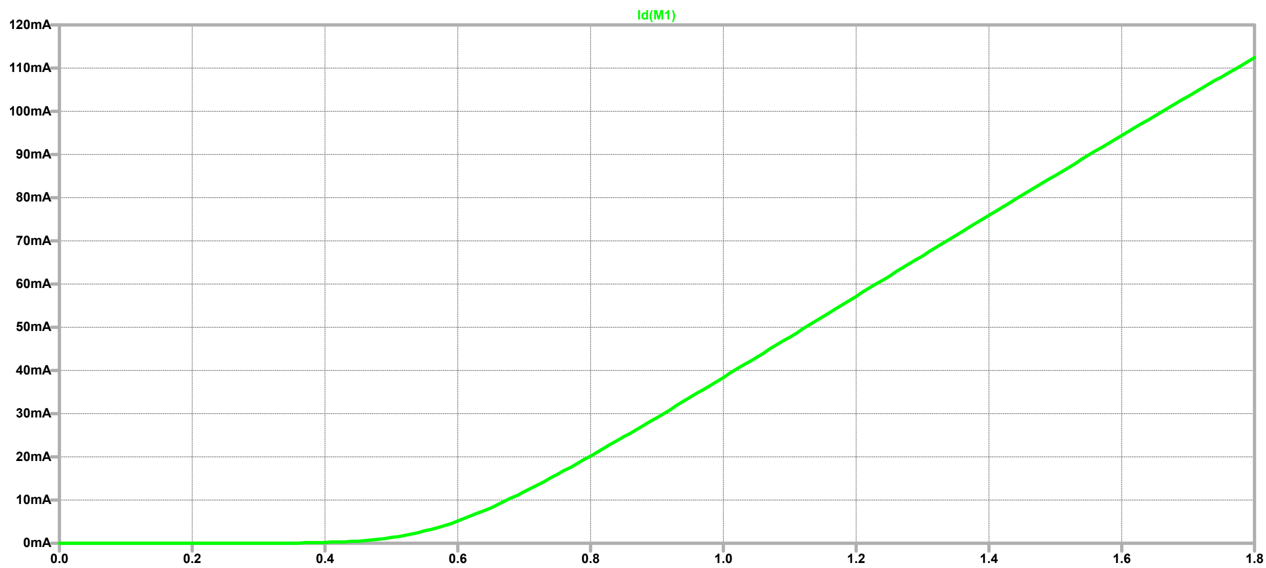

Figure 1: $I_{ds} - V_{gs}$ sweep

D. Impedance at low frequency:

(a) Input, $R_{in} = \infty\Omega$

(b) Output, $R_{out} = r_o = \frac{1}{\lambda I_d max} = 613\Omega$

The simulated input and output impedance from LTspice are shown in 2. It can be observed that Z_{in} tends to infinity at low frequencies, while Z_{out} is around 603Ω

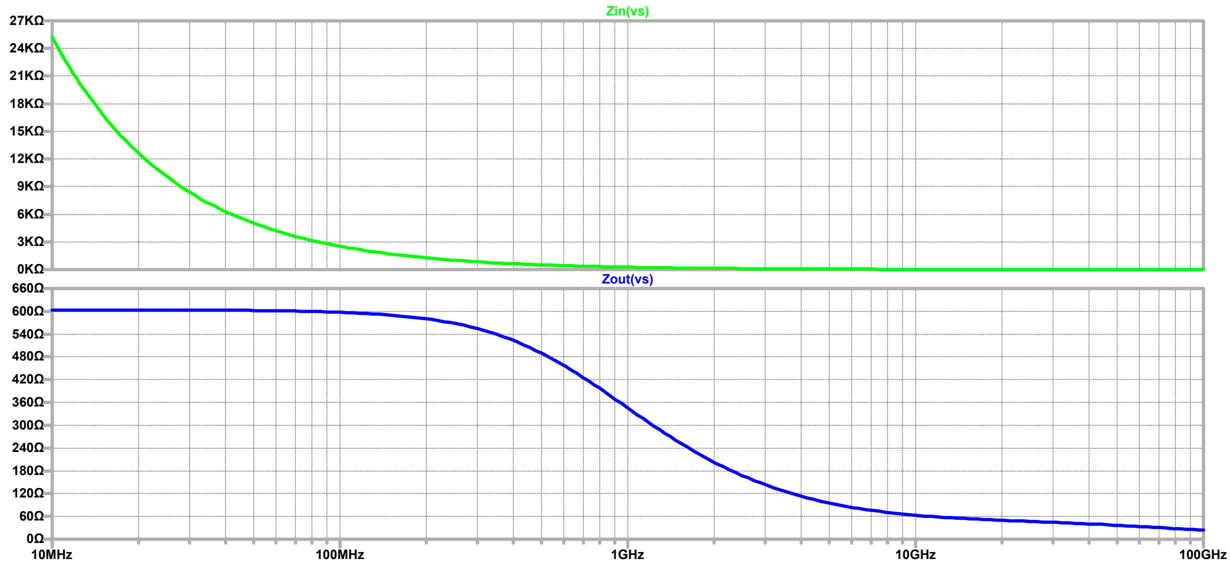

Figure 2: $Z_{in} and Z_{out} of amplifier$

E. Capacitance of:

1. C_{gs}

$$
\begin{aligned}
C_{gs} &= \frac{2WLC_{OX}}{3} + WC_{OV} \\
&= \frac{2W_g LC_{OX}}{3} + W_g C_{OV} \\
&= 2.79 \times 10^{-13} F
\end{aligned}
$$

2. C_{gd}

$$
\begin{aligned}
C_{gd} &= WC_{OV} \\
&= W_g C_{OV} \\
&= 7.32 \times 10^{-14} F
\end{aligned}
$$

Question 2

A. Ohmic matching,

1 Input

$$
\begin{aligned}
\frac{1}{R_{in,matched}} &= \frac{1}{R_1} + \frac{1}{R_{in}} \\
\frac{1}{50} &= \frac{1}{R_1} \\
R_1 &= 50\Omega
\end{aligned}
$$

2 Output

$$
\begin{aligned}
\frac{1}{R_{out,matched}} &= \frac{1}{R_2} + \frac{1}{R_{out}} \\
\frac{1}{50} &= \frac{1}{R_2} + \frac{1}{603} \\
R_2 &= 54.5\Omega
\end{aligned}
$$

B. Expected gain

$$\begin{aligned}
G_m &= g_m = 0.0774S \\
R_{out} &= r_o//R_2//R_L \\
&= 25\Omega \\
A_V &= -1.94
\end{aligned}$$

C. Input capacitance

$$\begin{aligned}
C_{in} &= C_{gs} + \frac{C_{ds}}{1 - A_V} \\
&= 4.94 \times 10^{-13} F
\end{aligned}$$

D. Matching input inductance, L_1.

Input impedance

$$\begin{aligned}
L_1 &\approx \frac{1}{\omega^2 C_{IN}} \\
&= 1.69 \times 10^{-9} H
\end{aligned}$$

Question 3

From previous section,

$$\begin{aligned}
G_m &= g_m = 0.0774S \\
R_{out} &= r_o//R_2//R_L \\
&= 25\Omega \\
A_V &= -1.94
\end{aligned}$$

Noise figure, F,

$$F = 1 + \frac{N_a}{N_i G}$$

$$\begin{aligned}
N_i &= \overline{v_{R_s}^2} \\
&= \frac{4kT}{R_s}(R_s//R_{in})^2 \\
&= \frac{4kT}{R_s}(R_s//R_1)^2
\end{aligned}$$

$$\begin{aligned}
N_a &= \overline{v_{R_1}^2} + \overline{v_M^2} + \overline{v_{R_2}^2} \\
&= \frac{4kTR_1(R_s//R_{in})^2}{R_1} A_v^2 + (4kT\gamma g_m + \frac{4kT}{R_2})R_{out}^2 \\
&= 4kT[\frac{(R_S//R_1)^2}{R_1} A_v^2 + (\gamma g_m + \frac{1}{R_2})R_{out}^2]
\end{aligned}$$

$$\begin{aligned}
F &= 1 + \frac{\frac{(R_S//R_1)^2}{R_1} A_v^2 + (\gamma g_m + \frac{1}{R_2})R_{out}^2}{\frac{[(R_s//R_1)A_v]^2}{R_s}} \\
&= 2.93 \\
&= 4.6dB
\end{aligned}$$

Question 4

A. Ohmic matching. If the circuit is correctly matched the real part of the input impedance, $Re\{Z_{in}(f = 5.5GHz)\} = 50\Omega$, the real part of the output impedance, $Re\{Z_{out}(f = 5.5GHz)\} = 50\Omega$. The simulated Z_{in} and Z_{out} are shown in Figure 3, the matched impedance values are shown in 1.

Since the resistance will also affect the resonanance frequency of an RLC circuit, the fine tuned values used are shown in Table 2.

B. Reactance matching. If the circuit is correctly matched the imaginary part of the input impedance, $Im\{Z_{in}(f = 5.5GHz)\} = 0\Omega$, the imaginary part of the output impedance, $Im\{Z_{out}(f = 5.5GHz)\} = 0\Omega$. The simulated Z_{in} and Z_{out} are shown in Figure 3, the matched impedance values are shown in 1.

Since the resistance will also affect the resonanance frequency of an RLC circuit, the fine tuned values used are shown in Table 2.

Table 1: Matched impedance at $f = 5.5GHz$

Impedance	Value
Z_{in}	$49.97 - 0.13i\Omega$
Z_{out}	$49.69 - 0.15i\Omega$

Table 2: Impedance matching parameters

Parameter	Value
R_1	49Ω
R_2	53Ω
L_1	$1.65nH$
L_2	$3.99nH$

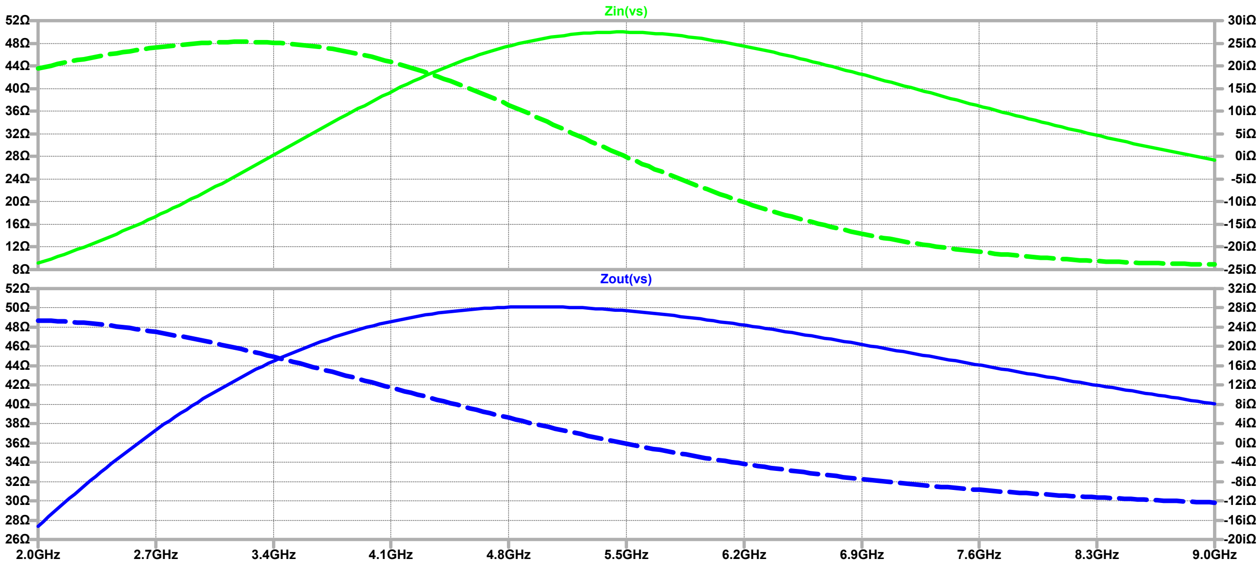

Figure 3: Z_{in} and Z_{out}

C. S-parameters,

1) No matching

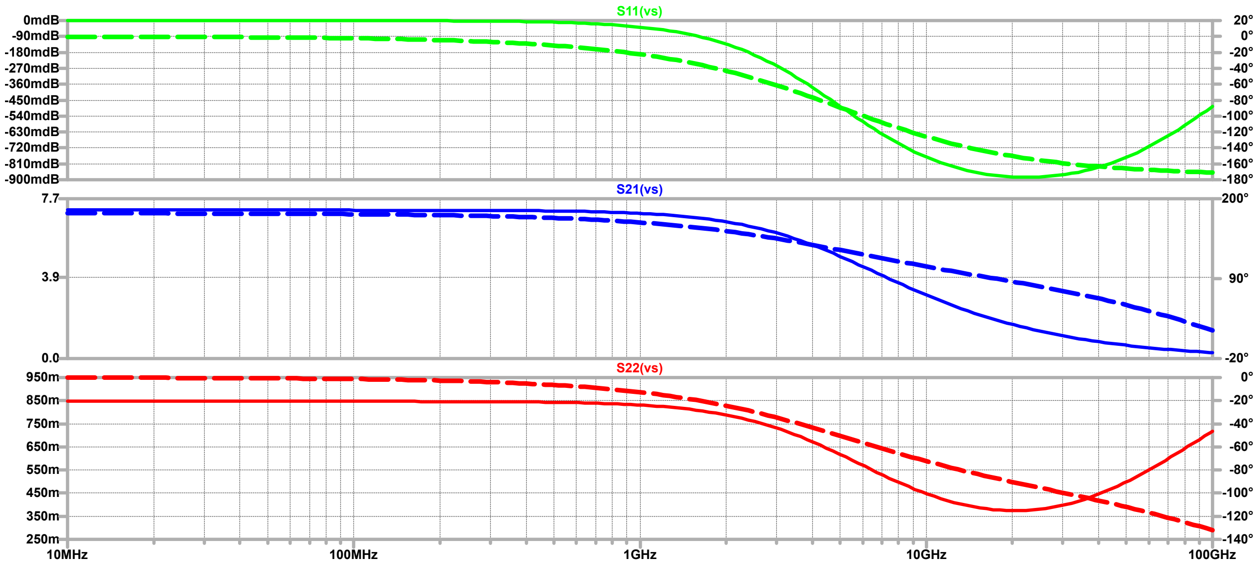

Figure 4: S-parameters without matching

2) Ohmic matching

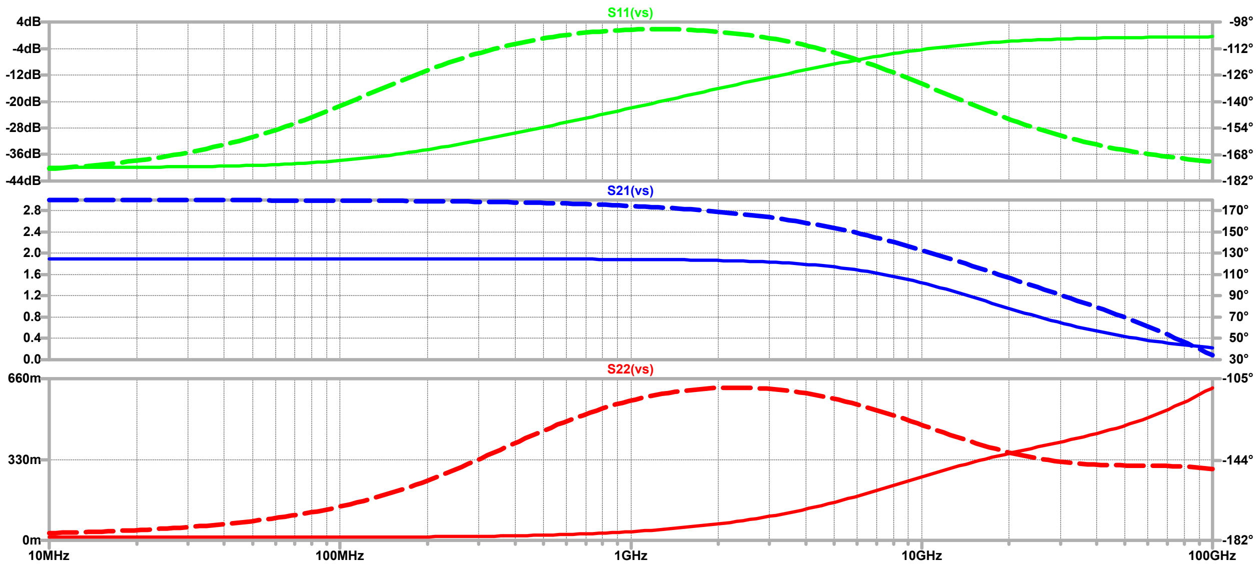

Figure 5: S-parameters with ohmic matching

3) Ohmic and conjugate matching

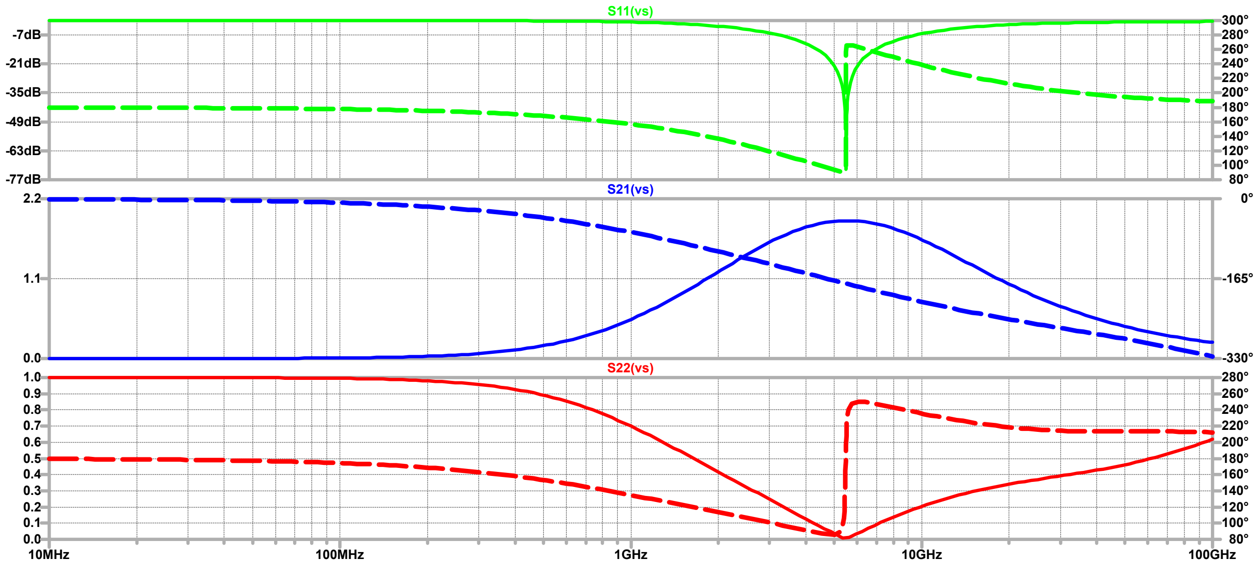

Figure 6: S-parameters with ohmic and conjugate matching

D. Noise Factor,

1) No matching

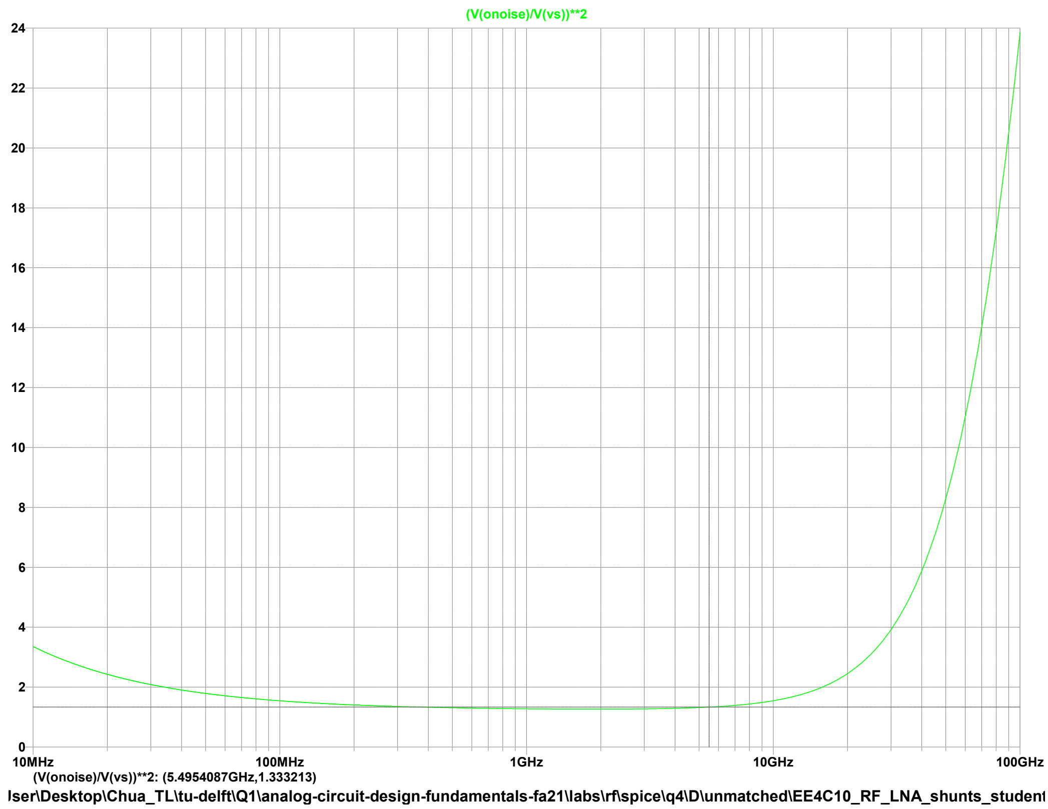

Figure 7: Noise Factor without matching

2) Ohmic matching

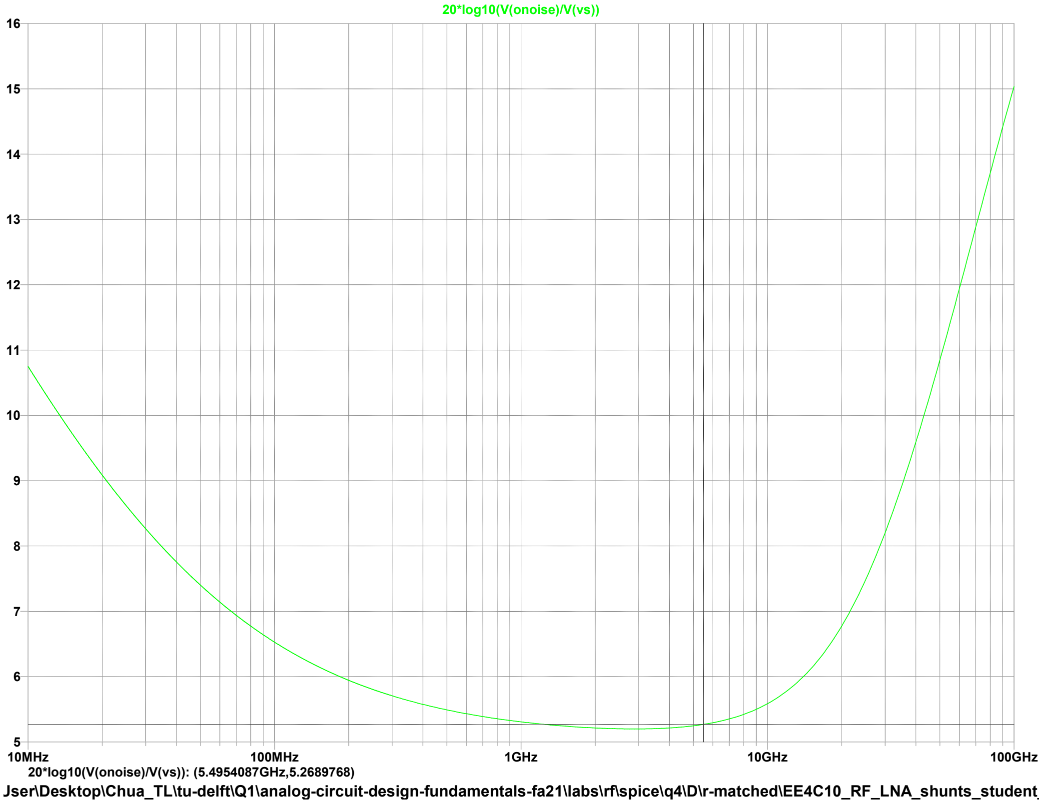

Figure 8: Noise Factor with ohmic matching

3) Ohmic and conjugate matching

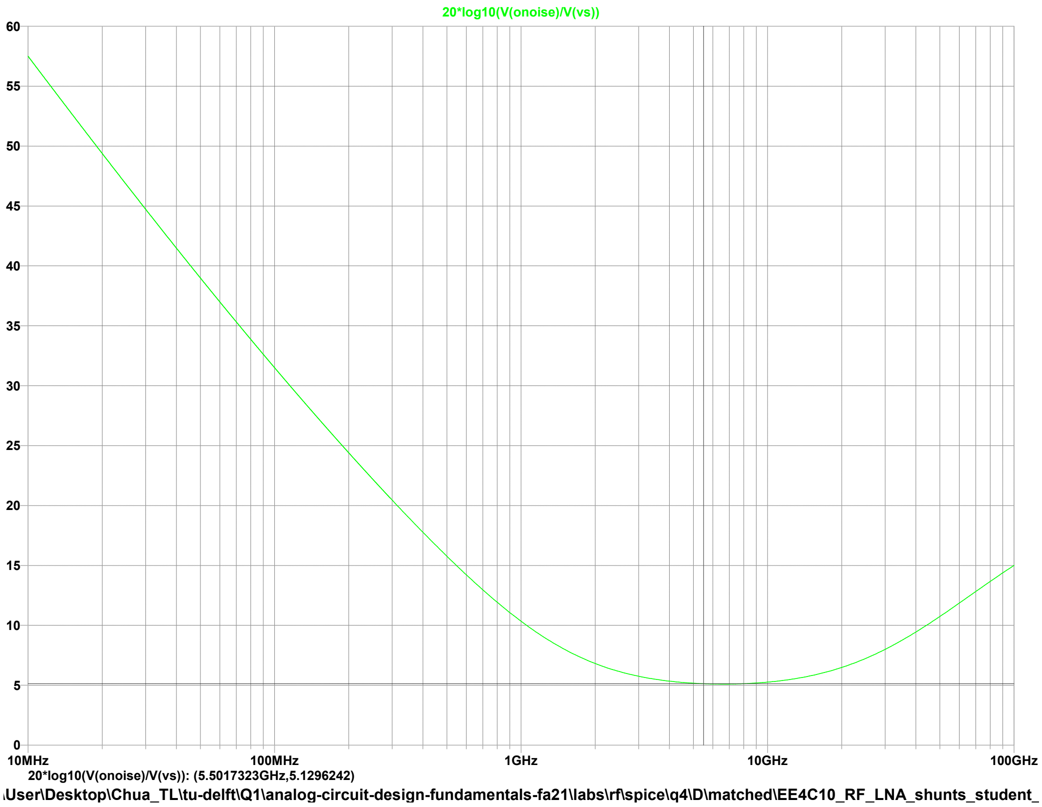

Figure 9: Noise Factor with ohmic and conjugate matching

E. LNA performance using simplistic "design method".

1) Advantages

- Low refection coefficient, $S_{11} = -71dB$.
- Simple matching procedure due to uncorrelated input and output.

2) Disadvantages.

- Low gain, $S_{21} = 1.9dB$.
- High noise figure of $F \approx 5dB$.
- The bandwith of the amplifier is small.

Part 2

Question 5

A. From Question 1, the gate width, W_g, and gate bias voltage, V_{gs},

$$\begin{aligned} W_g &= 200\mu m \\ V_{gs} &= 0.7V \end{aligned}$$

Input impedance of LNA,

$$R_{in} = \frac{V_X}{I_X}$$

$$\begin{aligned} g_m V_x + \frac{V_x - I_x(R_f r_o)}{r_o R_L} &= I_x \\ V_x(g_m + \frac{r_o + R_L}{r_o R_L}) &= I_X(1 + \frac{R_f(r_o + R_L)}{r_o R_L}) \\ R_f &= \frac{R_{in}(r_o + R_L + g_m r_o R_m) - r_o R_L}{r_o + R_L} \\ &= 182\Omega \end{aligned}$$

B. The input impedance is matched using the reseistance of the single loop feedback, however, the output impedance is still unmatched. Since the task is to only match the input impedance, a single-loop feedback is sufficient.

C. Methods for improving the performance of the single loop feedback:

- Using a cascode-stage. The input and output impedancences will be isolated, which will aid in the input and output impedance matching. However, the bias volatage has to be increased to maintain the current budget.
- Adding an extra stage for increasing the overall gain of the amplifier, this will increase the power consumption.
- From the slides, the 2 methods above can be combined with adding "phantom zeros" to increase or provide sufficient the gain bandwidth, which in the current design lacks.

Question 6

A. Input and output impedance with $R_f = 182\Omega$.

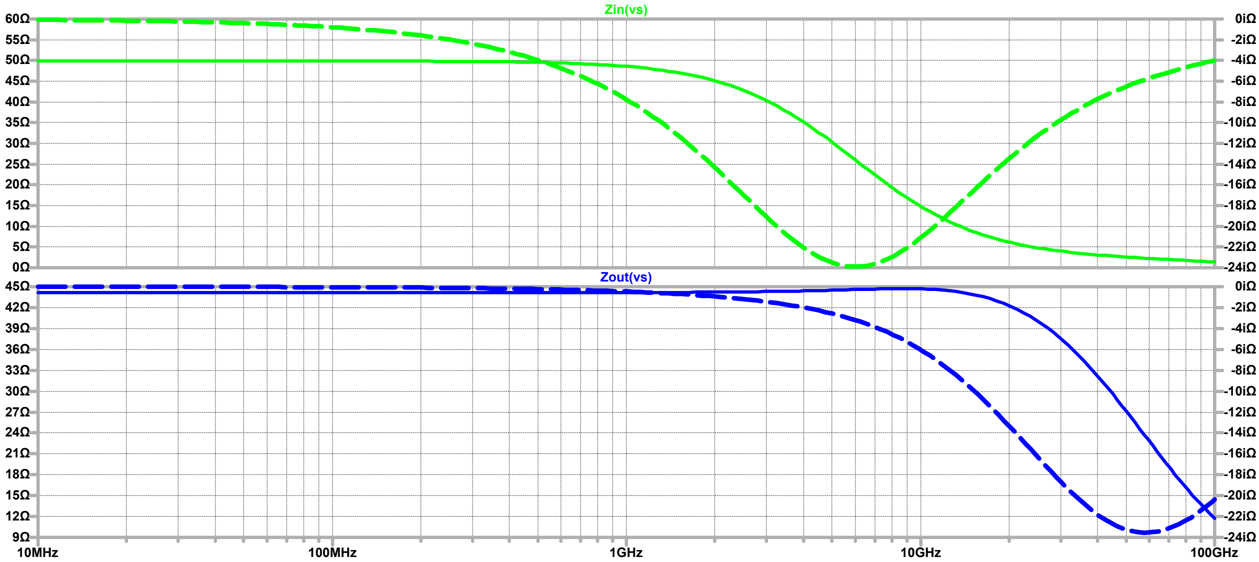

Figure 10: Input and output impedance with resistive feedback, $R_f = 182\Omega$.

B. S-Parameters with $R_f = 182\Omega$.

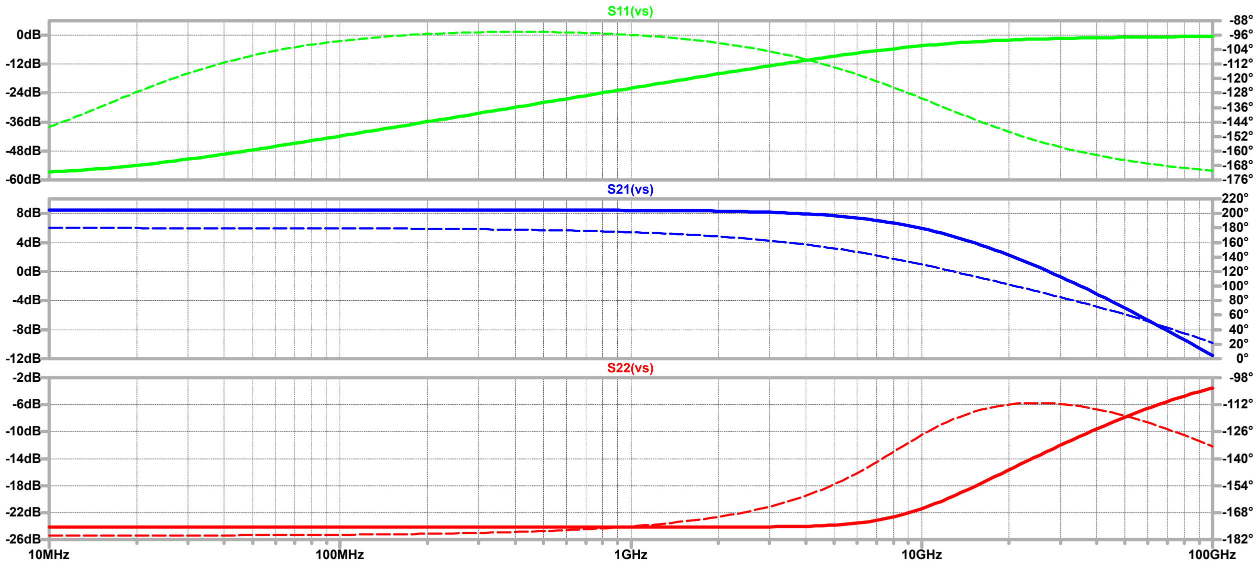

Figure 11: S-parameters with resistive feedback, $R_f = 182\Omega$.

C. Noise figure with $R_f = 182\Omega$.

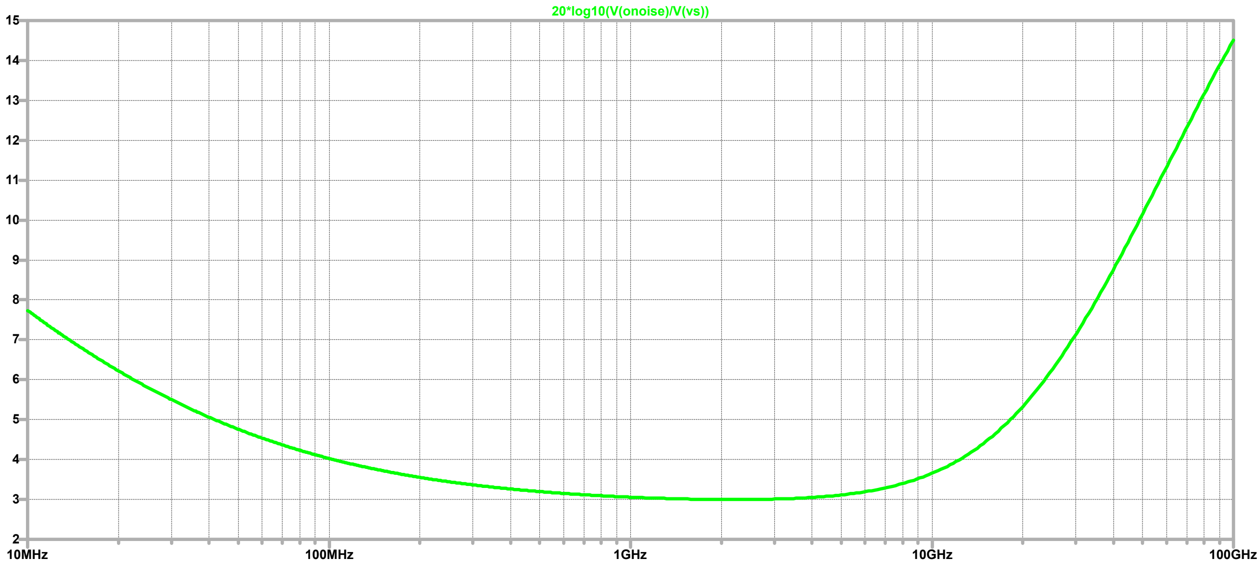

Figure 12: Noise figure with resistive feedback, $R_f = 182\Omega$.

D. 2 methods were attempted for designing the LNA:

(a) Matching $Z_{in} \approx 50\Omega$ and $Z_{out} \approx 50\Omega$ at 5.5GHz. After some fine tuning, the matching element values are shown in Table 3. The specifications of the resulting LNA are shown in Table 6, with the simulated results in Figure 13, 14, and 15.

Table 3: Impedance matching parameters for $Z_{in} \approx 50\Omega$ and $Z_{out} \approx 50\Omega$

Parameter	Value
R_f	154Ω
L_{in}	$1.2nH$
L_{out}	$2nH$

Table 4: LNA Specifications for matching parameters for $Z_{in} \approx 50\Omega$ and $Z_{out} \approx 50\Omega$

Parameter	Value
Z_{in}	$54.0 + 1.2i\Omega$
Z_{out}	$47.9 + 0.9i\Omega$
S_{11}	$-27.7dB$
Gain, S_{21}	$7.64dB$
S_{22}	$-32.7dB$
Bandwidth, BW	$> 1GHz$
Noise Figure, F	$3.4dB$

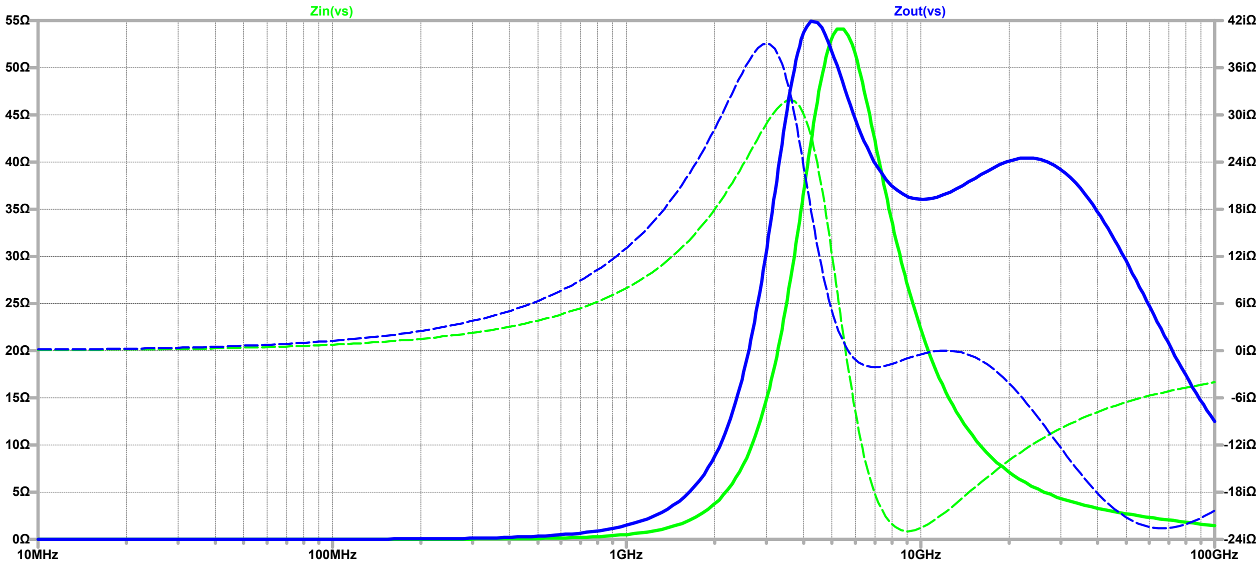

Figure 13: Input and output impedance with $Z_{in} \approx 50\Omega$ and $Z_{out} \approx 50\Omega$

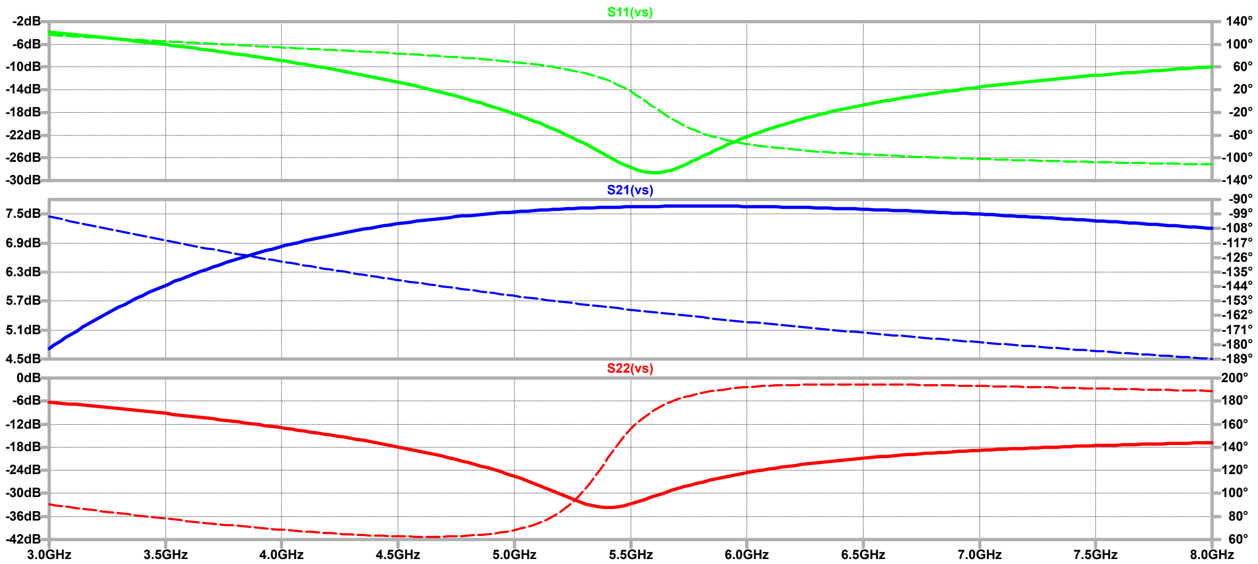

Figure 14: S-parameters with $Z_{in} \approx 50\Omega$ and $Z_{out} \approx 50\Omega$

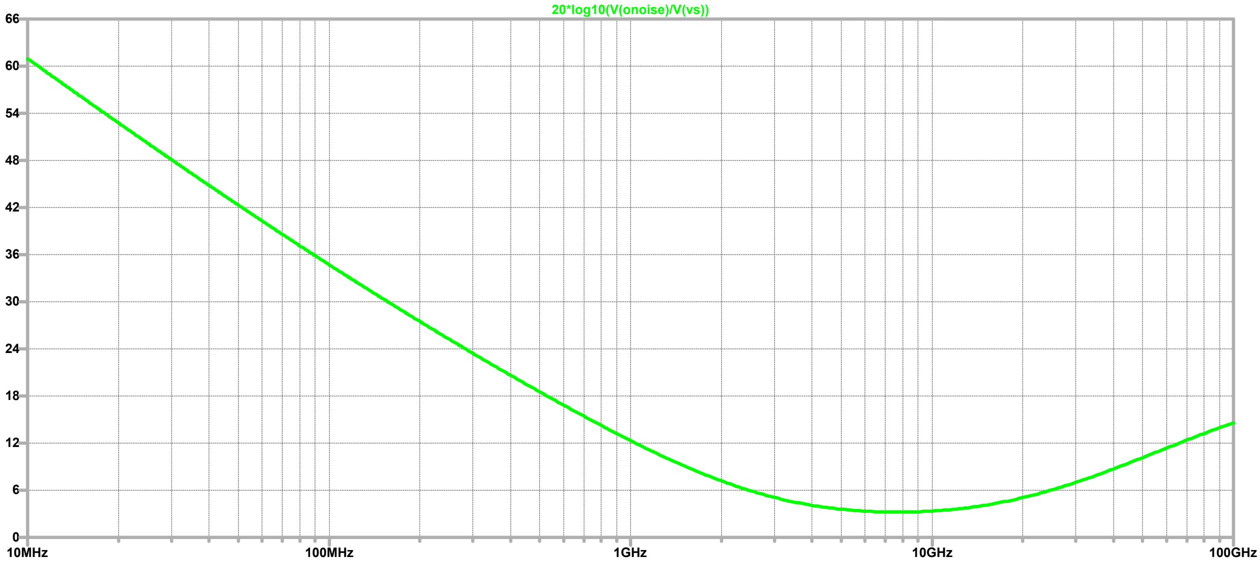

Figure 15: Noise figure with $Z_{in} \approx 50\Omega$ and $Z_{out} \approx 50\Omega$

(b) Matching the minimum of S11 and S22 to be at 5.5GHz. After some fine tuning, the matching element values are shown in Table 5. The specifications of the resulting LNA are shown in Table 6, with the simulated results in Figure 16, 17, and 18.

Table 5: Impedance matching parameters for minimum S_{11} and S_{22}.

Parameter	Value
R_f	182Ω
L_{in}	$1.3nH$
L_{out}	$2.5nH$

Table 6: LNA Specifications for matching parameters with minimum S_{11} and S_{22}.

Parameter	Value
Z_{in}	$58.8 - 2.5i\Omega$
Z_{out}	$52.3 - 5.2i\Omega$
S_{11}	$-21.6dB$
Gain, S_{21}	$8.7dB$
S_{22}	$-25.1dB$
Bandwidth, BW	$> 1GHz$
Noise Figure, F	$3.0dB$

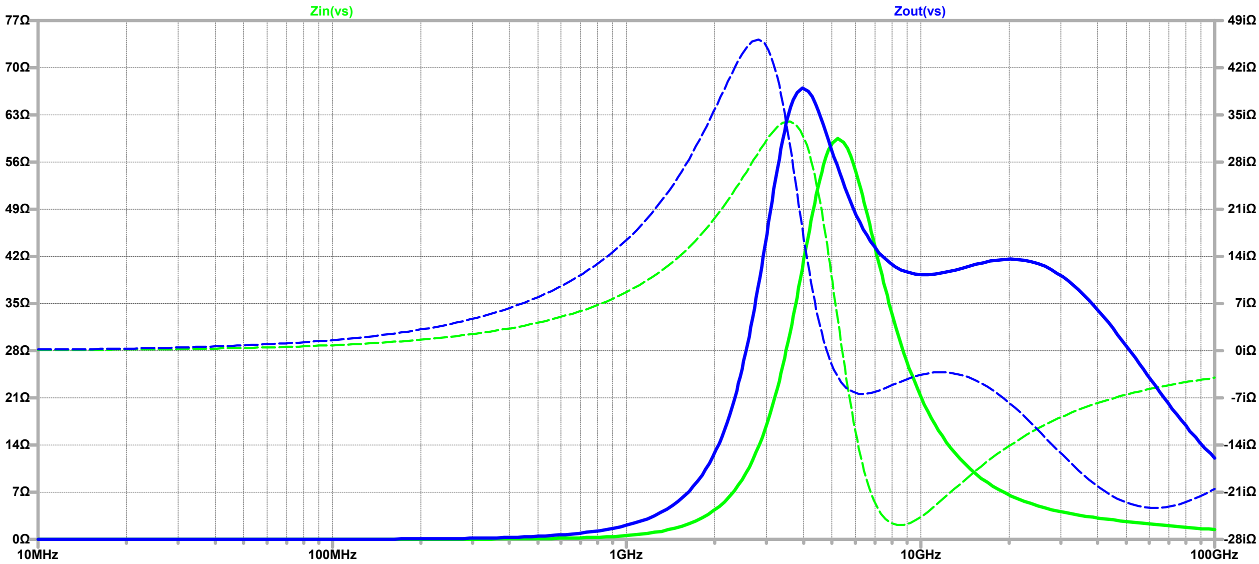

Figure 16: Input and output impedance with minimum S_{11} and S_{22}.

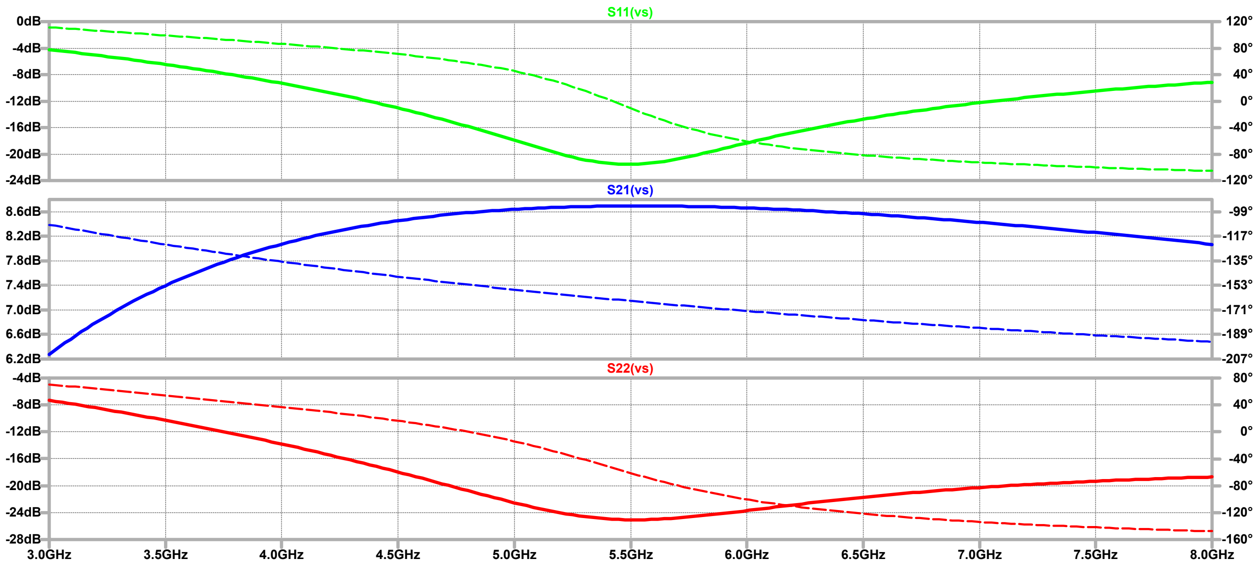

Figure 17: S-parameters with minimum S_{11} and S_{22}.

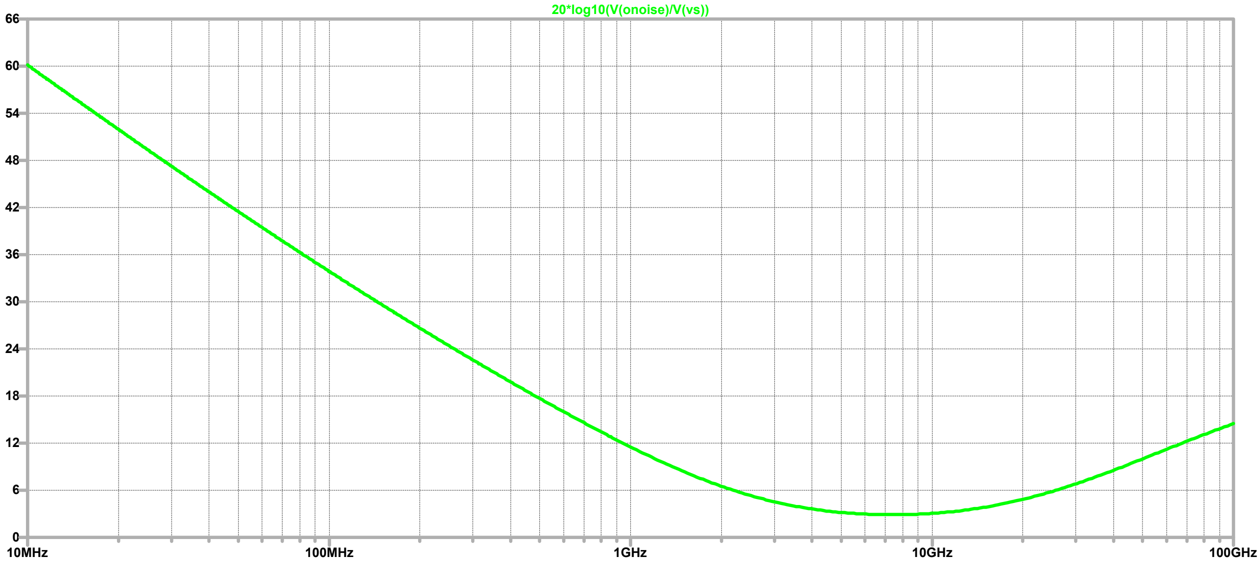

Figure 18: Noise figure with minimum S_{11} and S_{22}.

E. The final design of the LNA have met the required specifications. However, the input and output impedance matching are not exactly 50Ω. This can be improved using a cascode stage to isolate the input and output impedancences. On inspection, the bandwidth of the LNA is small, further improvements using "phantom zeroes" is most likely required.