TU Delft

EE4C10 Analog Circuit Design Fundamentals

Homework Assignment V

Start date: 8/10/2021

Due date: 15/10/2021

Please upload your homework via Brightspace

FORMULARY

Drain thermal noise of a MOSFET:

$$\overline{I_{n,th}^2} = 4kT\gamma g_m \left[\frac{I^2}{Hz}\right], \tag{1}$$

where $k = 1.38 \cdot 10^{-23} J/K$, and $\gamma = 2/3$.

Flicker noise at the gate

$$\overline{V_{n,1/f}^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \left[\frac{V^2}{Hz}\right]. \tag{2}$$

For this assignment, assume the absolute temperature T=300K.

INSTRUCTIONS

1. Solutions must be submitted in a PDF file named "Name_Surname_HW5.pdf". Descriptions of the simulation and simulation results must be included in the PDF file, while schematics used for simulations must be compressed in a single ZIP file named "Name_Surname_HW5.zip" containing the ltspice files. Converted photographs are not accepted. Please avoid hand-written reports and graphs. Simulation waveforms should have a white background.

2. Late submissions would not be accepted.

3. For the simulation's questions, attach an ltspice file used for each question that must be directly simulatable.

PROBLEMS

1. Consider the circuit in Figure 1. The transistor operates in saturation. Ignore channel length modulation.
   a. **(0.5 points)** Derive the analytical expressions for the input and output referred thermal noise power spectral density (PSD) in terms of g_m and R_D.
   b. **(0.5 points)** Assume $K = 10^{-25}V^2F, V_{th,n} = 0.5V, \mu_n C_{ox} = 300\mu A/V^2, W = 10\mu m, L = 1\mu m, C_{ox} = 9 \cdot 10^{-3}F/m^2, R_D = 10k\Omega$ and $V_{in,dc} = 0.7V$. Calculate the input and output referred flicker noise PSD.
   c. **(0.5 points)** Calculate the 1/f noise corner frequency and sketch the total input and output referred noise PSD, using the parameters given in (b).

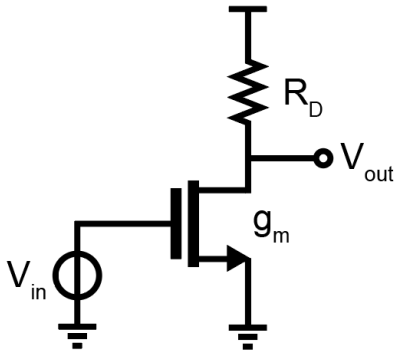

Figure 1

   d. **(0.5 points)** Calculate the RMS integrated noise voltage at the output from 1kHz to 10MHz. Which noise dominates: thermal or flicker noise?
   e. **(0.5 points)** Calculate the RMS integrated noise voltage at the output from 1kHz to 10kHz. Which noise dominates: thermal or flicker noise?
   f. **(0.5 points)** An input signal is provided to the amplifier. What is the SNR (in dB) when the output signal is $1V_{RMS}$ in the band from 1kHz to 10MHz?

2. Consider the circuit in Figure 2. The transistor operates in saturation. Ignore body effect.
   a. **(0.5 points)** Derive an analytical expression for the output referred thermal noise PSD in terms of g_m, r_0, and R_s.
   b. **(0.5 points)** What is the ratio between the thermal noise contributions of the transistors and R_s?
   c. **(0.5 points)** Calculate the input-referred thermal noise PSD given $I_D = 10\mu A$, $g_m/I_D = 10V^{-1}$, $g_m r_0 = 20$, and $R_S = 10k\Omega$.

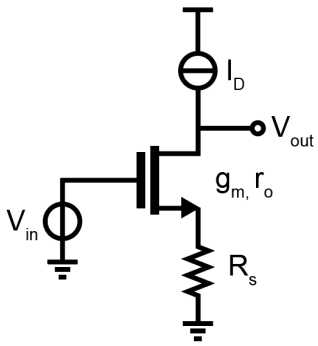

Figure 2

3. Consider the circuit in Figure 3. Ignore channel length modulation and body effect.
   a. **(0.5 points)** Derive an analytical expression for the noise contribution of the current mirror M_{N3} and M_{N4} to the thermal noise PSD *differentially* across V_{out} in terms of g_{m1-4} and C_L.

b. **(0.5 points)** Derive an analytical expression for the noise contribution of the current mirror M_{N3} and M_{N4} to the thermal noise PSD of the *common mode* of V_{out} in terms of g_{m1-4} and C_L, assuming M_{N3}=M_{N4}. How does the result change if I_B and the width of M_{N3} are doubled?
c. **(0.5 points)** Derive the analytical expressions for the differential input and output referred thermal noise PSD in terms of g_{m1-4} and C_L.
d. **(0.5 points)** Derive an expression for the integrated differential output thermal noise in terms of g_{m1}, g_{m2}, and C_L.
e. **(0.5 points)** Evaluate the result of (d) given M_{N3}=M_{N4}, $I_B = 20\mu A$, $C_L = 1pF$, $g_m/I_D = 20V^{-1}$ for $M_{N1,2}$, and $g_m/I_D = 5V^{-1}$ for $M_{N3,4}$ and $M_{P1,2}$.

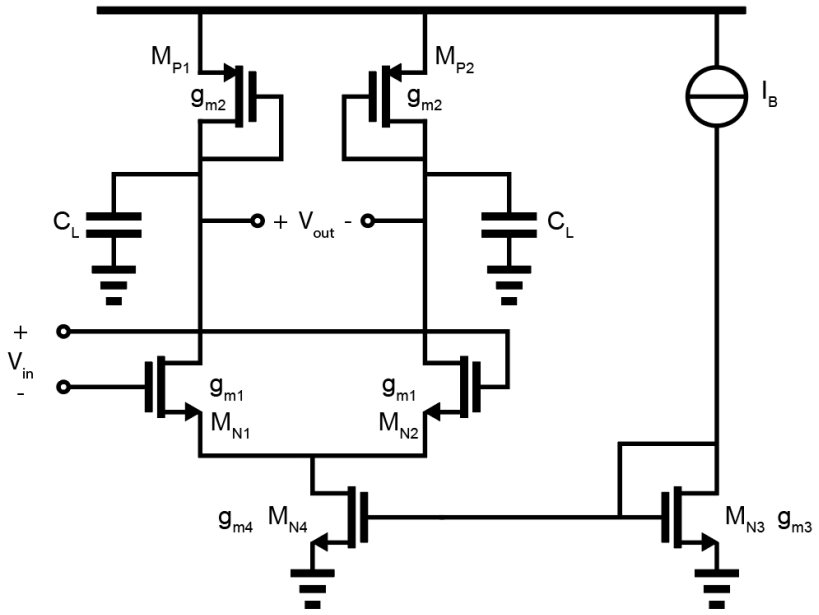

Figure 3

SIMULATIONS

Introduction

The noise simulation is a small signal analysis like an AC-analysis. The simulator calculates the transfer of each noise contribution to the output. To set-up the noise simulation you need to define the output node and input source, as well as the start frequency, stop frequency and number of points.

The output noise can be plotted by a left-click on the output node. To view the integrated output noise, Ctrl+left click the data trace label.

The simulator can show the noise contribution of each separate circuit element, by a left-click on the element. The different noise contributions of a transistor (flicker noise, thermal noise of channel, and the thermal noise of the drain and source resistances) can be plotted separately. By a right-click on the area of the plot and choosing 'Add Traces', you can plot all available noise contributions, as well as the total input referred noise.

Task

In this exercise, you will design a differential amplifier using the structure of Figure 3 to meet the specifications below.

Low freq. small signal gain $A_v=\lvert V_{out}/V_{in}\rvert$	≥5 V/V
3 dB bandwidth	≥ 2 MHz
Integrated output noise (1 Hz to 100 MHz)	≤ 100 μV_{RMS}
1/f noise corner	≤ 100 kHz
Supply voltage	1.8 V
Input common-mode voltage	0.9 V

Steps

1. **(0.5 points)** Analyze the amplifier circuit and derive the expressions for A_v and 3 dB bandwidth in terms of g_{m1-4} and C_L.
2. Consider the following noise budget as a starting point (note this is arbitrary at this point, but in practice, it would depend on the optimization target, e.g., chosen to minimize power consumption): the thermal noise and flicker should contribute equally (50%/50%) to the total output integrated noise. Find g_{m1-4} and C_L to meet the gain, bandwidth, and thermal noise targets.
3. **(0.5 points)** Size the transistors and I_B to give the target g_{m1-4} as defined in Step 2. Create a schematic in ltspice. Include in the report a schematic clearly showing transistor sizing, I_B and C_L.
4. **(0.5 points)** Simulate the circuit to verify if it satisfies A_v and the 3 dB bandwidth specifications. Plot $\lvert V_{out}/V_{in}\rvert$ from AC simulation and clearly annotate A_v and the 3 dB bandwidth.
5. **(0.5 points)** Perform a noise simulation and plot the output referred noise PSD in log scale. If there is too much 1/f noise, identify which devices contribute the most 1/f noise and increase their size. Note that this will increase the parasitic capacitance and thus the effective total load capacitance, so the other performance parameters might be affected. Reduce C_L accordingly and make other adjustments if needed until you meet all the specifications. For this point, you do not need to keep the 50%/50% noise budget for thermal and flicker noise.
6. **(0.5 points)** Perform a transient simulation and plot the transient waveform across V_{out} with a 10 mVpp sinusoidal input of 1 MHz.
7. **(0.5 points)** Compile a comparison table that summarizes your final simulated performance and compares it against the specifications. **Also make sure that your reported results for Step 3-6 correspond to the final circuit.**

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---- END OF THE ASSIGNMENT ----