TU Delft

EE4C10 Analog Circuit Design Fundamentals

Homework Assignment IV

Start date: 1/10/2021

Due date: 8/10/2021

Please upload your homework via Bright Space

INSTRUCTIONS

1. Solutions must be submitted in PDF file named "Name_Surname_HW4.pdf". Description of the simulations and the simulations results must be included in the PDF file, while the schematics used for simulations must be compressed in a single ZIP file named "Name_Surname_HW4.zip" containing the LTspice files. Converted photographs are not accepted. Hand-written reports and hand-drawn sketches are acceptable. Simulation waveforms should have a white background.

2. Late submissions would not be accepted.

3. For the simulations questions (3 & 4), attach directly simulatable LTspice files.

1. Consider the common gate stage as shown in figure 1. Assume M_1 in saturation and consider the body effect. Neglect the channel length modulation ($\lambda = 0$). Only consider the parasitic capacitances shown in the figure.
   a) Calculate the DC gain of the stage V_{out}/V_{in}.
   b) Write the expression of the output node.
   c) Calculate the input impedance Z_{in}.
   d) Calculate the total capacitance seen at the source of M_1 and write the expression of the pole.

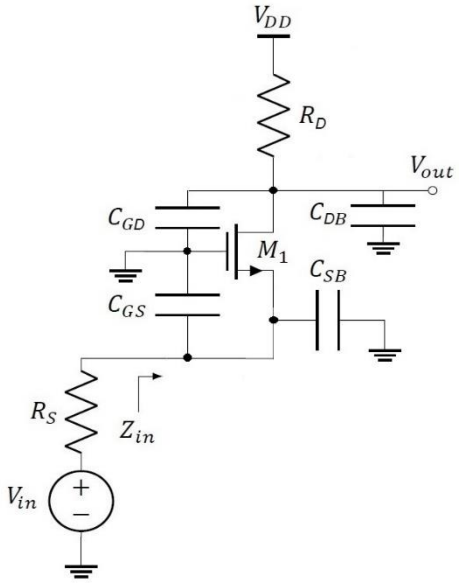

Figure 1 – Common gate stage

2. Consider the common drain stage as shown in figure 2. Assume M_1 in saturation and neglect both body effect and channel length modulation ($\lambda = 0$). Only consider the parasitic capacitances shown in the figure.
   a) Calculate the transfer function of the stage $V_{out}(s)/V_{in}(s)$.
   b) From the transfer function, find out the expressions for each pole.
   c) Calculate input impedance Z_{in}.

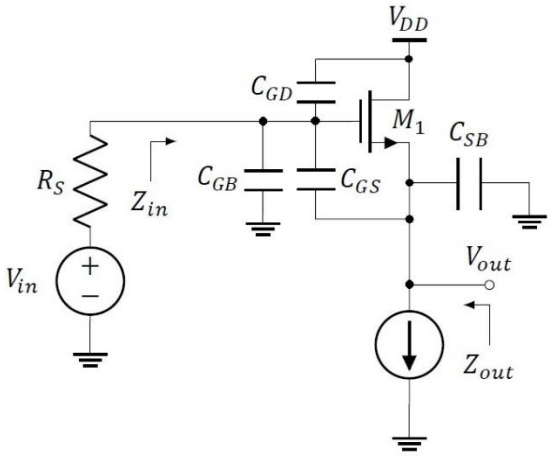

Figure 2 – common drain stage

3. Consider the circuit shown in Figure 3, designed in 0.18μm CMOS technology
   (a) Build a test bench and plot the V_{OUT}-vs.-V_{IN} transfer curve using DC sweep simulation (DC sweep range: 0V - 1.8V).
   (b) Plot the transient output signal for input signal $V_{in} = 0.9 + 0.001\text{Sin}(2000\pi t)$ from 0 to 5ms.
   (c) Plot the transfer function from 1Hz to 100GHz, report the DC gain and the dominant pole of the network.
   (d) Adding capacitor C_o = 0.1nF into the output node, plot the transfer function from 1Hz to 100GHz, report the DC gain and the dominant pole of the network.
   (e) Continue with the circuit in (d). Using the frequency of the dominant pole and total capacitance seen from the output node, try to estimate the equivalent resistance seen from the output node.

4. Consider the circuit shown in Figure 4, designed in 0.18μm CMOS technology
   (a) Build a test bench and plot the V_{OUT}-vs.-V_{IN} transfer curve using DC sweep simulation (DC sweep range: 0V - 1.8V).
   (b) Plot the transient output signal for input signal $V_{in} = 1.25 + 0.005\text{Sin}(2000\pi t)$ from 0 to 5ms.
   (c) Plot the transfer function from 1 to 10 GHz, report the DC gain and the dominant pole of the network.
   (d) Using the transfer function plotted in part c, estimate the GBWP (gain bandwidth product) of the network.

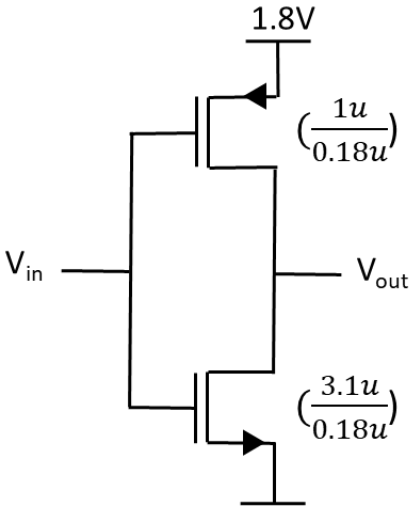

Figure 3 – CMOS Inverter

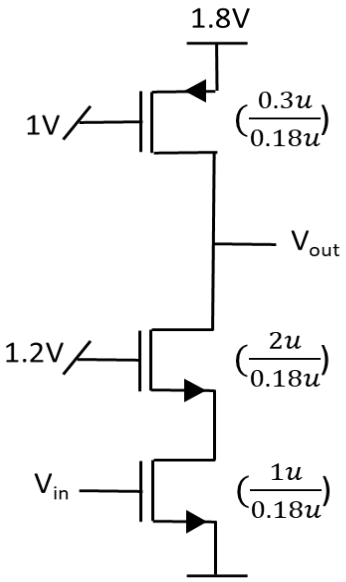

Figure 4 – Cascoded CMOS Network

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