EE4C10, Track Specific Assignment: RF Design of an LNA

Specifications

- Center frequency filter and LNA = 5.5GHz
- BW = 1 GHz
- Gain > 8.5 dB
- Current Budget = 12mA
- Supply voltage = 1.8 V
- Noise Figure = 3.0 dB @ 290K (standard noise reference temperature)
- S_{11} < -20dB

Available technology

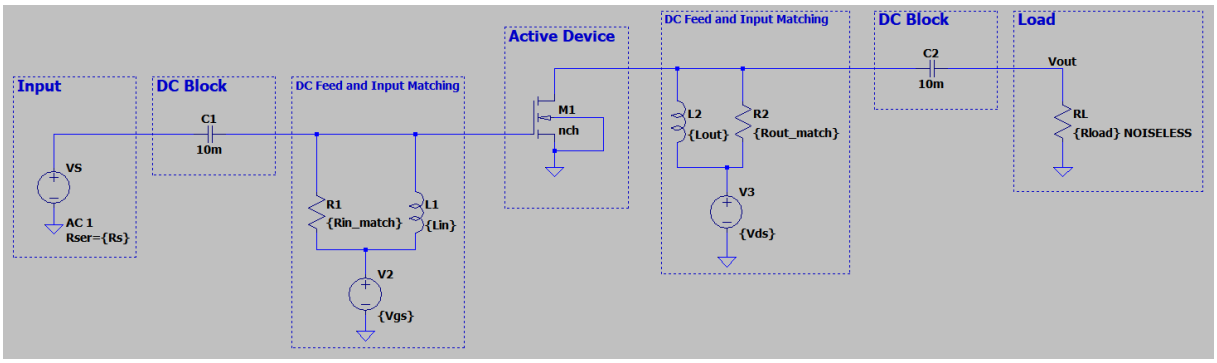
For reasons of simplicity we assume that the capacitances of the active devices have no DC dependency.

In a normal design you would need to determine the optimum transistor dimensions and its related biasing conditions yourself. However, we will address this in more detail within the RF track. So, to save you time we provide you with most of the transistor dimensions below.

- **L = 0.18 um**
- **W = to be determined later in the assignment**
- **Number of fingers = 5**
- $Kp = Cox.\mu_n = 2.6 \cdot 10^{-4}\ A/V^2$ → Kp is the trans-conductance coefficient, which depends on Cox (gate-oxide capacitance per unit area) and the μ_n (electron mobility)
- $C_{ox} = 8.58 \cdot 10^{-3}\ F/m\text{^}2$ → Oxide capacitance per gate area
- $C_{ov} = 3.66 \cdot 10^{-10}\ F/m$ → Overlap capacitance per gate width
- $\lambda = 0.136$ → gate channel-length modulation
- $I_{d,max} = 60\ A/m$ → maximum current per unit gate width (before performance drops due to high current effects)

Part I: LNA using shunt resistors

First, we are going to consider the consequences of using a (too) simplistic design approach toward achieving the required matching condition at the input/output of our "LNA". For this we first consider / use the circuit topology below.



As one can observe, a not so experienced RF designer has used simple shunt resistors at the input and output of a common-source FET stage, to achieve impedance matched conditions at input and output. In addition, also inductors have been added to resonate out the capacitive loading at input and output.

With the above in mind try to answer the following questions.

Question 1 – Device size, biasing and characterization

A. To achieve the highest speed for an active device you need to use the highest current density allowed before high current effects set in. For a given current budget, this approach will give you the optimum gate width (W_g) for a FET. For the current budget of 12mA, using the maximum current density indicated for the active devices, what is the optimum W for your FET device?

B. Using simple model equations, what is the highest gm which can be reached for the given current budget. Use the long-channel equations provided in slide 2, movie2: RF_Components?

C. For our current budget of $12\ mA$, choose the appropriate gate bias conditions, this can be done analytically or in simulation by sweeping the gate-source voltage and plotting the drain-current vs. V_{gs}, using operating point simulation.
Note: the total gate width in the simulation is the width of one device (W) multiplied by the number of fingers (M). Use 5 fingers, as provided in the template. It is not possible to use one finger, because then the device size is too large.
Now that the FET is correctly biased, check the calculated gm using LTspice.

D. When ignoring the device capacitances, what are the input and output impedances offered by the active device? Check your calculations in LTSPICE by using a two-port simulation. The simulation set-up is already prepared to run this simulation. Use 'add trace' to plot Zout(VS).

E. Calculate C_{gs} and C_{gd}. Take into account the width of the device. Use the equations provided in equations provided in slide 4, movie2: RF_Components.

Question 2 – Matching

Now that we have determined the size of the FET, and calculated the relevant properties, we can apply the correct matching conditions to the LNA.

A. What should be the value of the resistors (R1 and R2) to achieve impedance matched conditions for the ohmic part (ignore the capacitances for this question)?

B. With your already calculated gm (part I) and the effective resistors (R2 and RL) at the transistor output, calculate now the expected voltage-gain of the FET (ignoring RS).

C. Calculate the effective input capacitance (C_{in}) of the FET with C_{gs} and C_{gd}, using the previously calculated voltage gain, and the Miller approximation.

D. Using the calculated C_{in}, what should be the value of the inductors (L1) to achieve conjugate matched conditions (compensate imaginary part due to device capacitances)?

In previous questions, you have determined the component values for the input matching, as if the output impedance was already at matched impedances. It is also possible to find the capacitance seen from the output, however, in this particular case, the Miller approximation for determining the effective output capacitance does not work, due to the use of an ohmic source with a parallel inductor. Consequently, in this homework assignment we skip this part (and refer to the RF track for suitable techniques) and use in this assignment **L_{out}=3.9nH**.

Question 3 - Noise

Next, calculate analytically the in-band noise figure F of your LNA at 5.5GHz (slide 15, movie2: RF_Components). For this calculation:

- Assume the load (RL) to be noise free
- To keep the equations simple, ignore the impact of all reactive elements (remove all capacitors and inductors)
- Since your source impedance is equal to 50Ω (a value different from zero or infinity), your noise sources at the output of the FET should after transformation result in a noise current source, as well as, a noise voltage source at the input of your FET device (for reference, see Razavi page 239). After which, the total noise contributed by the network can be calculated as well the noise figure F.
- Since we are operating at RF, thermal noise dominates, and the 1/f-noise can be neglected.

Question 4 – Simulation

We are going to check our hand calculations using simulations.

A. First check the ohmic part of the matching (the shunt resistors). To do so, plot the simulated Zin(VS) and Zout(VS). How do you see whether the ohmic matching is correct?

B. Check the input and output impedance with the matching inductors. Plot Zin(VS) and Zout(VS). Show that the input and output capacitances are resonated out by the inductors at the RF bandwidth.

C. Plot S11, S21, S22. Do this for the circuit without matching, with ohmic matching only, and with conjugate matching. Note that S-parameters should be plotted in dB. The s-parameters are calculated in LTspice by the two-port simulation. After running the ac-simulation you can

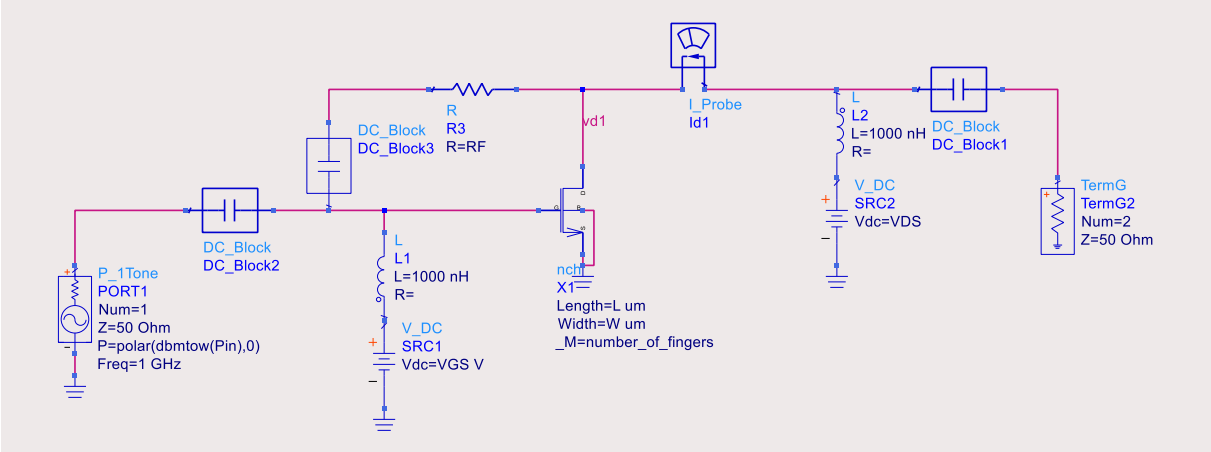
simply add them via 'add trace'.

D. Plot the noise figure (in dB), again for the circuit without matching, with ohmic matching only, and with conjugate matching. The noise figure equation should be added manually.

E. Explain very briefly your simulation results and the advantages / disadvantages of adding the resistors and inductors. Indicate what in your opinion is the achieved LNA performance using this simplistic “design method”. For this purpose, also consider the achieved matching (s11) gain (s21) and the noise figure.

Part II: LNA with resistive Feedback

To improve the filter – LNA performance, next we consider the use of a single resistive feedback loop to fix the input impedance (In this schematic we have used the inductors initially only as DC feed)



Question 5 – Design the resistive feedback

A. For our current budget of 12 mA, choose the appropriate device size of the FET and calculate analytically the value of feedback resistance to offer an ohmic part of the input impedance of 50 ohm, again neglecting the impact of all reactive elements (remove all capacitors and inductors).

B. Why can we use in this concept only one feedback loop to fix the input impedance, rather than the two feedback loops that are typically promoted in analogue feedback design (e.g. as in the slide set) to fix the input impedance to a specific impedance level (different from zero or infinity)?

C. BONUS: Can we still improve this performance for this single loop feedback concept (without changing the current budget)???
   → Indicate HOW (give clear suggestions, but you do not to implement a modified design)

Question 6 – Simulation of resistive feedback

Show that your earlier hand calculations are correct by providing simulation evidence (S11, S21 and the noise figure F).

A. Plot the input and output impedances of the LNA with resistive feedback.
B. Plot s11, s21 and s22 of the LNA with resistive feedback.
C. Plot the noise figure of the LNA with resistive feedback.
D. We did not resonate out the input and output capacitances with the feed inductor. Although they are not exactly the correct values, you can use values found in the previous part (with shunt resistors). Can you adjust the inductance Lin to improve the matching, and achieve the specified S11?
E. What are your main conclusions, about your LNA design?