TU Delft

EE4C10Analog Circuit Design Fundamentals

Homework Assignment II

Start date: 18/09/2020

Due date: 25/09/2020

Please upload your homework via Brightspace

FORMULARY

Quadratic Model: Eq. 1 and Eq. 2

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (1)$$

$$I_D = \mu C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (2)$$

INSTRUCTIONS

1. Solutions must be submitted in PDF file named "Name_Surname_HW2.pdf". Description of the simulations and the simulations results must be included in the PDF file, while the schematics used for simulations must be compressed in a single ZIP file named "Name_Surname_HW1.zip" containing the LTspice files. Converted photographs are not accepted. Hand-written reports and hand-drawn sketches are acceptable. Simulation waveforms should have a white background.

2. Late submissions would not be accepted.

3. For the simulations questions attach an LTspice file used for each question (from 4 to 6) that must be directly simulatable.

4. Please neglect the channel length modulation effect while calculating the bias points.

1. The circuit in Fig.1 has $(W/L)_1$= 36 μm/0.18 μm, $(W/L)_2$=18 μm/0.36 μm, $\mu_n C_{ox}$=210 μA/V^2, $\mu_p C_{ox}$=70 μA/V^2, λ_p= 0.1 V^{-1}, λ_n= 0.2 V^{-1}, V_{DD}=3.3 V, and I_{D1}=I_{D2}= 0.25 mA when both devices are saturated.
(a) Calculate the overdrive voltages (V_{gt}) of M1 and M2.
(b)Calculate the small-signal voltage gain (V_{OUT}/V_{IN})
(c) Calculate the maximum output swing while both devices are saturated.
(d) Propose a method to increase the maximum output swing while keeping the small signal voltage gain same.

2. In Fig. 2, assume$(W/L)_1$=36 μm/0.36 μm , $(W/L)_2$=18 μm/0.18 μm , I_{D1}=I_{D2}=0.35 mA, and R_D=5 kΩ, $V_{TH,N}$=0.5 V, $\mu_n C_{ox}$=300 μA/V^2, V_{DD}=3.3 V, λ_n=0.1. Neglect body effect.
(a) Choose V_B such that M_1 is 100 mV away from the triode region (V_{DS1}=V_{GS1}-V_{TH1}+100mV, M_1 operate in Saturation region), neglect λ_n. while calculating the bias point.
(b) Calculate the small-signal voltage gain (V_{OUT}/V_{IN}).
(c) Assume V_B=1.65 V, calculate the maximum output voltage swing to keep all transistors in saturation.
(d) Assume the maximum output swing is V_{OUT}=1.25 V_{PP}, Calculate the swing at node X.

3. (a) Sketch the output voltage (V_{OUT}) and small-signal gain (V_{OUT}/V_{IN}) roughly (without any calculation), of the folded-cascode stage shown in Fig. 3 (a) as V_{in} goes from 0 to V_{DD}. Assume that the current source I_{SS} is ideal. V_B is the bias voltage which ensures both transistors are in saturation when I_{D1}=I_{D2}=I_{ss}/2.
(b) Calculate the symbolic small signal (V_{OUT}/V_{IN}) gain of the folded-cascode stage shown in Fig. 3 (b) in terms of transistor parameters and the bias current I_{SS}. Please note this circuit is the same with Fig 3 (a) except an ideal current source with I_D=I_{SS}/3 is replaced by R_D. Neglect body effect. Assume all transistors are in saturation. Ignore channel-length modulation while calculating small signal parameters such as gm. (Hint: Try to draw the small signal model of the circuit to reach a straightforward solution.)

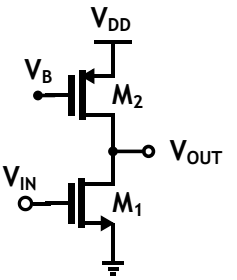

Figure 1.

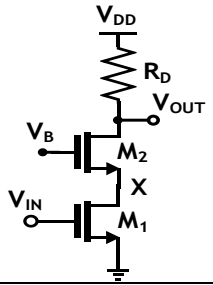

Figure 2.

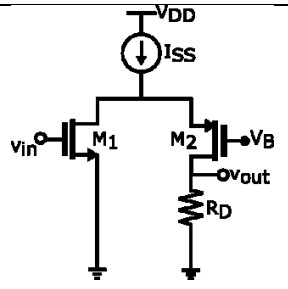

Figure 3 (a).

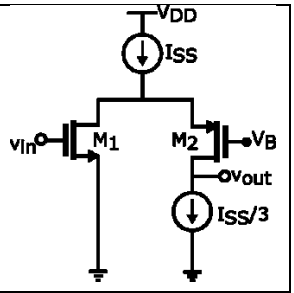

Figure 3 (b).

SIMULATION EXERCISES

Amplification is an important function in most analog and digital circuits. Four basic types of single-stage amplifiers, common-source (CS), common-gate (CG), source followers, and cascode topologies are introduced in this course. Based on these topologies, circuit designers can arrange them to create more advanced functional blocks. To understand the operating principle of these single-stage amplifiers, let's use the Ltspice too: (Note that the DC sweep simulation with the step size of 10mV and the range from 0 to V_{DD}=3.3 V). (While doing the simulations, please follow the

transistor size, resistance, and bias current given in Q1 to Q3. Use the 180 nm CMOS technology library provided in Brightspace for the transistor parameters.)

4. **(a)** Build a test bench with the CS stage in Fig.1 using the parameters in Q 1 and plot the V_{OUT}-vs.-V_{IN} transfer curve using DC sweep simulation.
   (b) Find the small-signal voltage gains (slope of V_{OUT}-vs.-V_{IN}) at V_{OUT}=0.6 V/2.8 V using the curve obtained in 4-(a).
   (c) Find the input voltage value (V_{IN}) when the voltage gain is maximum using the curve obtained in 4-(a).
   (d) Find the output swing range when the voltage gain is still larger than 1 using the curve obtained in 4-(a).
   (e) Plot small-signal voltage gain (V_{OUT}/V_{IN}) using AC sweep at V_{OUT}=0.6 V/2.8 V and compare the results with question 4-(b)

5. **(a)** Build a test bench with the cascode stage in Fig.2 and design a V_B value (please show reasoning and calculations) such that M_1 is 100 mV away from the triode region, then plot V_{OUT}-vs.-V_{IN} using DC sweep simulation. (Hint: You can start choosing a V_B which makes M1 operating on saturation region. With the given condition I_{D1}=0.35mA, we get V_{GS1} through simulation, then use this V_{GS1} to design V_B.)
   b) Plot large-signal I_{OUT}-vs.-V_{OUT} when V_{IN} is fixed for I_{D1}=0.35 mA using DC sweep simulation.

6. **(a)** From the large-signal I_{OUT}-vs.-V_{OUT} curve in Q 5, derive the large-signal curve R_{OUT}-vs.-V_{OUT} using DC sweep simulation 6-(a) determine the V_{out} value when the output impedance is maximum.

---- END OF THE ASSIGNMENT ----