TU Delft

EE4C10 Analog Circuit Design Fundamentals

Homework Assignment I

Start date: 30/08/2021

Due date: 10/09/2021

Please upload your homework via Brightspace

FORMULARY

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (1)$$

$$I_D = \mu C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (2)$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\varphi_F + V_{SB}} - \sqrt{|2\varphi_F|}\right) \quad (3)$$

$$I_D = I_0 e^{\frac{V_{GS}}{nV_T}} \quad (4)$$

$$Long\ Channel: I_0 = \mu C_{ox}(n-1)\frac{W}{L}V_T^2 \quad (5)$$

$$Slope\ factor: n = 1 + \frac{C_d}{C_{ox}} \quad (6)$$

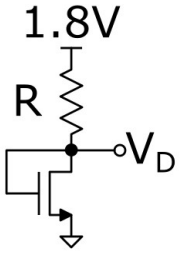
INSTRUCTIONS

1. Solutions must be submitted in PDF file named "Name_Surname_HW1.pdf". Descriptions of the simulation and simulation results must be included in the PDF file, while schematics used for simulations must be compressed in a single ZIP file named "Name_Surname_HW1.zip" containing the ltspice files. Converted photographs are not accepted. Please avoid hand-written reports and graphs. Simulation waveforms should have a white background.

2. Late submissions would not be accepted.

3. For the simulation's questions, attach a ltspice file used for each question that must be directly simulatable.

1. **(1 point)** The NMOS transistor in the circuit of Fig. 1 has $V_{TH} = 0.6$ V, $\mu_n C_{ox} = 130\ \mu A/V^2$ and W = 1.5 μm. Find the values required for L and V_D in order to establish a drain current of 40 μA for R = 20kΩ for
   a) $\lambda = 0\ V^{-1}$
   b) $\lambda = 0.06\ V^{-1}$.



2. **(1 point)** The PMOS transistors in the circuit of Fig. 2 have $V_{TH0} = 0.33$ V, $\mu_p C_{ox} = 120\ \mu A/V^2$, $\lambda = 0\ V^{-1}$, and $L_1 = L_2 = L_3 = 0.40$ μm.
   a) Considering that the bulk of the transistors are connected to the source, find the required values of gate width for each of M_1, M_2, and M_3 to obtain the voltage and current values indicated.
   b) Now, consider that the bulk terminals are attached to the V_{DD} and that $\gamma = 0.25\ V^{1/2}$ and $\varphi_F = 0.35$ V and calculate the new gate widths.

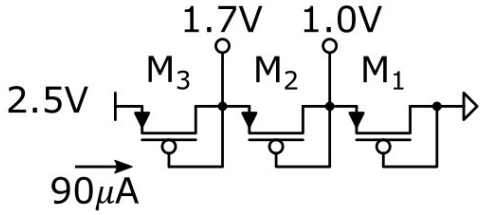


Figure 2.

The parameters of the quadratic and sub-threshold conduction models can be extracted from the BSIM model through SPICE simulation. Use $V_{DD} = 1.8$ V and W = 3 μm/L = 1 μm for the NMOS and PMOS transistors in questions from 3 to 6 and using LTSpice do the following:
[TIP: use the mathematic functions of the LTSPICE or MATLAB to process the data.]

3. **(1.5 points)**
   a) Build a test bench and trace the I_D-V_{GS} characteristic (set the body-source potential difference to 0 V) for the pmos and nmos transistors.
   b) Derive the parameters $\mu_{n(p)}C_{ox}$ and $V_{THn(p)}$ from this curve.

4. **(1 point)**
   a) Build a test bench and trace the I_D-V_{DS} for characteristic for $V_{GSn} = 0.9$ V and $V_{SGp} = 0.9$ V (set the body-source potential difference to 0 V).
   b) Derive the parameter $\lambda_{n(p)}$ from this curve.

5. **(1 point)**
   a) Plot g_m/I_D versus V_{GS} for both NMOS and PMOS
   b) Based on this information, get the maximum g_m/I_D of the technology at room temperature
   c) Derive the slope factor n.

6. **(1.5 points)** Consider Fig. 4 and that transistor M_1 is operating in saturation,
a) draw the low-frequency (i.e., without capacitances) small-signal model of the circuit considering non-zero λ
b) calculate the expression for the relation $A_v = V_{out}/V_{in}$ and the output impedance R_{OUT} seen by the terminal V_{OUT} considering $\lambda=0$
c) same as **6b),** but now with non-zero λ.

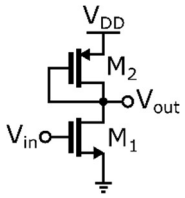


Figure 4.

7. **(3 points)** Consider the parameters extracted in exercises 3,4 and 5 with the circuit of Fig. 4 with the following sizing: $L_1 = 1$ µm, $W_1 = 3$ µm, $L_2 = 1$ µm and $W_2 = 15$ µm and with $V_{DD} = 1.8$ V and $\lambda_{n(p)} = 0$, do the following:
(If you were not able to do **3,4 and 5** use: $\mu_n C_{ox} = 500\ \mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $V_{THn} = 0.42V$, $V_{THp} = -0.43V$, $n = 1.1$)

a) Calculate and plot V_{out} versus V_{in} for V_{in} **from 0 V to 1.8 V** using the simplified models for strong and weak inversion levels in the correct regions.
b) Use LTSpice to plot V_{out} versus V_{in} for V_{in} **from 0 V to 1.8 V** and plot it together with the calculated expression on the **7a),**
c) Derive the small-signal gain $A_v = V_{out}/V_{in,}$ and find out the bias point for V_{GS1} for the maximum voltage gain.
d) Trace the small-signal model parameters A_v and R_{out} using AC sweep from 1MHz to 1GHz with the V_{GS1} bias point obtained in **7b)**.
e) Using the setup in **7d)** run both .ac and .op simultaneously in LTSpice (see figure 5) and view the View→SPICE Error Log (see figure 6). Use Gm and Gds in the Spice Error Log in the found equations from **6c)** and compare them with the results from **7d).**

Figure 5.

Figure 6.

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