PMICRO
Powerlink Microelectronics

PL1167

Single chip low power consumption and high performance

2.4GHz wireless radio frequency transceiver chip

Chip overview:

PL1167 is a world-wide ISM frequency converter working at 2.4~2.5GHz.
It is a single-chip low-power high-performance 2.4GHz wireless radio frequency transceiver chip.

The single-chip wireless transceiver integrates modules such as frequency synthesizer, power amplifier, crystal oscillator, and modem.

Output power, channel selection and protocol can be flexibly configured through SPI or I2C interface.

Supports functions such as frequency hopping and received signal strength detection, anti-interference performance Strong, can adapt to various complex environments and achieve excellent performance.

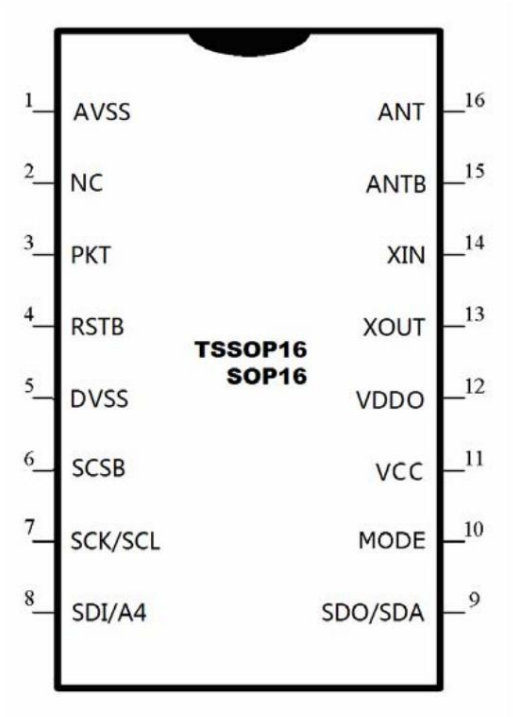
Built-in address, FEC and CRC check functions.

Built-in auto-answer and auto-resend functions.

The maximum transmit power of the chip can reach 5.5dBm, and the receiving sensitivity can reach -88dBm.

Built-in power management function, the standby current can be reduced to close to 1uA in power-down mode and standby mode.

Pin layout diagram:



Main features: Low

power consumption and high performance 2.4GHz wireless radio

frequency transceiver chip Wireless

speed: 1Mbps Built-in

hardware link layer Built-in received signal strength

detection circuit supports automatic response and

automatic retransmission functions Built-in address and FEC

and CRC check functions Very short channel Switching time, can

be used for frequency hopping. Use microstrip line

inductor and double-layer PCB board. Low

operating voltage: 1.9~3.6V. Package type: TSSOP16/

SOP16. TSSOP16/SOP16 can support SPI and I2C interfaces.

application:

Wireless mouse, keyboard, game console joystick, wireless data

communication, wireless

access control,

wireless networking

security system,

remote control

device, remote

sensing survey, smart

sports equipment,

smart home, industrial

sensor, industrial and commercial short-range communication

IP phone, cordless phone toy

RoHS GREEN

1 Overview

PL1167 is a single-chip low-power high-performance 2.4GHz wireless radio frequency transceiver chip working in the 2.4~2.5GHz world-wide ISM frequency band.

The single-chip wireless transceiver integrates modules such as frequency synthesizer, power amplifier, crystal oscillator, and modem.

Output power, channel selection and protocol can be flexibly configured through SPI or I2C interface.

Supports functions such as frequency hopping and received signal strength detection, anti-

It has strong interference performance and can adapt to various complex environments and achieve excellent performance.

Built-in address, FEC and CRC check functions.

Built-in auto-answer and auto-resend functions.

The maximum transmit power of the chip can reach 5.5dBm, and the receiving sensitivity can reach -88dBm.

Built-in power management function, the standby current can be reduced to close to 1uA in power-down mode and standby mode.

2 features

Low power consumption and high performance 2.4GHz wireless radio frequency transceiver chip Wireless speed: 1Mbps Built-in hardware link layer Built-in received signal strength detection circuit Supports automatic response and automatic retransmission functions Built-in address and FEC and CRC check functions

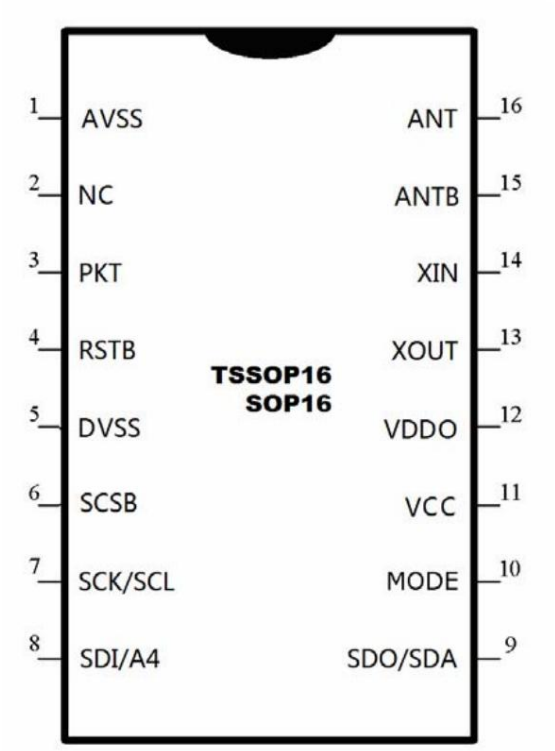
Extremely short channel switching time, can be used for frequency hopping. Use microstrip line inductor and double-layer PCB board. Low operating voltage: 1.9~3.6V. Package type: TSSOP16/SOP16. TSSOP16/SOP16 can support SPI and I2C interfaces.

3Quick reference data

Parameters	numerical value	unit
Minimum operating voltage	1.9	IN
Maximum transmit power	5.5	dBm
Data transfer rate Transmit	1	Mbps
mode power consumption @0dBm	16	mA
Receive mode power	17	mA
consumption Operating	-40 to +105	ÿ
temperature range	-88	dBm
Receive sensitivity Power consumption in power-down mode	1	uA

4 pin distribution diagram

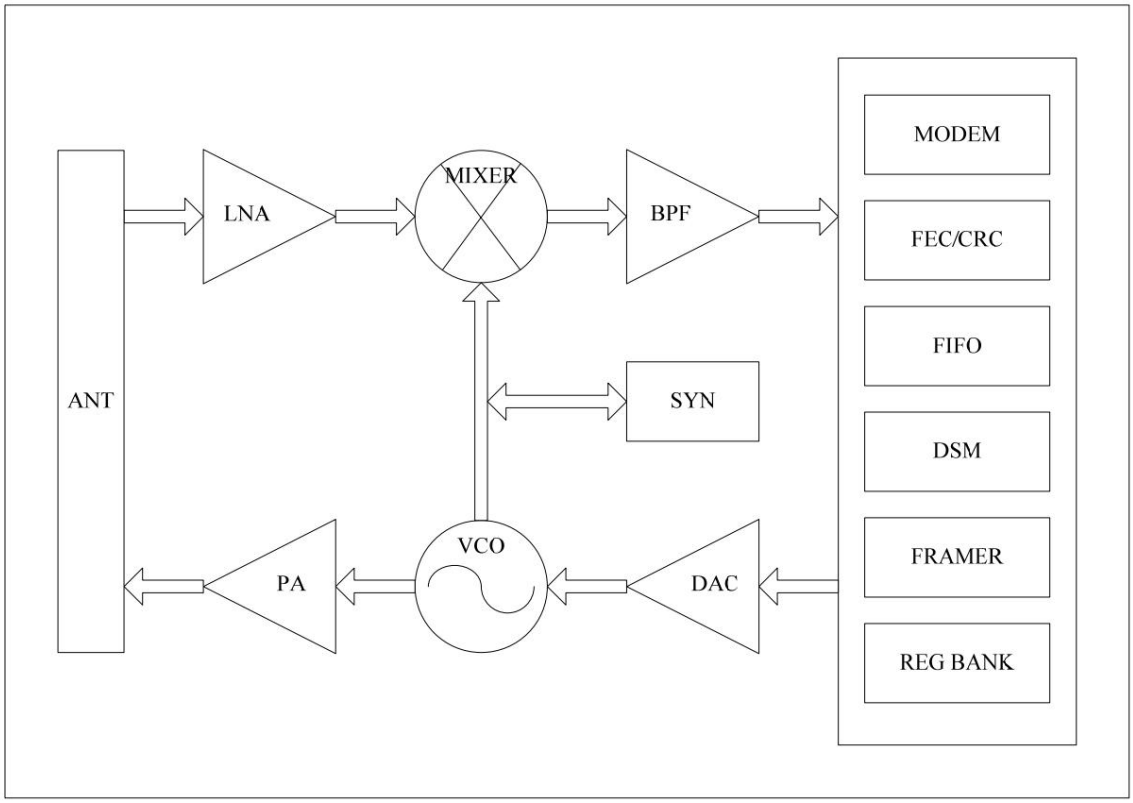
TSSOP16/SOP16 pin distribution diagram is as follows:



5 pin description

Pin	name	type	description
1	ASSS	power supply	Ground (0V)
2	N/C	hanging in the air	Leave unconnected
3	POINTS	Digital output	transmit/receive packet status indication bit
4	RSTB	Digital input	reset pin, active low level
5	DVSS	power supply	Ground (0V)
6	SCSB	Digital input	SPI: SPI interface slave mode enable signal, active low level Wake up the chip from SLEEP mode I2C: Wake up the chip from SLEEP mode
7	SCK/SCL	digital input	SCK: SPI interface clock input SCL: I2C interface clock input
8	SDI/A4	Digital input	SDI: SPI interface data input A4: I2C interface address bit 4
9	SDO/SDA	digital output Numeric I/O	SDO: SPI interface data output (three-state when invalid) SDA: I2C interface data input and output I/O digital
10	MODE		input interface mode selection: VSS: Select SPI interface VCC: Select I2C interface
11	VCC	power supply	Power supply (3.3V)
12	VDDO	power supply	1.8V internal LDO output, external capacitor
13	XOUT	Analog output	crystal oscillator output
14	ASK FOR	Analog input	crystal oscillator input
15	ANTB	antenna	Antenna interface
16	ON	antenna	Antenna interface

6Structure block diagram



7maximum ratings

parameter	symbol	scope	unit
VCC supply voltage	VCC	-0.3 to +3.6	IN
VDDO supply voltage input	VDDO	-0.3 to +2.5	IN
voltage output	COME	-0.3 to (VCC+0.3) -0.3	IN
voltage operating	VOUT	to (VCC+0.3)	
temperature	TOP	-40 to +105	ÿ
storage temperature	TST	-40 to +125	ÿ

Note: Exceeding the maximum rating may damage the device; chip functional characteristics beyond the recommended operating range cannot be guaranteed; working under Maximum rated conditions may affect device stability.

8Electrical Characteristics

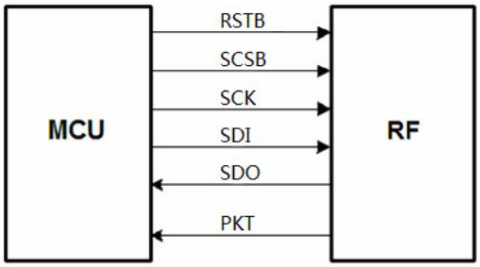
(VCC=+3VÿVSS=0VÿTA=ÿ40 to + ÿ 105ÿ)

Symbol parameters (conditions)	Description	Minimum	Typical	Maximum	Unit	
	working conditions					
VCC	VCC supply voltage		1.9	3.3	3.6	IN
TOP working temperature			-40		105	ÿ
	Digital input pin					
HIV	High level input voltage		0.8VCC		1.2VCC	IN
VIL low level input voltage			0		0.2VCC	IN
	Digital output pin					
VOH high level output voltage			0.8VCC		VCC	IN
VOL low level output voltage			0		0.2VCC	IN
	General RF conditions					
	Working		2402		2480	MHz
frequency band fOP fXTAL				12		MHz
crystal oscillator frequency ÿf1M frequency offset @1Mbps				280		KHz
RGFSK data transfer rate				[1]		Mbps
FCHANNELchannel spacing				[1]		MHz
	launch operation					
PRF maximum output power				0	5.5	dBm
PRFC RF power control range			18	20	22	dB
PRF1 first adjacent channel transmit power					-20	dBm
PRF2 second adjacent channel transmit power					-50	dBm
IVCC_H power consumption at high gain				16		mA
IVCC_L low gain power reception				12		mA
	operation					
IVCC receiving power				17		mA
consumptionRXSENS receiving sensitivity at 0.1% BER				-88		dBm

9 SPI interface

9.1 SPI interface description

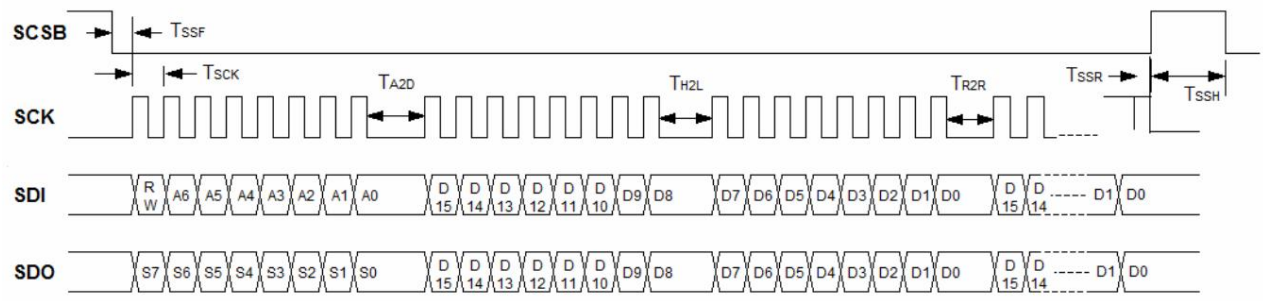
The PL1167 transceiver chip provides a simple MCU interface SPI mode. The chip's SPI interface only supports slave mode.



The SPI interface contains 7 related signals, as shown in the following table:

Pin description	
RSTB	Reset pin, active low level
MODE	Mode selection, when it is 0, select SPI mode.
SCSB	SPI interface slave mode enable signal, active low level Wake up the chip from SLEEP mode
SCK	SPI interface clock input
SDI	SPI interface data input
SDO	SPI interface data output
POINTS	Transmit/receive packet status indication bit

9.2 SPI command format



Note: The SPI bus establishes data on the rising edge of SCK and samples data on the falling edge.

Symbol	Minimum	Typical	Maximum	Description
TSSH	250ns			Time interval between two SPI commands
TSSF,TSSR	41.5ns			SCSB and SCK time interval
TA2D	*1			Address and data time interval
TH2L	*1			High and low byte data time interval
TR2R	*1			Time interval between two register data
TSCK	83ns			SCK clock cycle

Note: *1—When reading FIFO data, at least 450ns waiting time is required; for other registers, T3min = 41.5ns.

10 I2C interface

10.1 I2C interface description

Pin	describe
RSTB	Reset pin, active low level
MODE	Mode selection, when it is 1, select I2C mode
SCSB	Wake up the chip from SLEEP mode
SCL	I2C interface clock input
SDA	I2C data input and output I/O
A4	I2C interface address bit 4

10.2 I2C support features

I2C slave mode selection	Support or not
Standard mode – 100 kbps	yes
Fast mode – 400 kbps	yes
Enhanced Fast Mode – 1000 kbps	yes
High speed mode – 3200 kbps	no
clock stretching	no
10-bit slave address	no
Broadcast address	no
software reset	no
Device ID	no

10.3 I2C command format

Example I2C Data Transfers:

Master writes 1 or more data bytes to PL1167 FIFO register:

Start	Device_Addr[6:0]	W	A	Byte_Addr[7:0]	A	Data[7:0]	A	— — — —	A	Data[7:0]	A	Stop

Master writes 1 byte to PL1167 to specify FIFO register, then reads one or more bytes from PL1167 FIFO:

Start	Device_Addr[6:0]	W	A	Byte_Addr[7:0]	A	Sr	Device_Addr[6:0]	R	A	Data[7:0]	A		A	Data[7:0]	NA	Stop

Master may continue reading PL1167 FIFO:

Start	Device_Addr[6:0]	R	A	Data[7:0]	A	Data[7:0]	A	—	A	Data[7:0]	NA	Stop

Sr: repeated Start

A: Acknowledge **NA: No acknowledge**

Master to Slave **Slave to Master**

10.4 I2C device address

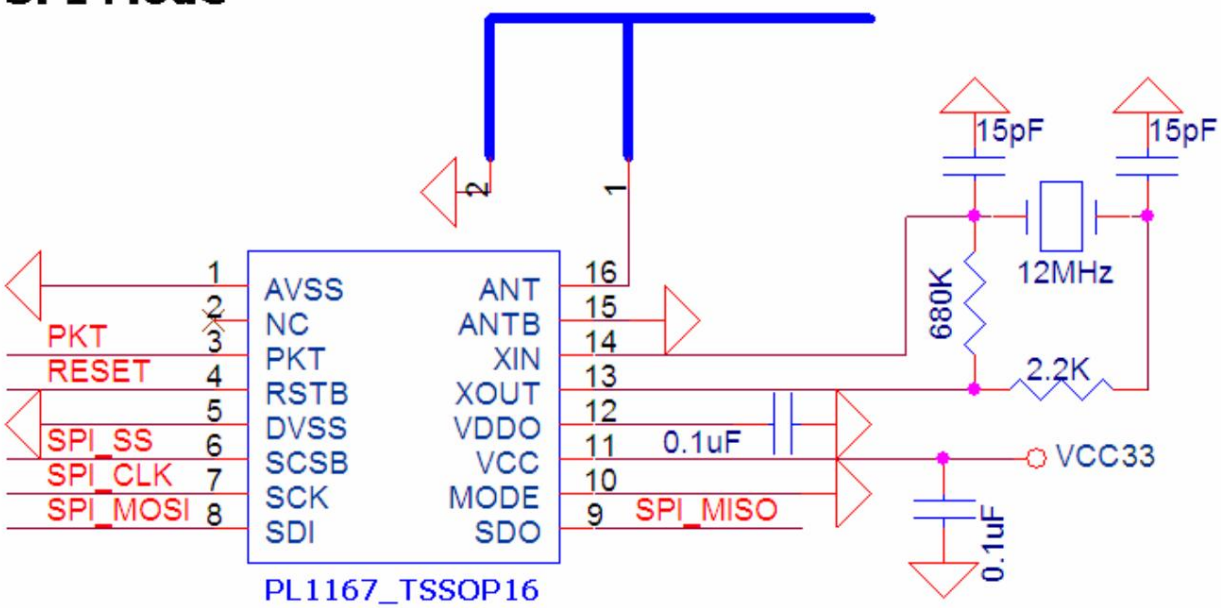
A6	A5 A4 A3 A2 A1				A0	R/W
0	1	A4 Pin 1		0	0	0	Read=1 Write=0

11 control register

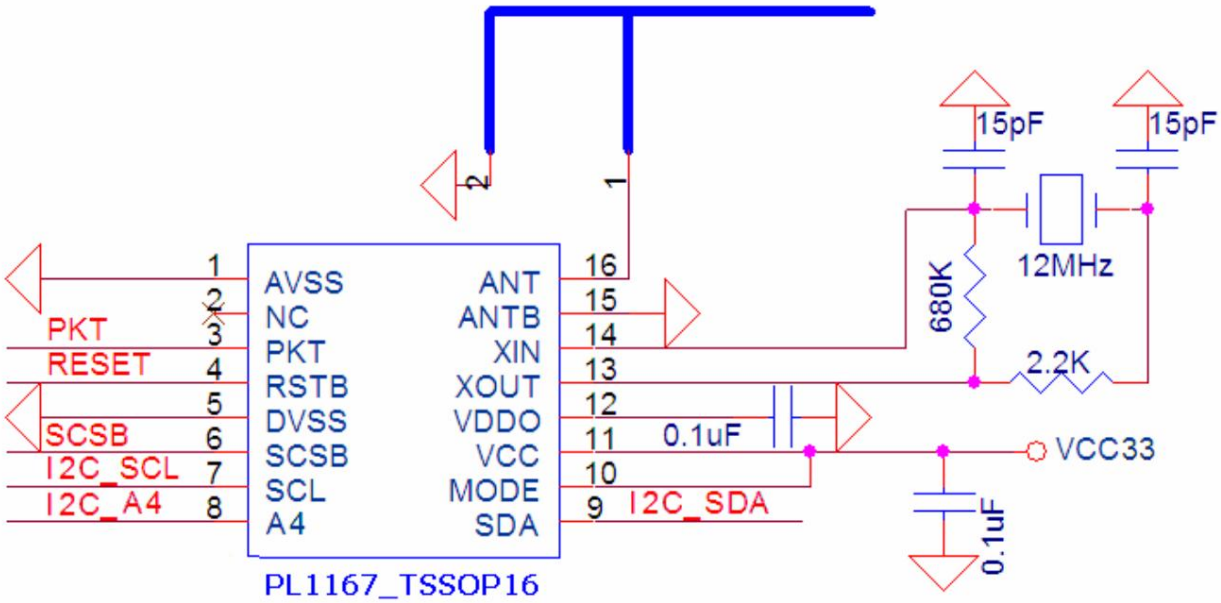
For the latest recommended control register values, please refer to the "User Manual", please contact Juyuanwei to obtain it.

12Typical applications

SPI Mode



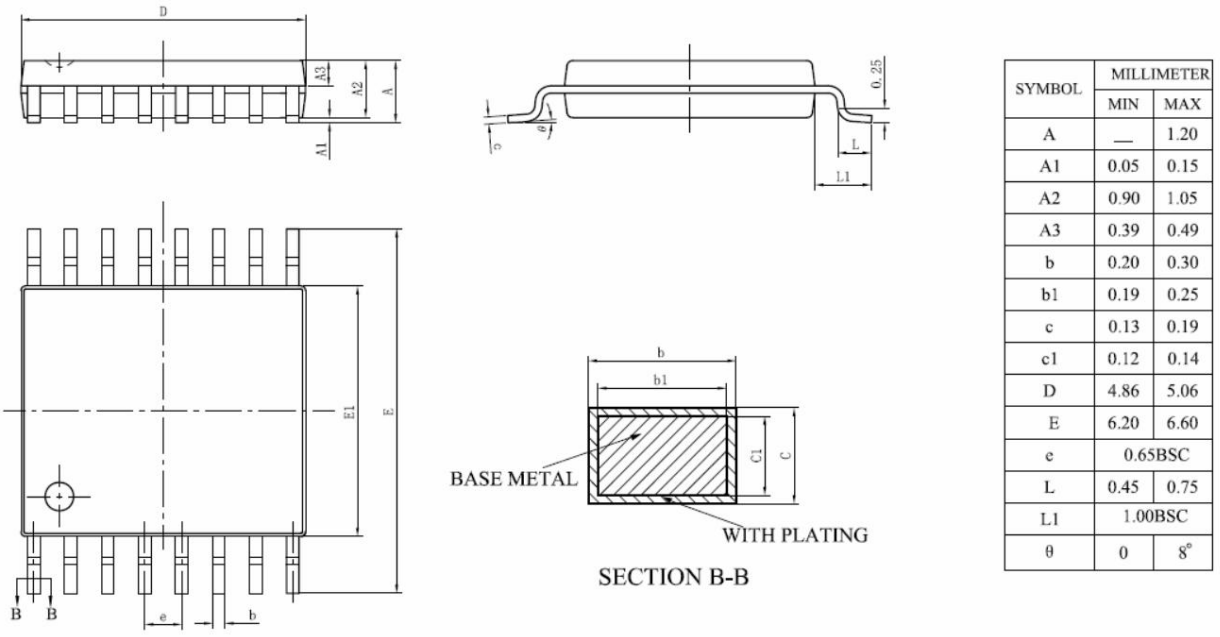
I2C Mode



13 packages

TSSOP16 package

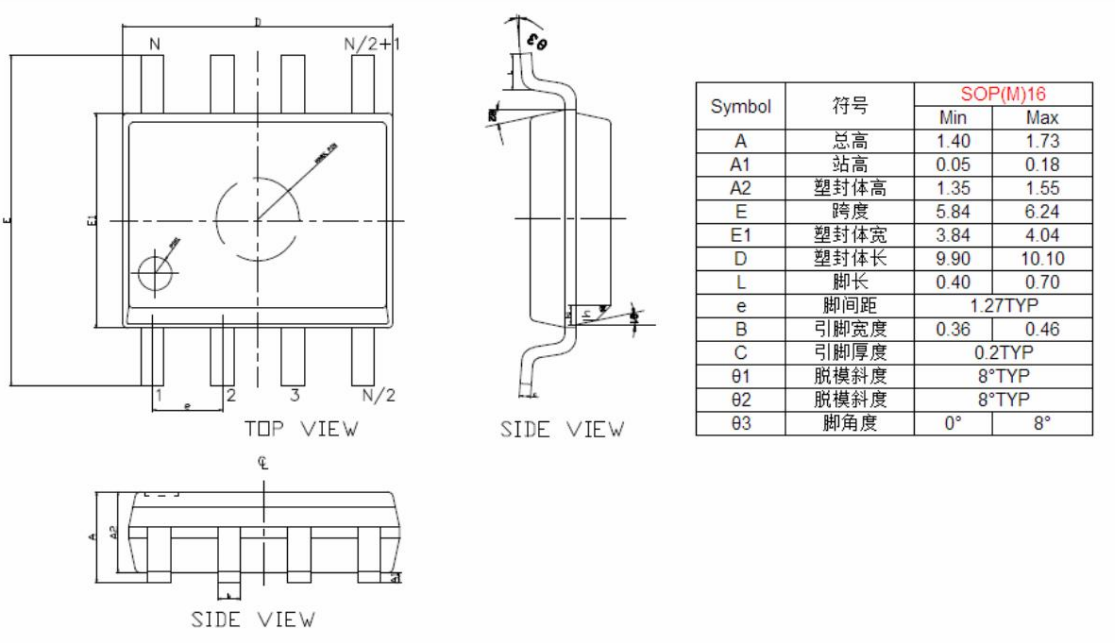
TSSOP16 package size



SYMBOL	MILLIMETER	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.20	0.30
b1	0.19	0.25
c	0.13	0.19
c1	0.12	0.14
D	4.86	5.06
E	6.20	6.60
e	0.65BSC	
L	0.45	0.75
L1	1.00BSC	
θ	0	8°

SOP16 package

SOP16 package size



Symbol	符号	SOP(M)16	
		Min	Max
A	总高	1.40	1.73
A1	站高	0.05	0.18
A2	塑封体高	1.35	1.55
E	跨度	5.84	6.24
E1	塑封体宽	3.84	4.04
D	塑封体长	9.90	10.10
L	脚长	0.40	0.70
e	脚间距	1.27TYP	
B	引脚宽度	0.36	0.46
C	引脚厚度	0.2TYP	
θ1	脱模斜度	8°TYP	
θ2	脱模斜度	8°TYP	
θ3	脚角度	0°	8°

14 version revision history

Version number	revision date	revision content
1.0	2012/07/10	First draft
1.1	2016/11/07	Officially released version: TSSOP16/SOP16 1) 9.2 SPI command format adds SPI instructions 2) 10.3 I2C command format correction 3) Corrected fOP: 2402~2480
1.2	2018/07/11	operating temperature parameters

15 things to note

In order to continuously improve the reliability, functionality or design of the product, Juyuanwei reserves the right to update and modify the product at any time without prior notice to customers.

Customers please confirm that they are using the latest complete version of the instructions before placing an order.