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Electronic Devices & VLSI

Practice Questions

1. Basics of Semiconductors

01. A Si crystal is doped with phosphorous atoms to the extent of 1 part of impurity atom per billion (PPB) Si atoms. The atomic concentration of Si is $5\times10^{22}/cm^3$, minority concentration of crystal in cm^{-3} is.
(Assume intrinsic concentration of Si is 1.5×10^{10} cm^{-3})
(a) 4.5×10^6 (b) 2.2×10^7
(c) 5.4×10^6 (d) 45×10^6

02. The concentration of minority carriers in an extrinsic semiconductor under equilibrium is
(a) directly proportional to the doping concentration
(b) inversely proportional to the doping concentration
(c) directly proportional to the intrinsic concentration
(d) inversely proportional to the intrinsic concentration

03. A potential difference of 5V is applied across an n-type specimen of length 100mm and cross sectional area 6 mm^2. Given μ_n=3800 cm^2/V-sec & μ_p=1800 cm^2/V-sec Drift velocity of majority carriers in cm/sec is.
(a) 900 (b) 1900
(c) 1800 (d) 3800

04. For n – type semiconductors with $n = N_D$ and $p = n_i^2/N_D$. The hole concentration will fall below the intrinsic value because some of the holes
(a) drop back to acceptor impurity states
(b) drop to donor impurity states
(c) virtually leave the crystal
(d) recombine with electrons

05. An intrinsic semiconductor is doped with $\frac{10^{15}}{1.6}$ acceptors/cm^3. Given μ_n = 4000 cm^2/V-sec & μ_p = 2000 cm^2/V-sec Conductivity of material in Ʊ/cm is. (Assume 100% doping efficiency)
(a) 0.4 (b) 0.1
(c) 0.2 (d) 0.8

06. For an n-type semiconductor having any doping level, which of the following hold(s) good:
1. $p_n N_D = n_i^2$ 2. $p_p N_D = n_i^2$
3. $n_n N_D = n_i^2$ 4. $p_n n_n = n_i^2$
Select the correct answer using the code given below:
(a) 1 and 4 (b) 2 and 4
(c) 3 and 4 (d) Only 4

07. A doped semiconductor exhibits Hall Effect. Given hall coefficient is $3.6\times10^{-4}m^3/C$ & resistivity

is 9×10^{-3} Ω-m. Density of carriers in m^{-3} in the specimen is. (Assume single carrier system)

(a) 1.74×10^{22} (b) 5.63×10^{16}

(c) 1.93×10^{24} (d) 1.74×10^{16}

08. The electron density profile in a piece of semiconductor at equilibrium is such that $n(x_1)=10n(x_2)$. The hole density profile will be such that ?

(a) $p(x_1) = 10p(x_2)$

(b) $p(x_2) = 10p(x_1)$

(c) $p(x_1) = 100p(x_2)$

(d) insufficient information to answer

09. A p-type semiconductor is exhibiting hall effect. Given resistivity = 3×10^3Ω-m, μ_p = 0.12m^2/V-sec & induced voltage 60mV. Hall coefficient R_H in m^3/C is

(a) 630 (b) 360

(c) 3.6 (d) 6.3

10. Drift current in a semiconductor is proportional to

(a) concentration gradient of charge carriers

(b) concentration of charge carriers

(c) Inverse of cross sectional area of specimen

(d) none

11. The diffusion constant and mobility for electrons in a semiconductor material at a given temperature are 20 cm^2/s and 1600 cm^2/V-s, respectively. The thermal voltage V_T for a diode made of this material at the same temperature is

(a) 125 mV (b) 32 mV

(c) 12.5 mV (d) 3.2 mV

12. The conductivity of a semiconductor crystal due to any current carrier is NOT proportional to

(a) mobility of the carrier

(b) effective densities of states

(c) Concentration of charge carriers

(d) surface states in semiconductor

13. Given doping concentration of p-type semiconductor is 2.29×10^{16} cm^{-3}. Find location of Fermi level.

(Assume $n_i = 1.5\times10^{10}cm^{-3}$).

(a) Fermi level lies 0.37eV above E_V

(b) Fermi level lies 0.37eV below E_V

(c) Fermi level lies 0.37eV below E_{Fi}

(d) Fermi level lies 0.37eV above E_{Fi}

14. Consider two metallic wires W_1 and W_2. They are made up of same material and each has circular cross section. The diameter of W_2 is twice that of W_1 and the length of W_2 is four times that of W_1. Which one of the following statements is TRUE?

(a) Resistance of W_1 is half that of W_2

(b) Resistance of W_1 is equal to that of W_2

(c) Resistance of W_1 is twice that of W_2

(d) Resistance of W_1 is eight times that of W_2

15. In a Hall effect experiment, a p-type semi conductor sample with hole concentration p_1 is used. The measured value of the Hall voltage is V_{H1}, it is now replaced by another p-type sample with hole concentration p_2 where $p_2 = 2\ p_1$, what is the new Hall voltage V_{H2}

(a) $2V_{H1}$

(b) $4V_{H1}$

(c) (1/2) V_{H1}

(d) (1/4) V_{H1}

16. Electron mobility & life-time in a semiconductor at room temperature are respectively 0.36 m^2/v-sec & 340 μs. The diffusion length is
    (a) 3.13 mm
    (b) 1.77 mm
    (c) 3.55 mm
    (d) 3.23 mm

17. Which one of the following pairs of semi conductors and current carriers is correctly matched?
    (a) Intrinsic → Number of electrons = number of holes
    (b) p – type → number of electrons > Number of holes
    (c) n – type → Number of electrons < number of holes
    (d) metal → holes >> electrons

Direction: Each of the following questions consists of two statements, one labeled as Statement (I) and the other as Statement (II). You are to examine these questions carefully and select the correct answers using the codes given below.

(a) Both Statement (I) and Statement (II) are true and Statement (II) is the correct explanation of Statement (I)
(b) Both Statement (I) and Statement (II) are true but Statement (II) is not a correct explanation of Statement (I).
(c) Statement (I) is true but Statement (II) is false.
(d) Statement (I) is false but Statement (II) is true.

18. **Statement (I):** In a p-type semi-conductor, with increase in the level of doping at a fixed temperature, the hole concentration increases but the electron concentration falls.
    Statement (II): Law of mass action holds good in case of semi-conductors.

19. **Statement (I):** In intrinsic elemental semi conductors, electrons and holes are created in pairs.
    Statement (II): In intrinsic silicon, the electron mobility is 2.81 times greater than the hole mobility

20. **Statement (I):** At room temperature Fermi level in p - type semiconductor lies nearer the valence band, where as in n - type semiconductor lies nearer the conduction band.
    Statement (II): At room temperature the p - type semiconductor is rich in holes whereas n - type is rich in electrons.

KEY for Objective

01. (a)	02. (b)	03. (b)	04. (d)	05. (c)
06. (d)	07. (a)	08. (b)	09. (b)	10. (b)
11. (c)	12. (d)	13. (c)	14. (b)	15. (c)
16. (b)	17. (a)	18. (a)	19. (b)	20. (a)

2. PN Junction Diode

01. In a p^+n junction diode under reverse bias, the magnitude of electric field is maximum at
(a) the edge of the depletion region on the p-side
(b) the edge of the depletion region on the n-side
(c) the p^+n junction
(d) the centre of the depletion region on the n-side

02. A p^+n junction has a built-in potential of 0.8 V. The depletion layer width at a reverse bias of 1.2 V is 2μm. For a reverse bias of 7.2 V, the depletion layer width will be
(a) 4 μm (b) 4.9 μm
(c) 8 μm (d) 12 μm

03. The current I in a forward biased p^+n junction, shown in figure-A is entirely due to diffusion of holes from x = 0 to x = L. The injected hole concentration distribution in n-region is linear as shown in figure-B with $p(0) = 10^{12}cm^{-3}$ & $L=10^{-3}cm$. The current density in the diode is (assume diffusion coefficient of holes is $12cm^2/sec$).

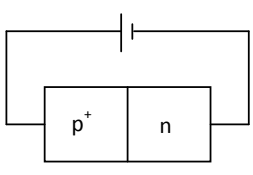


Figure A

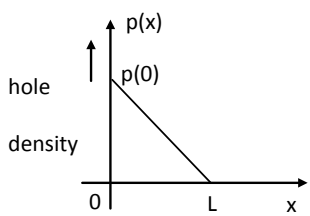


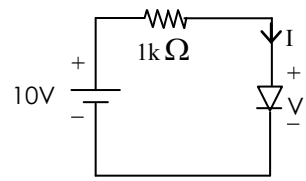
Figure B

(a) 1.92 mA/cm^2 (b) 2.19 mA/cm^2
(c) 19.2 mA/cm^2 (d) 1.29 mA/cm^2

04. At 300°K, for a diode current of 1mA, a certain germanium diode requires a forward bias of 0.1435V, whereas a certain silicon diode requires a forward bias of 0.718V. Under the conditions stated above the closest approximation of the ratio of reverse saturation current in Ge diode to that in silicon diode is
(a) 1 (b) 5
(c) 4×10^3 (d) 8×10^3

05. A p-n diode dynamic conductance is directly proportional to
(a) the applied voltage
(b) the temperature
(c) its current
(d) the thermal voltage

06. The I – V characteristics of diode in the circuit given below are



$$i = \begin{cases} \frac{V-0.7}{500}A, & V \geq 0.7V \\ 0A, & V < 0.7V \end{cases}$$

The current in the circuit is
(a) 10 mA (b) 9.3 mA
(c) 6.67 mA (d) 6.2 mA

07. The cut-in voltage V_γ and the thermal voltage V_T for the diode D in Fig. are 0.5 V and 26 mV, respectively.

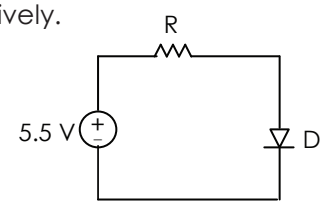


Fig.

If the value of resistor R is 20 Ω, the current flowing through the diode is
(a) 275 mA (b) 250 mA
(c) 200 mA (d) less than 200 mA

08. The reverse saturation current of a biased p-n junction diode increases 32 times due to a rise in ambient temperature. If the original temperature was 40°C. What is the final temperature?
(a) 90°C (b) 72°C
(c) 45°C (d) 50°C

09. A Si diode is carrying a constant current of 1mA. When the temperature of the diode is 20°C, V_D is found to be 700mV. If the temperature rises to 40°C V_D becomes approximately equal to
(a) 740 mV (b) 650 mV
(c) 680 mV (d) 700 mV

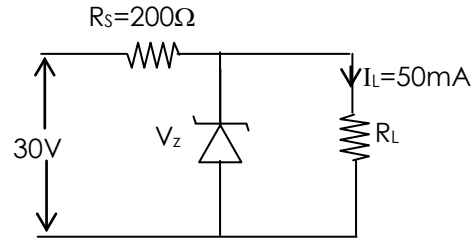
10. A silicon PN junction diode under reverse bias has depletion region of width 10μm. The relative permitivity of silicon ε_r = 11.7 and the permitivity of free space $\varepsilon_0 = 8.85\times10^{-12}$ F/m. The depletion capacitance of diode per unit area is
(a) 100μF/m^2 (b) 10.36μF/m^2
(c) 1μF/m^2 (d) 20μF/m^2

Key for Practice Questions

01. (c)	02. (a)	03. (a)	04. (c)	05. (c)
06. (d)	07. (b)	08. (a)	09. (b)	10. (b)

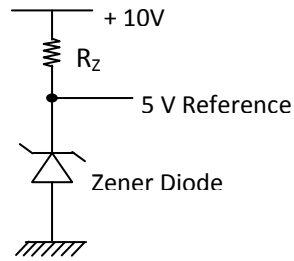
3. Zener Diode

01. The zener diode shown in the circuit is acting like regulator with a reverse breakdown voltage of 10 volts. The power dissipation in R_s would be



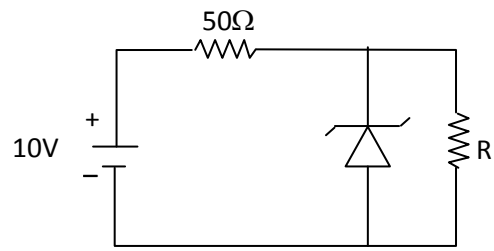
(a) 0.5 W (b) 1 W
(c) 1.5 W (d) 2 W

02. A 5V reference is drawn from the circuit shown in figure. If the zener diode is of 5 mW and 5V, then R_z in Ω will be



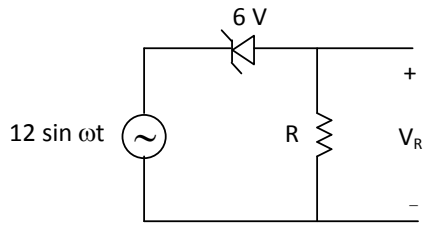
(a) 50
(b) 500
(c) 5000
(d) 50000

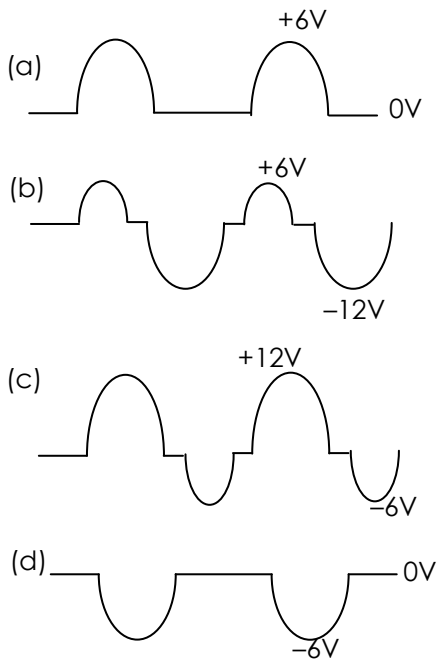
03. The 6 V Zener diode shown in the circuit is acting like regulator. It has zero resistance in breakdown and a knee current of 5 mA, then what is the minimum value of R so that the voltage across it does not fall below 6V ?



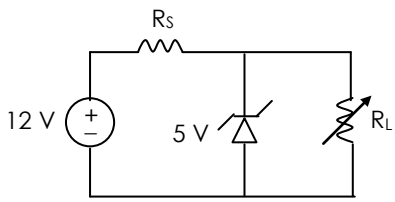
(a) 1200 ohms (b) 80 ohms
(c) 50 ohms (d) 40 ohms

04. For the circuit shown below, assume that the Zener diode is ideal with a breakdown voltage of 6 Volts. The waveform observed across R is



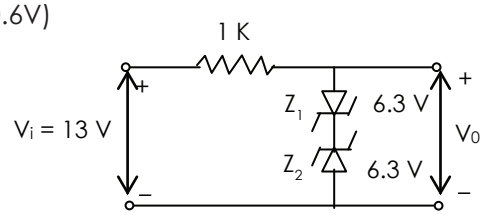


05. In the voltage regulator shown in figure. The load current can vary from 100 mA to 500mA. Assume that the Zener diode is ideal.(i.e., knee current is negligibly small and resistance is zero in the break down region), the value of R_S is



(a) 7 Ω (b) 70 Ω
(c) 70/3 Ω (d) 14 Ω

06. The o/p voltage (V_0) of the circuit shown in the figure is (Assume cut-in voltage of Z_1 & Z_2 is 0.6V)



(a) 0 (b) 5.7 V
(c) 6.9 V (d) 12.6 V

07. The ideal characteristics of a stabilizer is
(a) constant output voltage with low internal resistance.
(b) constant output current with low internal resistance.
(c) constant output voltage with high internal resistance.
(d) constant internal resistance with variable output voltage.

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(c) Statement (I) is true but Statement (II) is false.
(d) Statement (I) is false but Statement (II) is true.

08. **Statement (I):** If a p-n junction has break down voltage of less than 6V. It is due to Zener break down mechanism.
Statement (II): Heavily doped p-n junction have less break down voltage.

09. **Statement (I):** A DC voltage stabilizer is one which stabilizes the output voltage irrespective of variation in I/P voltage and load current.
Statement (II): A DC voltage stabilizer uses a Zener diode across the load to stabilize the voltage.

Key for Practice Questions

01. (d)	02. (c)	03. (b)	04. (b)	05. (d)
06. (c)	07. (a)	08. (a)	09. (b)	

4. Special Purpose Diodes

01. Consider the following statements: A tunnel diode is
1. made of Ge or GaAs.
2. an abrupt junction with both sides heavily doped.
3. an abrupt junction with one side heavily doped.
4. a majority carrier device.

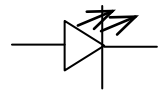
Which of these statements are correct?
(a) 1 and 2 (b) 3 and 4
(c) 1, 3 and 4 (d) 1, 2 and 4

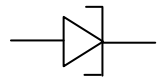
02. The values of voltage (V_D) across a tunnel diode corresponding to peak and valley currents are V_P and V_V respectively. The range of tunnel-diode voltage V_D for which the slope of its I-V_D characteristics is negative would be
(a) $V_D < 0$ (b) $0 \le V_D < V_P$
(c) $V_P \le V_D < V_V$ (d) $V_D \ge V_V$

03. Which one of the following diodes contains a metal-semiconductor junction?
(a) Tunnel diode (b) Zener diode
(c) Schottky diode (d) Gunn diode

04. Match List - I (circuit symbols) with List – II (devices) and select the correct answer using the codes given below the lists :

List – I **List – II**

(P)  1. Light emitting diode

(Q)  2. Tunnel diode

(R)  3. Varactor diode

Codes:

	A	B	C
(a)	1	2	3
(b)	2	3	1
(c)	2	1	3
(d)	3	2	1

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(d) Statement (I) is false but Statement (II) is true.

05. **Statement (I):** A tunnel diode can be used as an oscillator.
Statement (II): Voltage controlled negative resistance is exhibited by a tunnel diode.

Key for Practice Questions

01. (a)	02. (c)	03. (c)	04. (a)	05. (a)

5. Bipolar Junction Transistor

01. The DC current gain (β) of a BJT is 50. Assuming that the emitter injection efficiency is 0.995, the base transport factor is
(a) 0.980 (b) 0.985
(c) 0.990 (d) 0.995

02. For a BJT I_C = 4mA, output resistance is greater than 20 kΩ. Then V_A, Early voltage is
(a) < 80V (b) > 5V
(c) < 5V (d) > 80V

03. For a BJT in CE configuration early voltage is 100V. I_C = 1mA at V_{CE} = 10V. If Early voltage increases to infinity then I_C in mA is.
(Assume α is constant)
(a) 1.1
(b) 1
(c) 0.1
(d) 0.9

04. The phenomenon known as "Early Effect" in a bipolar transistor refers to a reduction of the effective base-width caused by
(a) electron-hole recombination at the base.
(b) the reverse biasing of the base-collector junction.
(c) the forward biasing of emitter-base junction.
(d) the early removal of stored base charge during saturation-to-cutoff switching.

05. If α = 0.995, I_E = 10mA, I_{CO} = 0.5 μA, then I_{CEO} is
(a) 100 μA (b) 25 μA
(c) 10.1 μA (d) 10.5 μA

06. Which one of the following statements is correct? In a transistor,
(a) I_{CBO} is equal to I_{CO}, and doubles for every ten degrees rise in temperature.
(b) I_{CBO} is greater than I_{CO}, and doubles for every ten degrees rise in temperature.
(c) I_{CBO} is greater than I_{CEO}, and does not depend upon temperature.
(d) I_{CEO} is equal to I_{CO} and doubles for every ten degrees rise in temperature.

07. For a BJT width of the Base is 50×10^{-6} cm. Doping of Base is 2×10^{16} cm^{-3}, and $\varepsilon = 10^{-12}$F/cm. Calculate punch through voltage.
(a) 2V (b) 4V
(c) 10V (d) 5V

08. For a CE active BJT, given CB gain 0.98, Base current 40 μA, I_{CBO} = 1μA, then collector current is.
(a) 2.01mA
(b) 1.96 mA
(c) 2 mA
(d) 2.1 mA

09. The reverse leakage currents in CB & CE configuration are 0.4 μA & 60 μA respectively. CB current gain is
(a) 0.98
(b) 0.99
(c) 0.97
(d) 0.96

10. The early effect in a bipolar junction transistor is caused by
(a) fast turn-on
(b) fast turn-off
(c) large collector-base reverse bias
(d) large emitter-base forward bias.

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(c) Statement (I) is true but Statement(II) is false.

(d) Statement (I) is false but Statement (II) is true.

11. **Statement (I):** The semiconductor devices like BJTs have a maximum temperature of operation, beyond which they do not function
Statement (II): Extrinsic P-type and N-type semiconductors behave as intrinsic semiconductor beyond that temperature and the effect of doping is lost.

12. **Statement (I)**: A bipolar junction transistor (BJT) has collector-base junction forward biased and emitter-base junction as reverse biased.
Statement(II): BJT acts as a current amplification device.

13. **Statement (I):** High power transistors are invariably made up of silicon.
Statement (II): Silicon is a direct band gap semi conductor.

Key for Practice Questions

01. (b)	02. (d)	03. (b)	04. (b)	05. (a)
06. (a)	07. (b)	08. (a)	09. (b)	10. (c)
11. (a)	12. (b)	13. (c)		

6. Junction Field Effect Transistor

01. The reverse gate voltage of a JFET changes from 4.4V to 4.2V and the drain current changes from 2.2mA to 2.6mA then transconductance in mʊ is.
(a) 0.9 (b) 1.1
(c) 0.5 (d) 2

02. For an N-channel JFET, having drain source voltage constant if the gate source voltage is increased (more negative) Pinch-OFF would occur for
(a) high value of drain current
(b) saturation value of drain current
(c) zero drain current
(d) gate current equal to drain current

03. For a JFET maximum drain current is 10mA given Pinch-OFF voltage as –4V, gate voltage –1V then drain current is
(a) 5.625 A (b) 5.625 mA
(c) 6.525 mA (d) 0.5625 mA

04. For a JFET in the Pinch-OFF region as the drain voltage is increased the drain current
(a) becomes zero
(b)abruptly decreases
(c) abruptly increases
(d) remains constant

05. Properly biased, JFET will act as a
(a) current controlled current source
(b) voltage controlled voltage source
(c) voltage controlled current source
(d) current controlled voltage source

06. Match List I with List II

List I

P. N-channel FET is better than p-channel

Q. Channel is wedge shaped

R. Channel is not completely closed

S. Input impedance is high

List II

1. Reverse bias increases along the channel
2. Drain current reverse biases the channel
3. Low leakage current at gate terminal
4. Better performance since $\mu_n >> \mu_p$

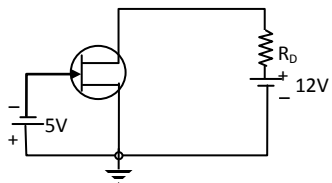
(a) P-4, Q-1, R-2, S-3

(b) P-4, Q-2, R-1, S-3

(c) P-3, Q-1, R-2, S-4

(d) P-3, Q-2, R-1, S-4

07. For JFET shown in circuit given V_P = –8V, I_{DSS} = 12mA. Calculate V_{DS} at which Pinch-OFF region starts



(a) – 3V (b) – 13V (c) +3V (d) +13V

08. Match List I with List II

List I

P. Voltage controlled device

Q. Current controlled device

R. Conductivity modulation device

S. Negative conductance device

List II

1. BJT
2. UJT
3. FET
4. IMPATT diode

(a) P-2, Q-3 R-1, S-4

(b) P-2, Q-3,R-4, S-1

(c) P-3, Q-1 R-2, S-4

(d) P-3, Q-1,R-4, S-2

09. For JFET, I_{DSS} = 12mA, V_P = – 6V, breakdown voltage 12V. Given V_{GS} = 0 and V_{DS} = 7V. Calculate drain current.

(a) 1.2 mA (b) 3 mA

(c) 6 mA (d) 12 mA

10. Match List – I (Device) With List – II (Application) and selection the correct answer using the code given below the Lists:

List –I	**List – II**
A. Diode	1. Amplifier
B. Transistor	2. Oscillator
C. Tunnel Diode	3. Rectifier
D. Zener Diode	4. Voltage regulator

Codes:

	A	**B**	**C**	**D**
(a)	4	1	2	3
(b)	3	2	1	4
(c)	4	2	1	3
(d)	3	1	2	4

11. For a n-channel JFET, I_{DSS} = 25mA, $V_{GS\,(OFF)}$ = –10V, V_{GS} = –5V. Transconductance in m℧ at zero bias is.

(a) 5 (b) 0.2

(c) 10 (d) 0.1

12. Consider following statements:

1. BJT is a current controlled device with high input impedance and high gain band width.
2. FET is a voltage controlled device with high input impedance and low gain bandwidth.
3. UJT is a negative resistance device and can be used as an oscillator.
4. BJT, FET and UJT can all be used for amplification.

Which of the statements given above are correct?

(a) 1 and 2 (b) 2 and 3
(c) 3 and 4 (d) 1 and 4

Direction: Each of the following questions consists of two statements, one labeled as Statement (I) and the other as Statement (II). You are to examine these questions carefully and select the correct answers using the codes given below.

(a) Both Statement (I) and Statement (II) are true and Statement (II) is the correct explanation of Statement (I)
(b) Both Statement (I) and Statement (II) are true but Statement (II) is not a correct explanation of Statement (I).
(c) Statement (I) is true but Statement(II) is false.
(d) Statement (I) is false but Statement (II) is true.

13. **Statement (I):** FET is unipolar device.
Statement (II): The current carriers in a FET are either holes or electrons.

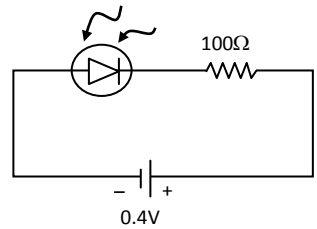
14. **Statement (I):** The input resistance of a silicon JFET is of the order of tens of hundreds of megaohms.
Statement (II): The gate-source junction of JFET is a reverse biased silicon diode and hence only a very small leakage current flows through the gate.

Key for Practice Questions

01. (d)	02. (c)	03. (b)	04. (d)	05. (c)
06. (a)	07. (c)	08. (d)	09. (d)	10. (d)
11. (a)	12. (b)	13. (a)	14. (a)	

7. Optoelectronic Devices

01.



A photo diode is connected as shown when it is illuminated by 100 lumen/cm^2, it carries current of 1.8mA. Calculate resistance offered by photo diode
(a) 122.2Ω
(b) 222.22Ω
(c) 12.22Ω
(d) 22.22Ω

02. In the above problem if illumination is doubled what is approximate resistance of diode
(a) 111.11Ω
(b) 11.11Ω
(c) 222.22Ω
(d) 22.22Ω

03. Avalanche photodiodes are preferred over PIN diodes in optical communication systems because of
(a) speed of operation
(b) higher sensitivity
(c) larger bandwidth
(d) larger power handling capacity

04. Dark current in a semiconductor photodiode is
(a) The forward bias current
(b) The forward saturation current
(c) The reverse saturation current
(d) The transient current

05. The longest wave length that can be absorbed by silicon which has a band gap of 1.12 eV is 1.1 μm. If the longest wave length that can be absorbed by another material is 0.87 μm, then the band gap of that material is
(a) 1.416 eV
(b) 0.886 eV
(c) 0.854 eV
(d) 0.706 eV

06. The sensitivity of a photodiode depends upon
(a) light intensity and depletion region width
(b) depletion region width and excess carrier life time
(c) excess carrier life time and forward bias current
(d) forward bias current and light intensity

07. A LED with cut-in voltage 1.8V is connected to a 24V supply with 820Ω series resistance. Assuming LED is glowing calculate current through circuit.
(a) 29.27 mA (b) 31.47 mA
(c) 27.70 mA (d) 27.07 mA

08. Which one of the following statements is correct? A photodiode works on the principle of
(a) photo-magnetic effect
(b) photo-resistive effect
(c) photo-electric effect
(d) photo-thermal effect

09. The phenomenon of injection electro-luminescence is the basis of working of
(a) Photodiodes
(b) Light emitting diodes
(c) phototransistors
(d) solar cells

10. A photo diode has a spectral sensitivity of 10mA /watt of incident radiation 890 A°. Find energy band gap of photo diode material for proper operation.
(a) 31.93 eV (b) 13.93 eV
(c) 4.89 eV (d) 7.18 eV

11. Which of the following statements is true for solar cell?
(a) It can store optical energy.
(b) It can store electrical energy.
(c) It converts electrical energy into optical energy.
(d) It converts optical energy into electrical energy.

12. A pin photo diode has a dark current of 1μA. Given responsivity as 0.45 Amp/Watt & optical power level as 50 μW. Calculate load current if it is properly operated as photo detector
(a) 22.5 μA
(b) 23.5 μA
(c) 2.25 μA
(d) 3.25 μA

13. Consider the following statements in connection with the biasing of semiconductor diodes.
1. LEDs are used, under forward bias condition.
2. Photodiodes are used under forward bias condition.
3. Zener diodes are used under reverse bias condition.
4. Variable capacitance diodes are used under reverse-bias condition.
Which of these statements are correct?
(a) 1, 2 and 3 (b) 1, 2 and 4
(c) 2, 3 and 4 (d) 1, 3 and 4

14. Choose proper substitutes for X and Y to make the following statement correct Tunnel diode and Avalanche photodiode are operated in X bias and Y bias respectively.
    (a) X : reverse, Y : reverse
    (b) X : reverse, Y : forward
    (c) X : forward, Y : reverse
    (d) X : forward, Y : forward

15. Consider the following statements in connection with the biasing of semiconductor diodes:
    1. LEDs are used under forward-bias condition.
    2. PIN photo diodes are used under reverse-bias condition.
    3. Avalanche photo diodes are used under sufficiently large reverse-bias to cause impact ionization.
    4. LASER diodes are used under reverse-bias condition.

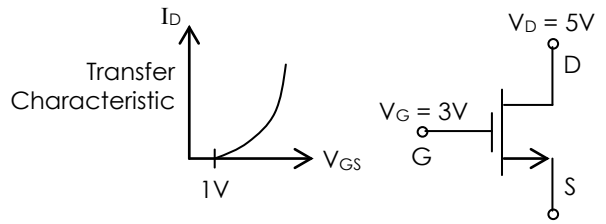
    Which of these statements are correct:
    (a) 1, 3 and 4 (b) 1, 2 and 3
    (c) 2, 3 and 4 (d) 1, 2 and 4

Key for Practice Questions

01. (a)	02. (b)	03. (b)	04. (c)	05. (a)
06. (a)	07. (d)	08. (c)	09. (b)	10. (b)
11. (d)	12. (b)	13. (d)	14. (c)	15. (b)

8. MOSFET

01. For an n-channel MOSFET and its transfer curve shown in figure, the threshold voltage is



    (a) 1Vand the device is in active region.
    (b) –1V and the device is in saturation region
    (c) 1V and the device is in saturation region.
    (d) –1V and the devices is in active region.

02. Consider the following two statements about the internal conditions in an n-channel MOSFET operative in the active region.
    S1: The inversion charge decreases from source to drain.
    S2: The channel potential increases from source to drain.
    Which of the following is correct?
    (a) Only S1 is true.
    (b) Both S1 and S2 are false.
    (c) Both S1 and S2 are true, but S2 is not reason for S1.
    (d) Both S1 and S2 are true, and S2 is a reason for S1

03. When the gate-to-source voltage (V_{GS}) of a MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1 mA, Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation. The drain current for an applied V_{GS} of 1400 m V is
    (a) 0.5 mA (b) 2.0 mA
    (c) 3.5 mA (d) 4.0 mA

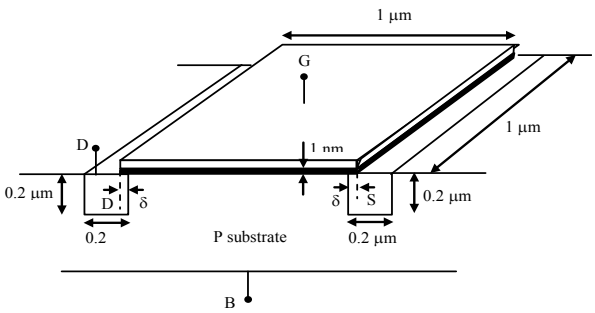
04. The source of a silicon ($n_i = 10^{10}$ per cm^3) n-channel MOS transistor has an area of 1 sq μm and a depth of 1 μm. If the dopant density in the source is $10^{19}/cm^3$, the number of holes in the source region with the above volume is approximately
(a) 10^7 (b) 100
(c) 10 (d) 0

05. A MOSFET device has both n-type source and drain and the drain current flows only when gate to source voltage exceeds +2.0V. Which of the following conclusion can be drawn about the device?
1. The device is an n-channel MOSFET
2. It is enhancement type MOSFET
3. It has threshold voltage of +2V
4. The channel conductance is determined by the hole mobility

Select the correct answer using the code given below:
(a) 1 and 3 (b) 1, 2 and 3
(c) 2 and 4 (d) 1, 2, 3 and 4

Common Data for Questions 06 & 07

In the three dimensional view of a silicon n-channel MOS transistor shown below, δ = 20 nm. The transistor is of width 1 μm. The depletion width formed at every p-n junction is 10 nm. The relative permitivities of Si and SiO_2, respectively, are 11.7 and 3.9, and $\varepsilon_0 = 8.9\times10^{-12}$ F/m.

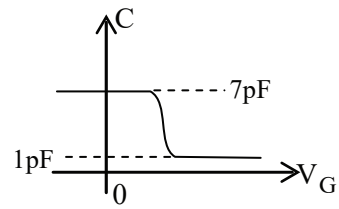


06. The source-body junction capacitance is approximately
(a) 2 fF (b) 7 fF
(c) 2 pF (d) 7 pF

07. The gate-source overlap capacitance is approximately
(a) 0.7 fF (b) 0.7 pF
(c) 0.35 fF (d) 0.24 pF

Common Data for Questions 08 & 09

The figure shows the high-frequency capacitance-voltage (C-V) characteristics of a Metal /SiO_2/silicon (MOS) capacitor having an area of $1\times10^{-4}/cm^2$. Assume that the permittivities of silicon and SiO_2 are 1×10^{-12} F/cm and 3.5×10^{-13} F/cm respectively



08. The gate oxide thickness in the MOS capacitor is:
(a) 50nm (b) 143nm
(c) 350nm (d) 1μm

09. The maximum depletion layer width in silicon is
(a) 0.143μm (b) 0.857μm
(c) 1μm (d) 1.143μm

10. The threshold voltage of an n-channel enhancement mode MOSFET is 0.5 V. When the device is biased at a gate voltage of 3V. Pinch-off would occur at a drain voltage of
(a) 1.5V (b) 2.5V
(c) 3.5V (d) 4.5V

11. The MOSFETS M_1 and M_2 are connected in parallel to carry a total current of 20 A. The drain to source voltage of M_1 is 2.5 V and that of M_2 is 3V. What are the drain currents of M_1 and M_2 when the current sharing series resistances are each of 0.5Ω?
(a) 10.5 A and 9.5 A
(b) 9.5 A and 10.5 A
(c) 10.5 A and 10.5 A
(d) 9.5 A and 9.5 A

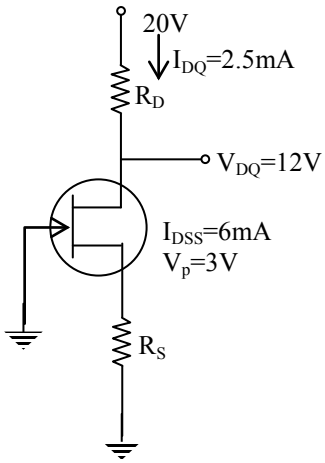
Key for Practice Questions

01. (c)	02. (d)	03. (d)	04. (d)	05. (b)
06. (b)	07. (a)	08. (a)	09. (b)	10. (b)
11. (a)				

9. BIASING

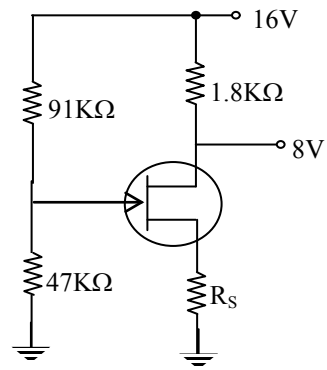
JFET BIASING

01. Given the values of V_{DQ} and I_{DQ} for this circuit, determine the required values of R_D & R_S.



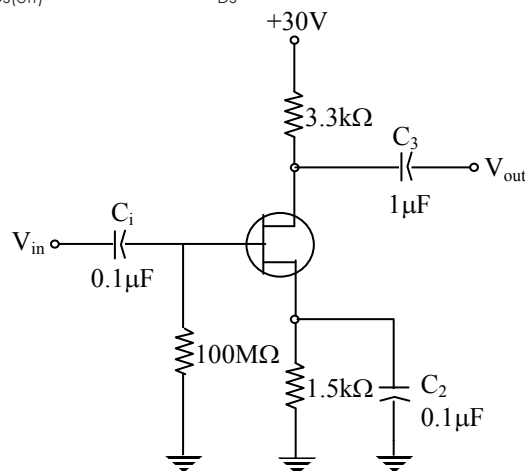
(a) 2 KΩ, 2 kΩ
(b) 1 KΩ, 5.3 KΩ
(c) 3.2 KΩ, 400 Ω
(d) 2.5 KΩ, 5.3 KΩ

02. Calculate the value of R_S. Assume V_{GSQ} = −2V.



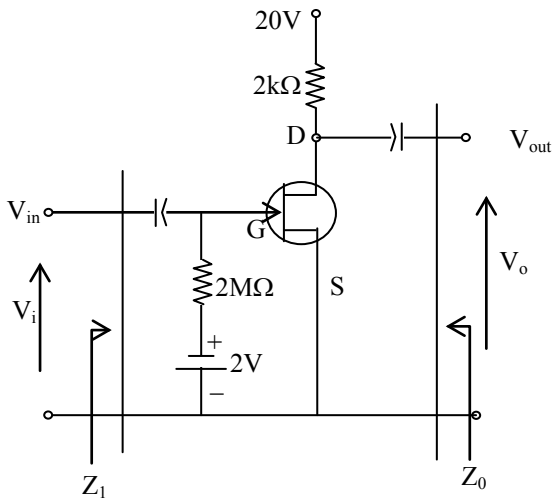
(a) 0 KΩ
(b) 1.68 KΩ
(c) 6.81 KΩ
(d) 8.5 KΩ

03. Refer to this figure. If I_D = 4 mA, I_{DSS} = 16 mA, and $V_{GS(off)}$ = –8 V, find V_{DS}.



(a) 19.2 V (b) –6 V
(c) 10.8 V (d) 30 V

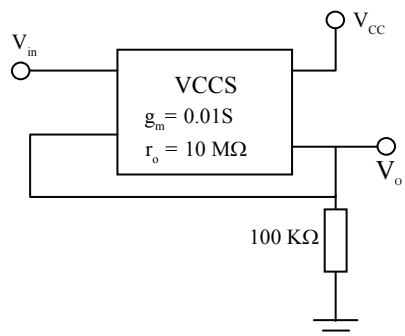
Common Data for Questions 04, 05 & 06
Given r_d = 20kΩ, I_{DSS} = 10mA, V_p = –8V



04. Z_i and Z_0 of the circuit are respectively
    (a) 2MΩ and 2kΩ
    (b) 2MΩ and $\frac{20}{11}$kΩ
    (c) Infinity and 2kΩ
    (d) Infinity and $\frac{20}{11}$kΩ

05. I_D and V_{DS} under DC conditions are respectively
    (a) 5.625mA and 8.75V
    (b) 7.500mA and 5.00V
    (c) 4.500mA and 11.00V
    (d) 6.250mA and 7.50V

06. Find the approximate output impedance of the VCCS (voltage-controlled current source) based circuit at port V_o.



(a) 0.01 Ω (b) 100 Ω
(c) 100 kΩ (d) 10 MΩ

KEY for Objective

01. (c) 02. (b) 03. (c) 04. (b) 05. (a)
06. (c)

Frequency Analysis

01. An amplifier rated at 30-W output is connected to a 5-Ω speaker. Calculate the input voltage for the rated output if the amplifier voltage gain is 20 dB.
    (a) 1.225 mV (b) 12.25 mV
    (c) 122.5 mV (d) 1.225 V

02. What magnitude voltage gain corresponds to a decibel gain of 50?
    (a) 31.6238 (b) 316.228
    (c) 3162.38 (d) 31623.8

03. A JFET with the following parameters is used in a single stage common source amplifier with a load resistance of 100kΩ. Calculate the high frequency cut-off (upper 3 dB cut off frequency) of the amplifier.
    g_m = 2.0mA/V R_D = 10kΩ
    r_d = 100kΩ C_{gd} = 2.0pF
    C_{ds} = 1.0pF

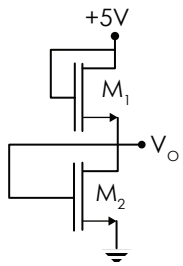
KEY for Objective

01. (d) 02. (b) 03. (6.12×10^6 Hz)

MOSFET BIASING

Common Data for Questions 01 & 02

Consider the circuit shown in figure. The both transistor have parameter as follows V_{TN} = 0.8V, K_n = 30 μA/V_2



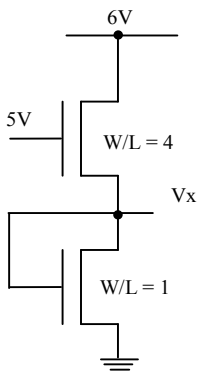
01. If the width-to length rations of M_1 and M_2 are $\left[\frac{W}{L}\right]_1 = \left[\frac{W}{L}\right]_2$ = 40. The output V_0 is

(a) –2.5 V (b) 2.5 V
(c) 5 V (d) 0 V

02. If the ratio is $\left[\frac{W}{L}\right]_1$ = 40 and $\left[\frac{W}{L}\right]_2$ then V_0 is

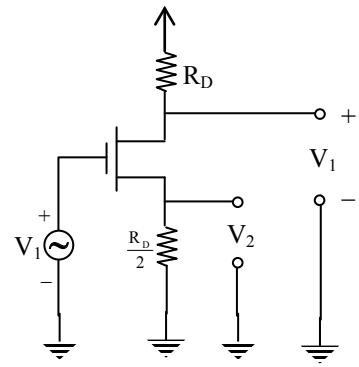
(a) 2.91V (b) 2.09V
(c) 3.41V (d) 1.59V

03. In the circuit shown below. For the MOS transistors, $\mu_n C_{ox}$ =100μ A/V^2 and the threshold voltage V_T = 1V. The voltage V_x at the source of the upper transistor is



(a) 1V (b) 2V
(c) 3V (d) 3.67V

04. In the MOSFET amplifier of Fig., the signal outputs V_1 and V_2 obey the relationship



(a) $V_1 = \frac{V_2}{2}$ (b) $V_1 = \frac{V_2}{2}$

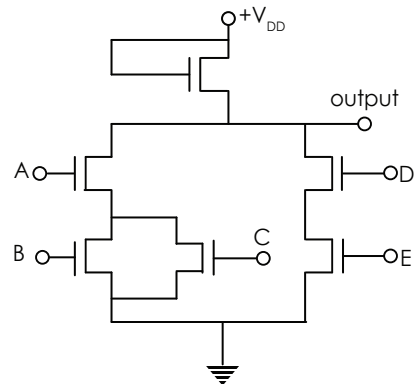
(c) $V_1 = 2V_2$ (d) $V_1 = -2V_2$

Key for Practice Questions

01. (b) 02. (a) 03. (c) 04. (d)

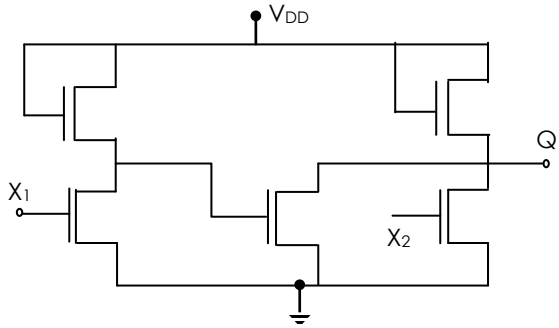
10. CMOS

01. An NMOS circuit is shown in the above figure. The logic function for the output (o/p) is



(a) $(\overline{A+B})C + \overline{D}\,\overline{E}$
(b) $(AB + \overline{C})(\overline{D} + E)$
(c) A(B+C)+DE
(d) $\overline{ABCDE}$

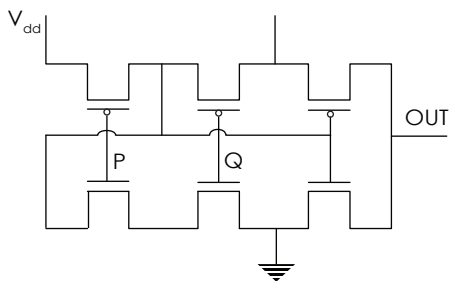
02. If X_1 and X_2 are the inputs to the circuit as shown in the below figure, then what is the output Q?



(a) $(X_1 + X_2)'$ (b) $(X_1 - X_2)'$

(c) $(X_1 - X_2)$ (d) $(X_1 - X_2')$

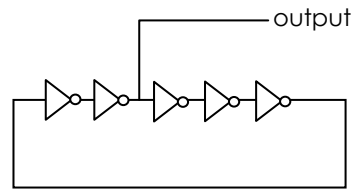
03. The logic function implemented by the following circuit at he terminal OUT is



(a) P NOR Q (b) P NAND Q

(c) P OR Q (d) P AND Q

04. The inverters in the ring oscillator circuit shown below are identical. If the output waveform has a frequency of 10MHz, the propagation delay pf each inverter is



(a) 5 ns (b) 10 ns

(c) 20 ns (d) 50 ns

Key for Practice Questions

01. (c) 02. (a) 03. (d) 04. (b)