Metal-Oxide-Semiconductor Field Effect Transistor

→ MOSFET or IGFET

- Enhancement Mode
  - n-channel
  - p-channel
- Depletion Mode
  - n-channel
  - p-channel

* Device structure

* Drain characteristics → V_{GS} = constant, $V_{DS} \nearrow$ → I_D

* Transfer characteristics → V_{DS} = constant, $V_{GS} \nearrow$ → I_D

→ Non-Ideal V-I characteristics

→ short-channel effects

→ MOSFET Transconductance

→ MOSFET Device Models

→ MOSFET Capacitance

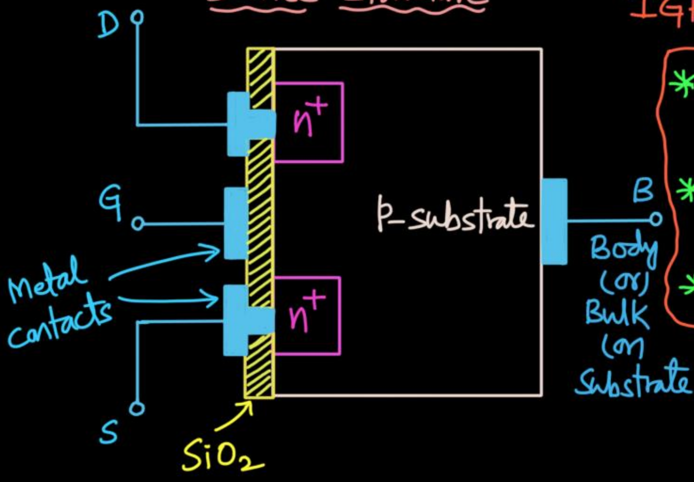
n-channel Enhancement Mode MOSFET

→ Comparision of n and p channel FET

→ Comparision of BJT and FET

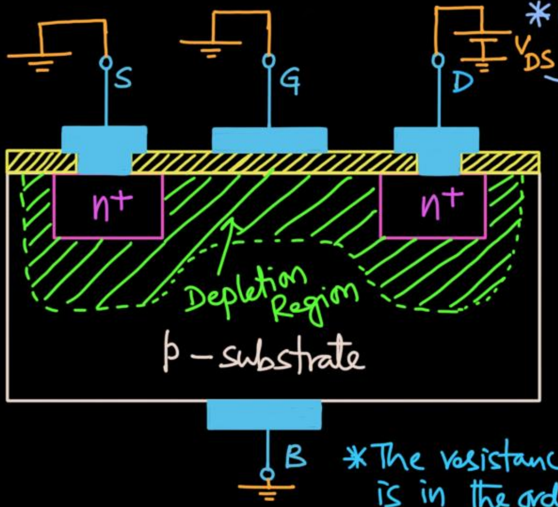
n-channel Enhancement Mode MOSFET

Device structure "IGFET"



* L – Length of the channel
  Typically, L → 0.03 μm to 1 μm
* W – Width of the channel
  Typically, W → 0.05 μm to 100 μm
* t_{ox} – Thickness of oxide layer
  Typically, t_{ox} → 1 nm to 100 nm

Drain characteristics → V_{GS} = constant, $V_{DS} \rightarrow I_D$



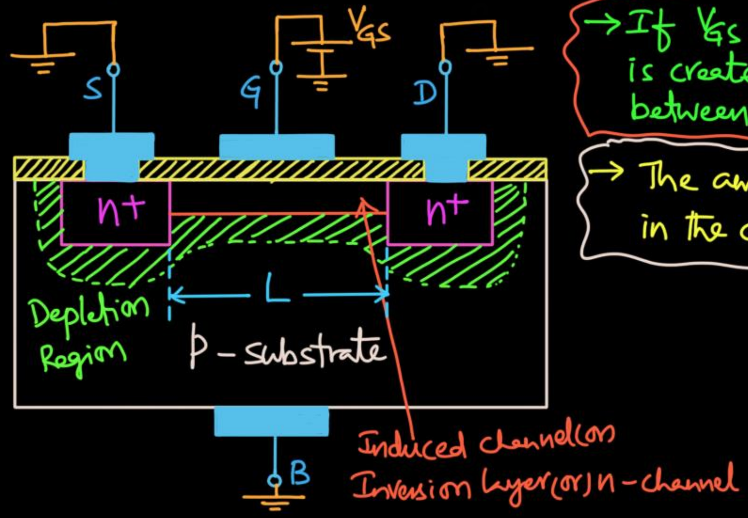
* Operation of device with zero gate voltage

→ The two back-to-back connected diodes will prevent the current flow. ⇒ $I_D = 0$

→ One diode is due to pn junction between p–B and n^+–S. The second diode is due to pn junction between p–B and n^+–D.

* The resistance between S and D is in the order of $10^{12}\ \Omega$.

Creating a channel for current flow



→ If $V_{GS} > V_T$, a channel is created for current flow between S and D

→ The amount of charge present in the channel depends on V_{GS}.

→ Now, there is a parallel plate capacitor that is present between G (+ve plate) and n-channel (-ve plate) with oxide region as dielectric.

→ The field present between G and channel with oxide as dielectric decides the amount of charge present in the channel.

$\Downarrow$

Field Effect Transistor

→ Once V_{GS} is more than V_T, then the channel is created for current flow. So

$$\boxed{V_{OV} \equiv V_{GS} - V_T}$$

Over drive Voltage (or) Effective voltage

Decides how much charge is present in the channel.

→ Initially, there is no channel between S and D. By applying appropriate G voltage, we are enhancing a channel between S and D which makes current to flow when a V_{DS} is applied.

$\Downarrow$

Enhancement Mode MOSFET

NMOS, NMOS Transistor

PMOS, PMOS Transistor

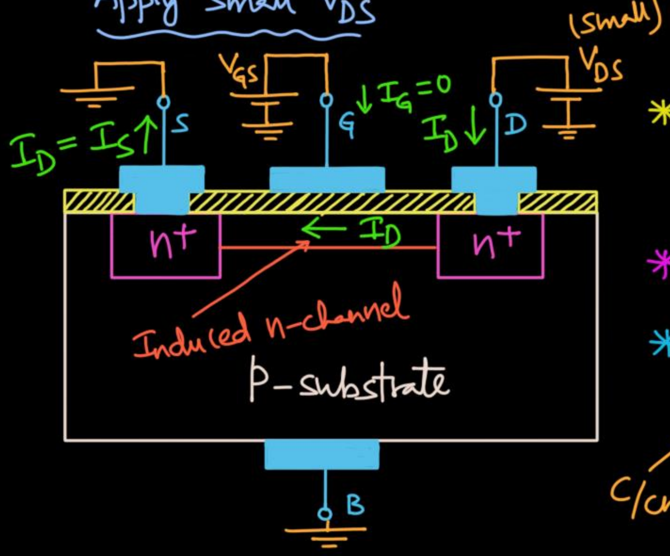
→ The magnitude of electron charge in the channel is given by $\boxed{|Q| = C_{ox}(WL)(V_{GS} - V_T)}$

L - Length of the channel, W - Width of the channel

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ - Oxide capacitance per unit gate area

t_{ox} - thickness of the oxide region - It is decided by the process technology used to fabricate MOSFET

Apply small V_{DS}



* If V_{DS} is applied, $\bar{e}$s move from S to D, results a current flow from D to S.

* $|Q| = C_{ox}(WL)(V_{GS} - V_T)$

* charge per unit channel length

$$\frac{|Q|}{L} = C_{ox} W (V_{GS} - V_T)$$

C/cm

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(1) Voltage along the channel

0 to V_{DS}

(2) Voltage between gate and various points along the channel

V_{GS} to V_{GD} $(V_{GS} - V_{DS})$

→ Since V_{DS} is small, the effective voltage between G and various points along the channel is $(V_{GS} - V_T)$ and the channel depth is uniform.

$$\frac{|Q|}{L} = C_{ox} W (V_{GS} - V_T)$$

$$I_D = \frac{|Q|}{L} v$$

$$I_D = C_{ox} W (V_{GS} - V_T) \mu_n E$$

$$I_D = C_{ox} W (V_{GS} - V_T) \mu_n \frac{V_{DS}}{L}$$

$$\boxed{I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T) V_{DS}} \quad \text{—} (1)$$

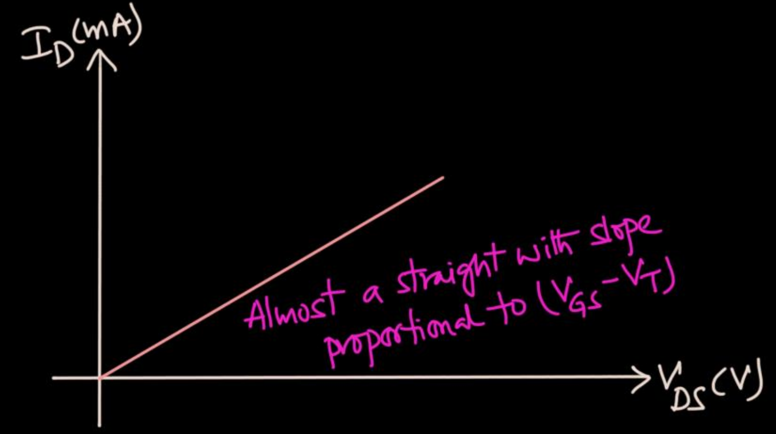
(A/cm^2) C/cm^3 cm/s

$$J = \rho v$$

$$\frac{I}{A} = \rho v$$

$$I = \underbrace{(\rho A)}_{C/cm} v$$

$$v = \mu_n E$$



→ The conductance of the channel is given by

$$\boxed{g_{DS} = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_T)} \ *$$

→ The conductance of the channel depends on

- * $\mu_n C_{ox}$
- * $\frac{W}{L}$
- * $(V_{GS} - V_T)$

$\mu_n C_{ox}$

μ_n: $cm^2/V\text{-}s$

$k_n' = \mu_n C_{ox}$ → Process transconductance parameter

k_n': A/V^2

C_{ox}: F/cm^2

$\underline{\left(\frac{W}{L}\right)}$

$\frac{W}{L} \rightarrow$ Aspect ratio

$$\boxed{K_n = \mu_n C_{ox}\left(\frac{W}{L}\right) = k_n'\left(\frac{W}{L}\right)}$$

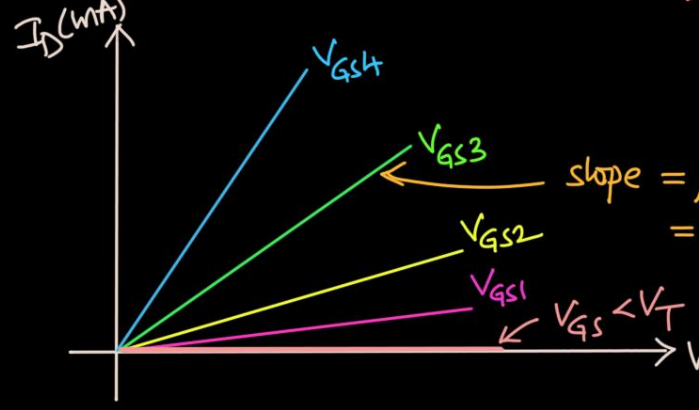
K_n – Transistor transconductance parameter (A/V^2)

$\underline{(V_{GS} - V_T)}$

* Decides amount of charge in the channel.

MOSFET as a voltage controlled resistor

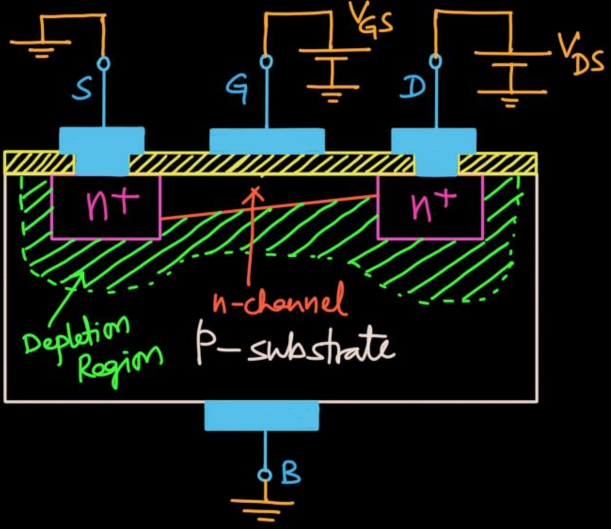
→ The resistance of the channel $r_{DS} = \dfrac{1}{g_{DS}}$

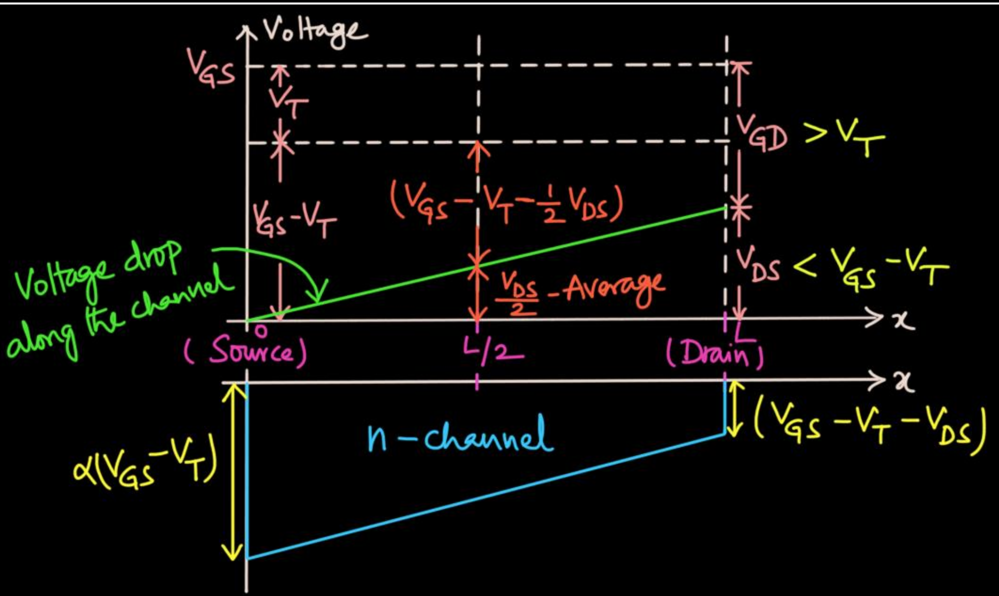


$$r_{DS} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)}$$

$$\text{slope} = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS3} - V_T) = g_{DS} = \frac{1}{r_{DS}}$$

Device operation as V_{DS} is increased





→ The voltage along the channel

0 to V_{DS}

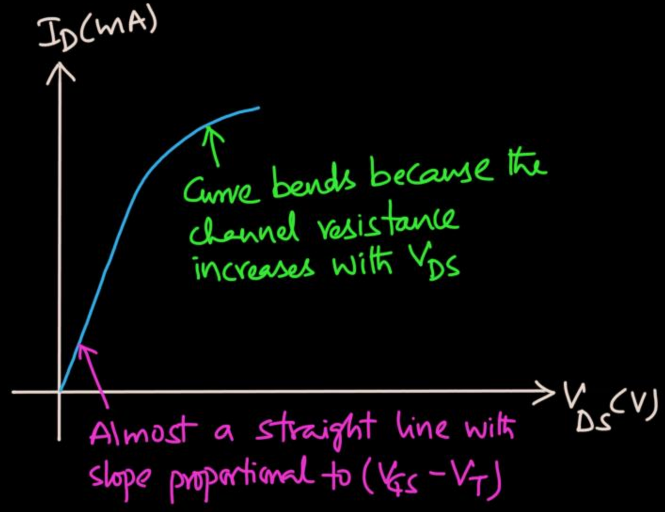
→ The voltage between G and various points along the channel

V_{GS} to V_{GD} $(V_{GS} - V_{DS})$

→ The effective voltage between G and various points along the channel

$(V_{GS} - V_T)$ to $(V_{GS} - V_T - V_{DS})$

→ The effective voltage between G and various points in the channel is varying from $(V_{GS} - V_T)$ to $(V_{GS} - V_T - V_{DS})$, due to this the channel shape is not uniform and it is tappered, the depth is deepest at the source end and shallowest at the drain end.



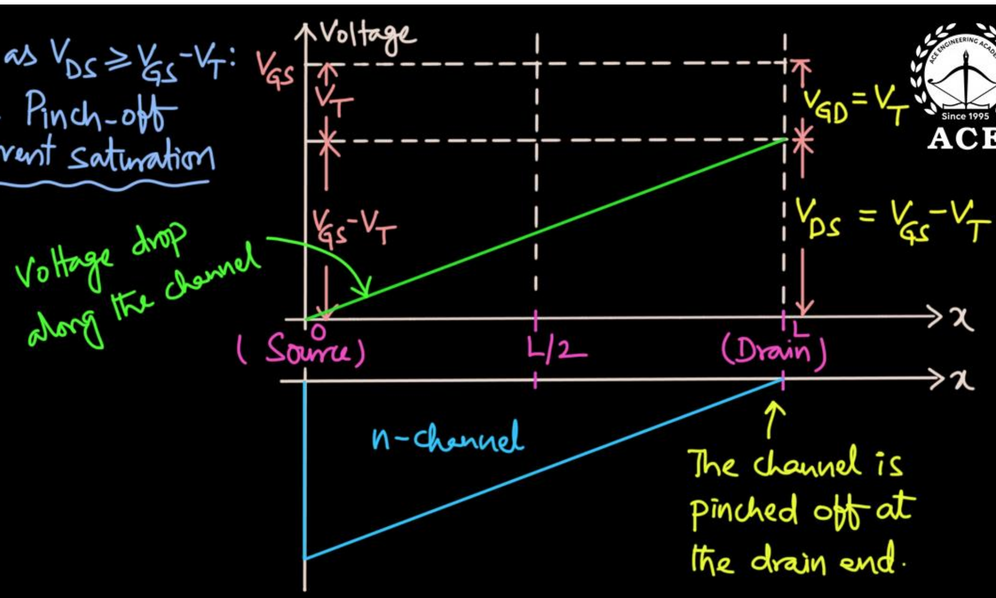
$$① \Rightarrow I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)V_{DS}$$

Replace $(V_{GS}-V_T)$ with $\left(V_{GS}-V_T-\frac{1}{2}V_{DS}\right)$

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS}-V_T-\frac{1}{2}V_{DS}\right)V_{DS}$$

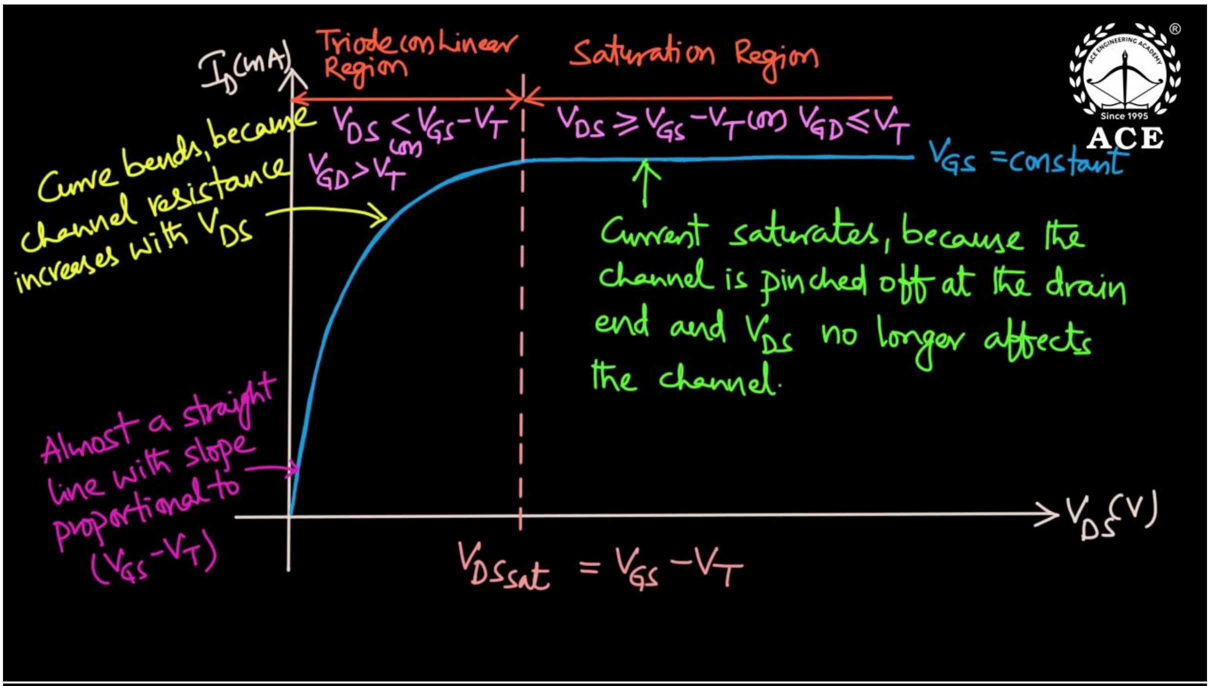
$$\boxed{I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right]} \quad ②$$

Operation as $V_{DS} \geq V_{GS} - V_T$: Channel Pinch-off and current saturation



→ For $V_{DS} = V_{GS} - V_T$ the channel is pinched off at the drain end. The drain current reaches a maximum value for this V_{DS}.

→ Now, if we increase V_{DS} beyond $V_{DSsat} = V_{GS} - V_T$, then V_{DS} has no effect on the channel profile.



$$(2) \Rightarrow I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Substitute $V_{DS} = V_{GS} - V_T$

$$\boxed{I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2} \quad - (3)$$

→ The channel pinch-off does not mean channel blockage; current contineous to flow through the pinched-off channel, the $\bar{e}$s reaching drain end are accelerated through the depletion region and into the drain terminal.

n-channel Enhancement Mode

(1) If $V_{GS} < V_T$; no channel; Transistor is cut-off; $I_D = 0$

(2) If $V_{GS} > V_T$; a channel is induced; transistor operates in linear or saturation region depending upon whether the channel is contineous or pinched-off at the drain end.

Triode (Deep Triode Region)

→ The channel is contineous ($V_{DS} << V_{GS} - V_T$)

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)V_{DS}$$

→ The channel is contineous ($V_{DS} < V_{GS} - V_T$ or $V_{GD} > V_T$)

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

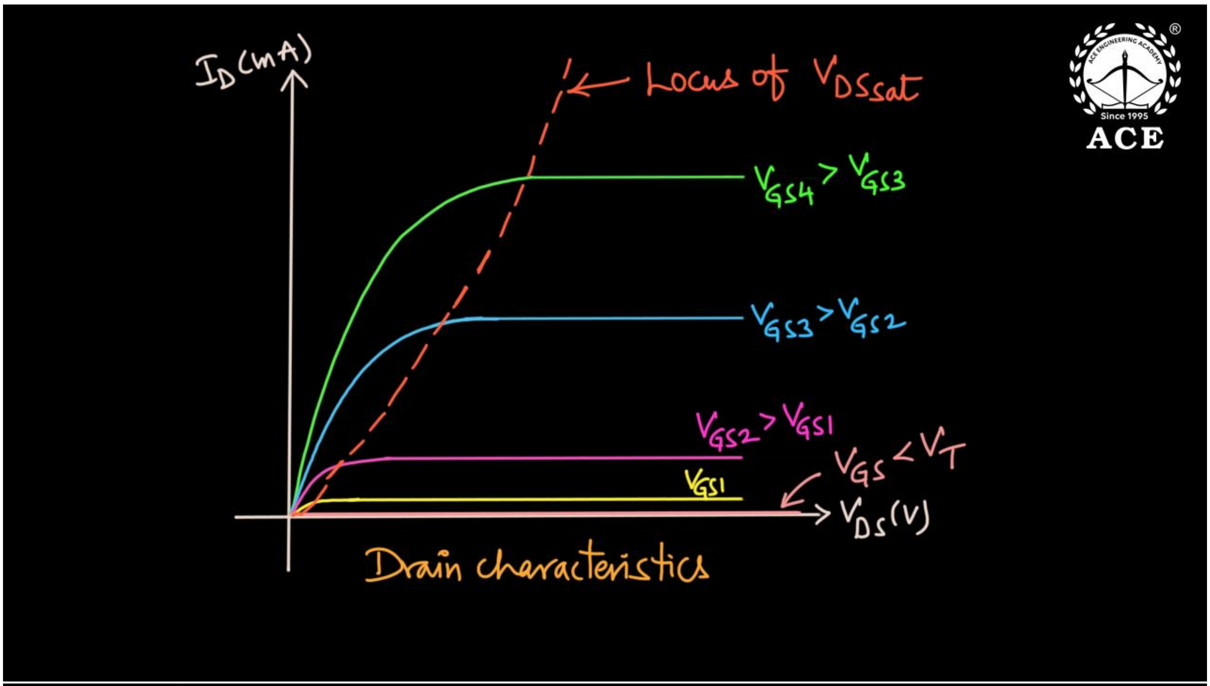
$V_{DS} \geq V_{GS} - V_T$ Saturation

(or)

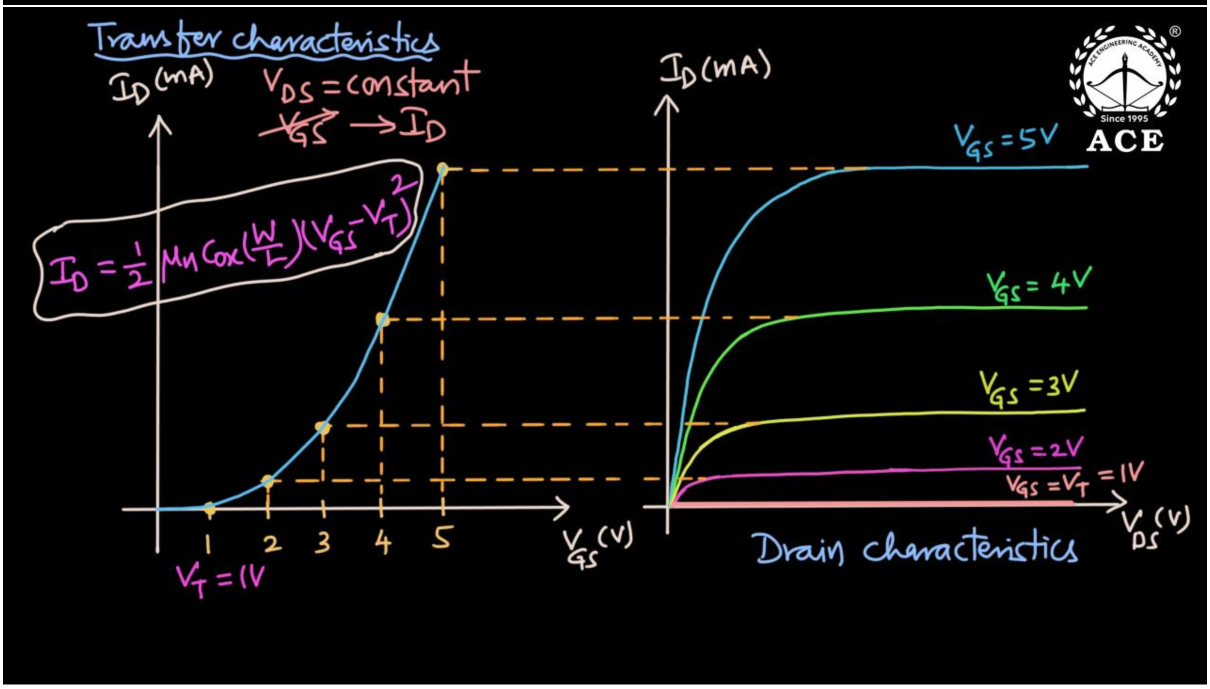
$V_{GD} \leq V_T$

→ The channel is pinched-off at the drain end.

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$



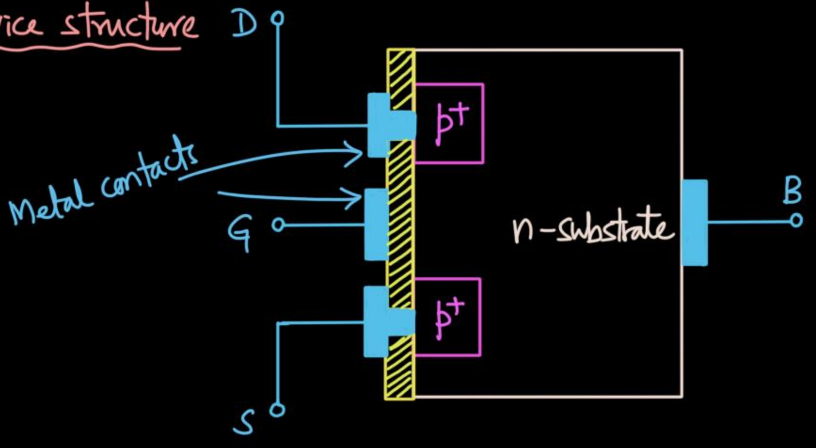
I_D (mA)
Locus of V_{DSsat}
$V_{GS4} > V_{GS3}$
$V_{GS3} > V_{GS2}$
$V_{GS2} > V_{GS1}$
V_{GS1}
$V_{GS} < V_T$
V_{DS} (V)
Drain characteristics
Since 1995
ACE

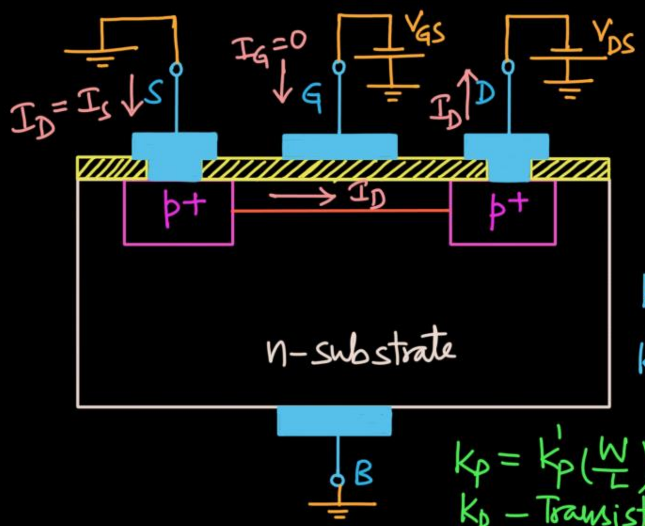


Transfer characteristics
I_D (mA)
V_{DS} = constant
$\cancel{V_{GS}} \rightarrow I_D$
$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_T)^2$
1 2 3 4 5
V_{GS} (V)
V_T = 1V
I_D (mA)
V_{GS} = 5V
V_{GS} = 4V
V_{GS} = 3V
V_{GS} = 2V
$V_{GS} = V_T$ = 1V
V_{DS} (V)
Drain characteristics
Since 1995
ACE

p-channel Enhancement Mode MOSFET

Device structure





Negative

$$V_{GS} \leq V_{TP}$$

$$|V_{GS}| \geq |V_{TP}|$$

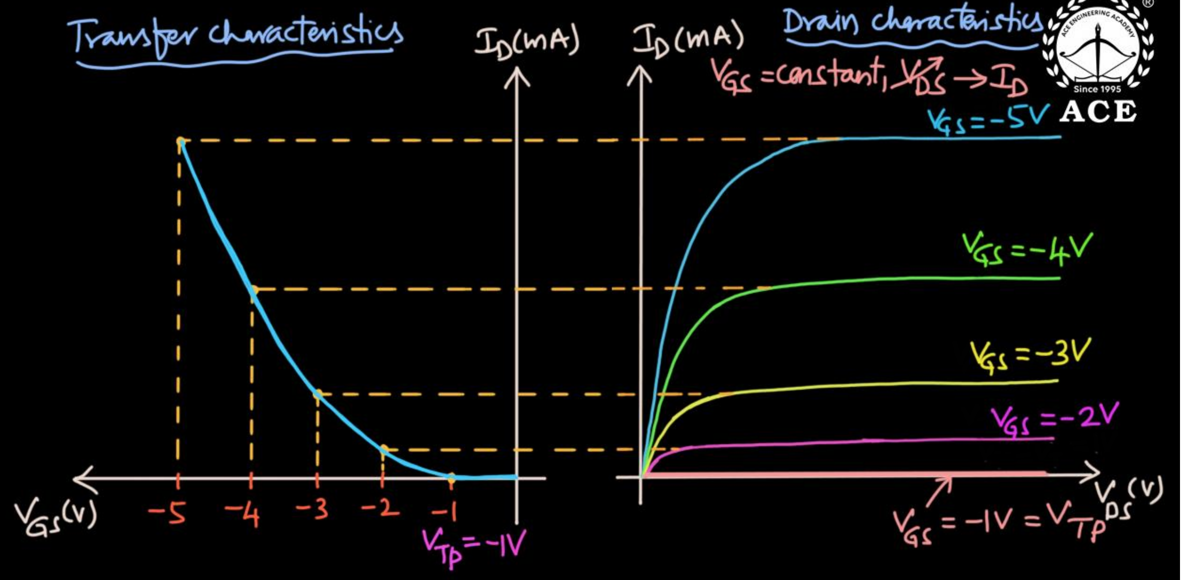
$\Rightarrow$ A channel is created.

$k'_p = \mu_p C_{ox}$

k'_p – process transconductance parameter.

$k_p = k'_p\left(\frac{W}{L}\right) = \mu_p C_{ox}\left(\frac{W}{L}\right)$

k_p – Transistor transconductance parameter



p-channel Enhancement Mode MOSFET

(1) If $V_{SG} < |V_{TP}|$; no channel; Transistor is in cut-off; $I_D = 0$

(2) If $V_{SG} \geq |V_{TP}|$; a channel is induced; transistor operates in triode or saturation region depending upon the channel is contineous or pinched off at the drain end.

Linear

→ The contineous channel is obtained by $V_{SD} < |V_{GS} - V_{TP}|$ (or) $V_{DG} > |V_{TP}|$

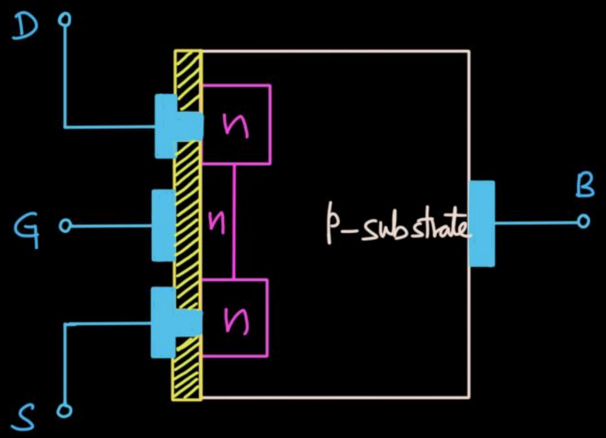
$$I_D = \mu_p C_{ox}\left(\frac{W}{L}\right)\left[(V_{SG} - |V_{TP}|)V_{SD} - \frac{1}{2}V_{SD}^2\right]$$

Saturation

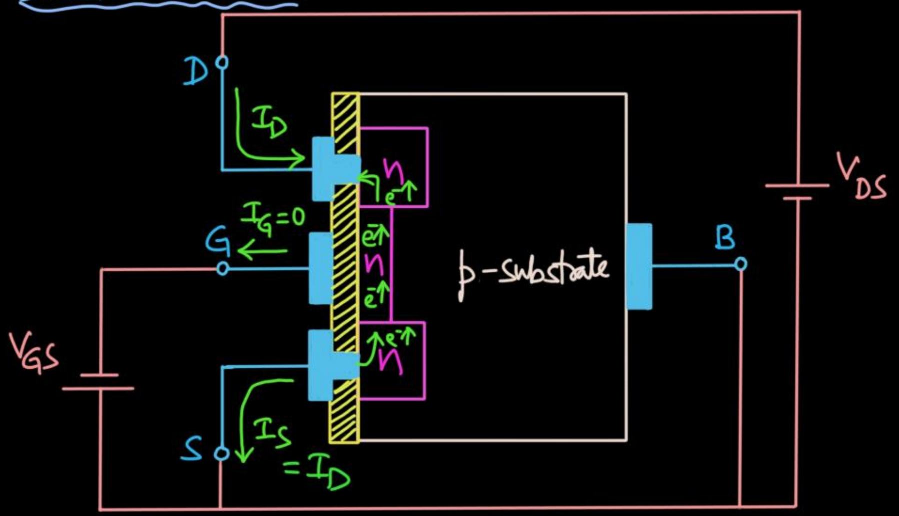
→ Pinched off channel is obtained by $V_{SD} \geq |V_{GS} - V_{TP}|$ or $V_{DG} \leq |V_{TP}|$

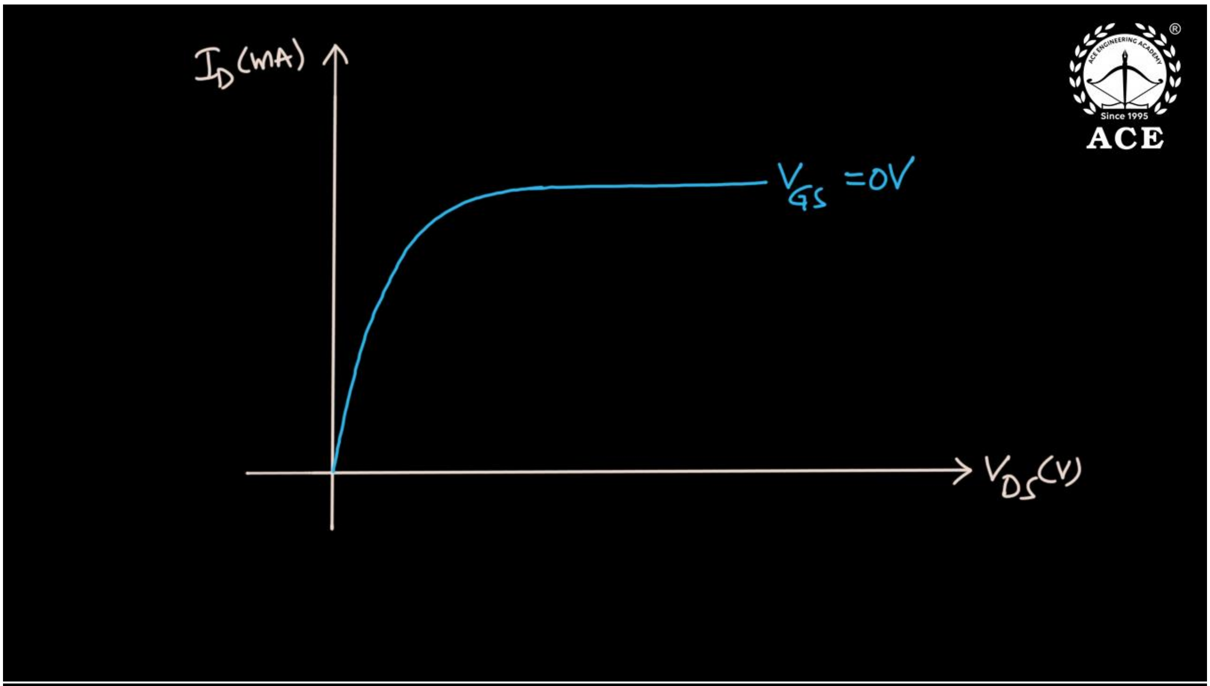
$$I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)(V_{SG} - |V_{TP}|)^2$$

n-Channel Depletion Mode MOSFET

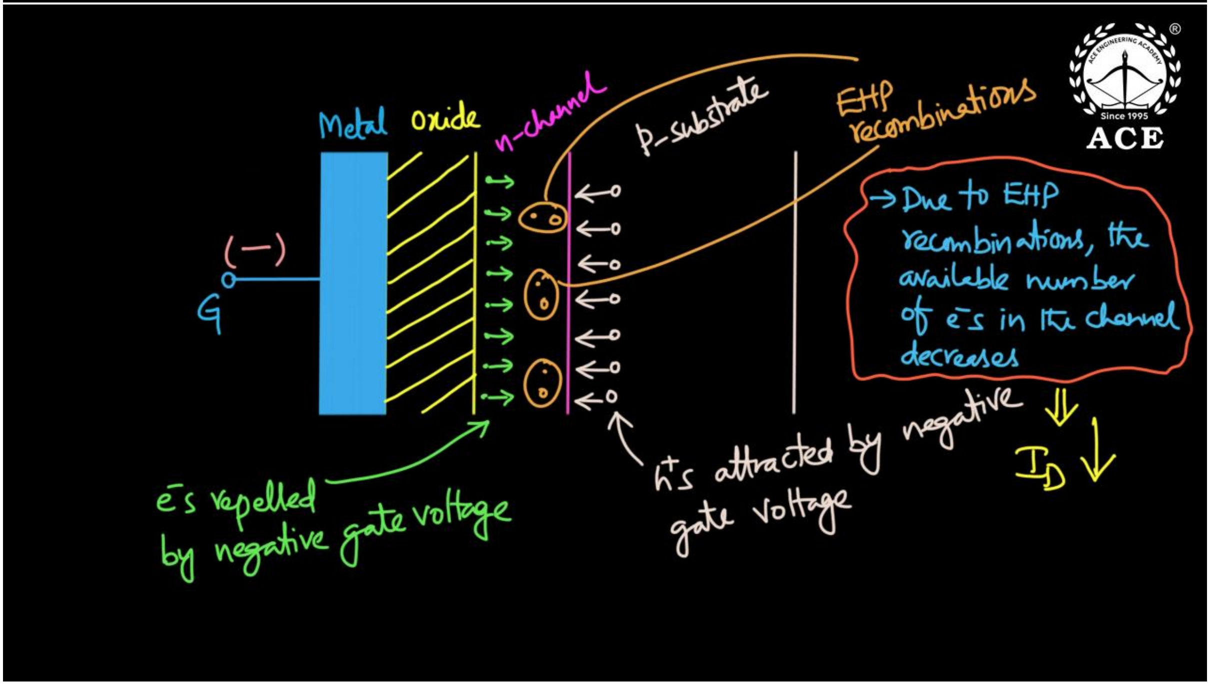


Drain characteristics

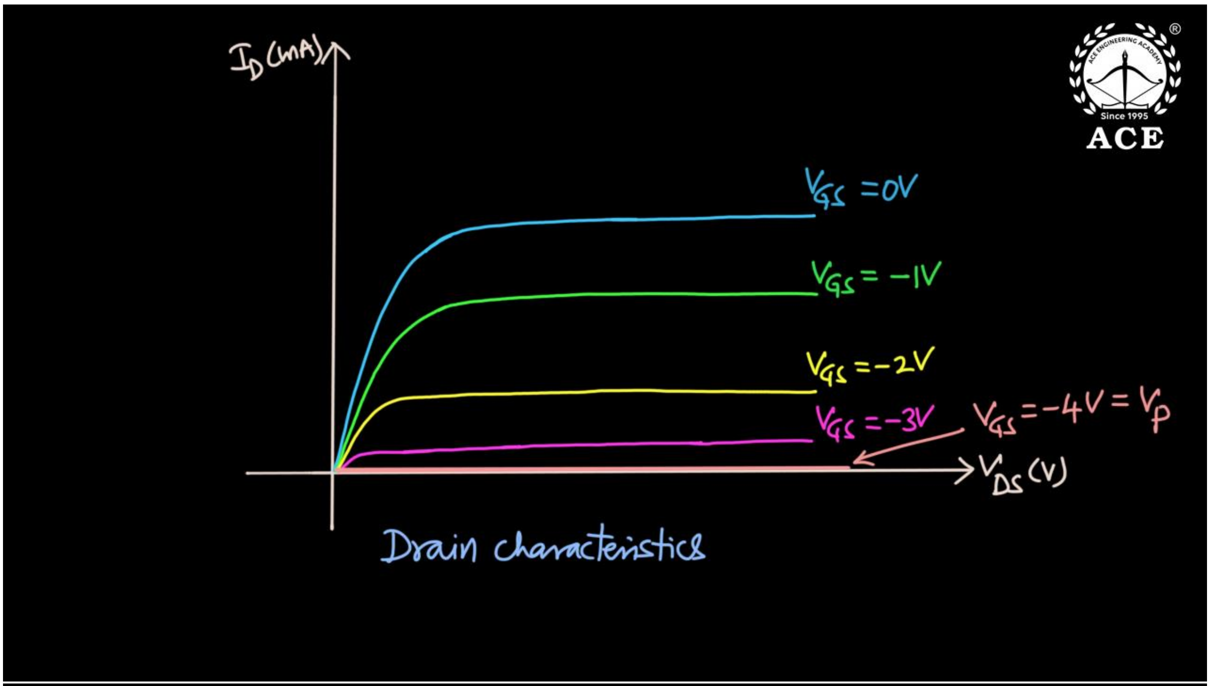




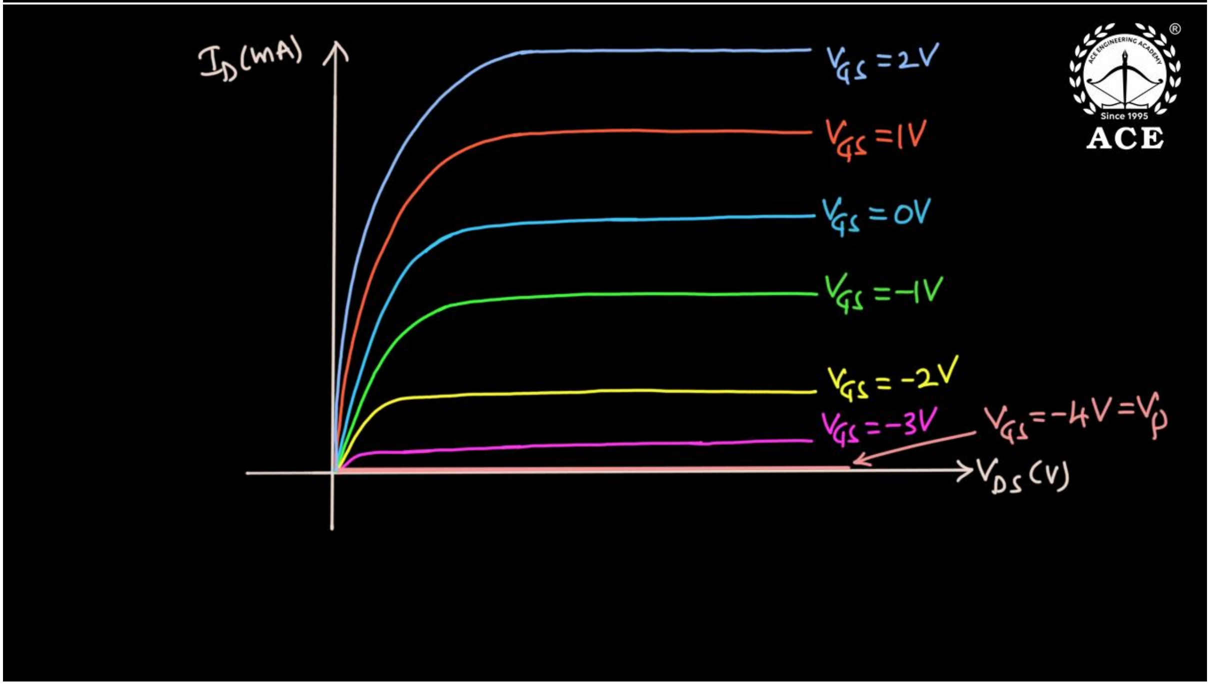
I_D (mA)
$V_{GS} = 0V$
V_{DS} (V)



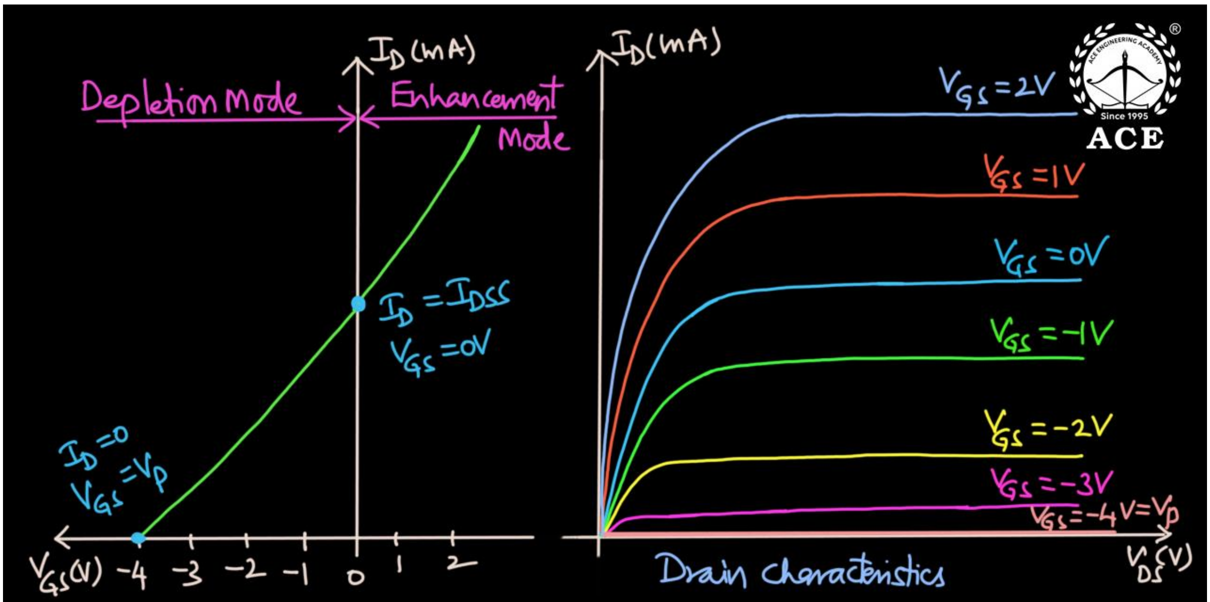
Metal
Oxide
n-channel
p-substrate
EHP recombinations
(−)
G
→ Due to EHP recombinations, the available number of e^-s in the channel decreases
⇓
I_D ↓
e^-s repelled by negative gate voltage
h^+s attracted by negative gate voltage



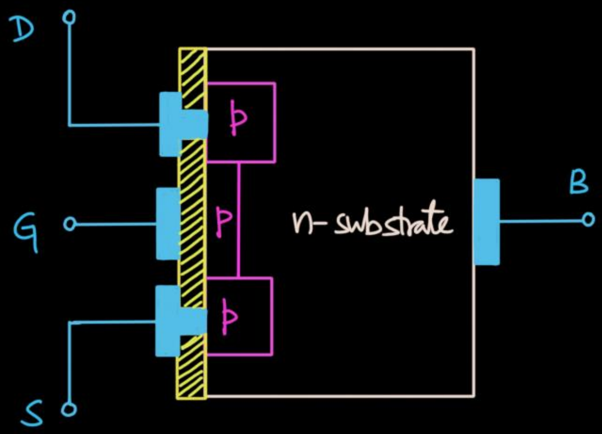
I_D (mA)
$V_{GS} = 0V$
$V_{GS} = -1V$
$V_{GS} = -2V$
$V_{GS} = -3V$
$V_{GS} = -4V = V_P$
V_{DS} (V)
Drain characteristics

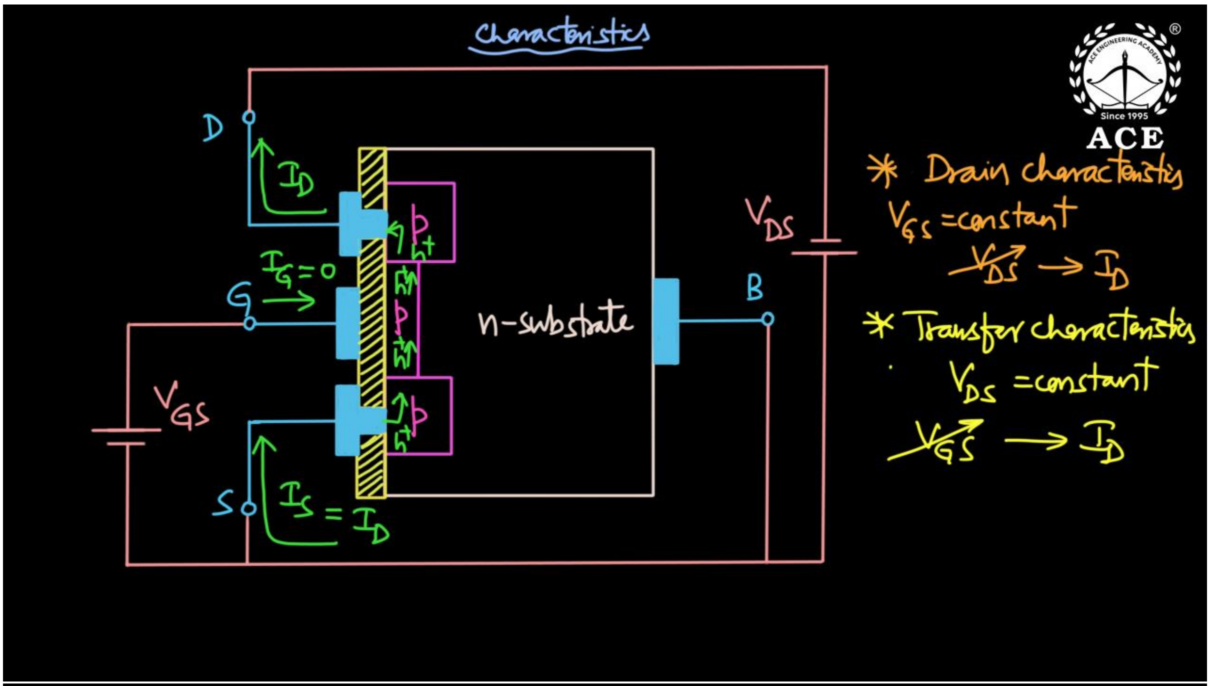


I_D (mA)
$V_{GS} = 2V$
$V_{GS} = 1V$
$V_{GS} = 0V$
$V_{GS} = -1V$
$V_{GS} = -2V$
$V_{GS} = -3V$
$V_{GS} = -4V = V_P$
V_{DS} (V)

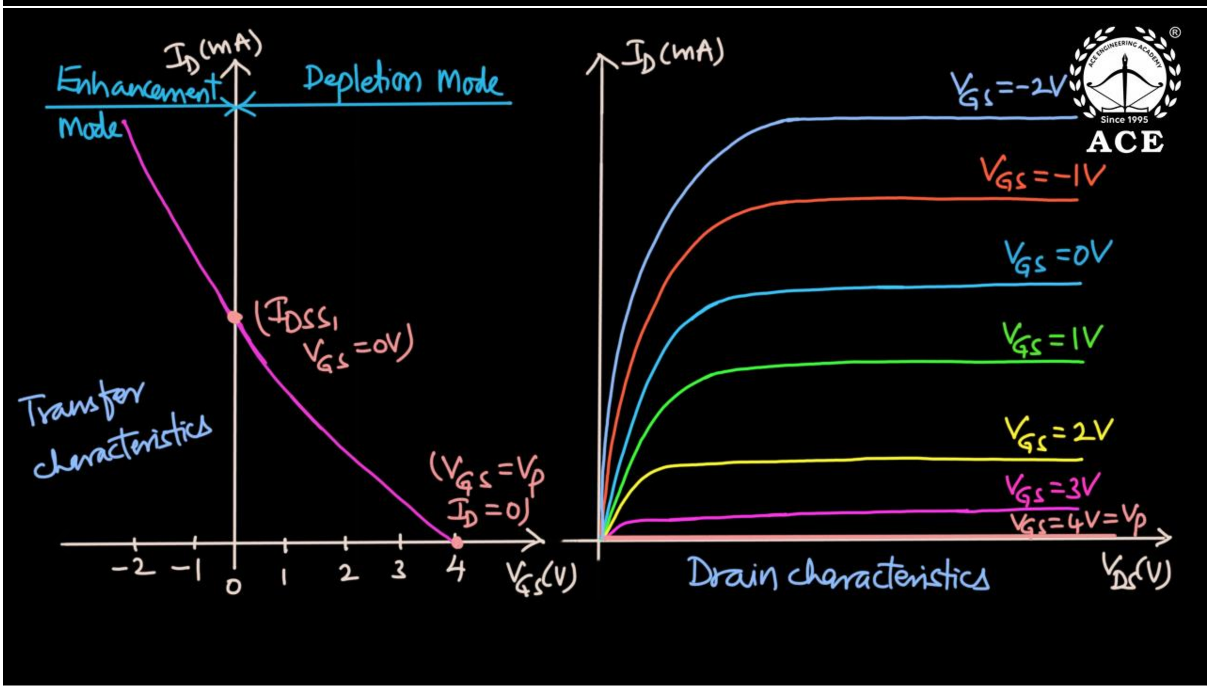


P-channel Depletion Mode MOSFET





Characteristics
D
I_D
I_G = 0
G
V_GS
S
I_S = I_D
p
n+
n-substrate
B
V_DS
* Drain characteristics
V_GS = constant
V_DS → I_D
* Transfer characteristics
V_DS = constant
V_GS → I_D



I_D (mA)
Enhancement Mode
Depletion Mode
(I_DSS, V_GS = 0V)
Transfer characteristics
(V_GS = V_P, I_D = 0)
−2 −1 0 1 2 3 4
V_GS(V)
V_GS = −2V
V_GS = −1V
V_GS = 0V
V_GS = 1V
V_GS = 2V
V_GS = 3V
V_GS = 4V = V_P
Drain characteristics
V_DS(V)