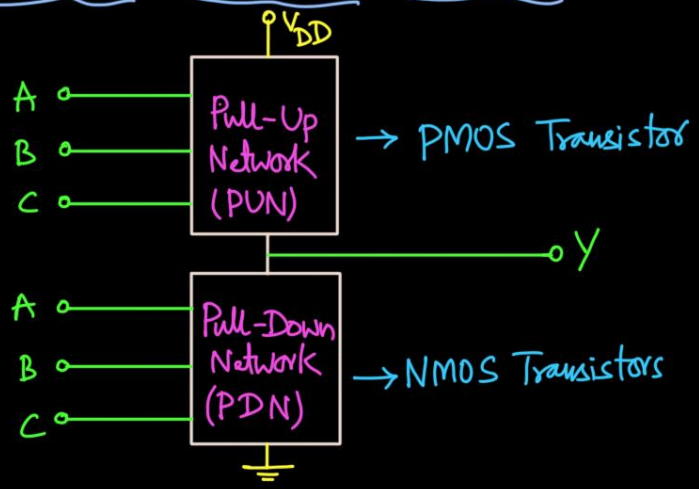
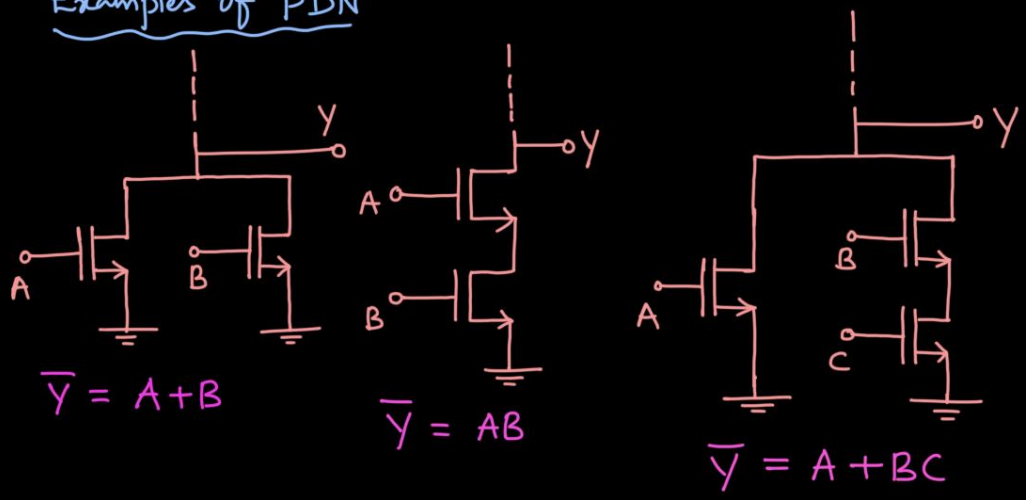
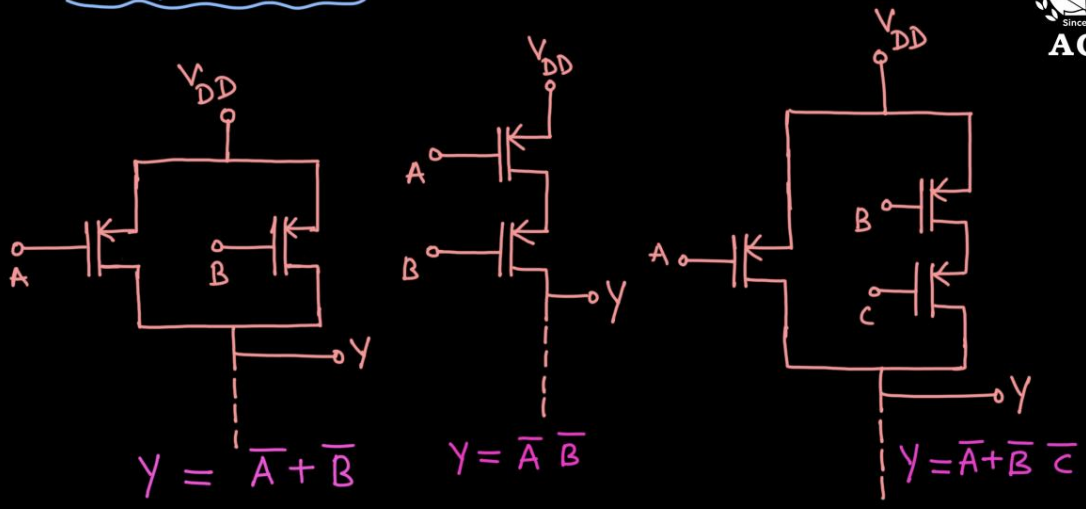
General structure of CMOS Logic



Examples of PDN



Examples of PUN



$Y = \overline{A} + \overline{B}$ $\quad Y = \overline{A}\,\overline{B}$ $\quad Y = \overline{A} + \overline{B}\,\overline{C}$

→ To implement AND functionality, the devices are connected in series.

→ To implement OR functionality, the devices are connected in parallel.

***

NMOS – Inputs are uncomplemented and output is complemented.

PMOS – Inputs are complemented and output is uncomplemented.

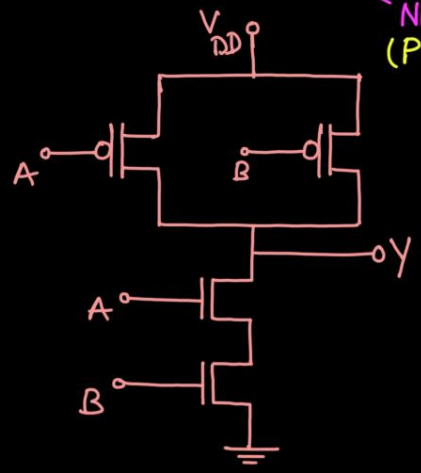
→ The PDN utilizes devices in parallel to form an OR function and devices in series to form an AND function; the same is true for PUN.
Here OR and AND notation refer to current flow or conduction of the device.

2 - Input NAND Gate

$Y = \overline{AB}$ (or) $\overline{Y} = AB$ (or) $Y = \overline{A} + \overline{B}$

$\overline{Y} = AB$ ↔ NMOS (PDN)

$Y = \overline{A} + \overline{B}$ ↔ PMOS (PUN)



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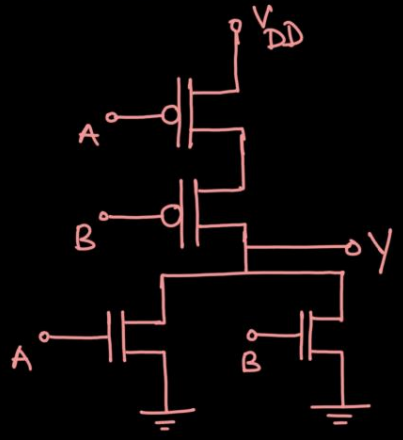
2 Input NOR Gate $Y = \overline{A+B}$ or $\overline{Y} = A+B$ or $Y = \overline{A}\,\overline{B}$

$\overline{Y} = A+B$ ↔ NMOS (PDN)

$Y = \overline{A}\,\overline{B}$ ↔ PMOS (PUN)



→ To implement n-input NAND or NOR gate using either NMOS or PMOS we require n transistors. But to implement the same using CMOS logic we need 2n transistors.

$\overline{Y} = A(B+CD)$ – NMOS (PDN)

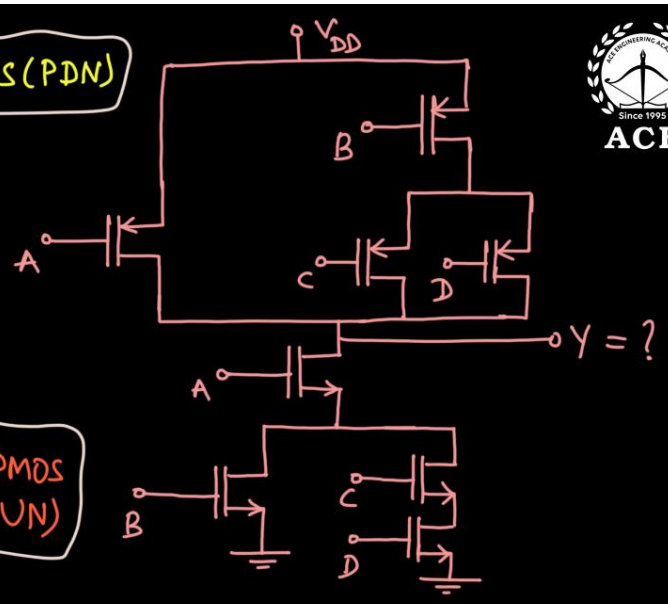
$\Rightarrow Y = \overline{A(B+CD)}$

$= \overline{A} + \overline{(B+CD)}$

$= \overline{A} + \overline{B}\,\overline{(CD)}$

$= \overline{A} + \overline{B}(\overline{C}+\overline{D})$

$Y = \overline{A} + \overline{B}(\overline{C}+\overline{D})$ – PMOS (PUN)



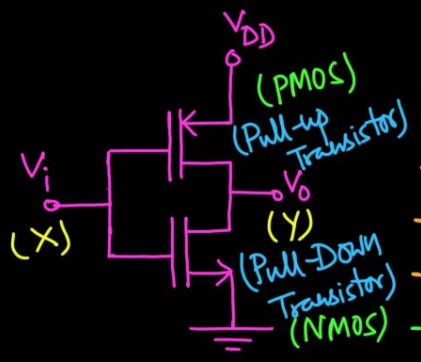
Summary of Synthesis Method

→ The "PDN" can be most directly synthesized by expressing "$\overline{Y}$" as a function of the "uncomplemented variables". If complemented variables appears in the expression then additional inverters are required

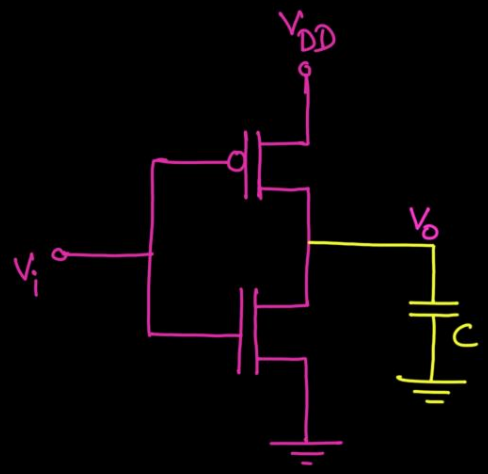
→ The "PUN" can be most directly synthesized by expressing "Y" as a function of the "complemented variables". If uncomplemented variables are present then additional inverters are required.

→ The PUN can be obtained from PDN and vice-versa using duality principle.

CMOS Inverter

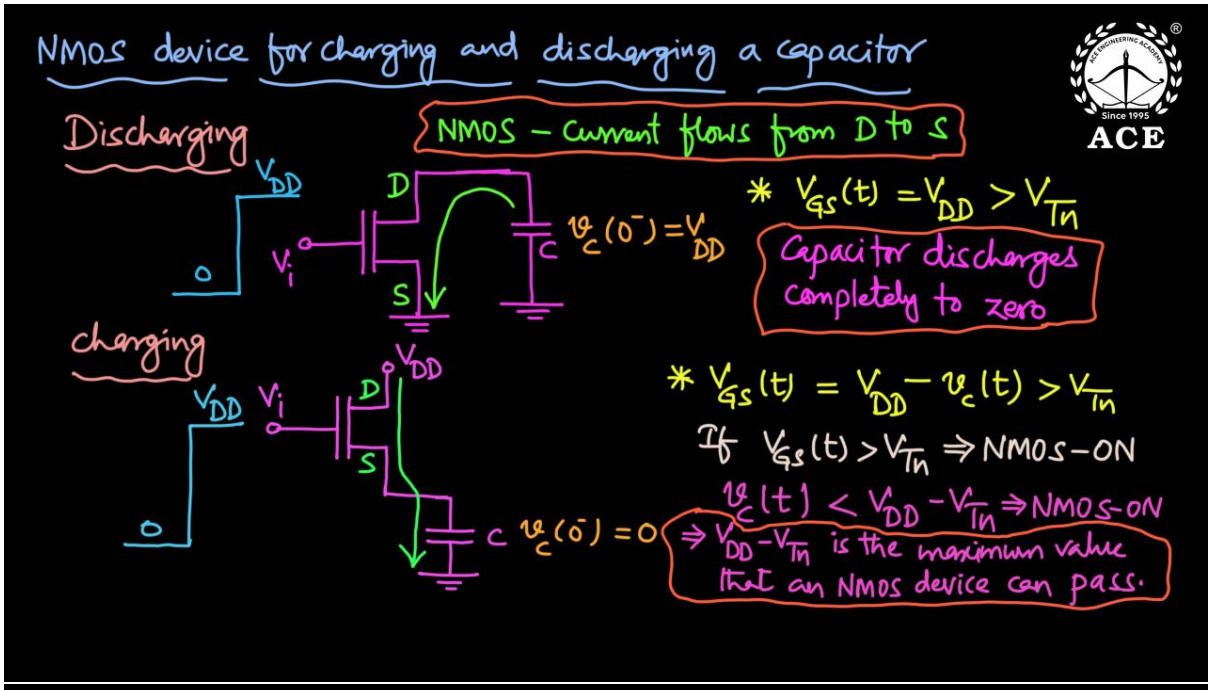


→ NMOS device for charging and discharging a capacitor
→ PMOS device for charging and discharging a capacitor
→ Voltage-Transfer-characteristics (VTC)
→ Noise Margins
→ Switching Threshold (or) Trip point
→ Propagation delay
→ Transistor sizing
→ Power dissipation

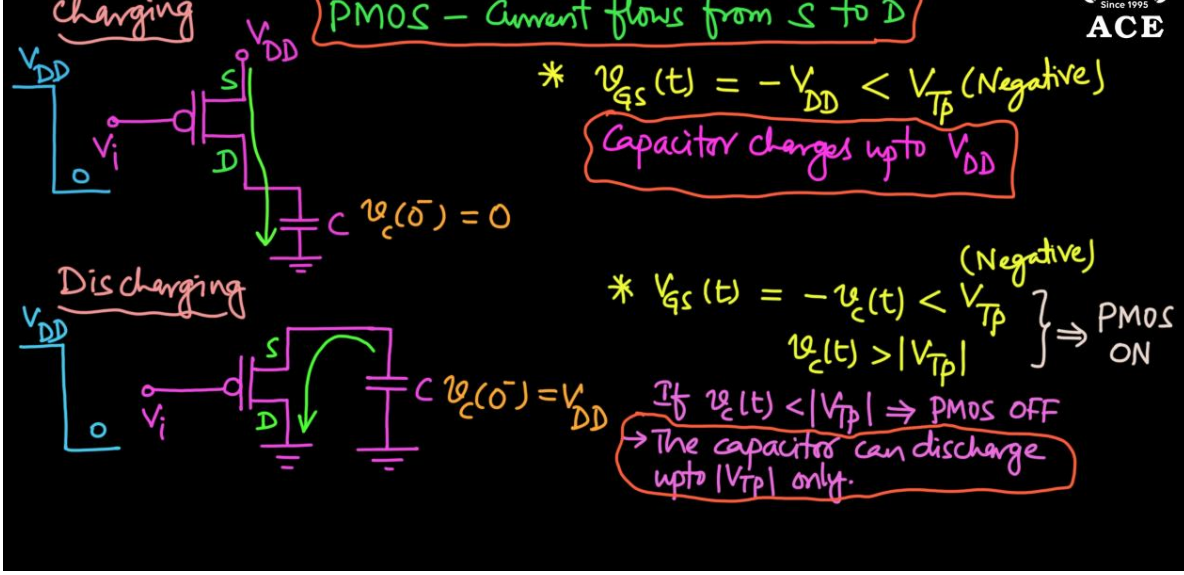


PMOS	Charging
NMOS	Discharging

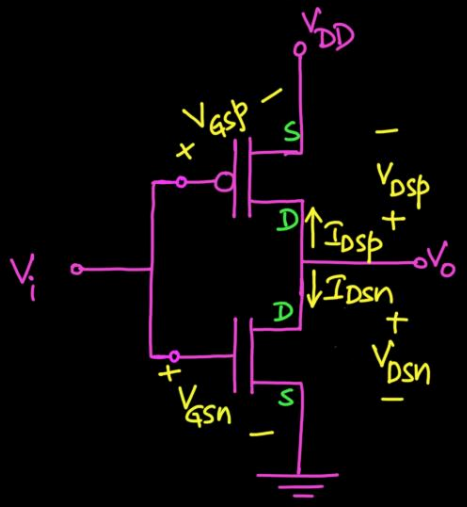
NMOS device for charging and discharging a capacitor



PMOS device for charging and discharging a capacitor



Voltage - Transfer - characteristics (VTC)



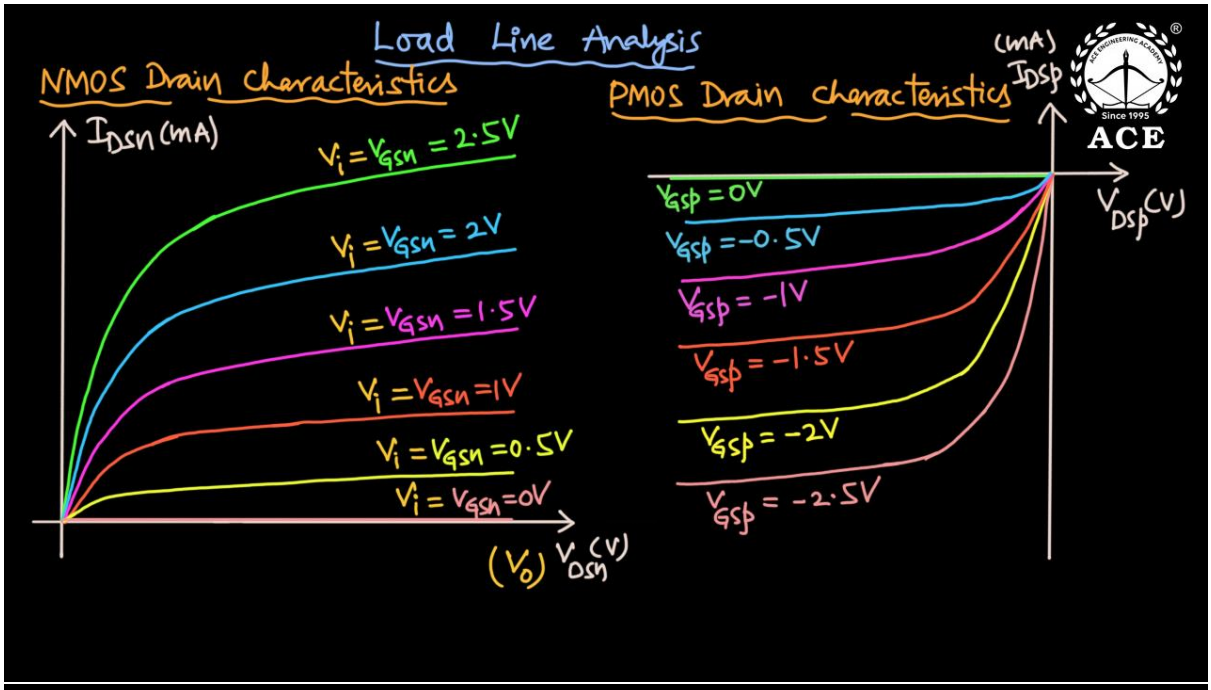
$$I_{DSP} = -I_{DSN} \quad ***$$

$$V_{GSN} = V_i \;, \quad V_{DSN} = V_o$$

$$V_{GSP} = V_i - V_{DD} \;, \quad V_{DSP} = V_o - V_{DD}$$

Relation between voltages of NMOS and PMOS devices of the CMOS Inverter

	Cut-off	Triode (or) Linear	Saturation
NMOS	$V_{GSN} < V_{tn}$ $V_i < V_{tn}$	$V_{GSN} > V_{tn}$ $V_i > V_{tn}$	$V_{GSN} > V_{tn}$ $V_i > V_{tn}$
		$V_{DSN} < V_{GSN} - V_{tn}$ $V_o < V_i - V_{tn}$	$V_{DSN} > V_{GSN} - V_{tn}$ $V_o > V_i - V_{tn}$
PMOS	$V_{GSP} > V_{tp}$ $V_i > V_{tp} + V_{DD}$	$V_{GSP} < V_{tp}$ $V_i < V_{tp} + V_{DD}$	$V_{GSP} < V_{tp}$ $V_i < V_{tp} + V_{DD}$
		$V_{DSP} > V_{GSP} - V_{tp}$ $V_o > V_i - V_{tp}$	$V_{DSP} < V_{GSP} - V_{tp}$ $V_o < V_i - V_{tp}$


Load Line Analysis
NMOS Drain characteristics
PMOS Drain characteristics
I_{DSn} (mA)
$V_i = V_{GSn} = 2.5V$
$V_i = V_{GSn} = 2V$
$V_i = V_{GSn} = 1.5V$
$V_i = V_{GSn} = 1V$
$V_i = V_{GSn} = 0.5V$
$V_i = V_{GSn} = 0V$
(V_o) V_{DSn} (V)
(mA) I_{DSp}
$V_{GSp} = 0V$
$V_{GSp} = -0.5V$
$V_{GSp} = -1V$
$V_{GSp} = -1.5V$
$V_{GSp} = -2V$
$V_{GSp} = -2.5V$
V_{DSp} (V)
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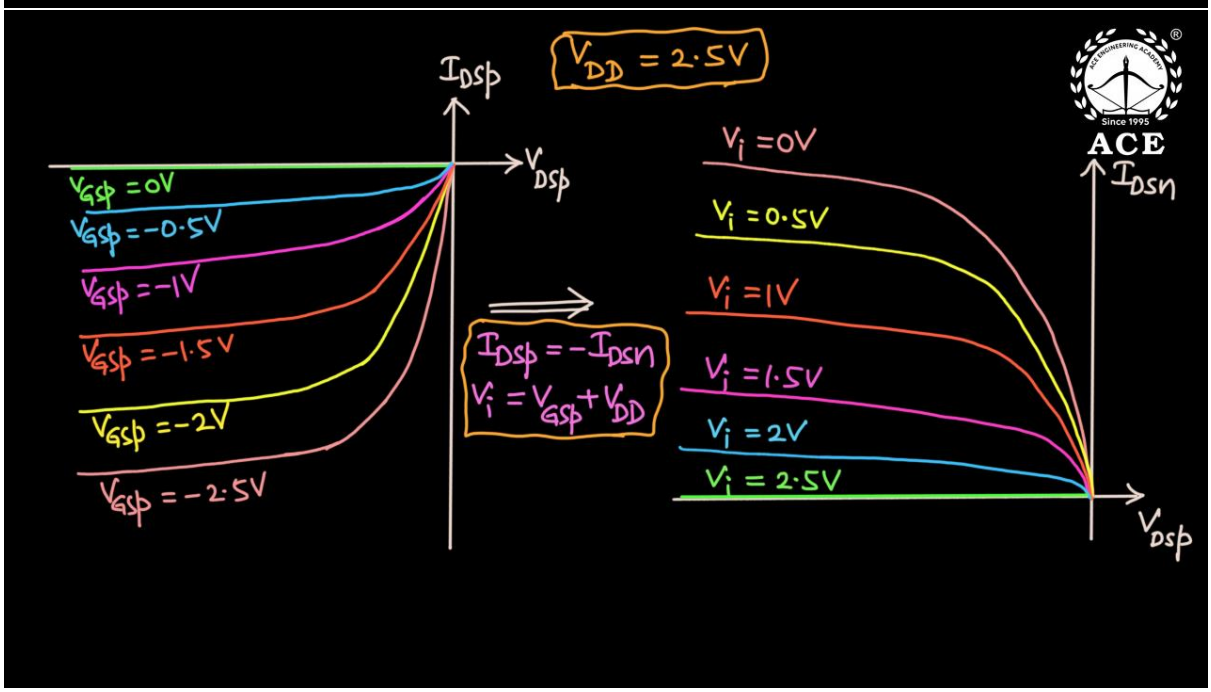
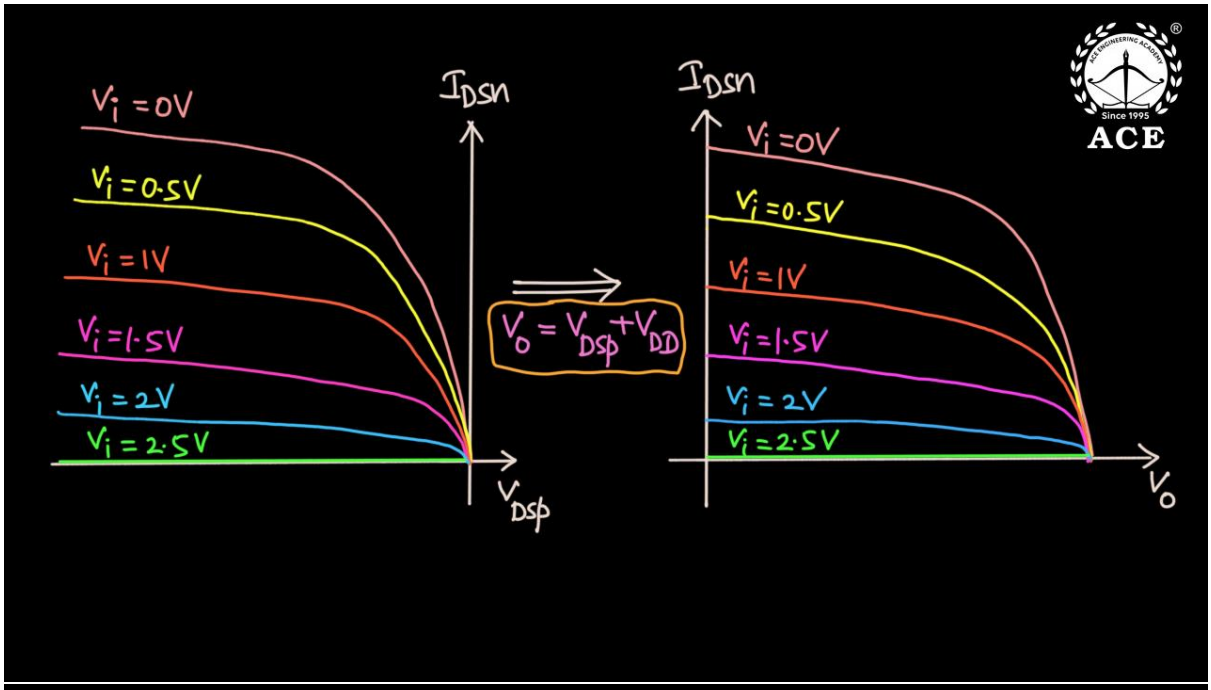
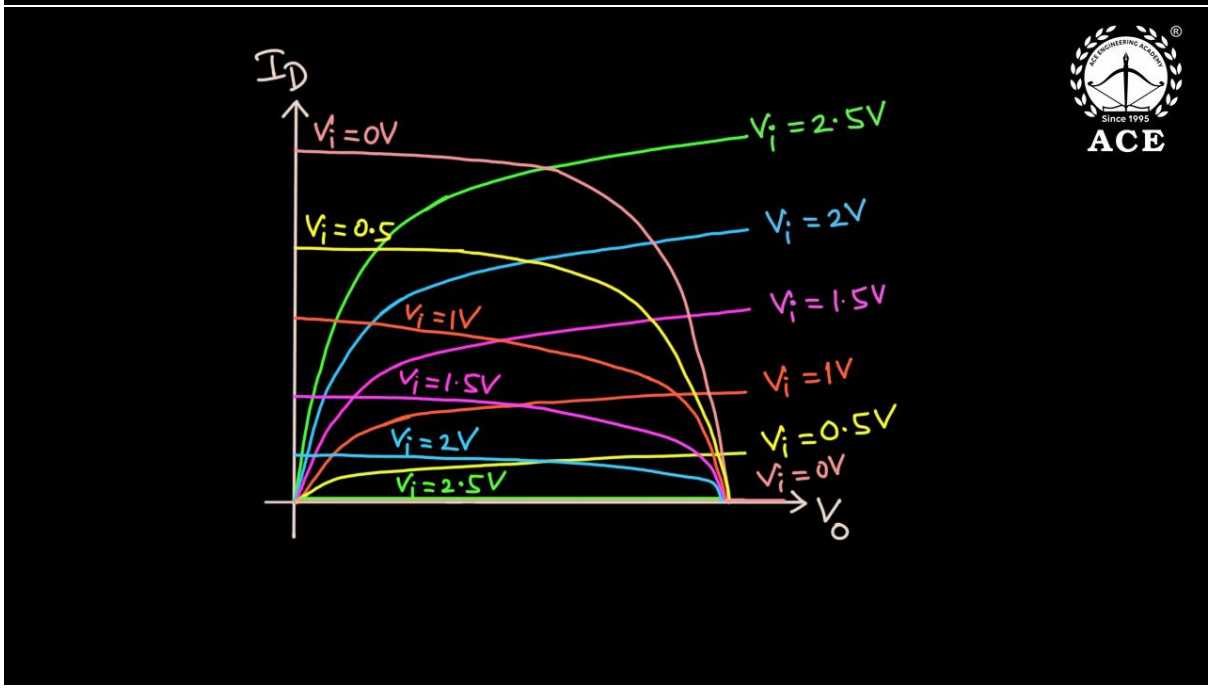
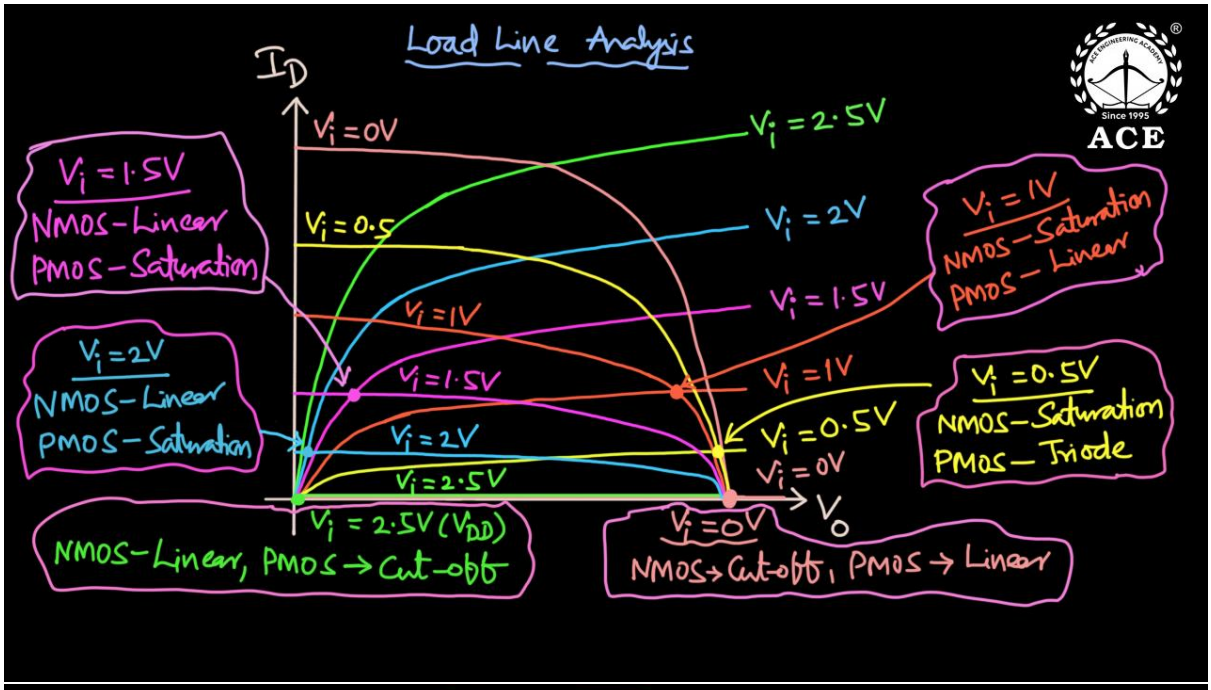
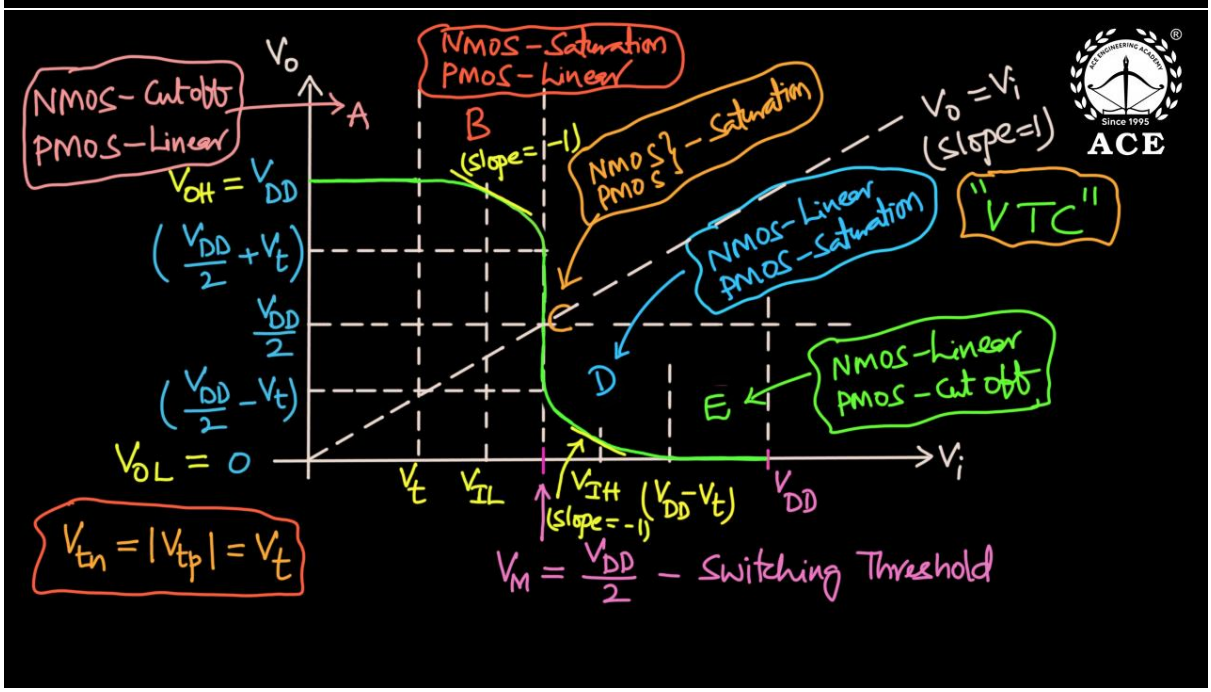

I_{DSp}
$V_{DD} = 2.5V$
$V_{GSp} = 0V$
$V_{GSp} = -0.5V$
$V_{GSp} = -1V$
$V_{GSp} = -1.5V$
$V_{GSp} = -2V$
$V_{GSp} = -2.5V$
V_{DSp}
$I_{DSp} = -I_{DSn}$
$V_i = V_{GSp} + V_{DD}$
$V_i = 0V$
$V_i = 0.5V$
$V_i = 1V$
$V_i = 1.5V$
$V_i = 2V$
$V_i = 2.5V$
I_{DSn}
V_{DSp}
ACE
Since 1995


$V_i = 0V$
$V_i = 0.5V$
$V_i = 1V$
$V_i = 1.5V$
$V_i = 2V$
$V_i = 2.5V$
I_{DSn}
V_{DSp}
$V_o = V_{DSp} + V_{DD}$
I_{DSn}
$V_i = 0V$
$V_i = 0.5V$
$V_i = 1V$
$V_i = 1.5V$
$V_i = 2V$
$V_i = 2.5V$
V_o
ACE
Since 1995

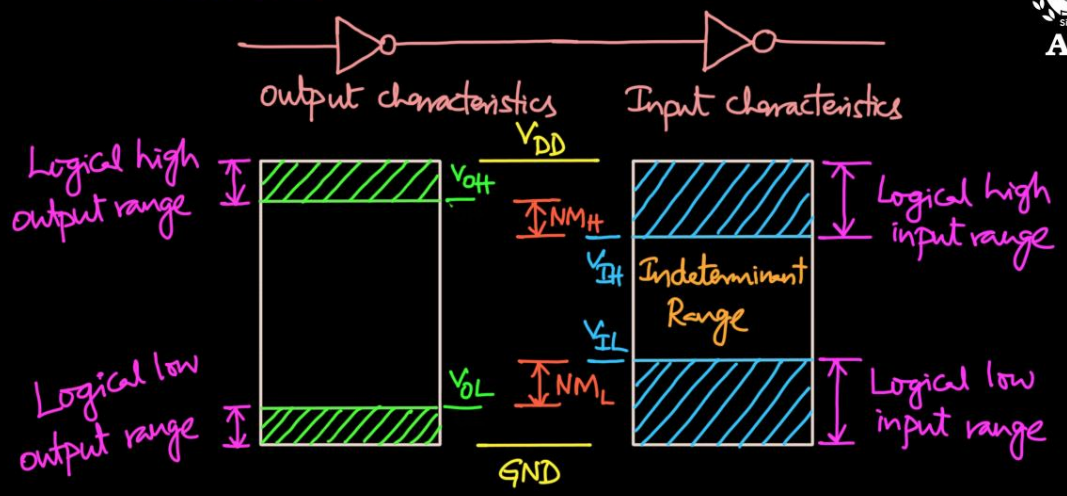

I_D
$V_i = 0V$
$V_i = 0.5$
$V_i = 1V$
$V_i = 1.5V$
$V_i = 2V$
$V_i = 2.5V$
$V_i = 2.5V$
$V_i = 2V$
$V_i = 1.5V$
$V_i = 1V$
$V_i = 0.5V$
$V_i = 0V$
V_o
ACE
Since 1995


Load Line Analysis
I_D
$V_i = 0V$
$V_i = 0.5$
$V_i = 1V$
$V_i = 1.5V$
$V_i = 2V$
$V_i = 2.5V$
V_o
$V_i = 1.5V$
NMOS – Linear
PMOS – Saturation
$V_i = 2V$
NMOS – Linear
PMOS – Saturation
$V_i = 1V$
NMOS – Saturation
PMOS – Linear
$V_i = 0.5V$
NMOS – Saturation
PMOS – Triode
$V_i = 2.5V (V_{DD})$
NMOS – Linear, PMOS → Cut-off
$V_i = 0V$
NMOS → Cut-off, PMOS → Linear


V_o
NMOS – Cut off
PMOS – Linear
A
NMOS – Saturation
PMOS – Linear
B
(slope = -1)
NMOS – Saturation
PMOS
$V_o = V_i$
(slope = 1)
"VTC"
NMOS – Linear
PMOS – Saturation
C
D
E
NMOS – Linear
PMOS – Cut off
$V_{OH} = V_{DD}$
$\left(\frac{V_{DD}}{2} + V_t\right)$
$\frac{V_{DD}}{2}$
$\left(\frac{V_{DD}}{2} - V_t\right)$
$V_{OL} = 0$
V_t
V_{IL}
V_{IH} (slope = -1)
$(V_{DD} - V_t)$
V_{DD}
V_i
$V_{tn} = |V_{tp}| = V_t$
$V_M = \frac{V_{DD}}{2}$ – Switching Threshold

Region	Condition	NMOS	PMOS	Output
A	$0 \le V_i < V_{tn}$	Cut-off	Triode	V_{DD}
B	$V_{tn} \le V_i < \frac{V_{DD}}{2}$	Saturation	Triode	$V_o > \frac{V_{DD}}{2}$
C	$V_i = \frac{V_{DD}}{2}$	Saturation	Saturation	V_o drops sharply
D	$\frac{V_{DD}}{2} < V_i \le (V_{DD} - V_{tp})$	Triode	Saturation	$V_o < \frac{V_{DD}}{2}$
E	$V_i > (V_{DD} - V_{tp})$	Triode	Cut-off	$V_o = 0$

Noise Margins



V_{OL} — maximum LOW output voltage

V_{OH} — minimum HIGH output voltage

V_{IL} — maximum LOW input voltage

V_{IH} — minimum HIGH input voltage

NM_L — Low noise margin

NM_H — High noise margin

$NM_L = V_{IL} - V_{OL}$

$NM_H = V_{OH} - V_{IH}$