PMOD: LED & SWITCHES

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5/11/2022

Introduction

- What is a PMOD?
  - SSD
  - LED
  - SWITCHES
- My Design
  - Project Outline
  - Code
  - Simulation
  - Troubleshooting / Difficulties

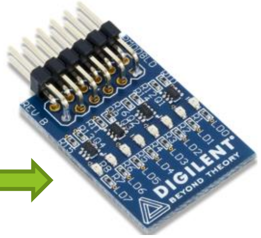
DIGILENT®
A National Instruments Company

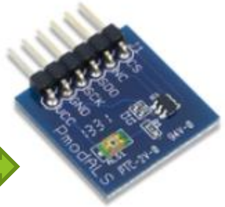
XILINX®

PMOD

- Created by Digilent
- Compact I/O interface board
- Used with FPGA and microcontroller development boards
- User Friendly

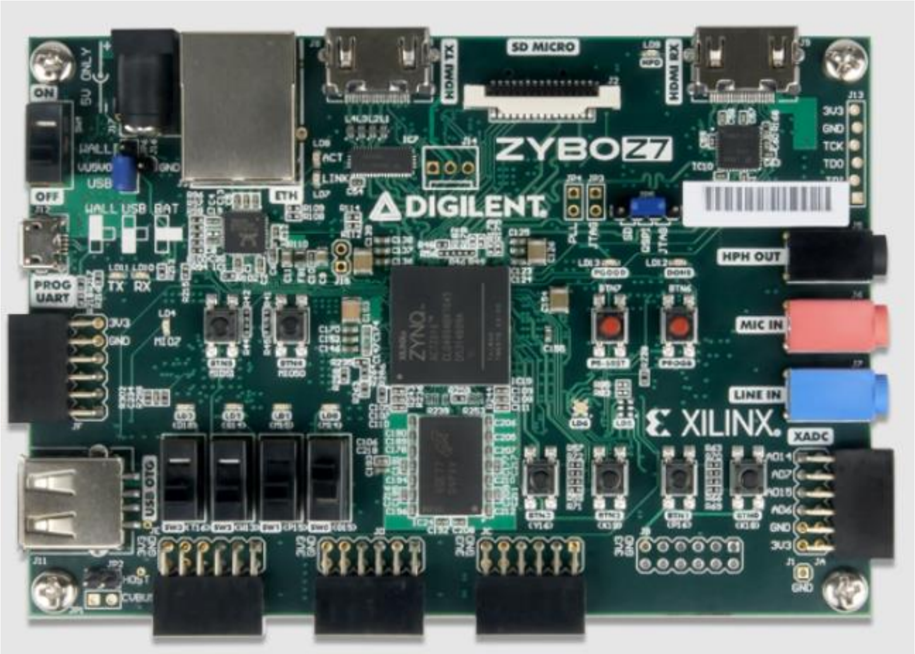
- Common Pmods:
  - LEDs
  - SSDs
  - Ambient Light Sensor
  - Bluetooth Interface





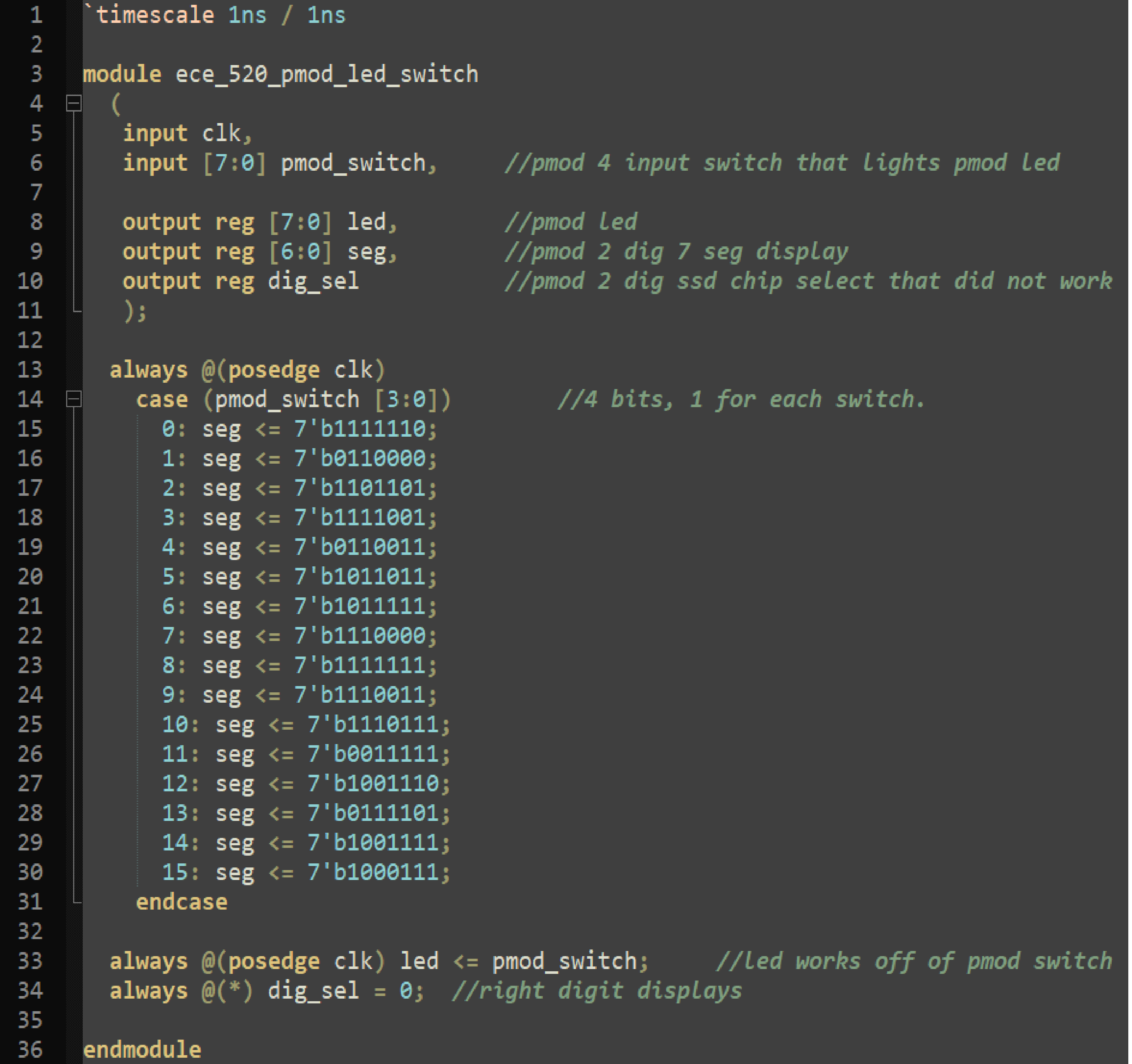
My Design

- Test Plan
  - Create inputs/outputs
  - Create a case from 00 to 15
  - Map pinouts of Pmod
  - Record results



Zybo Z7 10 FPGA Board

My Code



```verilog
`timescale 1ns / 1ns

module ece_520_pmod_led_switch
  (
   input clk,
   input [7:0] pmod_switch,     //pmod 4 input switch that lights pmod led

   output reg [7:0] led,        //pmod led
   output reg [6:0] seg,        //pmod 2 dig 7 seg display
   output reg dig_sel           //pmod 2 dig ssd chip select that did not work
   );

  always @(posedge clk)
    case (pmod_switch [3:0])        //4 bits, 1 for each switch.
      0: seg <= 7'b1111110;
      1: seg <= 7'b0110000;
      2: seg <= 7'b1101101;
      3: seg <= 7'b1111001;
      4: seg <= 7'b0110011;
      5: seg <= 7'b1011011;
      6: seg <= 7'b1011111;
      7: seg <= 7'b1110000;
      8: seg <= 7'b1111111;
      9: seg <= 7'b1110011;
      10: seg <= 7'b1110111;
      11: seg <= 7'b0011111;
      12: seg <= 7'b1001110;
      13: seg <= 7'b0111101;
      14: seg <= 7'b1001111;
      15: seg <= 7'b1000111;
    endcase

  always @(posedge clk) led <= pmod_switch;     //led works off of pmod switch
  always @(*) dig_sel = 0;  //right digit displays

endmodule
```

ZYBO Z7
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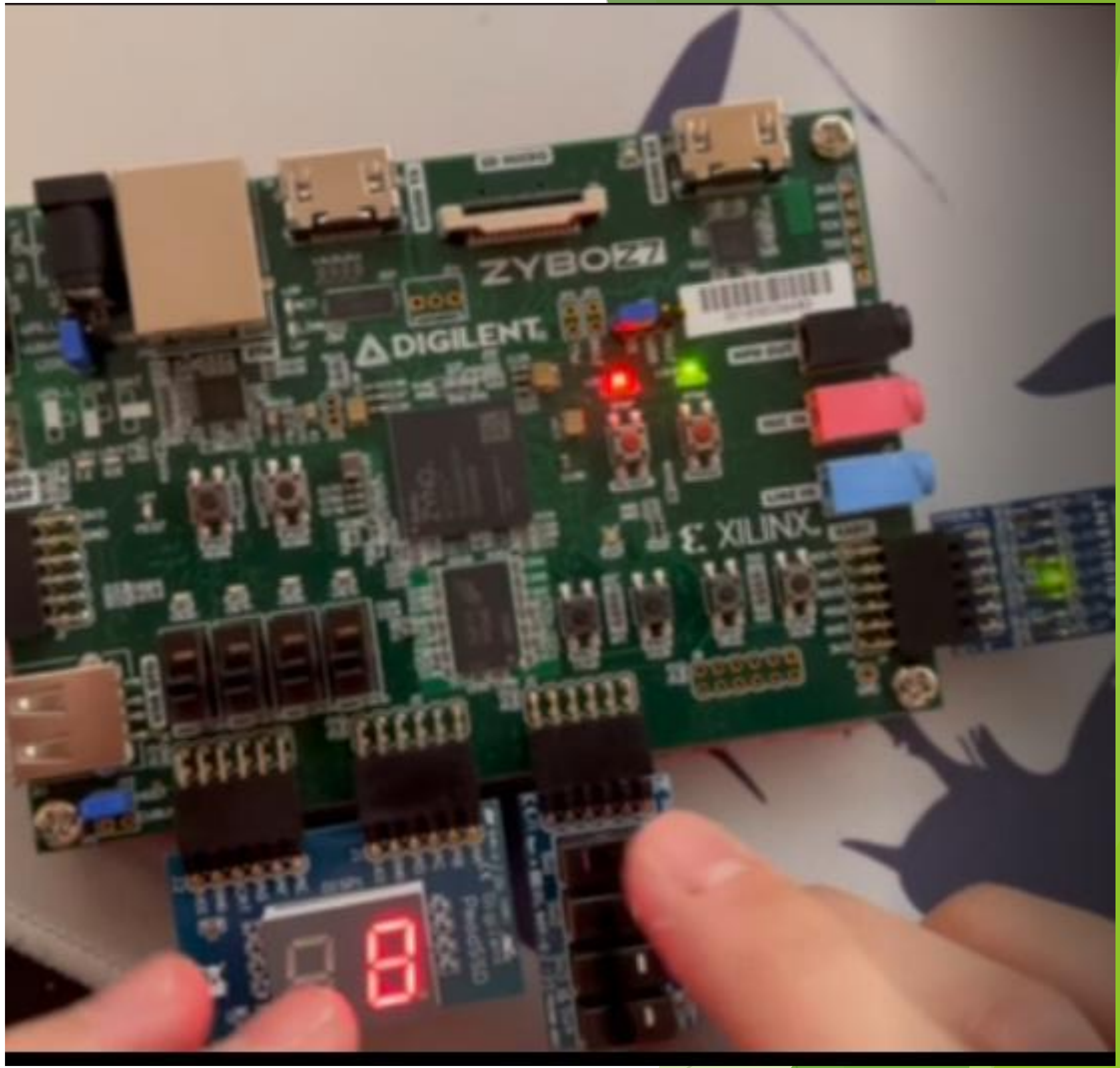

ZYBO Z7
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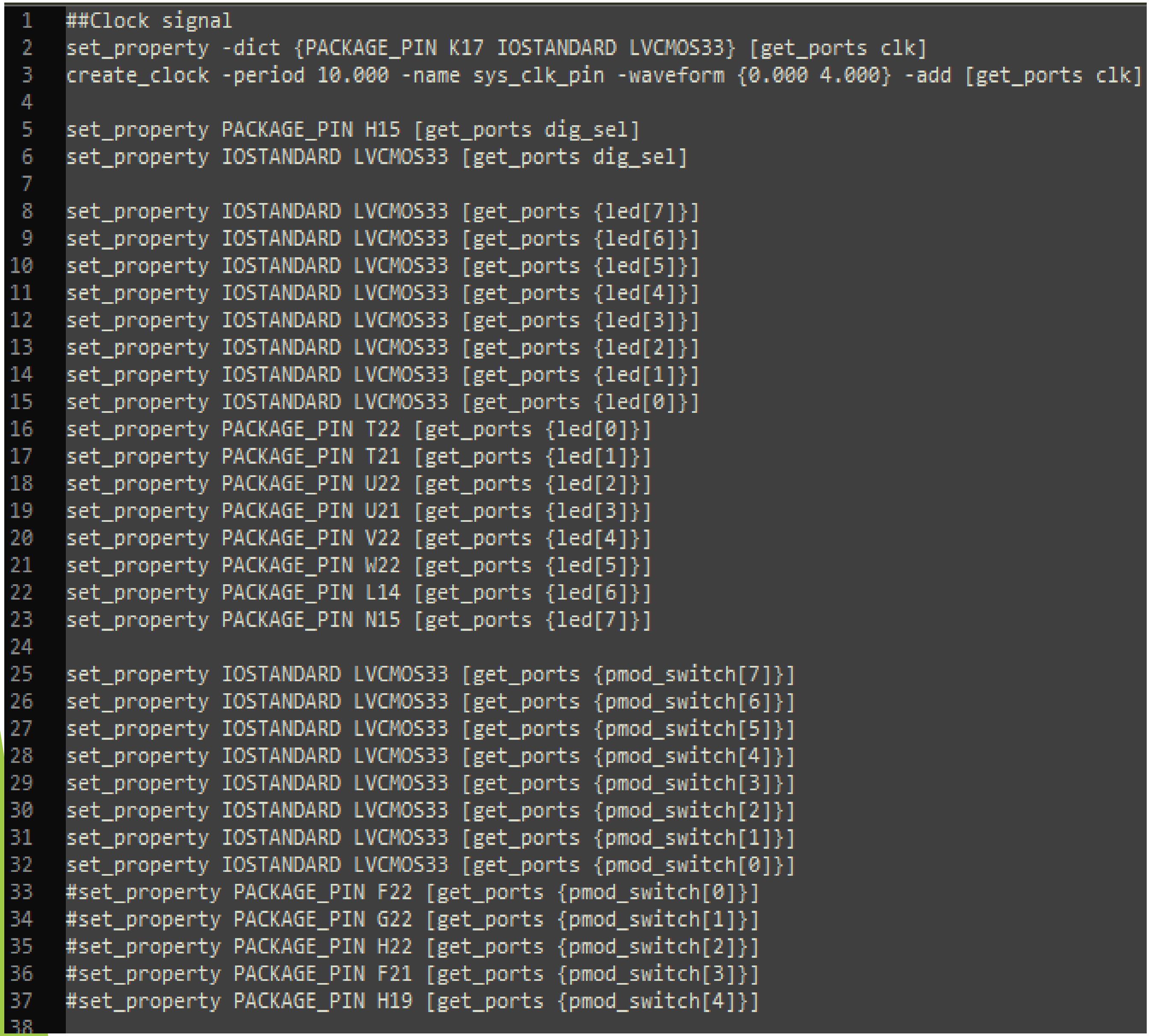
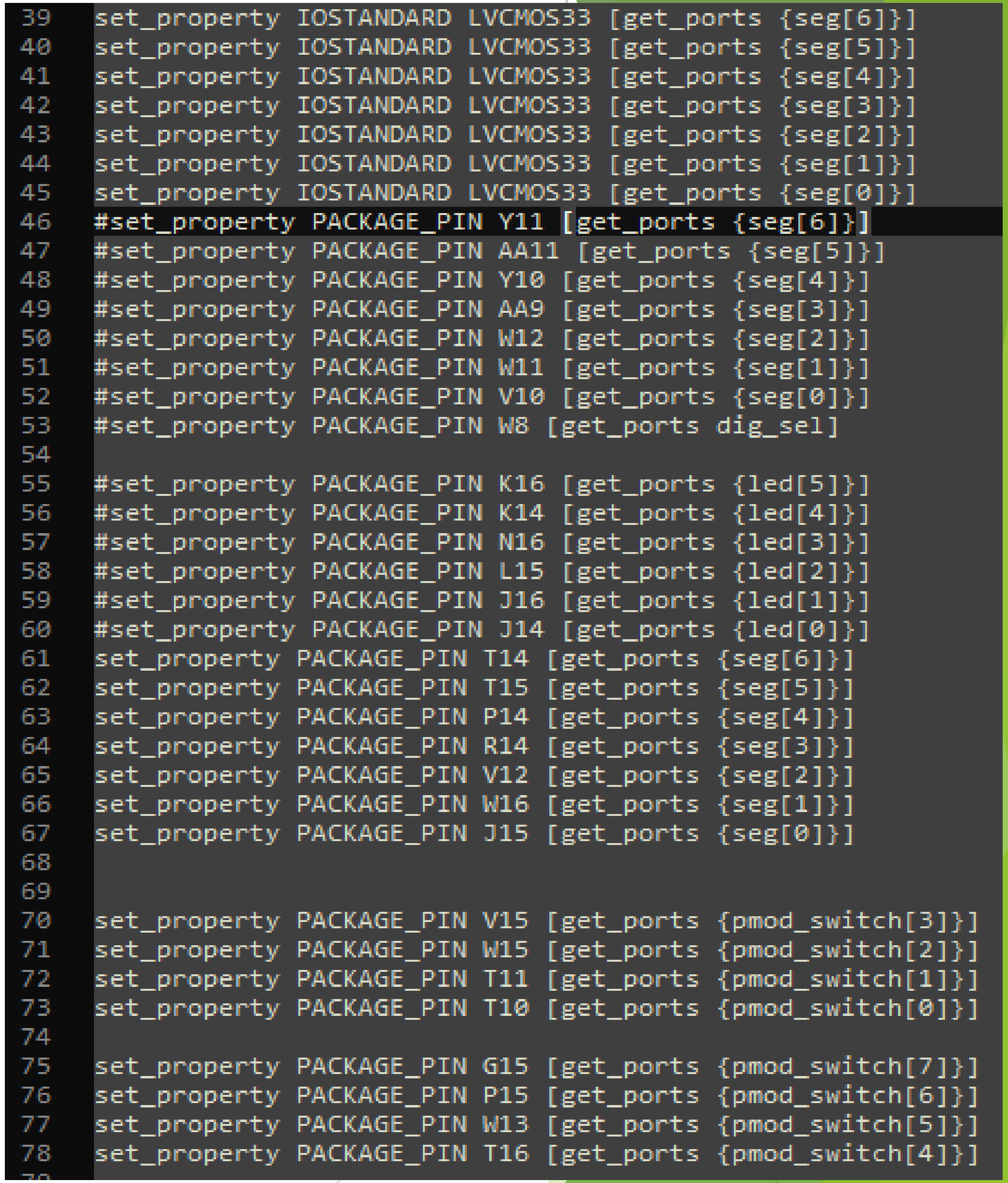


```
##Clock signal
set_property -dict {PACKAGE_PIN K17 IOSTANDARD LVCMOS33} [get_ports clk]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 4.000} -add [get_ports clk]

set_property PACKAGE_PIN H15 [get_ports dig_sel]
set_property IOSTANDARD LVCMOS33 [get_ports dig_sel]

set_property IOSTANDARD LVCMOS33 [get_ports {led[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[0]}]
set_property PACKAGE_PIN T22 [get_ports {led[0]}]
set_property PACKAGE_PIN T21 [get_ports {led[1]}]
set_property PACKAGE_PIN U22 [get_ports {led[2]}]
set_property PACKAGE_PIN U21 [get_ports {led[3]}]
set_property PACKAGE_PIN V22 [get_ports {led[4]}]
set_property PACKAGE_PIN W22 [get_ports {led[5]}]
set_property PACKAGE_PIN L14 [get_ports {led[6]}]
set_property PACKAGE_PIN N15 [get_ports {led[7]}]

set_property IOSTANDARD LVCMOS33 [get_ports {pmod_switch[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {pmod_switch[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {pmod_switch[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {pmod_switch[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {pmod_switch[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {pmod_switch[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {pmod_switch[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {pmod_switch[0]}]
#set_property PACKAGE_PIN F22 [get_ports {pmod_switch[0]}]
#set_property PACKAGE_PIN G22 [get_ports {pmod_switch[1]}]
#set_property PACKAGE_PIN H22 [get_ports {pmod_switch[2]}]
#set_property PACKAGE_PIN F21 [get_ports {pmod_switch[3]}]
#set_property PACKAGE_PIN H19 [get_ports {pmod_switch[4]}]
```

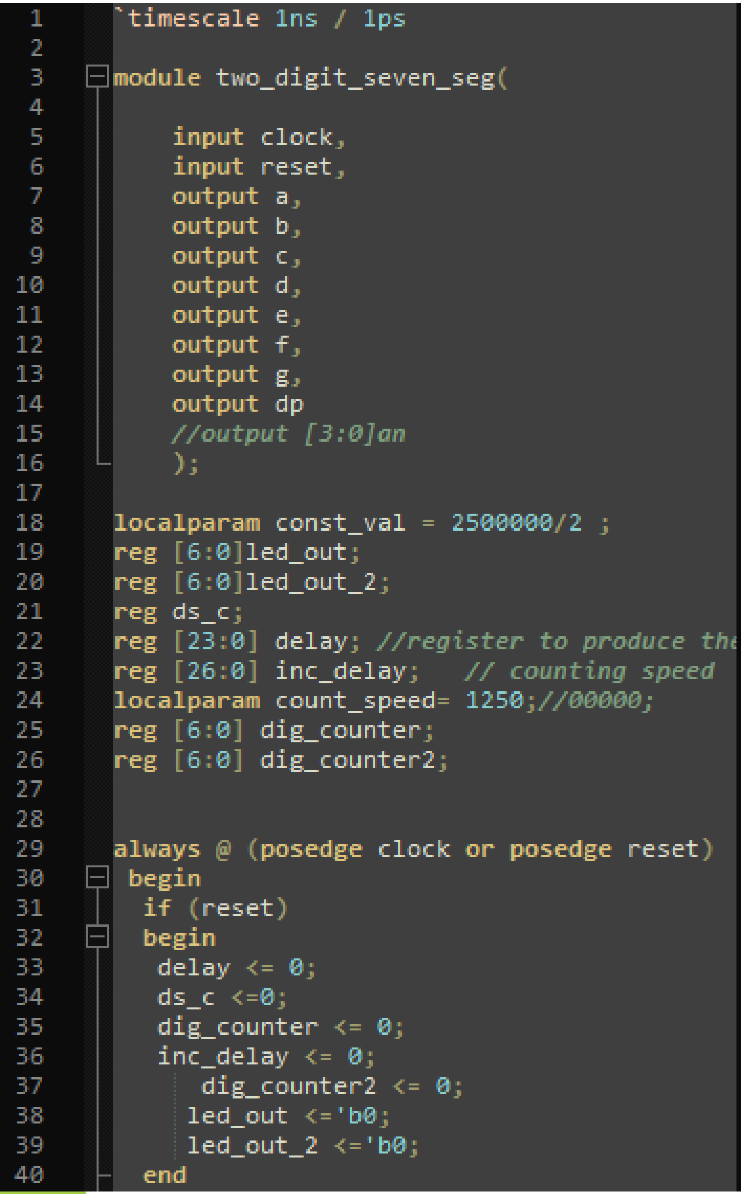


```
set_property IOSTANDARD LVCMOS33 [get_ports {seg[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}]
#set_property PACKAGE_PIN Y11 [get_ports {seg[6]}]
#set_property PACKAGE_PIN AA11 [get_ports {seg[5]}]
#set_property PACKAGE_PIN Y10 [get_ports {seg[4]}]
#set_property PACKAGE_PIN AA9 [get_ports {seg[3]}]
#set_property PACKAGE_PIN W12 [get_ports {seg[2]}]
#set_property PACKAGE_PIN W11 [get_ports {seg[1]}]
#set_property PACKAGE_PIN V10 [get_ports {seg[0]}]
#set_property PACKAGE_PIN W8 [get_ports dig_sel]

#set_property PACKAGE_PIN K16 [get_ports {led[5]}]
#set_property PACKAGE_PIN K14 [get_ports {led[4]}]
#set_property PACKAGE_PIN N16 [get_ports {led[3]}]
#set_property PACKAGE_PIN L15 [get_ports {led[2]}]
#set_property PACKAGE_PIN J16 [get_ports {led[1]}]
#set_property PACKAGE_PIN J14 [get_ports {led[0]}]
set_property PACKAGE_PIN T14 [get_ports {seg[6]}]
set_property PACKAGE_PIN T15 [get_ports {seg[5]}]
set_property PACKAGE_PIN P14 [get_ports {seg[4]}]
set_property PACKAGE_PIN R14 [get_ports {seg[3]}]
set_property PACKAGE_PIN V12 [get_ports {seg[2]}]
set_property PACKAGE_PIN W16 [get_ports {seg[1]}]
set_property PACKAGE_PIN J15 [get_ports {seg[0]}]


set_property PACKAGE_PIN V15 [get_ports {pmod_switch[3]}]
set_property PACKAGE_PIN W15 [get_ports {pmod_switch[2]}]
set_property PACKAGE_PIN T11 [get_ports {pmod_switch[1]}]
set_property PACKAGE_PIN T10 [get_ports {pmod_switch[0]}]

set_property PACKAGE_PIN G15 [get_ports {pmod_switch[7]}]
set_property PACKAGE_PIN P15 [get_ports {pmod_switch[6]}]
set_property PACKAGE_PIN W13 [get_ports {pmod_switch[5]}]
set_property PACKAGE_PIN T16 [get_ports {pmod_switch[4]}]
```

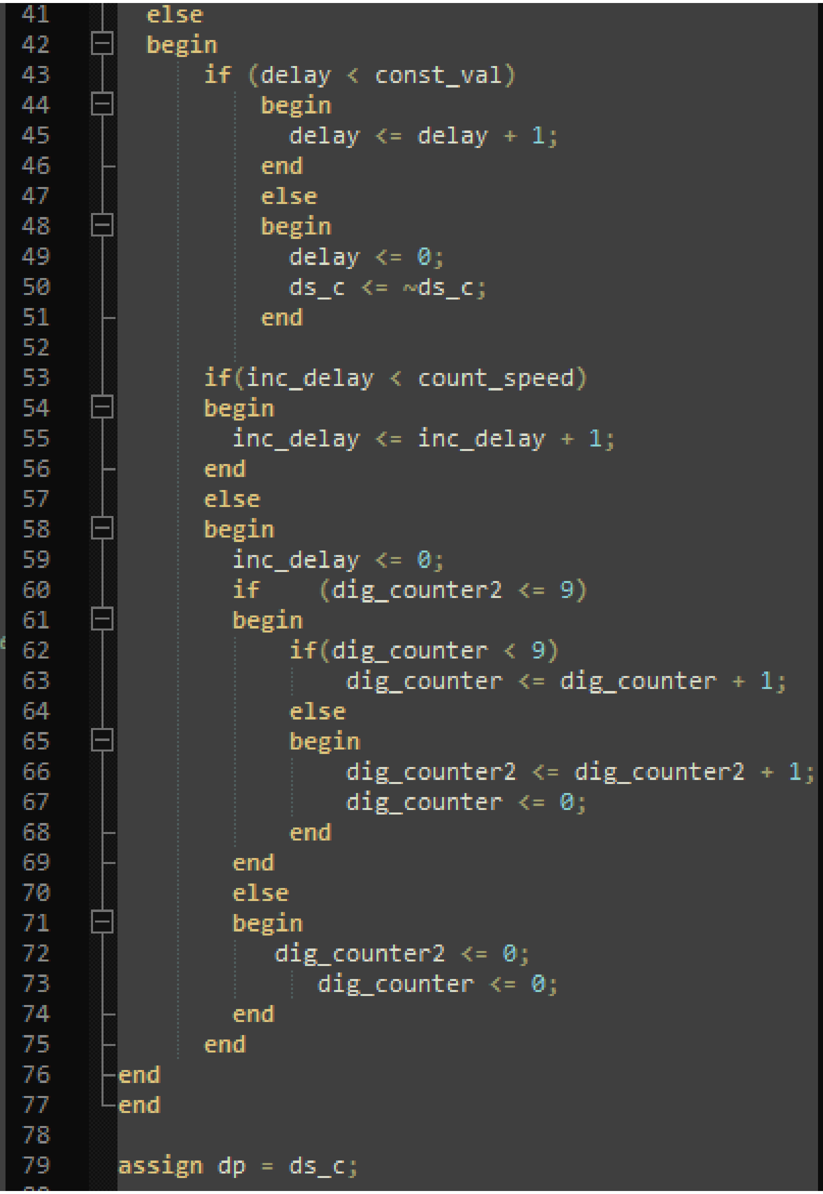
DEMO

Extra Slides

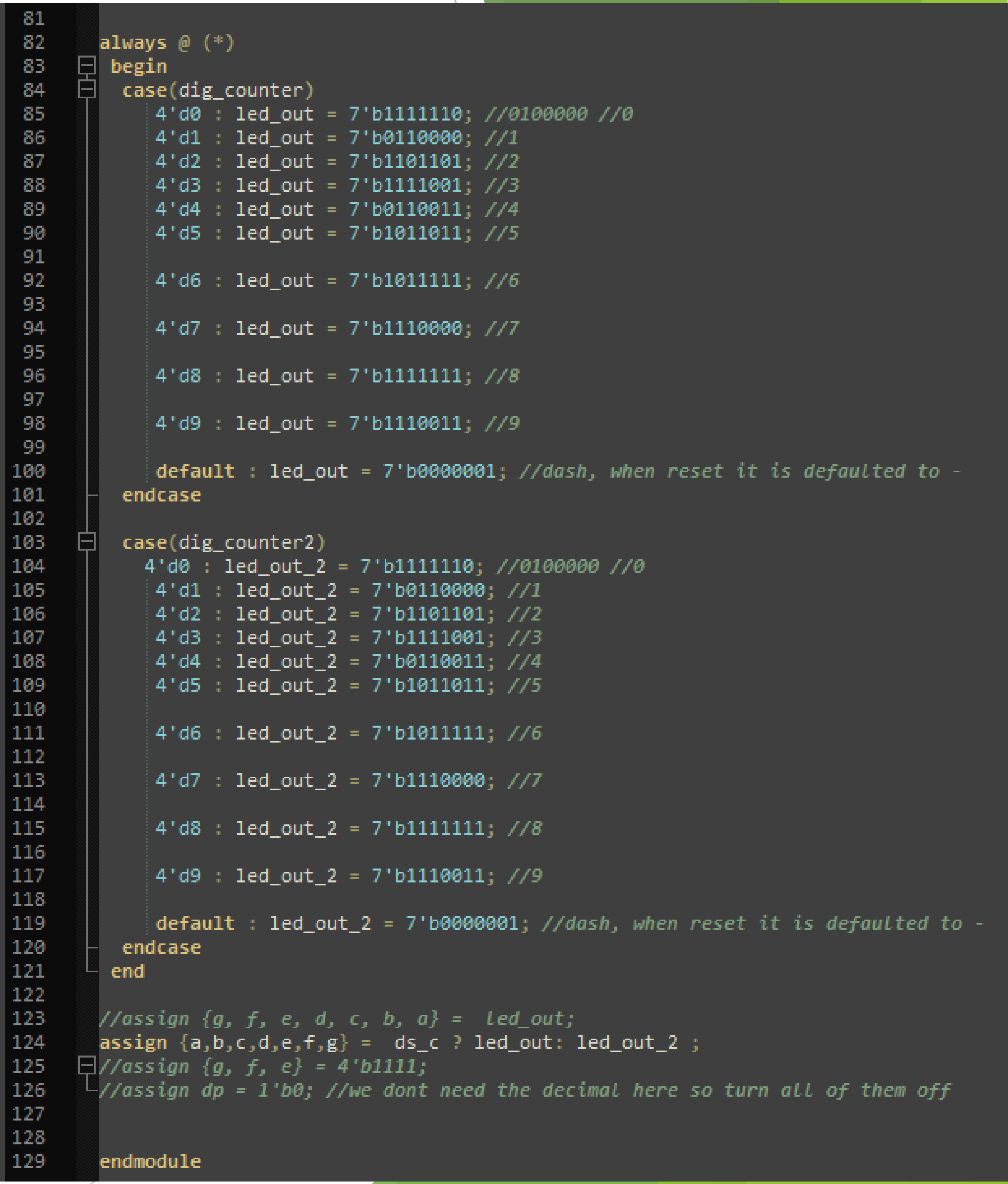
Counter 0 to 99 code



```verilog
`timescale 1ns / 1ps

module two_digit_seven_seg(

  input clock,
  input reset,
  output a,
  output b,
  output c,
  output d,
  output e,
  output f,
  output g,
  output dp
  //output [3:0]an
  );

localparam const_val = 2500000/2 ;
reg [6:0]led_out;
reg [6:0]led_out_2;
reg ds_c;
reg [23:0] delay; //register to produce the
reg [26:0] inc_delay;   // counting speed
localparam count_speed= 1250;//00000;
reg [6:0] dig_counter;
reg [6:0] dig_counter2;


always @ (posedge clock or posedge reset)
 begin
  if (reset)
  begin
   delay <= 0;
   ds_c <=0;
   dig_counter <= 0;
   inc_delay <= 0;
      dig_counter2 <= 0;
     led_out <='b0;
     led_out_2 <='b0;
  end
```

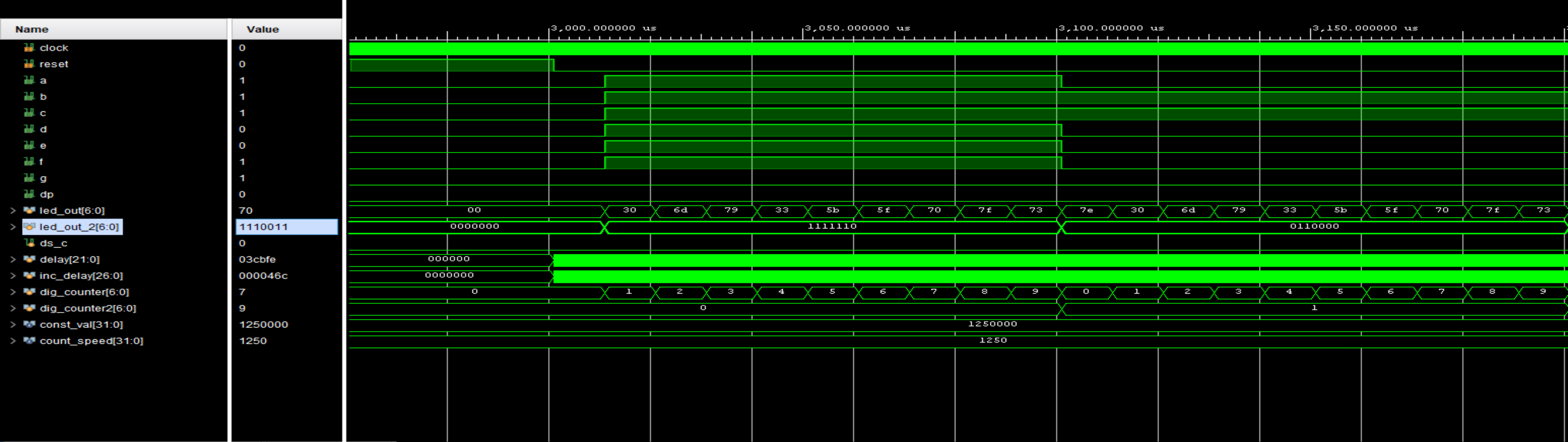


```verilog
 else
 begin
   if (delay < const_val)
     begin
      delay <= delay + 1;
     end
     else
     begin
      delay <= 0;
      ds_c <= ~ds_c;
     end

   if(inc_delay < count_speed)
   begin
    inc_delay <= inc_delay + 1;
   end
   else
   begin
    inc_delay <= 0;
    if    (dig_counter2 <= 9)
    begin
      if(dig_counter < 9)
        dig_counter <= dig_counter + 1;
      else
      begin
        dig_counter2 <= dig_counter2 + 1;
        dig_counter <= 0;
      end
    end
    else
    begin
     dig_counter2 <= 0;
       dig_counter <= 0;
    end
   end
end
end

assign dp = ds_c;
```

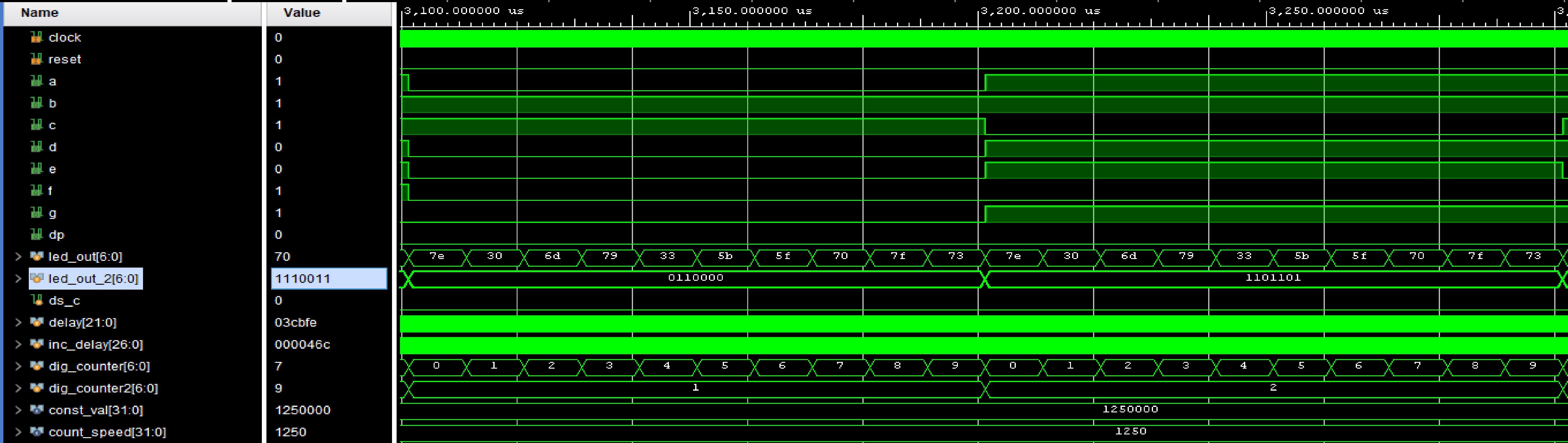


```verilog

always @ (*)
 begin
  case(dig_counter)
    4'd0 : led_out = 7'b1111110; //0100000 //0
    4'd1 : led_out = 7'b0110000; //1
    4'd2 : led_out = 7'b1101101; //2
    4'd3 : led_out = 7'b1111001; //3
    4'd4 : led_out = 7'b0110011; //4
    4'd5 : led_out = 7'b1011011; //5

    4'd6 : led_out = 7'b1011111; //6

    4'd7 : led_out = 7'b1110000; //7

    4'd8 : led_out = 7'b1111111; //8

    4'd9 : led_out = 7'b1110011; //9

    default : led_out = 7'b0000001; //dash, when reset it is defaulted to -
  endcase

  case(dig_counter2)
   4'd0 : led_out_2 = 7'b1111110; //0100000 //0
    4'd1 : led_out_2 = 7'b0110000; //1
    4'd2 : led_out_2 = 7'b1101101; //2
    4'd3 : led_out_2 = 7'b1111001; //3
    4'd4 : led_out_2 = 7'b0110011; //4
    4'd5 : led_out_2 = 7'b1011011; //5

    4'd6 : led_out_2 = 7'b1011111; //6

    4'd7 : led_out_2 = 7'b1110000; //7

    4'd8 : led_out_2 = 7'b1111111; //8

    4'd9 : led_out_2 = 7'b1110011; //9

    default : led_out_2 = 7'b0000001; //dash, when reset it is defaulted to -
  endcase
 end

//assign {g, f, e, d, c, b, a} =  led_out;
assign {a,b,c,d,e,f,g} =  ds_c ? led_out: led_out_2 ;
//assign {g, f, e} = 4'b1111;
//assign dp = 1'b0; //we dont need the decimal here so turn all of them off


endmodule
```

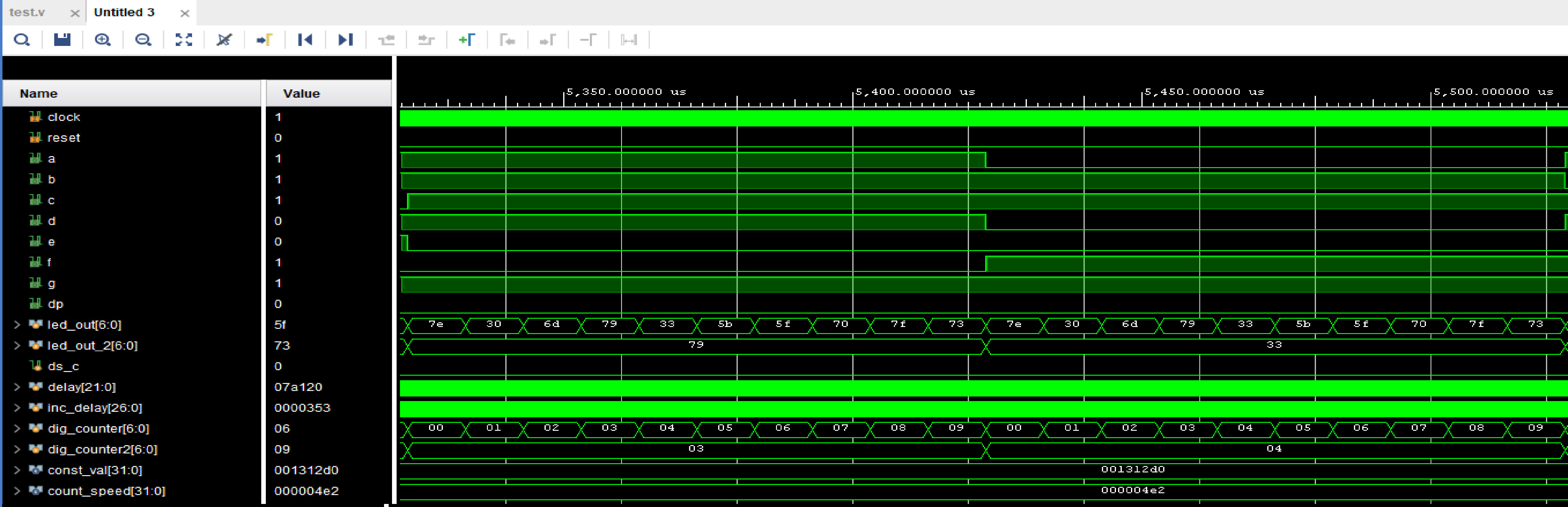
Simulations



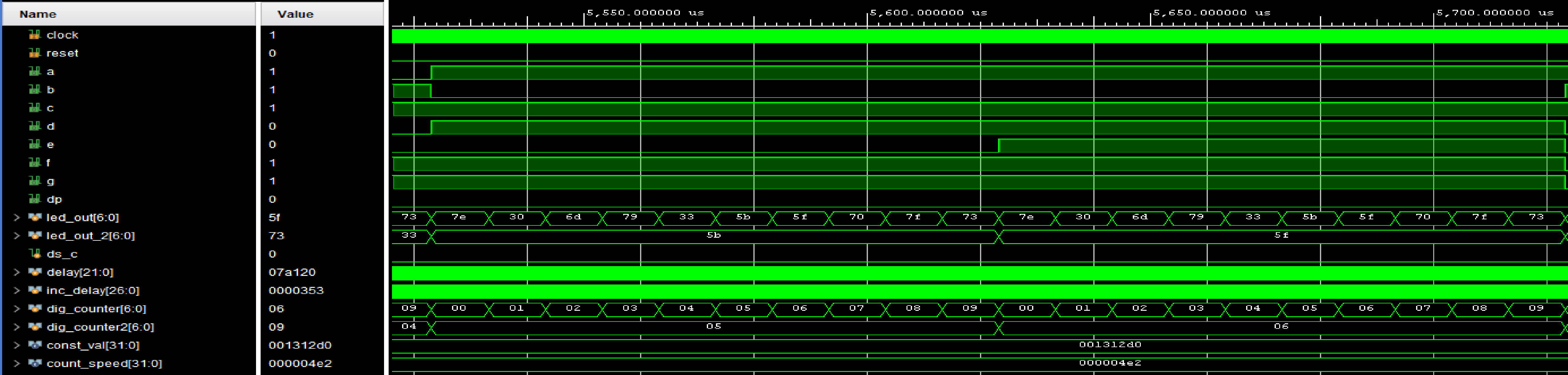
Name	Value
clock	0
reset	0
a	1
b	1
c	1
d	0
e	0
f	1
g	1
dp	0
led_out[6:0]	70
led_out_2[6:0]	1110011
ds_c	0
delay[21:0]	03cbfe
inc_delay[26:0]	000046c
dig_counter[6:0]	7
dig_counter2[6:0]	9
const_val[31:0]	1250000
count_speed[31:0]	1250



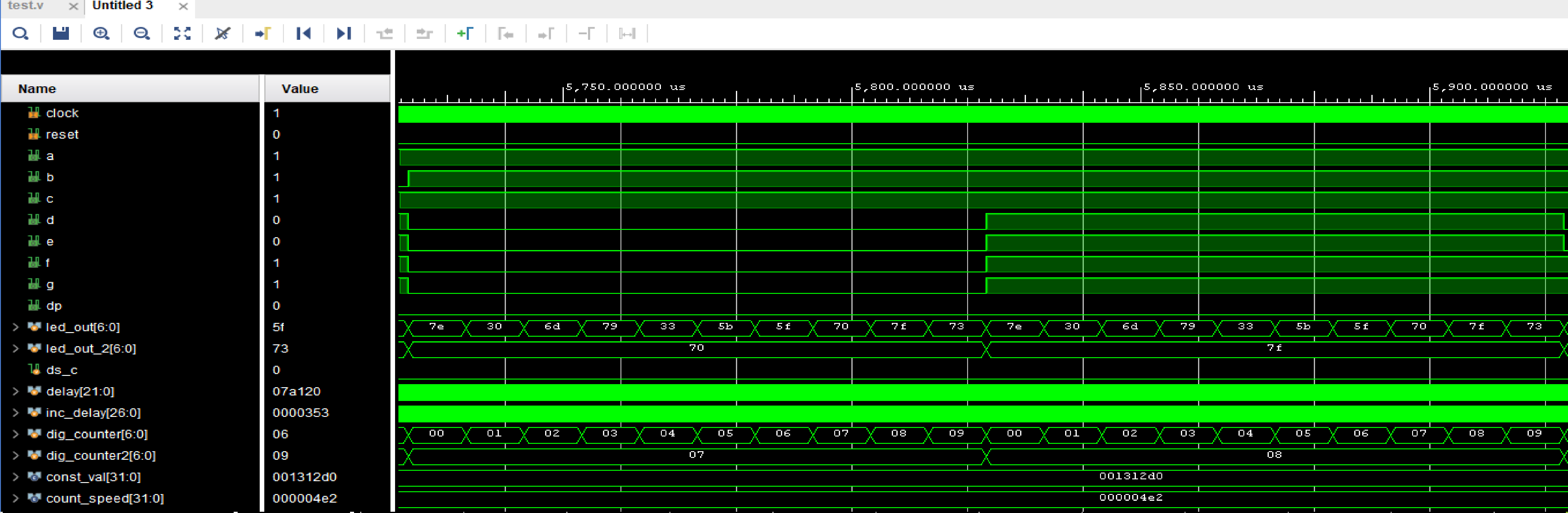
Name	Value
clock	0
reset	0
a	1
b	1
c	1
d	0
e	0
f	1
g	1
dp	0
led_out[6:0]	70
led_out_2[6:0]	1110011
ds_c	0
delay[21:0]	03cbfe
inc_delay[26:0]	000046c
dig_counter[6:0]	7
dig_counter2[6:0]	9
const_val[31:0]	1250000
count_speed[31:0]	1250



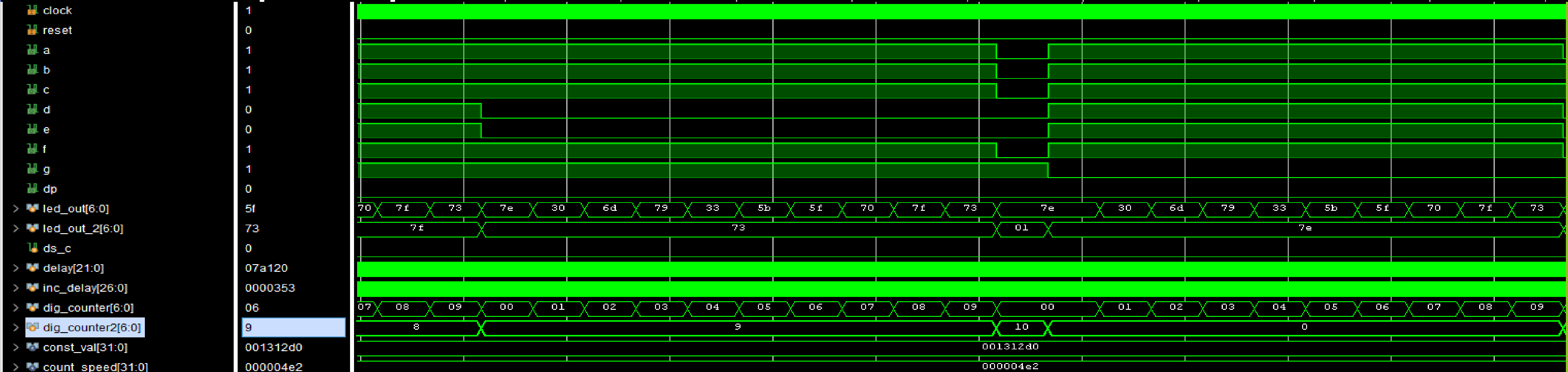
Name	Value
clock	1
reset	0
a	1
b	1
c	1
d	0
e	0
f	1
g	1
dp	0
led_out[6:0]	5f
led_out_2[6:0]	73
ds_c	0
delay[21:0]	07a120
inc_delay[26:0]	0000353
dig_counter[6:0]	06
dig_counter2[6:0]	09
const_val[31:0]	001312d0
count_speed[31:0]	000004e2



Name	Value
clock	1
reset	0
a	1
b	1
c	1
d	0
e	0
f	1
g	1
dp	0
led_out[6:0]	5f
led_out_2[6:0]	73
ds_c	0
delay[21:0]	07a120
inc_delay[26:0]	0000353
dig_counter[6:0]	06
dig_counter2[6:0]	09
const_val[31:0]	001312d0
count_speed[31:0]	000004e2

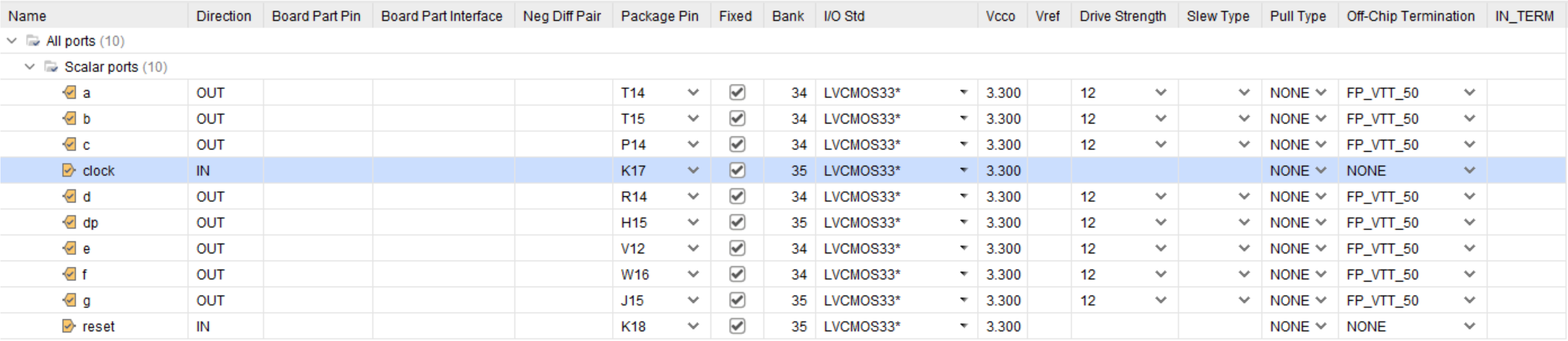


Name	Value
clock	1
reset	0
a	1
b	1
c	1
d	0
e	0
f	1
g	1
dp	0
led_out[6:0]	5f
led_out_2[6:0]	73
ds_c	0
delay[21:0]	07a120
inc_delay[26:0]	0000353
dig_counter[6:0]	06
dig_counter2[6:0]	09
const_val[31:0]	001312d0
count_speed[31:0]	000004e2

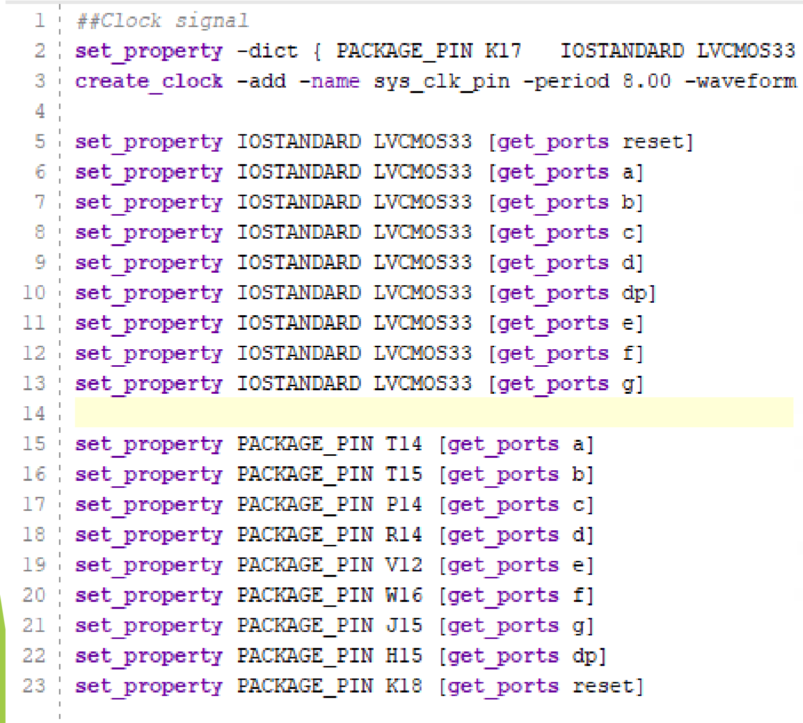


Name	Value
clock	1
reset	0
a	1
b	1
c	1
d	0
e	0
f	1
g	1
dp	0
led_out[6:0]	5f
led_out_2[6:0]	73
ds_c	0
delay[21:0]	07a120
inc_delay[26:0]	0000353
dig_counter[6:0]	06
dig_counter2[6:0]	9
const_val[31:0]	001312d0
count_speed[31:0]	000004e2

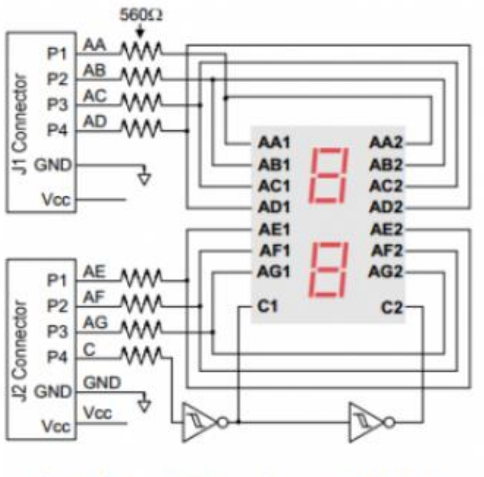
Constraints/XDC file



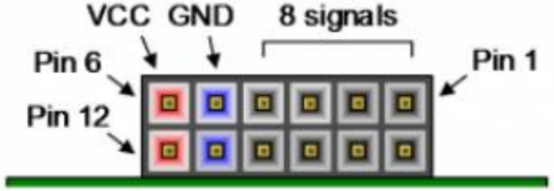
Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
All ports (10)															
Scalar ports (10)															
a	OUT				T14	☑	34	LVCMOS33*	3.300		12		NONE	FP_VTT_50	
b	OUT				T15	☑	34	LVCMOS33*	3.300		12		NONE	FP_VTT_50	
c	OUT				P14	☑	34	LVCMOS33*	3.300		12		NONE	FP_VTT_50	
clock	IN				K17	☑	35	LVCMOS33*	3.300				NONE	NONE	
d	OUT				R14	☑	34	LVCMOS33*	3.300		12		NONE	FP_VTT_50	
dp	OUT				H15	☑	35	LVCMOS33*	3.300		12		NONE	FP_VTT_50	
e	OUT				V12	☑	34	LVCMOS33*	3.300		12		NONE	FP_VTT_50	
f	OUT				W16	☑	34	LVCMOS33*	3.300		12		NONE	FP_VTT_50	
g	OUT				J15	☑	35	LVCMOS33*	3.300		12		NONE	FP_VTT_50	
reset	IN				K18	☑	35	LVCMOS33*	3.300				NONE	NONE	



```
##Clock signal
set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports {clock}]; #IO_L12P_T1_MRCC_35 Sch=sysclk
create_clock -add -name sys_clk_pin -period 8.00 -waveform {0 4} [get_ports { clock }];

set_property IOSTANDARD LVCMOS33 [get_ports reset]
set_property IOSTANDARD LVCMOS33 [get_ports a]
set_property IOSTANDARD LVCMOS33 [get_ports b]
set_property IOSTANDARD LVCMOS33 [get_ports c]
set_property IOSTANDARD LVCMOS33 [get_ports d]
set_property IOSTANDARD LVCMOS33 [get_ports dp]
set_property IOSTANDARD LVCMOS33 [get_ports e]
set_property IOSTANDARD LVCMOS33 [get_ports f]
set_property IOSTANDARD LVCMOS33 [get_ports g]

set_property PACKAGE_PIN T14 [get_ports a]
set_property PACKAGE_PIN T15 [get_ports b]
set_property PACKAGE_PIN P14 [get_ports c]
set_property PACKAGE_PIN R14 [get_ports d]
set_property PACKAGE_PIN V12 [get_ports e]
set_property PACKAGE_PIN W16 [get_ports f]
set_property PACKAGE_PIN J15 [get_ports g]
set_property PACKAGE_PIN H15 [get_ports dp]
set_property PACKAGE_PIN K18 [get_ports reset]
```

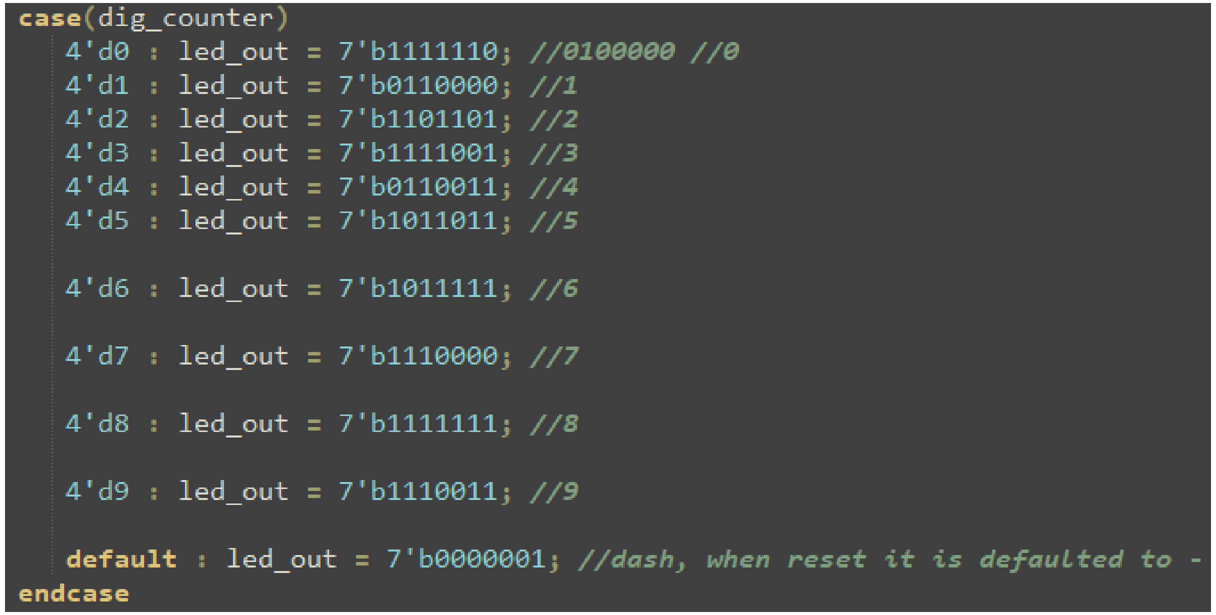


Seven-Segment Display Connection Diagram

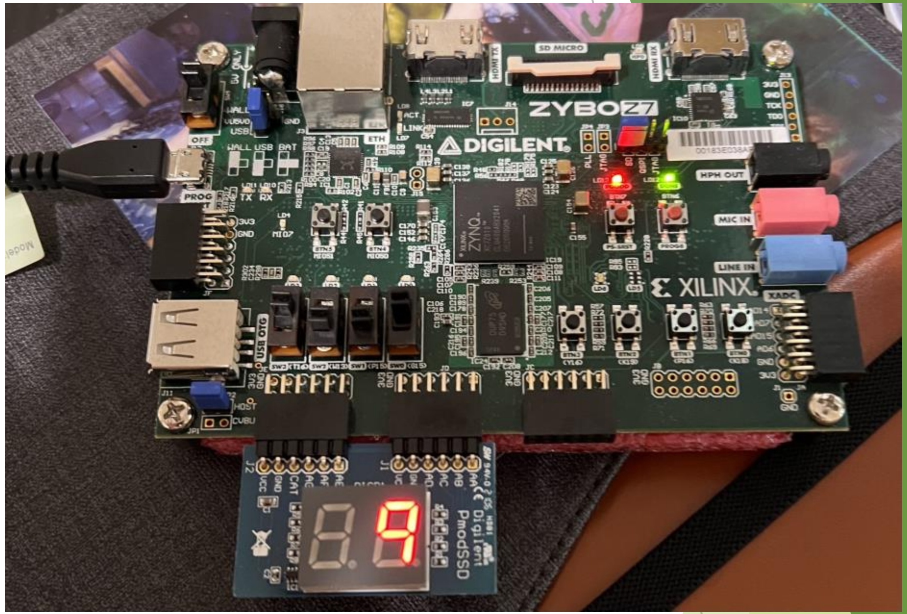


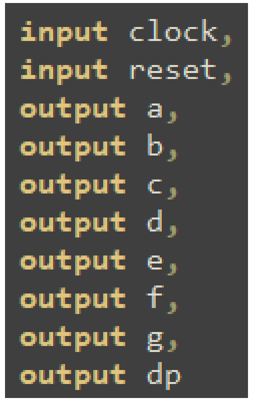
Zybo Pinouts for Pmods: JA -> JF

Results / Troubleshooting

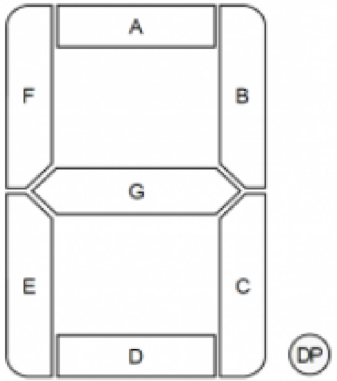


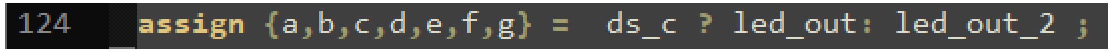
```
case(dig_counter)
    4'd0 : led_out = 7'b1111110; //0100000 //0
    4'd1 : led_out = 7'b0110000; //1
    4'd2 : led_out = 7'b1101101; //2
    4'd3 : led_out = 7'b1111001; //3
    4'd4 : led_out = 7'b0110011; //4
    4'd5 : led_out = 7'b1011011; //5

    4'd6 : led_out = 7'b1011111; //6

    4'd7 : led_out = 7'b1110000; //7

    4'd8 : led_out = 7'b1111111; //8

    4'd9 : led_out = 7'b1110011; //9

    default : led_out = 7'b0000001; //dash, when reset it is defaulted to -
endcase
```





```
input clock,
input reset,
output a,
output b,
output c,
output d,
output e,
output f,
output g,
output dp
```





```
assign {a,b,c,d,e,f,g} =  ds_c ? led_out: led_out_2 ;
```

Thank you

Questions?