Lab 5 report

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calculate the memory stall cycles:

Simulated program execution cycles 為利用 Lab 所提供的 assembly code，根據 loop 的執行方式，計算各個指令執行的次數，得出公式

Fig(a):

hit time cycle : send the address+access single cache content+send a word of data
=1+2+1=4

cache miss penalty : send the address+8*(send the address+access memory content+send a word of data+access single cache content)+access single cache content+send a word of data
=1 + 8*(1+100+1+2) + 2 + 1 = 836

total memory stall cycles : (hit time cycle*cache hit number)+(cache miss penalty*cache miss number)

Fig(b):

hit time cycle : send the address+access single cache content+send a word of data
=1+2+1=4

cache miss penalty : send the address+(send the address+access memory content+send a word of data+access single cache content)+access single cache content+send a word of data
=1 + (1+100+1+2) + 1= 108

total memory stall cycles : (hit time cycle*cache hit number)+(cache miss penalty*cache miss number)

Fig(c):

L1 hit time cycle : send the address+access L1 cache content+send a word of data
=1+1+1=3

L1 miss L2 hit time cycle : send the address+4*(send the address+access L2 cache content+send a word of data+access L1 cache content)+access L1 cache content+ send a word of data
=1 + 4*(1+10+1+1) + 1 + 1= 55

L2 cache miss penalty : send the address + 32*(send the address+access memory content+send a word of data+access L2 cache content) + 4*(send the address+ access L2 cache content+send a word of data+access L1 cache content) +access L1 cache content+send a word of data

=1 + 32*(1+100+1+10)+ 4 * (1+10+1+1)+ 1 + 1 = 3639

total memory stall cycles : (L1 hit time cycle * L1 hit number)+(L1 miss L2 hit penalty * L1 miss L2 hit number)+(L2 cache miss penalty * L2 miss number)

Compare and discuss the difference among the three memory organization

Memory Stall Result : Fig(b)<Fig(a)<Fig(c) :

Fig(a) :

相較於 Fig(b)，雖然 cache sizec 和 block size 相同，miss rate 也相同，但是其 word wide 只有 1，對於 8-word block 要八次 memory access 和八次的 data transfer，因此其效率也較差

Fig(b)擁有最少 memory stall 原因 :

Fig(b)的 cache word wide 為 8，相較於(a)，memory 一次可以讀取 8 word，對於 8-word block 只要一次 memory access 和一次的 data transfer，因此 stall cycle 也較少

Fig(c)擁有最多 memory stall 原因 :

Fig(c)的 two level memory organization 可以看出，L1 的 hit time 確實有減少，L2 的 miss rate 確實有減少，但是由於 L2 的 miss penalty 過高，導致一旦 L2 cache 為 miss，就會產生大量的 memory stall，最終導致效率最差。