

Simulated timing : 4

Area : 105639.386528

Cost : 422557.546112

ScreenShot :

The image displays two screenshots of a Verilog simulation window, likely from a software like ModelSim or similar. The window is titled '140.112.20.72' and shows a project tree on the left and a command window on the right.

Top Screenshot:

- Warnings: /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v:138: signed to unsigned assignment occurs. (VER-318)
- Warning: /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v:72: Net mem_wdata_D connected to instance rf is declared as reg data type but is not driven by a n always block. (VER-1004)
- Warning: /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v:73: Net mem_wen_D connected to instance ctrl is declared as reg data type but is not driven by a n always block. (VER-1004)
- Warning: /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v:75: Net mem_addr_D connected to instance alu is declared as reg data type but is not driven by a n always block. (VER-1004)
- Inferred memory devices in process in routine CHIP line 155 in file /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v'.

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
PC_reg	Flip-flop	32	Y	N	N	N	N	N	N
- Warning: /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v:185: unsigned to signed assignment occurs. (VER-318)
- Warning: /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v:186: unsigned to signed assignment occurs. (VER-318)
- Warning: /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v:205: signed to unsigned conversion occurs. (VER-318)
- Statistics for case statements in always block at line 183 in file /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v'

Line	full/parallel
189	auto/auto
- Statistics for case statements in always block at line 254 in file /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v'

Line	full/parallel
294	auto/auto
369	auto/auto
495	auto/auto
- Inferred memory devices in process in routine register file line 445 in file /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v'.

Bottom Screenshot:

- Inferred memory devices in process in routine register file line 445 in file /home/raid7_2/userb09/b09057/DSO_HM2/verilog/CHIP.v'.

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
r30_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r31_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r1_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r2_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r3_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r4_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r5_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r6_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r7_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r8_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r9_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r10_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r11_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r12_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r13_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r14_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r15_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r16_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r17_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r18_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r19_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r20_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r21_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r22_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r23_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r24_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r25_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r26_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r27_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r28_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
r29_r_reg	Flip-flop	32	Y	N	N	N	N	N	N
- Statistics for case statements in always block at line 565 in file