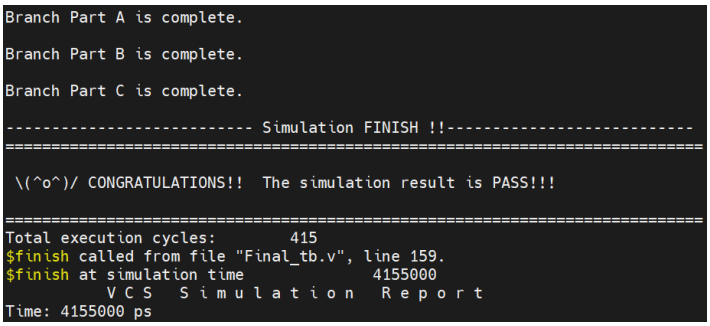
DSD Final Project Scores

1. BrPred

(1) Total execution cycles of given I_mem_BrPred:

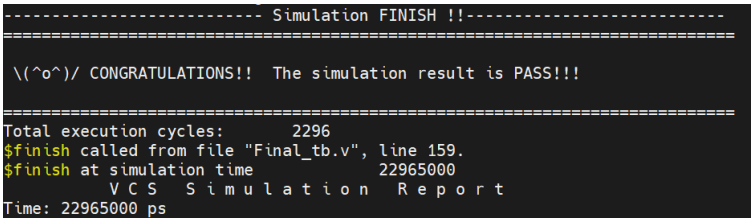
截圖:



Total execution cycles = 415

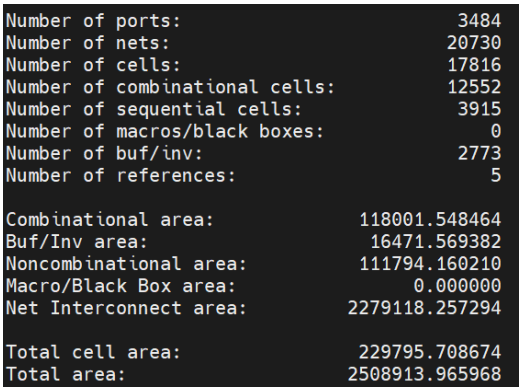
(2) Total execution cycles of given I_mem_hasHazard:

截圖:



Total execution cycles = 2296

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um^2)



Synthesis area of BPU = 229796 – 226678= 3118 um^2

2. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um^2)

截圖:

```
Number of ports:                         2926
Number of nets:                         20016
Number of cells:                        17087
Number of combinational cells:          12734
Number of sequential cells:              4059
Number of macros/black boxes:               0
Number of buf/inv:                       2388
Number of references:                      61

Combinational area:             124015.437415
Buf/Inv area:                    18415.092663
Noncombinational area:          104717.699512
Macro/Black Box area:                0.000000
Net Interconnect area:         2330405.253448

Total cell area:                228733.136928
Total area:                    2559138.390376
```

Total area = 228733 – 221961 = 6772 um^2

(2) Total Simulation Time of given I_mem_compression: (ns)

截圖:

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
$finish called from file "Final_tb_ex.v", line 159.
$finish at simulation time              4585000
          V C S   S i m u l a t i o n   R e p o r t
Time: 4585000 ps
```

(3) Area*Total Simulation Time: (um^2 * ns)

1.05E+9

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

10ns

3. Q_sort

(1) Area: (um^2)

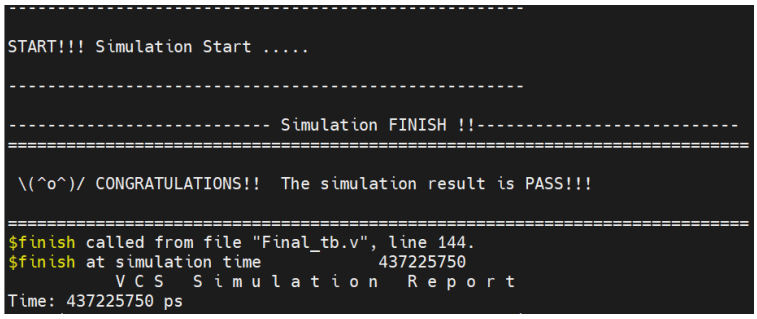
截圖:

```
Number of ports:                         2926
Number of nets:                         22169
Number of cells:                        19484
Number of combinational cells:          15141
Number of sequential cells:              4059
Number of macros/black boxes:               0
Number of buf/inv:                       3597
Number of references:                     105

Combinational area:             177252.690509
Buf/Inv area:                    34056.633681
Noncombinational area:          107088.967476
Macro/Black Box area:                0.000000
Net Interconnect area:         2408385.645477

Total cell area:                284341.657984
Total area:                    2692727.303462
```

(2) Best Total Simulation Time : (ns)

(either using compressed or uncompressed instructions)

截圖:



Compressed instructions

(3) Area*Total Simulation Time: (um^2 * ns)

1.24E+11

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

2.9ns