

DSD Final Project Scores

1. BrPred

(1) Total execution cycles of given I_mem_BrPred:

```
Branch Part A is complete.
Branch Part B is complete.
Branch Part C is complete.

----- Simulation FINISH !!-----
=====

\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
Total execution cycles:      415
$finish called from file "Final_tb.v", line 159.
$finish at simulation time    4155000
V C S   S i m u l a t i o n   R e p o r t
Time: 4155000 ps
```

截圖：

Total execution cycles = 415

(2) Total execution cycles of given I_mem_hasHazard:

```
----- Simulation FINISH !!-----
=====

\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
Total execution cycles:      2296
$finish called from file "Final_tb.v", line 159.
$finish at simulation time    22965000
V C S   S i m u l a t i o n   R e p o r t
Time: 22965000 ps
```

截圖：

Total execution cycles = 2296

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um²)

```
Number of ports:      3484
Number of nets:       20730
Number of cells:      17816
Number of combinational cells: 12552
Number of sequential cells: 3915
Number of macros/black boxes: 0
Number of buf/inv:    2773
Number of references: 5

Combinational area:    118001.548464
Buf/Inv area:          16471.569382
Noncombinational area: 111794.160210
Macro/Black Box area:  0.000000
Net Interconnect area: 2279118.257294

Total cell area:       229795.708674
Total area:            2508913.965968
```

Synthesis area of BPU = 229796 – 226678 = 3118 um²

2. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (μm^2)

```
Number of ports:          2926
Number of nets:           20016
Number of cells:          17087
Number of combinational cells: 12734
Number of sequential cells:  4059
Number of macros/black boxes: 0
Number of buf/inv:        2388
Number of references:      61

Combinational area:       124015.437415
Buf/Inv area:             18415.092663
Noncombinational area:    104717.699512
Macro/Black Box area:     0.000000
Net Interconnect area:    2330405.253448

Total cell area:          228733.136928
Total area:               2559138.390376
```

截圖:

$$\text{Total area} = 228733 - 221961 = 6772 \mu\text{m}^2$$

(2) Total Simulation Time of given I_mem_compression: (ns)

```
----- Simulation FINISH !!-----
=====
\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!
=====
$finish called from file "Final_tb_ex.v", line 159.
$finish at simulation time 4585000
VCS Simulation Report
Time: 4585000 ps
```

截圖:

(3) Area*Total Simulation Time: ($\mu\text{m}^2 * \text{ns}$)

$$1.05\text{E}+9$$

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

$$10\text{ns}$$

3. Q_sort

(1) Area: (μm^2)

```
Number of ports:          2926
Number of nets:           22169
Number of cells:          19484
Number of combinational cells: 15141
Number of sequential cells:  4059
Number of macros/black boxes: 0
Number of buf/inv:        3597
Number of references:      105

Combinational area:       177252.690509
Buf/Inv area:             34056.633681
Noncombinational area:    107088.967476
Macro/Black Box area:     0.000000
Net Interconnect area:    2408385.645477

Total cell area:          284341.657984
Total area:               2692727.303462
```

截圖:

(2) Best Total Simulation Time : (ns)

(either using compressed or uncompressed instructions)

```

-----
START!!! Simulation Start .....
-----
----- Simulation FINISH !!-----
=====
\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!
=====
$finish called from file "Final_tb.v", line 144.
$finish at simulation time 437225750
V C S S i m u l a t i o n R e p o r t
Time: 437225750 ps

```

截圖：

Compressed instructions

(3) Area*Total Simulation Time: ($\mu\text{m}^2 * \text{ns}$)

1.24E+11

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

2.9ns