(a) The cycle time you used in cache_syn.sdc and in tb_cache.v to pass the post-synthesis simulation respectively

DM：
cache_syn.sdc：10
tb_cache.v：15

(b) General specification of the cache unit.
(such as numbers of words, placement policy, and so on)

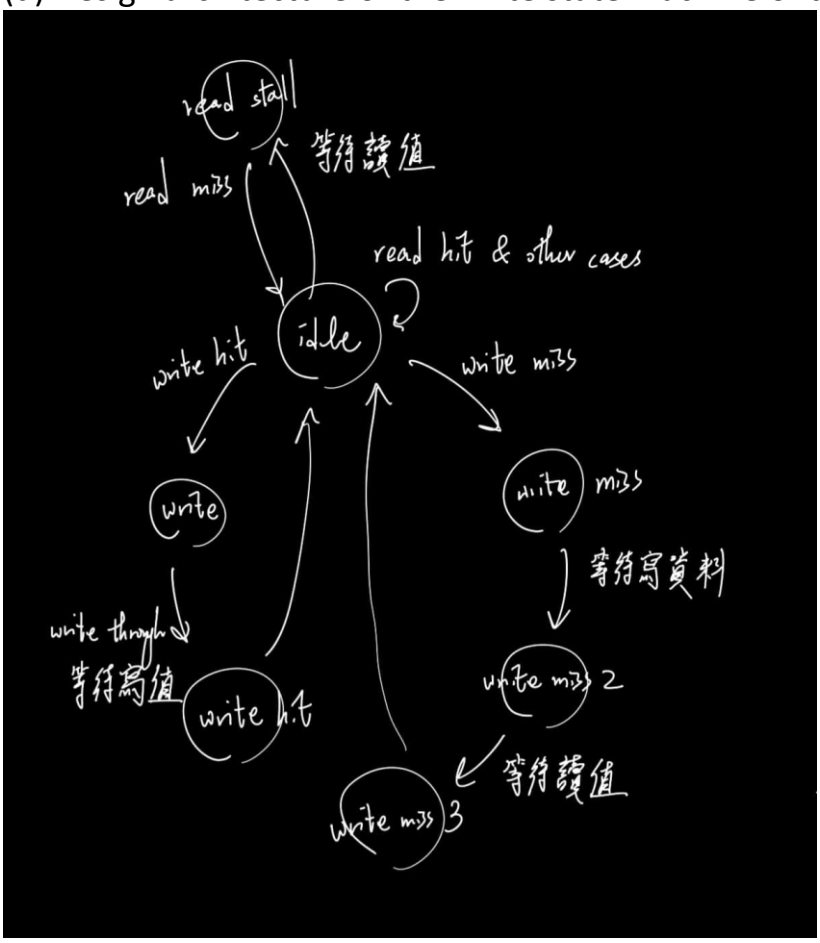
Dm：reg [153:0] cache [7:0]
2way：reg [309:0] cache [3:0]

Read hit：直接把結果用 proc_rdata 拿出來
Read miss：stall 變成 1，跟 memory 要資料，拿完資料寫進 cache 之後用 proc_rdata 拿出來
Write hit：直接把資料寫上去，之後再把資料傳給 memory
Write miss：先把 cache 資料 write 進 memory，再把資料從 memory read 出來，再把他寫掉，再回傳給 memory

(c) Read/write policy (write-through or write-back)

Write through

(d) Design architecture or the finite state machine of the cache unit




(e) Performance evaluation of your cache design, including the miss rates of read/write operations, the execution cycles, the stalled cycles

Dm：
Execution：17928
Miss rate：0.48

(f) Compare the performance of the two architectures, and discuss the reasons for such results

可以預期 2way 應該要比還來的好，因為他同一個 set 可以有兩個 tag，因此 miss rate 大概要是 dm 的二分之一，大約是 0.25，雖然我沒有做出來，但我還是有詢問其他同學，與這個數字接近