嵌入式微處理機系統

02_ An Overview of ARM Processor

國立台灣科技大學電機系
王乃堅老師
Feb. 2024

ARM Processor Family

Processor Family	# of pipeline stages	Memory organization	Clock Rate	MIPS/Mhz
ARM6	3	Unified	25 MHz	-
ARM7	3	Unified	66 MHz	0.9
ARM8	5	Unified	72 MHz	1.2
ARM9	5	Harvard	200 MHz	1.1
StrongARM	5	Harvard	233 MHz	1.15
ARM10	6	Harvard	400 MHz	1.25
ARM11	8/9	Harvard	533 MHz	2.1
Cortex-A8	13(dual issue)	Harvard	1 GHz	2.0
Cortex-M3	3	Harvard	100 MHz	-

ARM 和 8051 的比較

	ARM	8051
運算速率	70-700MIPS	10MIPS
記憶體定址	2GB	64KB
可使用週邊	多樣，特別是 Ethernet、LCD、USB 等	I^2C、UART、GPIO
軟體寫作	支援廣泛 可模組化	操作靈活
成本	中等或高	低

硬體平台比較

設備名稱	嵌入式系統	PC
CPU	嵌入式處理器(ARM，MIPS)	CPU(INTEL、AMD)
記憶體	SDRAM	SDRAM或DDR
儲存設備	FLASH	硬碟
輸入設備	按鍵、觸控螢幕	滑鼠、鍵盤
輸出設備	LCD	顯示器
聲音設備	音效晶片	音效卡
串列介面	MAX232	主機板提供
其他設備	USB	主機板提供或外接卡

軟體平台比較

	嵌入式系統	PC
開機程式	Bootloader引導，對不同電路進行移植	主機板BIOS引導，無須更改
作業系統	WinCE、VxWork、Linux…，需移植	Windows、Linux等，不需要移植
驅動程式	每個設備驅動都必須針對電路板進行重新開發或移植，一般不能直接下載使用	作業系統含有大多數驅動程式，或從網路上下載直接使用
開發環境	借助伺服器進行交叉編譯	在本機就可以開發調試
模擬器	需要	不需要

Embedded Processors

- ARM處理器
  - ARM公司(Advanced RISC Machines Limited，簡稱為ARM Limited)成立於1990年。1985年4月26日，第一個ARM原形在英國劍橋的Acorn計算機有限公司誕生(在美國LVSI公司製造)。目前ARM架構處理器已在高性能、低功耗、低成本的嵌入式應用領域佔據領先地位。
  - ARM處理器技術廣泛用於攜帶式通信產品、掌上型裝置、多媒體和嵌入式解決方案，已成為RISC標準。

Introduction

- 目前基於ARM核心的處理器有以下：
  - ARM7家族
  - ARM9家族
  - ARM9E家族
  - ARM10E家族
  - ARM11家族
  - SecureCore家族
  - OptimoDE資料核心
  - MPCore多處理器家族
  - Intel公司的StrongARM/XScale

Data Sizes and Instruction Set

- The ARM is a 32-bits architecture
- When used in relation to the ARM
  - Byte means 8 bits
  - Halfword means 16 bits (two bytes)
    - Must be aligned to two-byte boundaries
  - Word means 32 bits (four bytes)
    - Must be aligned to four-byte boundaries
- Most ARM's implement two instruction sets
  - 32-bits ARM Instruction Set
  - 16-bits Thumb Instruction Set

Processor Modes (1/2)

- The ARM has seven operating modes
  - User : the unprivileged mode under which most tasks run
  - FIQ : entered when a high priority (fast) interrupt is raised
  - IRQ : entered when a low priority (normal) interrupt is raised
  - Supervisor : entered on reset and when a software interrupt instruction (SWI) is executed
  - Abort : used to handle memory access violations
  - Undefined : used to handle undefined instructions
  - System : a privileged mode for operating system tasks; using the same registers as the User mode

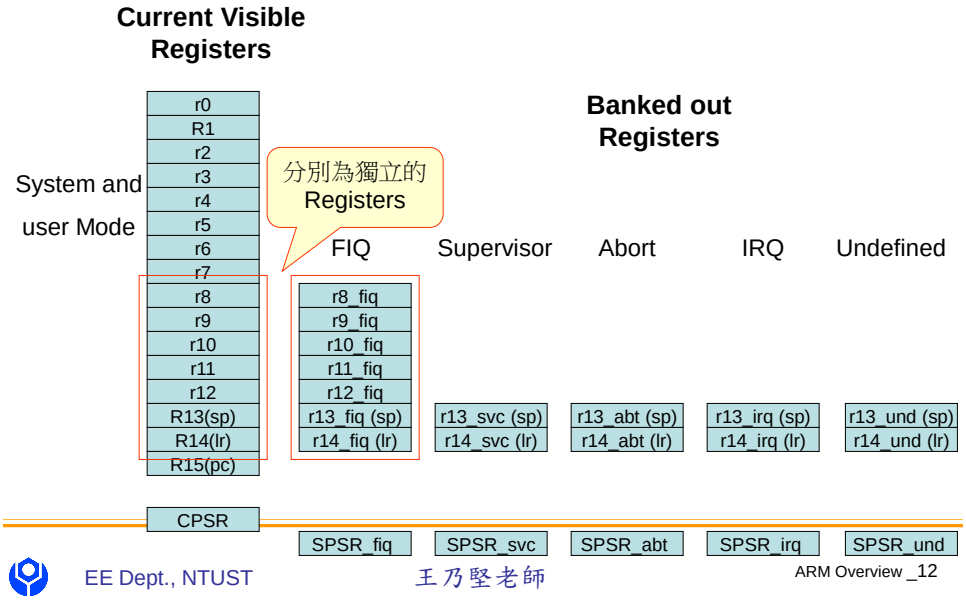
Processor Modes (2/2)

- Exception modes include
  - FIQ, IRQ, Supervisor, Abort, and Undefined
- Privileged modes include
  - FIQ, IRQ, Supervisor, Abort, Undefined, and System
- Processor states vs. processor modes
  - There are two processor states
    - ARM state: processors execute the ARM instruction set
    - Thumb state: processors execute the Thumb instruction set

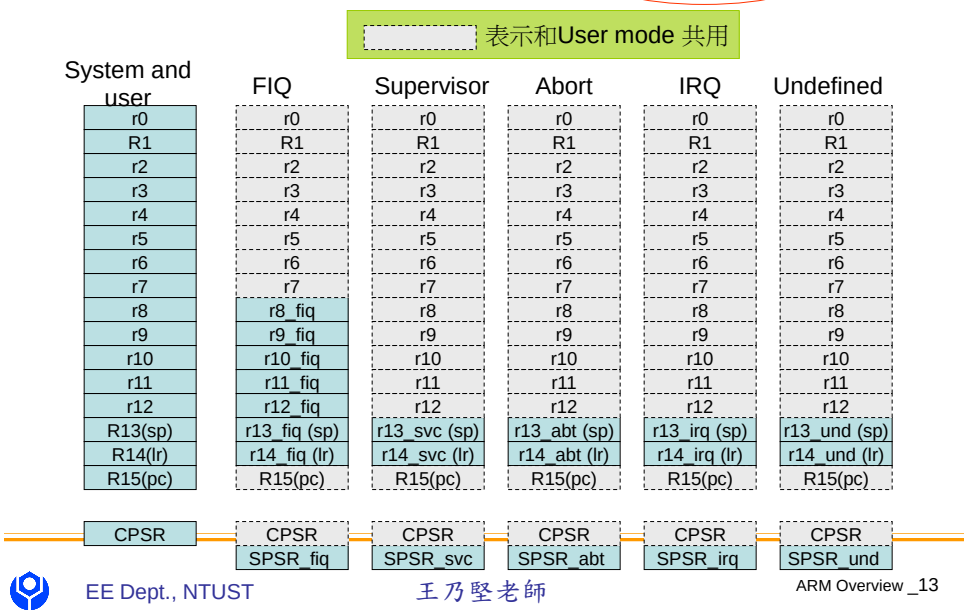
The Registers

- ARM has 37 registers, all of which are 32-bits
  - 31 general purpose registers
    - R0~R15
  - 6 program status registers
    - 1 dedicated current program status register (CPSR)
    - 5 dedicated saved program status register (SPSR)
  - The 37 registers are divided into 6 banks.
  - The current processor mode governs which of the 6 banks is accessible.

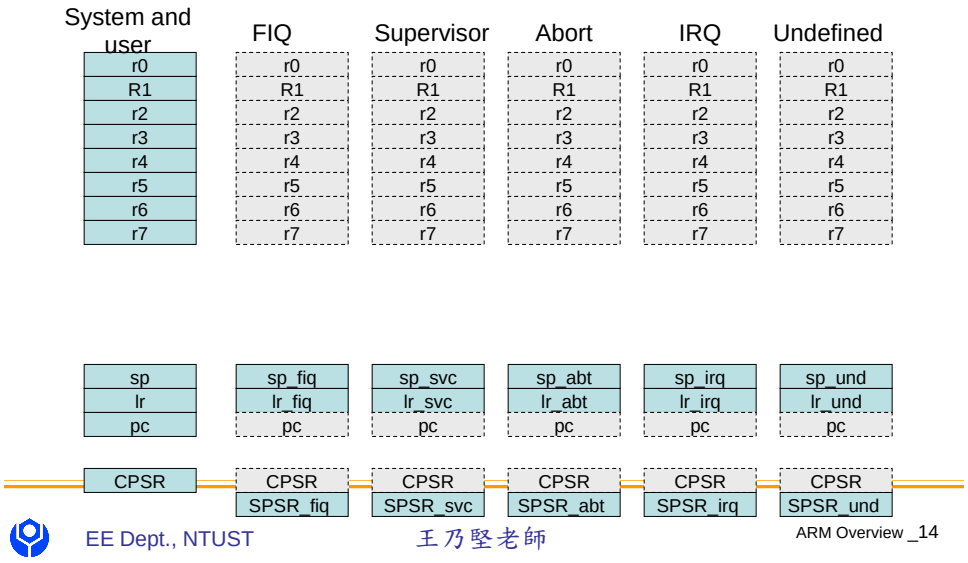
Register Banking



Register Organization in ARM State



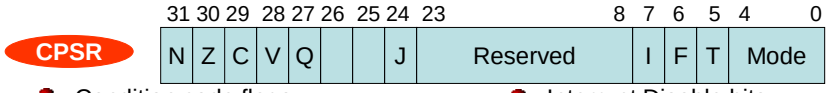
Register Organization in Thumb State



Register Access

- Each processor mode can access
  - a particular set of r0-r12 registers
  - A particular r13 (stack pointer, **SP**) and r14 (link register, **LR**)
  - The program counter, r15 (**PC**)
  - The current program status register (**CPSR**)
- Privileged modes (except System) can also access
  - A particular saved program status register (**SPSR**)

Program Status Register



- Condition code flags
  - **N** = Negative result form ALU
  - **Z** = Zero result form ALU
  - **C** = ALU operation Carried out
  - **V** = ALU operation overflow
- Sticky Overflow flag – Q flag
  - Architecture 5TE only
  - Indicates if saturation has occurred during certain operations
- J Bit
  - Architecture 5TEJ only
  - J = 0, Processor in ARM state or Thumb state, depending on the T bit
  - J = 1, Processor Jazelle state
  - BXJ
- Interrupt Disable bits
  - I = 1, disable the IRQ
  - F = 1,disables the FIQ
- T Bit
  - Architecture xT only
  - T = 0, Processor in ARM state
  - T = 1, Processor in Thumb state
  - BX, BLX
- Mode bits
  - Specify the processor mode

M[4:0]	Mode
10000	User
10001	FIQ
10010	IRQ
10011	Supervisor
10111	Abort
11011	Undefined
11111	System

Processor Nomenclature

- ARM{x}{y}{z}{T}{D}{M}{I}{E}{J}{F}{-S}
  - x-family
  - y-memory management/protection unit
  - z-cache
  - T-Thumb
  - D-JTAG debug
  - M-fast multiplier
  - I-Embedded ICE macrocell
  - E-enhanced instructions
  - J-Jazelle
  - F-vector floating-point unit
  - S-synthesizable

ARM9TDMI

- Architecture v4T
- 5 stage pipeline
  - Improves CPI to ~ 1.5
  - Improved maximum clock freq.
- Havard architecture
  - Increases available memory bandwidth
    - Instruction memory interface
    - Data memory interface
  - Simultaneous access to instruction and data memory can be achieved
- Normally supplied with caches attached
- ARM920T
  - 2 x 16K caches
  - Memory Management Unit (MMU)
  - Write Buffer
- ARM922T
  - As ARM920T but with 2 x 8K caches
- ARM940T
  - 2 x 4K caches
  - Has a Memory Protection Unit (MPU)

ARM920T functional block diagram

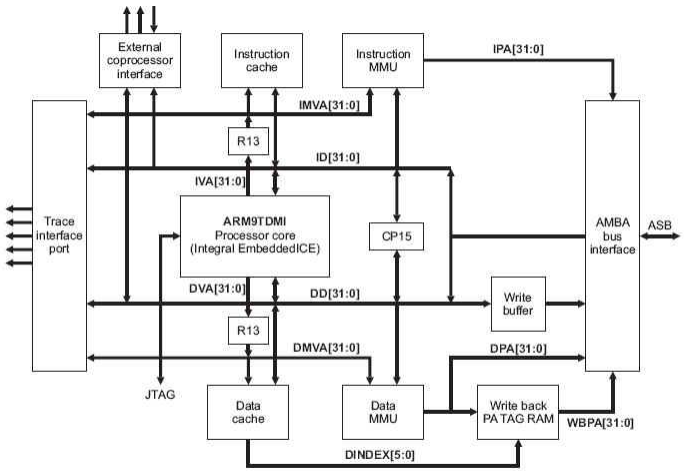


Figure 1-1 ARM920T functional block diagram

The ARM7TDMI Processor Core

- Architecture v4T
- Most popular low and ARM core
- 3 stage pipeline
- Von Neumann architecture
- CPI ~1.9
  - T Thumb instruction set support
    - 32-bits ARM instruction
    - 16-bits Thumb instruction
  - DI”Embedded ICE Logic”debug over JTAG support
  - M Enhanced multiplier (32x8) with instructions for 64-bits results
- ARRM720T is an ARM7TDMI with cache, MMU and write buffer

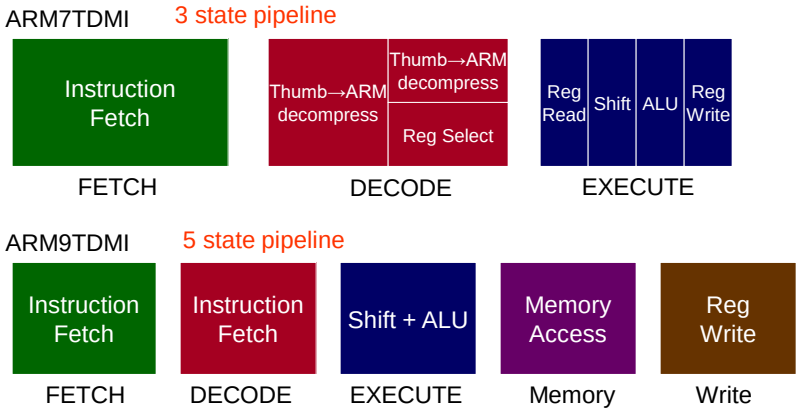
The Instruction Pipeline

- The ARM7TDMI uses a 3 stage pipeline in order to increase the speed of the flow instruction to the processor
- Allows several operations to be performed simultaneously, rather than serially

ARM	Thumb		
PC	PC	**Fetch**	Instruction fetched from memory
		⇩	
PC-4	PC-2	**Decode**	Decoding of registers used in instruction
		⇩	
PC-8	PC-4	**Execute**	Registers read form Register Bank Shift and ALU operation Write registers back to Register Bank

- The PC points to the instruction being fetched, not executed
  - ➢ Debug tools will hide this form you

Pipeline changes for ARM9TDMI



DSP Enhancements

Processor (Architecture)	16 x 16 multiply with 32 bits accumulate (cycles)	32 x 32 multiply with 64 bits accumulate (cycles)
ARM7(ARMv3)	~12	~44
ARM7TDMI(ARMv4)	4	7
ARM9TDMI(ARMv4T)	4	7
StrongARM(ARMv4)	2 or 3	4 or 5
ARM9E(ARMv5TE)	1	3
Xscale(ARMv5TE)	1	2-4
ARM1136(ARMv6)	0.5	2

可以快速的執行 加法 與乘法 的運算

ARM Developer Suite (ADS) Overview

- Main Components
  - ANSI C compilers – armcc and tcc
  - ISO/Embedded C++ compilers – armcpp and tcpp
  - ARM/Thumb assembler – armasm
  - Linker – armlink
  - Window IDE – Codewarrior
  - Debuggers – AXD, ADW, ADU and armsd
  - Format convertor – fromelf
  - Librarian – armar
  - C and C++ libraries
  - Instruction set simulator – ARMulator
  - Also ship with
    - ARM Firmware Suite
    - ARM Application Library