Embedded System HW1 Due: 3/18/2024 9am

- CPU(ARM): ADDR[31:0], DATA[31:0], nWE (Write Enable), nOE(Output Enable), nBE[3:0](Byte Enable), nWBE[3:0] (Write Byte Enable).
- (Note: nWE means #WE ... etc.)
- Memory: (D0- D7), (A0-A28), #OE, #WE, #CS
- Decoder: 3-8 decoder

Questions:

1. What is the max memory space of this system?
2. What is the memory space of each memory chip?
3. Design the whole system which can achieve the all memory space. (Draw the circuit) (Using: 3-8 decoder + basic logic gates is necessary)