

UMW2651 Device Specification

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Revision History

Version	Data	Owner	Note
V0.9	01/26/2018	Yunwei Zhang	First release.
V1.0	6/19/2018	Mina Yan	Correct the device name and 2 pin No
V1.1	9/5/2018	Siqi Wu	Update package information

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1 System Overview

1.1 Overview

UMW2651 is a highly integrated 4-in-1 connectivity single chip which offers the lowest RBOM in the industry for smart phone, tablet and mobile applications.

This chip includes 2.4 GHz and 5 GHz WLAN IEEE 802.11 a/b/g/n/ac 2x2 MU-MIMO 20/40/80 MHz VHT R2 MAC/PHY/Radio, Bluetooth 5 with supporting high power mode, Mesh, Direction Finding and Long Range, multiple mode concurrent reception of GPS/Galileo/Glonass/Beidou(B1C) satellite systems and a FM receiver. Additionally, this radio-on-a-chip integrates power amplifiers, receive low noise amplifiers and RF TR switch.

It supports SDIO 3.0 and PCIe Gen 2 compliant slave interfaces for Wi-Fi, high-speed 4-wire UART for Bluetooth and GNSS, I2C/UART for Android Context Hub.

Advanced Spreadtrum Green Wi-Fi power management features optimize Wi-Fi active and low power states to extend operating lifetime for battery driven devices.

Spreadtrum Chorale provides high performance multiple radio coexistence and antenna sharing technology for Wi-Fi, Bluetooth, GNSS and LTE operating concurrently in compact system design.

1.2 Features

1.2.1 General Features

- Dual ARM Cortex M4 architecture with platform computing offloading and advanced energy efficient management features
- Rich interfaces support variant application development – PCIe Gen 2, SDIO 3.0, 4 x UART, I2S/PCM, I2C, WCI-2, JTAG, GPIOs
- Spreadtrum Memory Bandwidth Management feature enables flexible in-chip memory allocation and extension capability of dynamically swapping applications, data and code between host and SoC memory domains
- Android Context Hub interface supports low power and offloading profiles of context awareness applications
- Supports standard crystal TSX and reference clock output
- Supports external Wi-Fi 5 GHz PA and LNA
- Supports worldwide regulatory
- 204 Ball BGA package (6.9X6.9 mm, 0.4 mm pitch)

1.2.2 Wi-Fi Features

- Dual band 2.4/5 GHz 2x2 20/40/80 MHz IEEE 802.11a/b/g/n/ac
- Complies with Wi-Fi VHT R2, supports MU-MIMO DL and beamformee
- Spreadtrum Extreme provides QAM-256 in 2.4 GHz band to improve 33% PHY data rate
- Spreadtrum Chorale antenna sharing and coexistence solution delivers excellent LTE, Wi-Fi MIMO, Bluetooth 5, GNSS concurrent operation performance in a compact and cost effective system design
- Spreadtrum Green Wi-Fi provides excellent low power consumption features for Wi-Fi normal operation and low power states
- Supports IEEE 802.11 FTM, Wi-Fi Location and timing measurement

- Supports WMM-PS QoS, Wi-Fi Direct, Miracast R2, Passpoint 2.0, Wi-Fi Aware, etc.
- Supports WEP,WPA/WPA2/WPA3-Personal/WPA3-Enhanced Open, WPS 2.0, WAPI, WPI-SMS4, EAP-TLS/EAP-TTLS/EAP-PEAP/EAP-SIM/EAP-AKA/EAP-AKA', IEEE 802.11w Protected Management Frame
- Complies with IEEE 802.11 d/e/h/i/k/r/u/v/z
- Supports both single and multiple channel concurrency
- Supports background scan, ARP, TCP/UDP checksum offload, IPv6 NS/RA offloading
- Supports spur immunity to avoid performance degradation caused by spur generated by PCB

1.2.3 Bluetooth Features

- Bluetooth 5, Bluetooth Smart Ready compliant
- Bluetooth classic and Low Energy dual mode concurrent operation
- Supports LE 2 Mbps, LE Advertise Extension, Long Range, AoD Rx Direction Finding and Mesh
- Integrated 10 dBm high efficiency on-chip PA for low energy application
- Integrated 20 dBm high power on-chip PA for Bluetooth high power mode application
- Integrated wide-band speech processing to improve voice quality
- Supports Low Energy background scan for context awareness applications
- Supports multiple piconets and up to 16 concurrent Bluetooth Low Energy concurrent links

1.2.4 GNSS Features

- Triple mode concurrent reception of GPS/Galileo/GLONASS/Beidou(B1C) to improve location accuracy and positioning performance
- Fully A-GNSS compliant and capabilities, supports SUPL/A-Beidou/A- GLONASS
- Integrated high performance RF path to reduce system design complexity
- Supports Satellite Based Argumentation systems (SBAS)
- Supports high definition location accuracy, less than 1 m
- Excellent tracking and hot start sensitivity
- Supports inertia tracking

1.2.5 FM Features

- Supports frequency range of 65MHz ~ 108MHz
- Supports RDS
- Digital stereo demodulator
- Digital audio interface (I2S)
- Stereo Mono blending and auto selectivity

2 Package Information

Plastic-encapsulated surface mount packages are sensitive to damage induced by absorbed moisture and temperature. All the chips are MSL 3, which had been marked on the label for every package.

Device Name	UWM2651
Body Size	6.9X6.9 mm
Ball count	204
Ball Pitch	0.4mm
Ball Size	0.25mm
Ball Matrix	17X17

2.1 Top Marking Definition

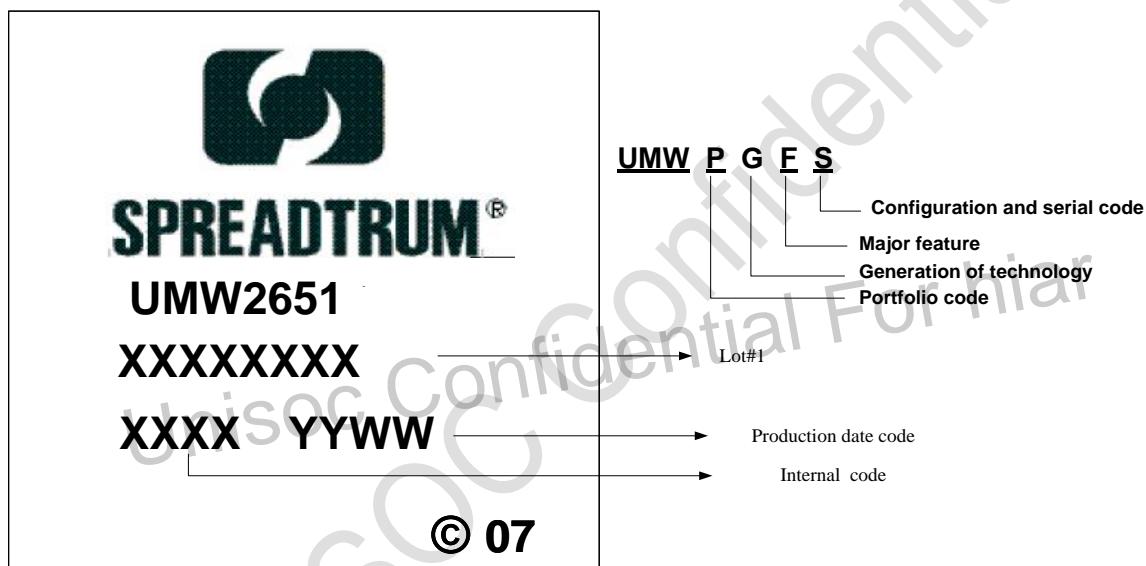


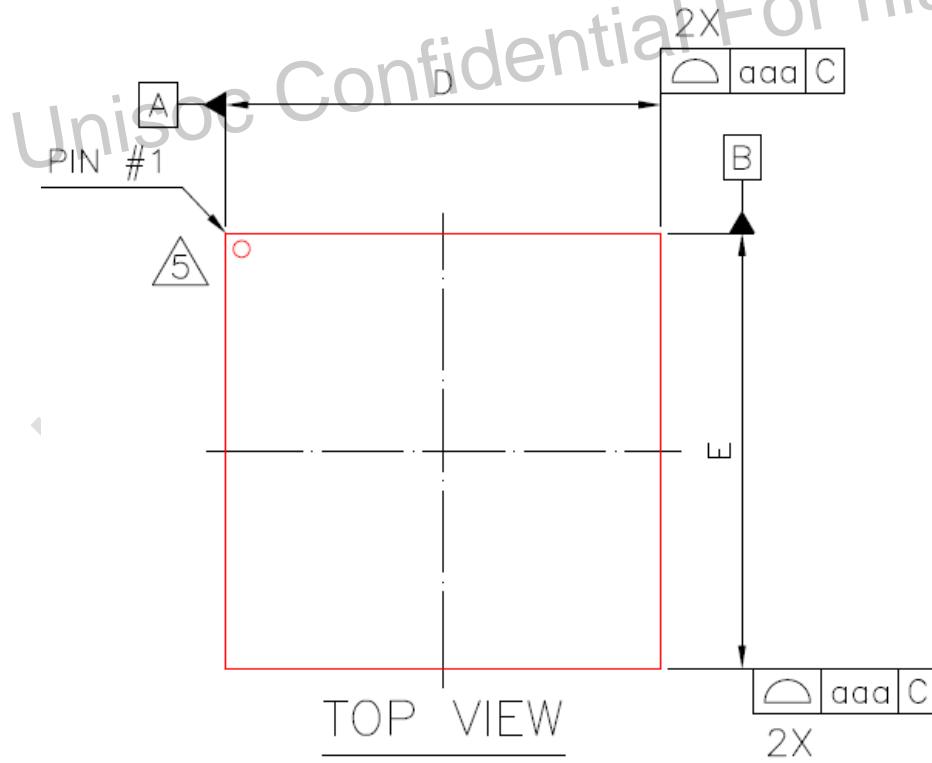
Figure 2-1 Top marking definition

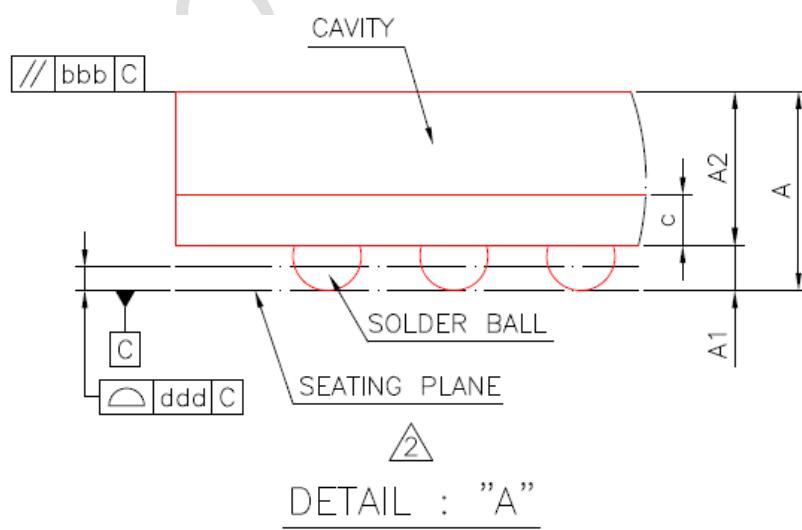
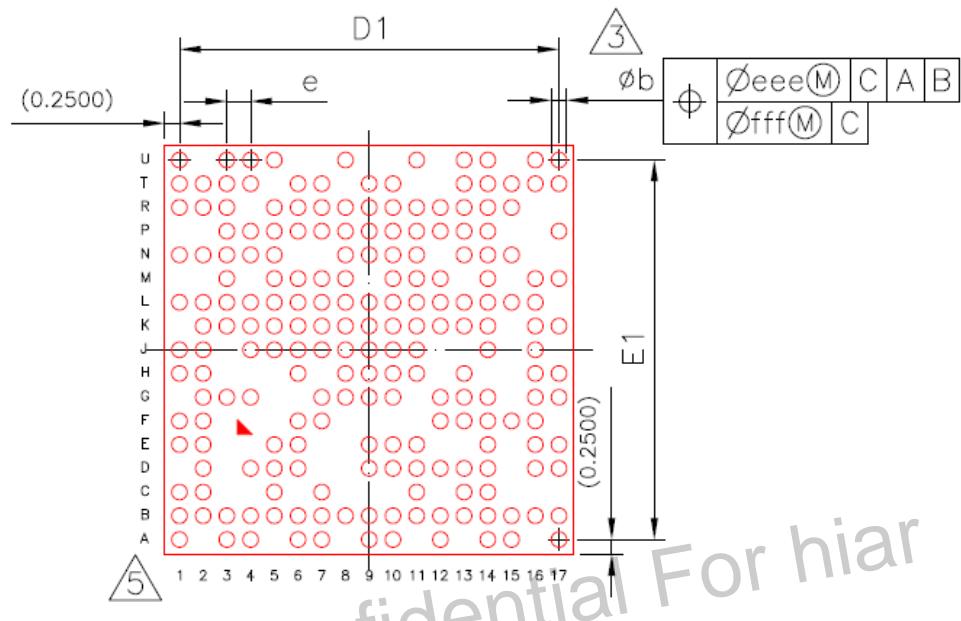
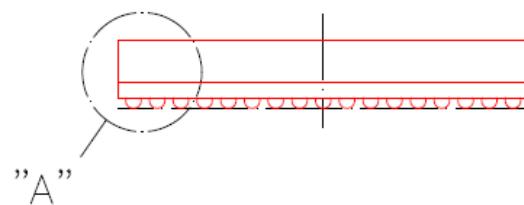
2.2 Ball Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	NC		U3TXD	IISLRCK		DVDD_IN	MTCK		ESMD3	ESMCLK		SD_CLK		PCIE_REFCLKP	PCIE_TXP		NC A	
B	UOCTS	UORTS	USRXD	IISDO	CHIP_EN	DVDD_IN	MTMS	VDDEFU	ESMD2	ESMCSN	SD_D0	PCIE_RST_L	PCIE_WAKE_L	PCIE_REFCLKN	PCIE_TXN	PCIE_RXN	PCIE_RXO B	
C	UOTXD	UORXD			IISDI		DVDD_CORE				SD_D3		PCIE_RESREF	PCIE_VPH			C	
D		U1CTS		VSS	IISCLK	RST_N			ESMD1	ESMDO	SD_D2	SD_CMD	VSS	VSS		PCIE_VPTXN	PCIE_VP D	
E	U1RXD	U1RTS			VSS	VSS			VSS	VSS	SD_D1			DVDD_CORE		WCI_2_TXD	WCI_2_RXD E	
F	U1TXD	DVDD_CORE				VSS	VDIO					PCIE_CLKREQ_L	PTEST	XTEN	VSS	TSEN_VREFN		F
G		RFCTL0	RFCTL1	RFCTL7			VSS	VSS	VSS			GNSS_LNA_EN	INT	DCXO_BONDING_OPT		TSEN_IN	TSEN_VREFP G	
H	GPIO3	GPIO2				RFCTL6		VSS	VSS	VSS	VSS		AVDD_RTC			XTAL_IN	XTAL_OUT H	
J	GPIO0	GPIO1			RFCTL2	RFCTL3	RFCTL4	RFCTL5	VSS	VSS	VSS	VSS		VSS		REF_FREQ_SE L		J
K		AVDD1V2_AF_E1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CLK_32K	DCXO_26MHz_OUT	DCXO_LP_MODE	AVDD1V8_DC_XO		K	
L	AVDD1V2_WP_TRX1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD1V2_AF_E2	AVDD1V2_GNSS		L	
M			VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS		VSS		VSS	GNSS_RF_IN M		
N	EPA_PRI_PKO	VSS	VSS	VSS				VSS	VSS	VSS	VSS		VSS	VSS	VSS		N	
P			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD1V2_WP_TRX2	VSS	VSS		VSS	P	
R	VSS	VSS	AVDD3V3_PRI		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	BT_TRX_P	VSS		R	
T	WF_5G_PRI_T_RX	VSS	SG_PRI_AUX_RX	VSS		EPA_DIV_PKO	WF_5G_DIV_TRX		SG_DIV_AUX_TX	VSS			VSS	AVDD3V3_BT_PA	VSS	FM_SANT AVSS_FM T		
U	NC		SG_PRI_AUX_RX	VSS	WF_2G_PRI_T_RX			SG_DIV_AUX_RX		AVDD3V3_DV_V		WF_2G_DIV_TRX	VSS		FM_LANT	NC U		
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2-2 Ball pinout

2.3 Package Outline





NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
- ⚠** PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- ⚠** DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
- ⚠** THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. REFERENCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5
7. PKG BALL DIAMETER IS 0.25 ± 0.05 mm
BEFORE REFLOW.

Figure 2-3 Package outline

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.0693	1.1400	1.2000	0.0421	0.0449	0.0472
A1	0.1300	0.1800	0.2300	0.0051	0.0071	0.0091
A2	0.9100	0.9600	1.0100	0.0358	0.0378	0.0398
c	0.2200	0.2600	0.3000	0.0087	0.0102	0.0118
D	6.8000	6.9000	7.0000	0.2677	0.2717	0.2756
E	6.8000	6.9000	7.0000	0.2677	0.2717	0.2756
D1	----	6.4000	----	----	0.2520	----
E1	----	6.4000	----	----	0.2520	----
e	----	0.4000	----	----	0.0157	----
b	0.2100	0.2600	0.3100	0.0083	0.0102	0.0122
aaa	0.1000			0.0039		
bbb	0.1000			0.0039		
ddd	0.0800			0.0031		
eee	0.1500			0.0059		
fff	0.0500			0.0020		
MD/ME	17 / 17					

Figure 2-4 Package parameters

2.4 Reflow Profile

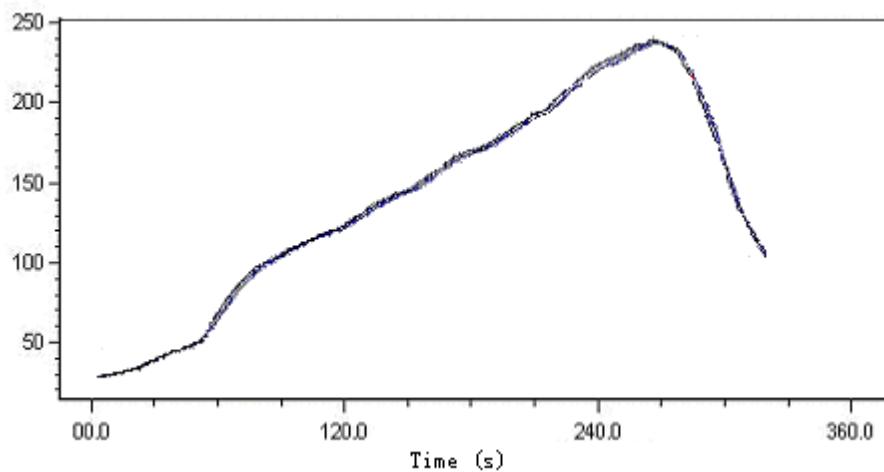


Figure 2-5 Reflow profile

Note:

- 1) Recommended reflow profile for lead-free solder paste
 - Ramp at 1-2°C per second to 245+/-5°C
 - Dwell at 235°C for 10 seconds
 - Dwell at 217°C for 30~60s
 - Total reflow time is about 220~270 s
 - Cold down ramp < 4°C/s
- 2) Recommended solder paste type
 - SnAgCu solder paste
 - Metal contents should be about 88.5%
- 3) Recommended parameter for stencil making
 - Metal mask thickness: 5 mils
 - Opening area ratio: 100%

3 Pin Information

3.1 Pin Symbol Descriptions

The following table explains the symbols used in the pin lists.

Table 1-1 Definition of pin symbols

Field	Symbol	Type Description
Pin Type	I	Digital input
	O	Digital output
	O/T	Digital output with tri-state option
	I/O	Digital bi-directional pin
	I/O/T	Digital bi-directional pin with tri-state option
	PI	Power pin, input from external power supply
	PIO	Power pin, input from external or floating to use internal LDO power supply
	PO	Power pin, output for external devices
	G	Ground pin
	AI	Analog input pin
	AO	Analog output pin
	AIO	Analog bi-directional pin
Pin Value	IPU	Input with pull-up
	IPD	Input with pull-down
	OH	Output "1"
	OL	Output "0"
	Z	Tri-state
Power	VBAT	Battery power supply input
	VDDCORE	Power supply for core, the internal power source is DCDC_CORE

Field	Symbol	Type Description
	VDDIO	Power supply for I/O, the internal power source is LDO_VDD18/LDO_VDD28/LDO_VDDMEM

3.2 Pin List

Table 3-2 Pin list description

Pin No.	Pin Name	Power	Pull up	Pull down	Drive Strength	At Reset	After Reset	Description
JTAG								
B7	MTMS	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0, wpu	ARM JTAG TMS
A7	MTCK	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0, wpdo	ARM JTAG TCK
WCI-2								
E17	WCI_2_RXD	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0, wpu	WCI-2 Coexistence interface RX
E16	WCI_2_TXD	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0, oe=1,1	WCI-2 Coexistence interface TX
GPIO								
J1	GPIO0	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0, wpu	GPIO0
J2	GPIO1	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0, wpu	GPIO1
H2	GPIO2	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0, wpu	GPIO2
H1	GPIO3	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0, wpu	GPIO3
Clock								
K13	CLK_32K							32KHz clock output in XO mode/32KHz clock input in buffer mode
K14	DCXO_26M_OUT							Reference clock output in XO mode
H16	XTAL_IN							Crystal positive /reference clock buffer input
H17	XTAL_OUT							Crystal negative
System								



D6	RST_N	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0, wpu	External reset input, Active low
F14	XTLEN	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0, oe=1, 0	Crystal enable control
G12	GNSS_LNA_EN	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1,oe=0, wpu,fun_sel=3	GNSS LNA enable
F13	PTEST	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0, wpdo	Production test mode
B5	CHIP_EN	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0,oe=0	Chip enable
K16	DCXO_LP_MODE							Low power control in XO mode
G14	DCXO_BONDING_OPT							XO/buffer mode selection
J16	REF_FREQ_SEL							Reference clock frequency selection
G13	INT	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0,oe=1,0	Interrupt output to AP
IIS								
B4	IISDO	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0, oe=1, 0	IIS port data output
D5	IISCLK	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0, oe=1, 0	IIS port bit clock
A4	IISLRCK	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0, oe=1, 1	IIS port Left/Right clock
C5	IISDI	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1, oe=0,wpdo	IIS port data input
UART								
C1	U0TXD	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0,oe=1,1	UART port0 TX
C2	U0RXD	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1,oe=0,wpu	UART port0 RX
B2	U0RTS	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0,oe=1,1	UART port0 RTS
B1	U0CTS	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=1,oe=0,wpu	UART port0 CTS
F1	U1TXD	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8mA		ie=0, oe=1,1	UART port1 TX



E1	U1RXD	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpu	UART port1 RX
E2	U1RTS	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=0, oe=1, 1	UART port1 RTS
D2	U1CTS	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpu	UART port1 CTS
A3	U3TXD	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=0, oe=1, 1	UART port3 TX
B3	U3RXD	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpu	UART port3 RX
SDIO								
C11	SD_D3	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1, oe=0, wpu	SDIO port data 3
D11	SD_D2	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1, oe=0, wpu	SDIO port data 2
E11	SD_D1	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1, oe=0, wpu	SDIO port data 1
B11	SD_D0	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/		ie=1, oe=0, wpu	SDIO port data 0

					104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)			
D12	SD_CMD	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1, oe=0, wpu	SDIO port command
A12	SD_CLK	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1, oe=0, wpdo	SDIO port clock
SPI NOR FLASH								
D10	ESMD0	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1,oe=0,wpu	Serial Flash data 0
D9	ESMD1	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh		ie=1,oe=0,wpu	Serial Flash data 1



					m(PMOS)			
B9	ESMD2	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1,oe=0,wpu	Serial Flash data 2
A9	ESMD3	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1,oe=0,wpu	Serial Flash data 3
B10	ESMCSN	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1,oe=0,wpu	Serial Flash chip select
A10	ESMCLK	VDDIO	4.7K/20K+/-50%	50K+/-70%	26/30/35/ 41/52/70/ 104/202oh m(NMOS) 23/28/33/ 39/49/65/ 98/200oh m(PMOS)		ie=1,oe=0,wpu	Serial Flash clock
PCIE								
A14	PCIE_REFCLKP							PCIE reference clock positive
B14	PCIE_REFCLKN							PCIE reference clock negative



A15	PCIE_TXP							PCIE differential TX+
B15	PCIE_TXN							PCIE differential TX-
B17	PCIE_RXP							PCIE differential RX+
B16	PCIE_RXN							PCIE differential RX-
C13	PCIE_RESREF							PCIE reference resistor
B13	PCIE_WAKE_L	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpu	PCIE Wake-up Output, Low Active
F12	PCIE_CLKREQ_L	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpu	PCIE Clock Request Output, Low Active
B12	PCIE_RST_L	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpdo	PCIE Reset Input, Low Active
C14	PCIE_VPH							PCIE High-voltage supply
D17	PCIE_VP							PCIE PHY analog and digital supply
D16	PCIE_VPTXN							PCIE PHY transmit supply
RF Control								
G2	RFCTL0	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpdo,fun_sel=3	RF Control 0
G3	RFCTL1	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpdo,fun_sel=3	RF Control 1
J4	RFCTL2	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpdo,fun_sel=3	RF Control 2
J5	RFCTL3	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpdo,fun_sel=3	RF Control 3
J6	RFCTL4	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A		ie=1, oe=0, wpdo,fun_sel=3	RF Control 4
J7	RFCTL5	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A	ie=1,oe=0 ,wpu	ie=1, oe=0, wpdo,fun_sel=3	RF Control 5
H6	RFCTL6	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A	ie=1,oe=0 ,wpu	ie=1, oe=0, wpdo,fun_sel=3	RF Control 6
G4	RFCTL7	VDDIO	4.7K/20K+/-50%	50K+/-70%	2/4/6/8m A	ie=1,oe=0 ,wpu	ie=1, oe=0, wpdo,fun_sel=3	RF Control 7



				A		3	
RF							
T16	FM_SANT						FM short antenna
U16	FM_LANT						FM long antenna
T17	AVSS_FM						FM GND
R14	BT_TRX_P						BT RF port (Standalone)
M17	GNSS_RF_IN						GNSS RF input port
N1	EPA_PRI_PKD						External Primary PA Power Detect
T1	WF_5G_PRI_T_RX						5GHz Primary TRX(Internal PA/Switch/LNA Path)
U5	WF_2G_PRI_T_RX						2.4GHz Primary TRX
T6	EPA_DIV_PKD						External Diversity PA Power Detect
T7	WF_5G_DIV_T_RX						5GHz Diversity TRX(Internal PA/Switch/LNA Path)
U13	WF_2G_DIV_T_RX						2.4GHz Diversity TRX
U3	5G_PRI_AUX_TX						5GHz Primary Aux TX
T3	5G_PRI_AUX_RX						5GHz Primary Aux RX
T9	5G_DIV_AUX_TX						5GHz Diversity Aux TX
U8	5G_DIV_AUX_RX						5GHz Diversity Aux RX
TSEN							
G17	TSEN_VREFP						TSX temperature sense reference positive
F16	TSEN_VREFN						TSX temperature sense reference negative
G16	TSEN_IN						TSX temperature sense input
Power							
K17	AVDD1V8_DCXO						1.8V supply for DCXO
B8	VDDEFU						1.8V supply for efuse



H13	AVDD_RTC							Power supply for GNSS RTC counter
K2	AVDD1V2_AFE_1							1.2V supply for Wi-Fi ADCs/DACs and BBPLL
L15	AVDD1V2_AFE_2							1.2V supply for GNSS ADC
L1	AVDD1V2_WF_TRX1							1.2V supply for Wi-Fi VCO and Wi-Fi TRX1
P12	AVDD1V2_WF_TRX2							1.2V supply for BT/FM ad Wi-Fi TRX2
L16	AVDD1V2_GNSS							1.2V supply for GNSS VCO/GNSS RX
T14	AVDD3V3_BT_PA							3.3V supply for BT PA
R3	AVDD3V3_PRI							3.3V supply for Wi-Fi primary PA
U11	AVDD3V3_DIV							3.3V supply for Wi-Fi diversity PA
F7	VDDIO							1.8V supply for digital IO
A6	DVDD_IN							Supply for internal digital core LDO
B6	DVDD_IN							Supply for internal digital core LDO
C7	DVDD_CORE							Internal digital core LDO output
E14	DVDD_CORE							Internal digital core LDO output
F2	DVDD_CORE							Internal digital core LDO output
NC								
A1	NC							Not Connected
A17	NC							Not Connected
U17	NC							Not Connected
U1	NC							Not Connected
GND								
D4	VSS							GND
D13	VSS							GND



D14	VSS							GND
E5	VSS							GND
E6	VSS							GND
E9	VSS							GND
E10	VSS							GND
F6	VSS							GND
F15	VSS							GND
G7	VSS							GND
G8	VSS							GND
G9	VSS							GND
G10	VSS							GND
H8	VSS							GND
H9	VSS							GND
H10	VSS							GND
H11	VSS							GND
J8	VSS							GND
J9	VSS							GND
J10	VSS							GND
J11	VSS							GND
J14	VSS							GND
K3	VSS							GND
K4	VSS							GND
K5	VSS							GND
K6	VSS							GND
K7	VSS							GND
K8	VSS							GND
K9	VSS							GND
K10	VSS							GND
K11	VSS							GND
K12	VSS							GND
L2	VSS							GND
L3	VSS							GND
L4	VSS							GND
L5	VSS							GND
L6	VSS							GND
L7	VSS							GND
L8	VSS							GND
L9	VSS							GND
L10	VSS							GND
L11	VSS							GND
L12	VSS							GND
L13	VSS							GND
L14	VSS							GND



M3	VSS							GND
M5	VSS							GND
M6	VSS							GND
M7	VSS							GND
M8	VSS							GND
M10	VSS							GND
M11	VSS							GND
M12	VSS							GND
M14	VSS							GND
M16	VSS							GND
N2	VSS							GND
N3	VSS							GND
N4	VSS							GND
N5	VSS							GND
N8	VSS							GND
N9	VSS							GND
N10	VSS							GND
N11	VSS							GND
N13	VSS							GND
N14	VSS							GND
N15	VSS							GND
P3	VSS							GND
P4	VSS							GND
P5	VSS							GND
P6	VSS							GND
P7	VSS							GND
P8	VSS							GND
P9	VSS							GND
P10	VSS							GND
P11	VSS							GND
P13	VSS							GND
P14	VSS							GND
P17	VSS							GND
R1	VSS							GND
R2	VSS							GND
R5	VSS							GND
R6	VSS							GND
R7	VSS							GND
R8	VSS							GND
R9	VSS							GND
R10	VSS							GND
R11	VSS							GND
R12	VSS							GND

R13	VSS										GND
R15	VSS										GND
T2	VSS										GND
T4	VSS										GND
T10	VSS										GND
T13	VSS										GND
T15	VSS										GND
U4	VSS										GND
U14	VSS										GND

3.3 Pin Multiplexed Function List

Marlin3 adopts programmable pin multiplexing to reduce pin number as well as providing enough flexibility. Multiple signals are connected to a multiplexer that connects to the same I/O pin showed in the following table.

Table 3-3 Pin multiplexed function list

PIN Name	Function 1	Type	Function 2	Type	Function 3	Type	Function 4	Type	Function 5	Type	Function 6	Type
IISDO	IISDO	O/T	IIS1DO	O/T	COEX3	I/O	GPIO4	I/O/T	DB0(G0)	O	WB9	O
IISCLK	IISCLK	I/O/T	IIS1CK	I/O/T	COEX4	I/O	GPIO5	I/O/T	DB1(G0)	O	WB10	O
IISLRCK	IISLRCK	I/O/T	IIS1LRCK	I/O/T	COEX5	I/O	GPIO6	I/O/T	DB2(G0)	O	WB11	O
IISDI	IISDI	I			COEX6	I/O	GPIO7	I/O/T	DB3(G0)	O	WB12	O
U0TXD	U0TXD	O	-	-	-	-	GPIO43	I/O/T	-	-	PCIe_DB G12	O
U0RXD	U0RXD	I	-	-	-	-	GPIO44	I/O/T	-	-	PCIe_DB G13	O
U0RTS	U0RTS	O	-	-	-	-	GPIO45	I/O/T	-	-	PCIe_DB G14	O
U0CTS	U0CTS	I	-	-	-	-	GPIO46	I/O/T	-	-	PCIe_DB G15	O
SD_D3	SD_D3	I/O/T					GPIO15	I/O/T	DB3(G1)	O	PCIe_DB G0	O
SD_D2	SD_D2	I/O/T					GPIO16	I/O/T	DB4(G1)	O	PCIe_DB G1	O
SD_D1	SD_D1	I/O/T					GPIO17	I/O/T	DB5(G1)	O	PCIe_DB	O



									G2			
SD_D0	SD_D0	I/O/T				GPIO18	I/O/T	DB6(G1)	O	PCIe_DB G3	O	
SD_CLK	SD_CLK	I/O/T				GPIO19	I/O/T			PCIe_DB G4	O	
SD_CMD	SD_CMD	I/O/T				GPIO20	I/O/T	DB7(G1)	O	PCIe_DB G5	O	
GPIO1	GPIO1	I/O/T						DB5(G0)	O	WB1	O	
WCI_2_T XD	WCI_2_T XD	O			COEX1	I/O	GPIO9	I/O/T	DB7(G0)	O	WB4	O
WCI_2_R XD	WCI_2_R XD	I			COEX0	I/O	GPIO8	I/O/T	DB2(G1)	O	WB3	O
GPIO0	GPIO0	I/O/T			COEX2	I/O			DB4(G0)	O	WB0	O
RFCTL0	RFCTL0	O			SOC_DB G0	O	GPIO32	I/O/T			WB13	O
RFCTL1	RFCTL1	O			SOC_DB G1	O	GPIO33	I/O/T			WB14	O
RFCTL2	RFCTL2	O			SOC_DB G2	O	GPIO34	I/O/T			WB15	O
RFCTL3	RFCTL3	O			SOC_DB G3	O	GPIO35	I/O/T			WB16	O
RFCTL4	RFCTL4	O			SOC_DB G4	O	GPIO36	I/O/T			WB17	O
RFCTL5	RFCTL5	O			SOC_DB G5	O	GPIO37	I/O/T			WB18	O
RFCTL6	RFCTL6	O	PPS(G1)	O	SOC_DB G6	O	GPIO38	I/O/T			WB19	O
RFCTL7	RFCTL7	O	T_DIG(G 1)	I	SOC_DB G7	O	GPIO39	I/O/T			WB20	O
U1TXD	U1TXD	O					GPIO21	I/O/T			PCIe_DB G8	O
U1RXD	U1RXD	I					GPIO22	I/O/T			PCIe_DB	O



										G9	
U1RTS	U1RTS	O					GPIO23	I/O/T		PCIe_DB G10	O
U1CTS	U1CTS	I					GPIO24	I/O/T		PCIe_DB G11	O
GNSS_LN A_EN	GNSS_LN A_EN	O			FDMA_C EN	I	GPIO25	I/O/T			
MTMS	MTMS	I/O	PPS(G0)	O	FDMA_M ISO	O	GPIO11	I/O/T	DB0(G1)	O	WB5
MTCK	MTCK	I	T_DIG(G 0)	I	FDMA_M OSI	I	GPIO12	I/O/T	DB1(G1)	O	WB6
XTLEN	XTLEN	I/O			FDMA_C LK	I	GPIO43	I/O/T	-	-	
INT	INT	O			COEX7	I/O	GPIO10	I/O/T			
U3TXD	U3TXD	O	I2C_SDA	I/O/T			GPIO30	I/O/T		PCIe_DB G6	O
U3RXD	U3RXD	I	I2C_SCL	I/O/T			GPIO31	I/O/T		PCIe_DB G7	O
GPIO2	GPIO2	I/O/T	CLK_OUT 0	O					DB6(G0)	O	WB2
GPIO3	GPIO3	I/O/T	CLK_OUT 1	O							
ESMD3	ESMD3	I/O	U2TXD(G 0)	O			GPIO13	I/O/T		WB7	O
ESMD2	ESMD2	I/O	U2RXD(G 0)	I			GPIO14	I/O/T		WB8	O
ESMD1	ESMD1	I/O					GPIO26	I/O/T		WB21	O
ESMD0	ESMD0	I/O					GPIO27	I/O/T		WB22	O
ESMCSN	ESMCSN	O					GPIO28	I/O/T		WB23	O
ESMCLK	ESMCLK	O					GPIO29	I/O/T			
PCIE_CLK REQ_L	PCIE_CLK REQ_L	I/O					GPIO40	I/O/T			

PCIE_RST_L	PCIE_RST_L	I	U2RXD(G1)	I			GPIO41	I/O/T				
PCIE_WAKE_L	PCIE_WAKE_L	O	U2TXD(G1)	O			GPIO42	I/O/T				

3.4 Control Registers

3.4.1 Memory Map

Base address: 0x4084_0000

Table 3-4 Pin register memory map

Offset Addr	Name	Default value after reset
0x0000	PIN_CRTL_REG0	32'b0
0x0004	PIN_CRTL_REG1	32'b0
0x0008	PIN_CRTL_REG2	32'b0
0x000C	PIN_CRTL_REG3	32'b0
0x0010	GPIO0_REG	32'b0000_8100
0x0014	GPIO1_REG	32'b0000_8100
0x0018	GPIO2_REG	32'b0000_8100
0x001C	GPIO3_REG	32'b0000_8100
0x0020	ESMD3_REG	32'b0000_8100
0x0024	ESMD2_REG	32'b0000_8100
0x0028	ESMD1_REG	32'b0000_8100
0x002C	ESMD0_REG	32'b0000_8100
0x0030	ESMCSN_REG	32'b0000_8100
0x0034	ESMSMP_REG	32'b0000_8100
0x0038	ESMCLK_REG	32'b0000_8100
0x003C	IISDO_REG	32'b0000_8000



0x0040	IISCLK_REG	32'b0000_8000
0x0044	IISLRCK_REG	32'b0000_8000
0x0048	IISLDI_REG	32'b0000_8080
0x004C	MTMS_REG	32'b0000_810A
0x0050	MTCK_REG	32'b0000_8086
0x0054	XTLEN_REG	32'b0000_8000
0x0058	INT_REG	32'b0000_8000
0x005C	PTEST_REG	32'b0000_8080
0x0060	CHIP_EN_REG	32'b0000_8000
0x0064	RST_N_REG	32'b0000_8100
0x0068	WCI_2_RXD_REG	32'b0000_8100
0x006C	WCI_2_TXD_REG	32'b0000_8000
0x0070	U0TXD_REG	32'b0000_8000
0x0074	U0RXD_REG	32'b0000_8100
0x0078	U0RTS_REG	32'b0000_8000
0x007C	U0CTS_REG	32'b0000_8100
0x0080	U3TXD_REG	32'b0000_8000
0x0084	U3RXD_REG	32'b0000_8100
0x0088	RFCTL0_REG	32'b0000_80B0
0x008C	RFCTL1_REG	32'b0000_80B0
0x0090	RFCTL2_REG	32'b0000_80B0
0x0094	RFCTL3_REG	32'b0000_80B0
0x0098	RFCTL4_REG	32'b0000_80B0
0x009C	RFCTL5_REG	32'b0000_80B0
0x00A0	RFCTL6_REG	32'b0000_80B0

0x00A4	RFCTL7_REG	32'b0000_80B0
0x00A8	SD_D3_REG	32'b0000_8100
0x00AC	SD_D2_REG	32'b0000_8100
0x00B0	SD_D1_REG	32'b0000_8100
0x00B4	SD_D0_REG	32'b0000_8100
0x00B8	SD_CLK_REG	32'b0000_8080
0x00BC	SD_CMD_REG	32'b0000_8100
0x00C0	GNSS_LNA_EN_REG	32'b0000_8130
0x00C4	U1TXD_REG	32'b0000_8000
0x00C8	U1RXD_REG	32'b0000_8100
0x00CC	U1RTS_REG	32'b0000_8000
0x00D0	U1CTS_REG	32'b0000_8100
0x00D4	PCIE_CLKREQ_L_REG	32'b0000_8100
0x00D8	PCIE_RST_L_REG	32'b0000_8080
0x00DC	PCIE_WAKE_L_REG	32'b0000_8100

3.4.2 Register Description

3.4.2.1 PIN_CRTL_REG0

0x00000000		output to prdata(0x00000000)														PIN_CRTL_REG0						
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16						
Name	pin_ctrl_reg0																					
Type	RW																					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Name	pin_ctrl_reg0																					
Type	RW																					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

output to prdata

Field Name	Bit	Type	Set/Clear	Reset Value	Description
pin_ctrl_reg0	[31: 0]	RW	NA	0	<p>[9]: spi switch2rf master enable. 置, when set 1: rf spi will be controller by core spi master</p> <p>When set 0: if only under analog mode, rf spi can be controlled by external spi PAD. (there's no difference to be set 0/1 under normal mode)</p> <p>[8]: pin rf share enable, only when RF module use the shared pin, this bit should set 1 to isolated digital parts.</p> <p>[6:0]: ESM* PAD drive strength bit 2,should be used along with ESM*bsr_drv[1:0]</p>

3.4.2.2 PIN_CRTL_REG1

0x00000004		output to prdata(0x00000000)															PIN_CRTL_REG1			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	pin_ctrl_reg1																			
Type	RW																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	pin_ctrl_reg1																			
Type	RW																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

output to prdata

Field Name	Bit	Type	Set/Clear	Reset Value	Description
pin_ctrl_reg1	[31: 0]	RW	NA	0	reserved

3.4.2.3 PIN_CRTL_REG2

0x00000008		output to prdata(0x00000000)													PIN_CRTL_REG2				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	pin_ctrl_reg2																		
Type	RW																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	pin_ctrl_reg2																		
Type	RW																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

output to prdata

Field Name		Bit	Type	Set/Clear	Reset Value	Description											
pin_ctrl_reg2	[31: 0]	RW	NA	0	reserved												

3.4.2.4 PIN_CRTL_REG3

0x0000000C		output to prdata(0x00000000)													PIN_CRTL_REG3				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	pin_ctrl_reg3																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	pin_ctrl_reg3							pin_ctrl_reg3_8	pin_ctrl_reg3_7_4				pin_ctrl_reg3_3_0						
Type	RO							RW	RO				RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

output to prdata

Field Name	Bit	Type	Set/Clear	Reset Value	Description
pin_ctrl_reg3	[31: 9]	RO	NA	0	
pin_ctrl_reg3_8	[8]	RW	NA	0	ALL IO wpdi control
pin_ctrl_reg3_7_4	[7: 4]	RO	NA	0	
pin_ctrl_reg3_3_0	[3: 0]	RW	NA	0	These bit only affect under ptest_bsc_mode or ptest_func_mode, can set pad drive strength.

3.4.2.5 GPIO0_REG

0x00000010				GPIO0 register(0x00008100)												GPIO0_REG								
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16								
Name	Reserved																							
Type	RO																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Name	GPIO0_bsr_drv		Reserve d	GPIO0_bsr_wpu s	GPIO0_bsr_se	Reserved		GPIO0_fun_wpu	GPIO0_fun_wpd o	GPIO0_fun_sel				GPIO0_slp_wpu	GPIO0_slp_wpd o	GPIO0_slp_ie	GPIO0_slp_oe							
Type	RW		RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW							
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO0 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
GPIO0_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
GPIO0_bsr_wpus	[12]	RW	NA	0	
GPIO0_bsr_se	[11]	RW	NA	0	

reserved	[10: 9]	RO	NA	0	
GPIO0_fun_wpu	[8]	RW	NA	0x1	
GPIO0_fun_wpdo	[7]	RW	NA	0	
GPIO0_fun_sel	[6: 4]	RW	NA	0	
GPIO0_slp_wpu	[3]	RW	NA	0	
GPIO0_slp_wpdo	[2]	RW	NA	0	
GPIO0_slp_ie	[1]	RW	NA	0	
GPIO0_slp_oe	[0]	RW	NA	0	

3.4.2.6 GPIO1_REG

0x00000014				GPIO1 register(0x00008100)												GPIO1_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	GPIO1_bsr_drv	Reserve d	GPI O1_bsr_wpu s	GPI O1_bsr_se	Reserved		GPI O1_fun_wpu	GPI O1_fun_wpd o	GPIO1_fun_sel				GPI O1_slp_wpu	GPI O1_slp_wpd o	GPI O1_slp_i e	GPI O1_slp_oe				
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW				
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0				

GPIO1 register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
GPIO1_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
GPIO1_bsr_wpus	[12]	RW	NA	0	
GPIO1_bsr_se	[11]	RW	NA	0	

reserved	[10: 9]	RO	NA	0	
GPIO1_fun_wpu	[8]	RW	NA	0x1	
GPIO1_fun_wpdo	[7]	RW	NA	0	
GPIO1_fun_sel	[6: 4]	RW	NA	0	
GPIO1_slp_wpu	[3]	RW	NA	0	
GPIO1_slp_wpdo	[2]	RW	NA	0	
GPIO1_slp_ie	[1]	RW	NA	0	
GPIO1_slp_oe	[0]	RW	NA	0	

3.4.2.7 GPIO2_REG

0x000000018				GPIO2 register(0x00008100)												GPIO2_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	GPIO2_bsr_drv	Reserve d	GPI O2_bsr_wpus	GPI O2_bsr_se	Reserved		GPI O2_fun_wpu	GPI O2_fun_wpd o	GPIO2_fun_sel				GPI O2_slp_wpu	GPI O2_slp_wpd o	GPI O2_slp_ie	GPI O2_slp_oe			
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW			
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0			

GPIO2 register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
GPIO2_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
GPIO2_bsr_wpus	[12]	RW	NA	0	
GPIO2_bsr_se	[11]	RW	NA	0	

reserved	[10: 9]	RO	NA	0	
GPIO2_fun_wpu	[8]	RW	NA	0x1	
GPIO2_fun_wpdo	[7]	RW	NA	0	
GPIO2_fun_sel	[6: 4]	RW	NA	0	
GPIO2_slp_wpu	[3]	RW	NA	0	
GPIO2_slp_wpdo	[2]	RW	NA	0	
GPIO2_slp_ie	[1]	RW	NA	0	
GPIO2_slp_oe	[0]	RW	NA	0	

3.4.2.8 GPIO3_REG

0x00000001C				GPIO3 register(0x00008100)												GPIO3_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	GPIO3_bsr_drv	Reserve d	GPI O3_bsr_wpu s	GPI O3_bsr_se	Reserved		GPI O3_fun_wpu	GPI O3_fun_wpd o	GPIO3_fun_sel				GPI O3_slp_wpu	GPI O3_slp_wpd o	GPI O3_slp_i e	GPI O3_slp_oe			
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW			
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0			

GPIO3 register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
GPIO3_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
GPIO3_bsr_wpus	[12]	RW	NA	0	
GPIO3_bsr_se	[11]	RW	NA	0	

reserved	[10: 9]	RO	NA	0	
GPIO3_fun_wpu	[8]	RW	NA	0x1	
GPIO3_fun_wpdo	[7]	RW	NA	0	
GPIO3_fun_sel	[6: 4]	RW	NA	0	
GPIO3_slp_wpu	[3]	RW	NA	0	
GPIO3_slp_wpdo	[2]	RW	NA	0	
GPIO3_slp_ie	[1]	RW	NA	0	
GPIO3_slp_oe	[0]	RW	NA	0	

3.4.2.9 ESMD3_REG

0x00000020				ESMD3 register(0x00008100)												ESMD3_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	ESMD3_bsr_drv	Reserve d	ESM D3_bsr_wpus	ESM D3_bsr_se	Reserved		ESM D3_fun_wpu	ESM D3_fun_wpd o	ESMD3_fun_sel				ESM D3_slp_wpu	ESM D3_slp_wpd o	ESM D3_slp_ie	ESM D3_slp_oe				
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW				
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0				

ESMD3 register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
ESMD3_bsr_drv	[15: 14]	RW	NA	0x2	bsr_drv[2]: PIN_CTRL_REG0[5]
reserved	[13]	RO	NA	0	
ESMD3_bsr_wpus	[12]	RW	NA	0	
ESMD3_bsr_se	[11]	RW	NA	0	

reserved	[10: 9]	RO	NA	0	
ESMD3_fun_wpu	[8]	RW	NA	0x1	
ESMD3_fun_wpdo	[7]	RW	NA	0	
ESMD3_fun_sel	[6: 4]	RW	NA	0	
ESMD3_slp_wpu	[3]	RW	NA	0	
ESMD3_slp_wpdo	[2]	RW	NA	0	
ESMD3_slp_ie	[1]	RW	NA	0	
ESMD3_slp_oe	[0]	RW	NA	0	

3.4.2.10 ESMD2_REG

0x00000024				ESMD2 register(0x00008100)												ESMD2_REG							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16							
Name	Reserved																						
Type	RO																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Name	ESMD2_bsr_drv		Reserve d	ESM D2_bsr_wpu s	ESM D2_bsr_se	Reserved		ESM D2_fun_wpu	ESM D2_fun_wpdo	ESMD2_fun_sel			ESM D2_slp_wpu	ESM D2_slp_wpdo	ESM D2_slp_ie	ESM D2_slp_oe							
Type	RW		RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW							
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ESMD2 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
ESMD2_bsr_drv	[15: 14]	RW	NA	0x2	bsr_drv[2]: PIN_CTRL_REG0[4]
reserved	[13]	RO	NA	0	
ESMD2_bsr_wpus	[12]	RW	NA	0	
ESMD2_bsr_se	[11]	RW	NA	0	

reserved	[10: 9]	RO	NA	0	
ESMD2_fun_wpu	[8]	RW	NA	0x1	
ESMD2_fun_wpdo	[7]	RW	NA	0	
ESMD2_fun_sel	[6: 4]	RW	NA	0	
ESMD2_slp_wpu	[3]	RW	NA	0	
ESMD2_slp_wpdo	[2]	RW	NA	0	
ESMD2_slp_ie	[1]	RW	NA	0	
ESMD2_slp_oe	[0]	RW	NA	0	

3.4.2.11 ESMD1_REG

0x00000028				ESMD1 register(0x00008100)												ESMD1_REG							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16							
Name	Reserved																						
Type	RO																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Name	ESMD1_bsr_drv		Reserve d	ESM D1_bsr_wpu s	ESM D1_bsr_se	Reserved		ESM D1_fun_wpu	ESM D1_fun_wpdo	ESMD1_fun_sel				ESM D1_slp_wpu	ESM D1_slp_wpdo	ESM D1_slp_ie	ESM D1_slp_oe						
Type	RW		RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW						
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ESMD1 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
ESMD1_bsr_drv	[15: 14]	RW	NA	0x2	bsr_drv[2]: PIN_CTRL_REG0[3]
reserved	[13]	RO	NA	0	
ESMD1_bsr_wpus	[12]	RW	NA	0	
ESMD1_bsr_se	[11]	RW	NA	0	

reserved	[10: 9]	RO	NA	0	
ESMD1_fun_wpu	[8]	RW	NA	0x1	
ESMD1_fun_wpdo	[7]	RW	NA	0	
ESMD1_fun_sel	[6: 4]	RW	NA	0	
ESMD1_slp_wpu	[3]	RW	NA	0	
ESMD1_slp_wpdo	[2]	RW	NA	0	
ESMD1_slp_ie	[1]	RW	NA	0	
ESMD1_slp_oe	[0]	RW	NA	0	

3.4.2.12 ESMD0_REG

0x00000002C				ESMD0 register(0x00008100)												ESMD0_REG							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16							
Name	Reserved																						
Type	RO																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Name	ESMD0_bsr_drv		Reserve d	ESM DO_bsr_wpus	ESM DO_bsr_se	Reserved		ESM DO_fun_wpu	ESM DO_fun_wpdo	ESMD0_fun_sel			ESM DO_slp_wpu	ESM DO_slp_wpdo	ESM DO_slp_ie	ESM DO_slp_oe							
Type	RW		RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW							
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ESMD0 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
ESMD0_bsr_drv	[15: 14]	RW	NA	0x2	bsr_drv[2]: PIN_CTRL_REG0[2]
reserved	[13]	RO	NA	0	
ESMD0_bsr_wpus	[12]	RW	NA	0	
ESMD0_bsr_se	[11]	RW	NA	0	

reserved	[10: 9]	RO	NA	0	
ESMD0_fun_wpu	[8]	RW	NA	0x1	
ESMD0_fun_wpdo	[7]	RW	NA	0	
ESMD0_fun_sel	[6: 4]	RW	NA	0	
ESMD0_slp_wpu	[3]	RW	NA	0	
ESMD0_slp_wpdo	[2]	RW	NA	0	
ESMD0_slp_ie	[1]	RW	NA	0	
ESMD0_slp_oe	[0]	RW	NA	0	

3.4.2.13 ESMCSN_REG

0x00000030		ESMCSN register(0x00008100)															ESMCSN_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	ESMCSN_bsr_drv	Reserve d	ESM CSN_bsr_wp us	ESM CSN_bsr_se	Reserved		ESM CSN_fun_wpu	ESM CSN_fun_wp do	ESMCSN_fun_sel				ESM CSN_slp_wp u	ESM CSN_slp_wp do	ESM CSN_slp_ie	ESM CSN_slp_oe				
Type	RW		RO	RW	RW		RW	RW	RW				RW	RW	RW	RW				
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0		

ESMCSN register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
ESMCSN_bsr_drv	[15: 14]	RW	NA	0x2	bsr_drv[2]: PIN_CTRL_REG0[1]
reserved	[13]	RO	NA	0	
ESMCSN_bsr_wp us	[12]	RW	NA	0	

ESMCSN_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
ESMCSN_fun_wp_u	[8]	RW	NA	0x1	
ESMCSN_fun_wp_do	[7]	RW	NA	0	
ESMCSN_fun_sel	[6: 4]	RW	NA	0	
ESMCSN_slp_wpu	[3]	RW	NA	0	
ESMCSN_slp_wpd_o	[2]	RW	NA	0	
ESMCSN_slp_ie	[1]	RW	NA	0	
ESMCSN_slp_oe	[0]	RW	NA	0	

3.4.2.14 ESMSMP_REG

0x00000034			ESMSMP register(0x00008100)												ESMSMP_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	ESMSMP_bs_r_drv		Reserve d	ESM SMP _bsr _wp_us	ESM SMP _bsr _se	Reserved		ESM SMP _fun _wp_u	ESM SMP _fun _wp do	ESMSMP_fun_sel			ESM SMP _slp _wp_u	ESM SMP _slp _wp do	ESM SMP _slp _ie	ESM SMP _slp _oe			
Type	RW		RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW			
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0			

ESMSMP register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
ESMSMP_bsr_drv	[15: 14]	RW	NA	0x2	bsr_drv[2]: PIN_CTRL_REG0[6]
reserved	[13]	RO	NA	0	

ESMSMP_bsr_wp_us	[12]	RW	NA	0	
ESMSMP_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
ESMSMP_fun_wp_u	[8]	RW	NA	0x1	
ESMSMP_fun_wp_do	[7]	RW	NA	0	
ESMSMP_fun_sel	[6: 4]	RW	NA	0	
ESMSMP_slp_wp_u	[3]	RW	NA	0	
ESMSMP_slp_wp_do	[2]	RW	NA	0	
ESMSMP_slp_ie	[1]	RW	NA	0	
ESMSMP_slp_oe	[0]	RW	NA	0	

3.4.2.15 ESMCLK_REG

0x00000038			ESMCLK register(0x00008100)												ESMCLK_REG					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	ESMCLK_bsr_drv	Reserve d	ESM CLK_bsr_wp_us	ESM CLK_bsr_se	Reserved		ESM CLK_fun_wp_u	ESM CLK_fun_wp_do	ESMCLK_fun_sel			ESM CLK_slp_wp_u	ESM CLK_slp_wp_do	ESM CLK_slp_ie	ESM CLK_slp_oe					
Type	RW	RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW	RW	RW			
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0			

ESMCLK register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

ESMCLK_bsr_drv	[15: 14]	RW	NA	0x2	bsr_drv[2]: PIN_CTRL_REG0[0]
reserved	[13]	RO	NA	0	
ESMCLK_bsr_wpus	[12]	RW	NA	0	
ESMCLK_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
ESMCLK_fun_wpu	[8]	RW	NA	0x1	
ESMCLK_fun_wpdo	[7]	RW	NA	0	
ESMCLK_fun_sel	[6: 4]	RW	NA	0	
ESMCLK_slp_wpu	[3]	RW	NA	0	
ESMCLK_slp_wpdo	[2]	RW	NA	0	
ESMCLK_slp_ie	[1]	RW	NA	0	
ESMCLK_slp_oe	[0]	RW	NA	0	

3.4.2.16 IISDO_REG

0x0000003C		IISDO register(0x00008000)															IISDO_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	IISDO_bsr_drv	Reserve d	IISD_O_bs r_wpu s	IISD_O_bs r_s e	Reserved		IISD_O_f un_wpu	IISD_O_f un_wpdo	IISDO_fun_sel			IISD_O_sl p_w pu	IISD_O_sl p_w pdo	IISD_O_sl p_ie	IISD_O_sl p_o e					
Type	RW		RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW	RW	RW		
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

IISDO register

Field Name	Bit	Type	Set/Clear	Reset Value	Description

reserved	[31: 16]	RO	NA	0	
IISDO_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
IISDO_bsr_wpus	[12]	RW	NA	0	
IISDO_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
IISDO_fun_wpu	[8]	RW	NA	0	
IISDO_fun_wpdo	[7]	RW	NA	0	
IISDO_fun_sel	[6: 4]	RW	NA	0	
IISDO_slp_wpu	[3]	RW	NA	0	
IISDO_slp_wpdo	[2]	RW	NA	0	
IISDO_slp_ie	[1]	RW	NA	0	
IISDO_slp_oe	[0]	RW	NA	0	

3.4.2.17 IISCLK_REG

0x00000040		IISCLK register(0x00008000)															IISCLK_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	IISCLK_bsr_drv	Reserve d	IISC_LK_bsr_wpus	IISC_LK_bsr_se	Reserved		IISC_LK_f un_wpu	IISC_LK_f un_wpd o	IISCLK_fun_sel				IISC_LK_s lp_wpu	IISC_LK_s lp_wpd o	IISC_LK_s lp_ie	IISC_LK_s lp_o e				
Type	RW		RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW			
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

IISCLK register

Field Name	Bit	Type	Set/Clear	Reset Value	Description



reserved	[31: 16]	RO	NA	0	
IISCLK_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
IISCLK_bsr_wpus	[12]	RW	NA	0	
IISCLK_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
IISCLK_fun_wpu	[8]	RW	NA	0	
IISCLK_fun_wpdo	[7]	RW	NA	0	
IISCLK_fun_sel	[6: 4]	RW	NA	0	
IISCLK_slp_wpu	[3]	RW	NA	0	
IISCLK_slp_wpdo	[2]	RW	NA	0	
IISCLK_slp_ie	[1]	RW	NA	0	
IISCLK_slp_oe	[0]	RW	NA	0	

3.4.2.18 IISLRCK_REG

0x00000044		IISLRCK register(0x00008000)															IISLRCK_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	IISLRCK_bsr_drv	Reserve d	IISL RCK_bsr_wpus	IISL RCK_bsr_se	Reserved		IISL RCK_fun_wpu	IISL RCK_fun_wpdo	IISLRCK_fun_sel				IISL RCK_slp_wp_u	IISL RCK_slp_wpdo	IISL RCK_slp_ie	IISL RCK_slp_oe				
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW				
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

IISLRCK register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description

reserved	[31: 16]	RO	NA	0	
IISLRCK_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
IISLRCK_bsr_wpus	[12]	RW	NA	0	
IISLRCK_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
IISLRCK_fun_wpu	[8]	RW	NA	0	
IISLRCK_fun_wpdo	[7]	RW	NA	0	
IISLRCK_fun_sel	[6: 4]	RW	NA	0	
IISLRCK_slp_wpu	[3]	RW	NA	0	
IISLRCK_slp_wpdo	[2]	RW	NA	0	
IISLRCK_slp_ie	[1]	RW	NA	0	
IISLRCK_slp_oe	[0]	RW	NA	0	

3.4.2.19 IISDI_REG

0x00000048		IISDI register(0x00008080)															IISDI_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	IISDI_bsr_dr	v	Res	er	ve	d	IISDI	_bsr	_wp	us	IISDI	_bsr	_se	Reserved	IISDI	IISDI	IISDI	IISDI		
Type	RW		RO	RW		RW		RO		RW		RW		RW		RW				
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0		

IISDI register

Field Name	Bit	Type	Set/Clear	Reset Value	Description

reserved	[31: 16]	RO	NA	0	
IISDI_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
IISDI_bsr_wpus	[12]	RW	NA	0	
IISDI_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
IISDI_fun_wpu	[8]	RW	NA	0	
IISDI_fun_wpdo	[7]	RW	NA	0x1	
IISDI_fun_sel	[6: 4]	RW	NA	0	
IISDI_slp_wpu	[3]	RW	NA	0	
IISDI_slp_wpdo	[2]	RW	NA	0	
IISDI_slp_ie	[1]	RW	NA	0	
IISDI_slp_oe	[0]	RW	NA	0	

3.4.2.20 MTMS_REG

0x0000004C		MTMS register(0x0000810A)															MTMS_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	MTMS_bsr_drv	Reserve d	MT MS_bsr_wpus	MT MS_bsr_se	Reserved		MT MS_fun_wpu	MT MS_fun_wpd o	MTMS_fun_sel				MT MS_slp_wpu	MT MS_slp_wpd o	MT MS_slp_ie	MT MS_slp_oe				
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW				
Reset	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0				

MTMS register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description

reserved	[31: 16]	RO	NA	0	
MTMS_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
MTMS_bsr_wpus	[12]	RW	NA	0	
MTMS_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
MTMS_fun_wpu	[8]	RW	NA	0x1	
MTMS_fun_wpdo	[7]	RW	NA	0	
MTMS_fun_sel	[6: 4]	RW	NA	0	
MTMS_slp_wpu	[3]	RW	NA	0x1	
MTMS_slp_wpdo	[2]	RW	NA	0	
MTMS_slp_ie	[1]	RW	NA	0x1	
MTMS_slp_oe	[0]	RW	NA	0	

3.4.2.21 MTCK_REG

0x00000050		MTCK register(0x00008086)															MTCK_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	MTCK_bsr_drv	Reserve d	MTC_K_b sr_wpu s	MTC_K_b sr_se	Reserved		MTC_K_fu n_w pu	MTC_K_fu n_w pdo	MTCK_fun_sel				MTC_K_sl p_w pu	MTC_K_sl p_w pdo	MTC_K_sl p_ie	MTC_K_sl p_o e				
Type	RW		RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW			
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0				

MTCK register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description

reserved	[31: 16]	RO	NA	0	
MTCK_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
MTCK_bsr_wpus	[12]	RW	NA	0	
MTCK_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
MTCK_fun_wpu	[8]	RW	NA	0	
MTCK_fun_wpdo	[7]	RW	NA	0x1	
MTCK_fun_sel	[6: 4]	RW	NA	0	
MTCK_slp_wpu	[3]	RW	NA	0	
MTCK_slp_wpdo	[2]	RW	NA	0x1	
MTCK_slp_ie	[1]	RW	NA	0x1	
MTCK_slp_oe	[0]	RW	NA	0	

3.4.2.22 XTLEN_REG

0x00000054		XTLEN register(0x00008000)															XTLEN_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	XTLEN_bsr_drv	Reserve d	XTL EN_bsr_wpus	XTL EN_bsr_se	Reserved		XTL EN_fun_wpu	XTL EN_fun_wpd o	XTLEN_fun_sel				XTL EN_slp_wpu	XTL EN_slp_wpd o	XTL EN_slp_ie	XTL EN_slp_oe				
Type	RW		RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW	RW		
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

XTLEN register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description



reserved	[31: 16]	RO	NA	0	
XTLEN_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
XTLEN_bsr_wpus	[12]	RW	NA	0	
XTLEN_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
XTLEN_fun_wpu	[8]	RW	NA	0	
XTLEN_fun_wpdo	[7]	RW	NA	0	
XTLEN_fun_sel	[6: 4]	RW	NA	0	
XTLEN_slp_wpu	[3]	RW	NA	0	
XTLEN_slp_wpdo	[2]	RW	NA	0	
XTLEN_slp_ie	[1]	RW	NA	0	
XTLEN_slp_oe	[0]	RW	NA	0	

3.4.2.23 INT_REG

0x00000058		INT register(0x00008000)															INT_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	INT_bsr_drv	Reserve d	INT_bsr_wpus	INT_bsr_se	Reserved		INT_fun_wpu	INT_fun_wpdo	INT_fun_sel			INT_slp_wpu	INT_slp_wpdo	INT_slp_ie	INT_slp_oe					
Type	RW		RO	RW	RW		RW	RW	RW			RW	RW	RW	RW		RW			
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

INT register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

INT_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
INT_bsr_wpus	[12]	RW	NA	0	
INT_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
INT_fun_wpu	[8]	RW	NA	0	
INT_fun_wpdo	[7]	RW	NA	0	
INT_fun_sel	[6: 4]	RW	NA	0	
INT_slp_wpu	[3]	RW	NA	0	
INT_slp_wpdo	[2]	RW	NA	0	
INT_slp_ie	[1]	RW	NA	0	
INT_slp_oe	[0]	RW	NA	0	

3.4.2.24 PTEST_REG

0x0000005C		PTEST register(0x00008080)															PTEST_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	PTEST_bsrDrv	Reserved	PTE_ST_bsr_wpus	PTE_ST_bsr_se	Reserved		PTE_ST_fun_wpu	PTE_ST_fun_wpd0	PTEST_fun_sel			PTE_ST_slp_wpu	PTE_ST_slp_wpd0	PTE_ST_slp_ie	PTE_ST_slp_o					
Type	RW	RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW		RW			
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0		

PTEST register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

PTEST_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
PTEST_bsr_wpus	[12]	RW	NA	0	
PTEST_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
PTEST_fun_wpu	[8]	RW	NA	0	
PTEST_fun_wpdo	[7]	RW	NA	0x1	
PTEST_fun_sel	[6: 4]	RW	NA	0	
PTEST_slp_wpu	[3]	RW	NA	0	
PTEST_slp_wpdo	[2]	RW	NA	0	
PTEST_slp_ie	[1]	RW	NA	0	
PTEST_slp_oe	[0]	RW	NA	0	

3.4.2.25 CHIP_EN_REG

0x00000060		CHIP_EN register(0x00008000)															CHIP_EN_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	CHIP_EN_bs r_drv	Reserve d	CHI P_E N_b sr_ wpu s	CHI P_E N_b sr_s e	Reserved		CHI P_E N_f un_ wpu	CHI P_E N_f un_ wpd o	CHIP_EN_fun_sel				CHI P_E N_si p_w pu	CHI P_E N_si p_w pdo	CHI P_E N_si p_ie	CHI P_E N_si p_o e				
Type	RW		RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW			
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

CHIP_EN register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

CHIP_EN_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
CHIP_EN_bsr_wpus	[12]	RW	NA	0	
CHIP_EN_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
CHIP_EN_fun_wp_u	[8]	RW	NA	0	
CHIP_EN_fun_wpdo	[7]	RW	NA	0	
CHIP_EN_fun_sel	[6: 4]	RW	NA	0	
CHIP_EN_slp_wp_u	[3]	RW	NA	0	
CHIP_EN_slp_wpdo	[2]	RW	NA	0	
CHIP_EN_slp_ie	[1]	RW	NA	0	
CHIP_EN_slp_oe	[0]	RW	NA	0	

3.4.2.26 RST_N_REG

0x00000064			RST_N register(0x00008100)															RST_N_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16						
Name	Reserved																					
Type	RO																					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Name	RST_N_bsr_drv		Reserve d	RST_N_bsr_wpus	RST_N_bsr_se	Reserved		RST_N_fun_wpu	RST_N_fun_wpd o	RST_N_fun_sel				RST_N_slp_wpu	RST_N_slp_wpd o	RST_N_slp_ie	RST_N_slp_oe					
Type	RW		RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW					
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RST_N register

Field Name	Bit	Type	Set/Clear	Reset	Description
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				Value	
reserved	[31: 16]	RO	NA	0	
RST_N_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
RST_N_bsr_wpus	[12]	RW	NA	0	
RST_N_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
RST_N_fun_wpu	[8]	RW	NA	0x1	
RST_N_fun_wpdo	[7]	RW	NA	0	
RST_N_fun_sel	[6: 4]	RW	NA	0	
RST_N_slp_wpu	[3]	RW	NA	0	
RST_N_slp_wpdo	[2]	RW	NA	0	
RST_N_slp_ie	[1]	RW	NA	0	
RST_N_slp_oe	[0]	RW	NA	0	

3.4.2.27 WCI_2_RXD_REG

0x00000068		WCI_2_RXD register(0x00008100)															WCI_2_RXD_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	WCI_2_RXD_bsr_drv	Reserve d	WCI_2_RXD_bsr_wpus	WCI_2_RXD_bsr_se	Reserved		WCI_2_RXD_fun_wpu	WCI_2_RXD_fun_wpdo	WCI_2_RXD_fun_sel				WCI_2_RXD_slp_wp_u	WCI_2_RXD_slp_wpdo	WCI_2_RXD_slp_ie	WCI_2_RXD_slp_oe				
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW				
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0				

WCI_2_RXD register

Field Name	Bit	Type	Set/Cle	Reset	Description
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			ar	Value	
reserved	[31: 16]	RO	NA	0	
WCI_2_RXD_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
WCI_2_RXD_bsr_wpus	[12]	RW	NA	0	
WCI_2_RXD_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
WCI_2_RXD_fun_wpu	[8]	RW	NA	0x1	
WCI_2_RXD_fun_wpdo	[7]	RW	NA	0	
WCI_2_RXD_fun_sel	[6: 4]	RW	NA	0	
WCI_2_RXD_slp_wpu	[3]	RW	NA	0	
WCI_2_RXD_slp_wpdo	[2]	RW	NA	0	
WCI_2_RXD_slp_ie	[1]	RW	NA	0	
WCI_2_RXD_slp_oe	[0]	RW	NA	0	

3.4.2.28 WCI_2_TXD_REG

0x00000006C			WCI_2_TXD register(0x00008000)												WCI_2_TXD_REG					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	WCI_2_TXD_bsr_drv	Reserve d	WCI_2_TXD_bsr_wp us	WCI_2_TXD_bsr_se	Reserved			WCI_2_TXD_fun_wpu	WCI_2_TXD_fun_wp do	WCI_2_TXD_fun_sel				WCI_2_TXD_slp_wp u	WCI_2_TXD_slp_wp do	WCI_2_TXD_slp_ie	WCI_2_TXD_slp_oe			
Type	RW	RO	RW	RW	RO			RW	RW	RW				RW	RW	RW	RW			
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

WCI_2_TXD register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
WCI_2_TXD_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
WCI_2_TXD_bsr_wpus	[12]	RW	NA	0	
WCI_2_TXD_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
WCI_2_TXD_fun_wpu	[8]	RW	NA	0	
WCI_2_TXD_fun_wpdo	[7]	RW	NA	0	
WCI_2_TXD_fun_sel	[6: 4]	RW	NA	0	
WCI_2_TXD_slp_wpu	[3]	RW	NA	0	
WCI_2_TXD_slp_wpdo	[2]	RW	NA	0	
WCI_2_TXD_slp_ie	[1]	RW	NA	0	
WCI_2_TXD_slp_oe	[0]	RW	NA	0	

3.4.2.29 U0TXD_REG

0x00000070		U0TXD register(0x00008000)													U0TXD_REG					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	U0TXD_bsr_reserve	UOT_XD	UOT_XD	Reserved		UOT_XD	UOT_XD	U0TXD_fun_sel				UOT_XD	UOT_XD	UOT_XD	UOT_XD					



	drv	d	bsr_wpu_s	bsr_se		fun_wpu	fun_wpd_o		slp_wpu	slp_wpd_o	slp_ie	slp_oe
Type	RW	RO	RW	RW	RO	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0

U0TXD register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
U0TXD_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
U0TXD_bsr_wpus	[12]	RW	NA	0	
U0TXD_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
U0TXD_fun_wpu	[8]	RW	NA	0	
U0TXD_fun_wpdo	[7]	RW	NA	0	
U0TXD_fun_sel	[6: 4]	RW	NA	0	
U0TXD_slp_wpu	[3]	RW	NA	0	
U0TXD_slp_wpdo	[2]	RW	NA	0	
U0TXD_slp_ie	[1]	RW	NA	0	
U0TXD_slp_oe	[0]	RW	NA	0	

3.4.2.30 U0RXD_REG

0x00000074		U0RXD register(0x00008100)													U0RXD_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	Reserved																	
Type	RO																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	U0RXD_bsr_drv	Reserve	U0RXD_bsr	U0RXD_bsr	Reserved		U0RXD_fun	U0RXD_fun	U0RXD_fun_sel			U0RXD_slp	U0RXD_slp	U0RXD_slp_i	U0RXD_slp			

			d	wpu s	se			wpu	wpd o					wpu	wpd o	e	oe
Type	RW		RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

U0RXD register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
U0RXD_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
U0RXD_bsr_wpus	[12]	RW	NA	0	
U0RXD_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
U0RXD_fun_wpu	[8]	RW	NA	0x1	
U0RXD_fun_wpd o	[7]	RW	NA	0	
U0RXD_fun_sel	[6: 4]	RW	NA	0	
U0RXD_slp_wpu	[3]	RW	NA	0	
U0RXD_slp_wpdo	[2]	RW	NA	0	
U0RXD_slp_ie	[1]	RW	NA	0	
U0RXD_slp_oe	[0]	RW	NA	0	

3.4.2.31 U0RTS_REG

0x00000078		U0RTS register(0x00008000)															U0RTS_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	U0RTS_bsr_drv	Reserve	U0RTS_bsr	U0RTS_bsr	Reserved		U0RTS_f un	U0RTS_f un	U0RTS_fun_sel				U0RTS_s lp	U0RTS_s lp	U0RTS_s lp_i	U0RTS_s lp_o				

		d	wpu s	se		wpu	wpd o		wpu	wpd o	e	e
Type	RW	RO	RW	RW	RO	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0

UORTS register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
UORTS_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
UORTS_bsr_wpus	[12]	RW	NA	0	
UORTS_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
UORTS_fun_wpu	[8]	RW	NA	0	
UORTS_fun_wpdo	[7]	RW	NA	0	
UORTS_fun_sel	[6: 4]	RW	NA	0	
UORTS_slp_wpu	[3]	RW	NA	0	
UORTS_slp_wpdo	[2]	RW	NA	0	
UORTS_slp_ie	[1]	RW	NA	0	
UORTS_slp_oe	[0]	RW	NA	0	

3.4.2.32 UOCTS_REG

0x0000007C			UOCTS register(0x00008100)												UOCTS_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	UOCTS_bsr_drv	Reserve d	UOC TS_ bsr_ wpu	UOC TS_ bsr_	Reserved		UOC TS_f un_	UOC TS_f un_	UOCTS_fun_sel				UOC TS_s lp_	UOC TS_s lp_wpd	UOC TS_s lp_i	UOC TS_s lp_o			

			s	se			wpu	o					wpu	o	e	e
Type	RW		RO	RW	RW		RW	RW	RW				RW	RW	RW	RW
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

UOCTS register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
UOCTS_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
UOCTS_bsr_wpus	[12]	RW	NA	0	
UOCTS_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
UOCTS_fun_wpu	[8]	RW	NA	0x1	
UOCTS_fun_wpdo	[7]	RW	NA	0	
UOCTS_fun_sel	[6: 4]	RW	NA	0	
UOCTS_slp_wpu	[3]	RW	NA	0	
UOCTS_slp_wpdo	[2]	RW	NA	0	
UOCTS_slp_ie	[1]	RW	NA	0	
UOCTS_slp_oe	[0]	RW	NA	0	

3.4.2.33 U3TXD_REG

0x00000080				U3TXD register(0x00008000)												U3TXD_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	U3TXD_bsr_drv	Reserve d	U3T XD_bsr_wpu	U3T XD_bsr_se	Reserved		U3T XD_fun_wpu	U3T XD_fun_wpd	U3TXD_fun_sel				U3T XD_slp_wpu	U3T XD_slp_wpd	U3T XD_slp_ie	U3T XD_slp_oe			

			s					o				o			
Type	RW	RO	RW	RW	RO	RO	RW								
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

U3TXD register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
U3TXD_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
U3TXD_bsr_wpus	[12]	RW	NA	0	
U3TXD_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
U3TXD_fun_wpu	[8]	RW	NA	0	
U3TXD_fun_wpdo	[7]	RW	NA	0	
U3TXD_fun_sel	[6: 4]	RW	NA	0	
U3TXD_slp_wpu	[3]	RW	NA	0	
U3TXD_slp_wpdo	[2]	RW	NA	0	
U3TXD_slp_ie	[1]	RW	NA	0	
U3TXD_slp_oe	[0]	RW	NA	0	

3.4.2.34 U3RXD_REG

0x00000084		U3RXD register(0x00008100)													U3RXD_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	U3RXD_bsr_drv	Reserve d	U3R XD_bsr_wpu	U3R XD_bsr_se	Reserved		U3R XD_fun_wpu	U3R XD_fun_wpd	U3RXD_fun_sel				U3R XD_slp_wpu	U3R XD_slp_wpd	U3R XD_slp_ie	U3R XD_slp_oe			



			s					o				o			
Type	RW	RO	RW	RW	RO	RO	RW								
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

U3RXD register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
U3RXD_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
U3RXD_bsr_wpus	[12]	RW	NA	0	
U3RXD_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
U3RXD_fun_wpu	[8]	RW	NA	0x1	
U3RXD_fun_wpd0	[7]	RW	NA	0	
U3RXD_fun_sel	[6: 4]	RW	NA	0	
U3RXD_slp_wpu	[3]	RW	NA	0	
U3RXD_slp_wpdo	[2]	RW	NA	0	
U3RXD_slp_ie	[1]	RW	NA	0	
U3RXD_slp_oe	[0]	RW	NA	0	

3.4.2.35 RFCTL0_REG

0x00000088				RFCTL0 register(0x000080B0)												RFCTL0_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	RFCTL0_bsr_drv	Reserve d	RFC TLO _bsr _wp	RFC TLO _bsr	Reserved		RFC TLO _fun _wp	RFC TLO _fun _wp	RFCTL0_fun_sel				RFC TLO _slp _wp	RFC TLO _slp _wp	RFC TLO _slp	RFC TLO _slp			

			us	_se			u	do				u	do	_ie	_oe
Type	RW		RO	RW	RW		RW	RW	RW			RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0

RFCTL0 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RFCTL0_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
RFCTL0_bsr_wpus	[12]	RW	NA	0	
RFCTL0_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
RFCTL0_fun_wpu	[8]	RW	NA	0	
RFCTL0_fun_wpd0	[7]	RW	NA	0x1	
RFCTL0_fun_sel	[6: 4]	RW	NA	0x3	
RFCTL0_slp_wpu	[3]	RW	NA	0	
RFCTL0_slp_wpdo	[2]	RW	NA	0	
RFCTL0_slp_ie	[1]	RW	NA	0	
RFCTL0_slp_oe	[0]	RW	NA	0	

3.4.2.36 RFCTL1_REG

0x0000008C			RFCTL1 register(0x000080B0)												RFCTL1_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	RFCTL1_bsr_drv	RFC TL1_bsr_wp	Reserve d	RFC TL1_bsr	Reserved		RFC TL1_fun_wp	RFC TL1_fun_wp	RFCTL1_fun_sel			RFC TL1_slp_wp	RFC TL1_slp_wp	RFC TL1_slp	RFC TL1_slp				



			us		_se			u	do				u	do	_ie	_oe
Type	RW		RW	RO	RW	RO		RW	RW	RW			RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0

RFCTL1 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RFCTL1_bsr_drv	[15: 14]	RW	NA	0x2	
RFCTL1_bsr_wpus	[12]	RW	NA	0	
reserved	[13]	RO	NA	0	
RFCTL1_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
RFCTL1_fun_wpu	[8]	RW	NA	0	
RFCTL1_fun_wpd0	[7]	RW	NA	0x1	
RFCTL1_fun_sel	[6: 4]	RW	NA	0x3	
RFCTL1_slp_wpu	[3]	RW	NA	0	
RFCTL1_slp_wpdo	[2]	RW	NA	0	
RFCTL1_slp_ie	[1]	RW	NA	0	
RFCTL1_slp_oe	[0]	RW	NA	0	

3.4.2.37 RFCTL2_REG

0x00000090			RFCTL2 register(0x000080B0)												RFCTL2_REG					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	RFCTL2_bsr_drv	Reserve d	RFC TL2_bsr_wp	RFC TL2_bsr	Reserved		RFC TL2_fun_wp	RFC TL2_fun_wp	RFCTL2_fun_sel				RFC TL2_slp_wp	RFC TL2_slp	RFC TL2_slp	RFC TL2_slp				



			us	_se			u	do				u	do	_ie	_oe
Type	RW		RO	RW	RW		RW	RW	RW			RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0

RFCTL2 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RFCTL2_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
RFCTL2_bsr_wpus	[12]	RW	NA	0	
RFCTL2_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
RFCTL2_fun_wpu	[8]	RW	NA	0	
RFCTL2_fun_wpd0	[7]	RW	NA	0x1	
RFCTL2_fun_sel	[6: 4]	RW	NA	0x3	
RFCTL2_slp_wpu	[3]	RW	NA	0	
RFCTL2_slp_wpdo	[2]	RW	NA	0	
RFCTL2_slp_ie	[1]	RW	NA	0	
RFCTL2_slp_oe	[0]	RW	NA	0	

3.4.2.38 RFCTL3_REG

0x00000094			RFCTL3 register(0x000080B0)												RFCTL3_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	RFCTL3_bsr_drv	Reserve d	RFC TL3 _bsr _wp	RFC TL3 _bsr _bsr	Reserved		RFC TL3 _fun _wp	RFC TL3 _fun _wp	RFCTL3_fun_sel			RFC TL3 _slp _wp							



			us	_se			u	do				u	do	_ie	_oe
Type	RW		RO	RW	RW		RW	RW	RW			RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0

RFCTL3 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RFCTL3_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
RFCTL3_bsr_wpus	[12]	RW	NA	0	
RFCTL3_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
RFCTL3_fun_wpu	[8]	RW	NA	0	
RFCTL3_fun_wpd0	[7]	RW	NA	0x1	
RFCTL3_fun_sel	[6: 4]	RW	NA	0x3	
RFCTL3_slp_wpu	[3]	RW	NA	0	
RFCTL3_slp_wpdo	[2]	RW	NA	0	
RFCTL3_slp_ie	[1]	RW	NA	0	
RFCTL3_slp_oe	[0]	RW	NA	0	

3.4.2.39 RFCTL4_REG

0x00000098			RFCTL4 register(0x000080B0)												RFCTL4_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	RFCTL4_bsr_drv	Reserve d	RFC TL4 _bsr_wp	RFC TL4 _bsr	Reserved		RFC TL4 _fun_wp	RFC TL4 _fun_wp	RFCTL4_fun_sel				RFC TL4 _slp_wp	RFC TL4 _slp_wp	RFC TL4 _slp	RFC TL4 _slp			

			us	_se			u	do				u	do	_ie	_oe
Type	RW		RO	RW	RW		RW	RW	RW			RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0

RFCTL4 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RFCTL4_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
RFCTL4_bsr_wpus	[12]	RW	NA	0	
RFCTL4_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
RFCTL4_fun_wpu	[8]	RW	NA	0	
RFCTL4_fun_wpd0	[7]	RW	NA	0x1	
RFCTL4_fun_sel	[6: 4]	RW	NA	0x3	
RFCTL4_slp_wpu	[3]	RW	NA	0	
RFCTL4_slp_wpdo	[2]	RW	NA	0	
RFCTL4_slp_ie	[1]	RW	NA	0	
RFCTL4_slp_oe	[0]	RW	NA	0	

3.4.2.40 RFCTL5_REG

0x0000009C			RFCTL5 register(0x000080B0)												RFCTL5_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	RFCTL5_bsr_drv	Reserve d	RFC TLS	RFC TLS	RFC TLS	Reserved		RFC TLS	RFC TLS	RFCTL5_fun_sel			RFC TLS	RFC TLS	RFC TLS	RFC TLS			



			us	_se			u	do				u	do	_ie	_oe
Type	RW		RO	RW	RW		RW	RW	RW			RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0

RFCTL5 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RFCTL5_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
RFCTL5_bsr_wpus	[12]	RW	NA	0	
RFCTL5_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
RFCTL5_fun_wpu	[8]	RW	NA	0	
RFCTL5_fun_wpd0	[7]	RW	NA	0x1	
RFCTL5_fun_sel	[6: 4]	RW	NA	0x3	
RFCTL5_slp_wpu	[3]	RW	NA	0	
RFCTL5_slp_wpdo	[2]	RW	NA	0	
RFCTL5_slp_ie	[1]	RW	NA	0	
RFCTL5_slp_oe	[0]	RW	NA	0	

3.4.2.41 RFCTL6_REG

0x000000A0			RFCTL6 register(0x000080B0)												RFCTL6_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	RFCTL6_bsr_drv		Reserve d	RFC TL6_bsr_wp	RFC TL6_bsr	Reserved		RFC TL6_fun_wp	RFC TL6_fun_wp	RFCTL6_fun_sel			RFC TL6_slp_wp	RFC TL6_slp	RFC TL6_slp	RFC TL6_slp			



			us	_se			u	do				u	do	_ie	_oe
Type	RW		RO	RW	RW		RW	RW	RW			RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0

RFCTL6 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RFCTL6_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
RFCTL6_bsr_wpus	[12]	RW	NA	0	
RFCTL6_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
RFCTL6_fun_wpu	[8]	RW	NA	0	
RFCTL6_fun_wpd0	[7]	RW	NA	0x1	
RFCTL6_fun_sel	[6: 4]	RW	NA	0x3	
RFCTL6_slp_wpu	[3]	RW	NA	0	
RFCTL6_slp_wpdo	[2]	RW	NA	0	
RFCTL6_slp_ie	[1]	RW	NA	0	
RFCTL6_slp_oe	[0]	RW	NA	0	

3.4.2.42 RFCTL7_REG

0x000000A4			RFCTL7 register(0x000080B0)												RFCTL7_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	RFCTL7_bsr_drv	Reserve d	RFC TL7_bsr_wp	RFC TL7_bsr	Reserved		RFC TL7_fun_wp	RFC TL7_fun	RFCTL7_fun_sel			RFC TL7_slp_wp	RFC TL7_slp	RFC TL7_slp	RFC TL7_slp				

			us	_se			u	do				u	do	_ie	_oe
Type	RW		RO	RW	RO		RW	RW	RW			RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0

RFCTL7 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RFCTL7_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
RFCTL7_bsr_wpus	[12]	RW	NA	0	
RFCTL7_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
RFCTL7_fun_wpu	[8]	RW	NA	0	
RFCTL7_fun_wpd0	[7]	RW	NA	0x1	
RFCTL7_fun_sel	[6: 4]	RW	NA	0x3	
RFCTL7_slp_wpu	[3]	RW	NA	0	
RFCTL7_slp_wpdo	[2]	RW	NA	0	
RFCTL7_slp_ie	[1]	RW	NA	0	
RFCTL7_slp_oe	[0]	RW	NA	0	

3.4.2.43 SD_D3_REG

0x000000A8			SD_D3 register(0x00008100)												SD_D3_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	Reserved																SD_D3_bsr_drv	
Type	RO																RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Name	SD_D3_bsr_drv	Reserve d	SD_D3_bsr_wpu s	SD_D3_bsr_se	Reserved	SD_D3_fun_wpu	SD_D3_fun_wpdo	SD_D3_fun_sel	SD_D3_slp_wpu	SD_D3_slp_wpdo	SD_D3_slp_ie	SD_D3_slp_oe
Type	RW	RO	RW	RW	RO	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	1	0	0	0	0	0

SD_D3 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 17]	RO	NA	0	
SD_D3_bsr_drv	[16: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
SD_D3_bsr_wpus	[12]	RW	NA	0	
SD_D3_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
SD_D3_fun_wpu	[8]	RW	NA	0x1	
SD_D3_fun_wpdo	[7]	RW	NA	0	
SD_D3_fun_sel	[6: 4]	RW	NA	0	
SD_D3_slp_wpu	[3]	RW	NA	0	
SD_D3_slp_wpdo	[2]	RW	NA	0	
SD_D3_slp_ie	[1]	RW	NA	0	
SD_D3_slp_oe	[0]	RW	NA	0	

3.4.2.44 SD_D2_REG

0x000000AC			SD_D2 register(0x000008100)												SD_D2_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	Reserved																SD_D2_bsr_drv	
Type	RO																RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	



Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_D2_bsr_drv	Reserved	SD_D2_bsr_wpus	SD_D2_bsr_se	Reserved		SD_D2_fun_wpu	SD_D2_fun_wpdo	SD_D2_fun_sel			SD_D2_slp_wpu	SD_D2_slp_o	SD_D2_slp_ie	SD_D2_slp_oe	
Type	RW	RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW	
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

SD_D2 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 17]	RO	NA	0	
SD_D2_bsr_drv	[16: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
SD_D2_bsr_wpus	[12]	RW	NA	0	
SD_D2_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
SD_D2_fun_wpu	[8]	RW	NA	0x1	
SD_D2_fun_wpdo	[7]	RW	NA	0	
SD_D2_fun_sel	[6: 4]	RW	NA	0	
SD_D2_slp_wpu	[3]	RW	NA	0	
SD_D2_slp_wpdo	[2]	RW	NA	0	
SD_D2_slp_ie	[1]	RW	NA	0	
SD_D2_slp_oe	[0]	RW	NA	0	

3.4.2.45 SD_D1_REG

0x000000B0				SD_D1 register(0x000008100)												SD_D1_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved															SD_D1_bsr_drv				
Type	RO															RW				



Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	SD_D1_bsr_drv	Reserve d	SD_D1_bsr_wpu s	SD_D1_bsr_se	Reserved	SD_D1_fun_wpu	SD_D1_fun_wpdo	SD_D1_fun_sel	SD_D1_slp_wpu	SD_D1_slp_wpdo	SD_D1_slp_ie	SD_D1_slp_oe					
Type	RW	RO	RW	RW	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	

SD_D1 register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 17]	RO	NA	0	
SD_D1_bsr_drv	[16: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
SD_D1_bsr_wpus	[12]	RW	NA	0	
SD_D1_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
SD_D1_fun_wpu	[8]	RW	NA	0x1	
SD_D1_fun_wpdo	[7]	RW	NA	0	
SD_D1_fun_sel	[6: 4]	RW	NA	0	
SD_D1_slp_wpu	[3]	RW	NA	0	
SD_D1_slp_wpdo	[2]	RW	NA	0	
SD_D1_slp_ie	[1]	RW	NA	0	
SD_D1_slp_oe	[0]	RW	NA	0	

3.4.2.46 SD_D0_REG

0x000000B4				SD_D0 register(0x000008100)												SD_D0_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved												SD_D0_bsr_drv						



Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_D0_bsr_drv	Reserve d	SD_D0_bsr_wpu s	SD_D0_bsr_se	Reserved		SD_D0_fun_wpu	SD_D0_fun_wpdo	SD_D0_fun_sel		SD_D0_slp_wpu	SD_D0_slp_wpdo	SD_D0_slp_ie	SD_D0_slp_oe		
Type	RW		RO	RW	RW	RO		RW	RW	RW		RW	RW	RW	RW	
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

SD_D0 register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 17]	RO	NA	0	
SD_D0_bsr_drv	[16: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
SD_D0_bsr_wpus	[12]	RW	NA	0	
SD_D0_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
SD_D0_fun_wpu	[8]	RW	NA	0x1	
SD_D0_fun_wpdo	[7]	RW	NA	0	
SD_D0_fun_sel	[6: 4]	RW	NA	0	
SD_D0_slp_wpu	[3]	RW	NA	0	
SD_D0_slp_wpdo	[2]	RW	NA	0	
SD_D0_slp_ie	[1]	RW	NA	0	
SD_D0_slp_oe	[0]	RW	NA	0	

3.4.2.47 SD_CLK_REG

0x000000B8				SD_CLK register(0x00008080)											SD_CLK_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	Reserved													SD_CLK_bsr				

																	_drv
Type	RO																RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	SD_CLK_bsr_drv	Reserve d	SD_CLK_bsr_wpus	SD_CLK_bsr_se	Reserved		SD_CLK_fun_wpu	SD_CLK_fun_wpd0	SD_CLK_fun_sel			SD_CLK_slp_wpu	SD_CLK_slp_wpd0	SD_CLK_slp_ie	SD_CLK_slp_oe		
Type	RW	RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW		
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	

SD_CLK register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 17]	RO	NA	0	
SD_CLK_bsr_drv	[16: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
SD_CLK_bsr_wpus	[12]	RW	NA	0	
SD_CLK_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
SD_CLK_fun_wpu	[8]	RW	NA	0	
SD_CLK_fun_wpd0	[7]	RW	NA	0x1	
SD_CLK_fun_sel	[6: 4]	RW	NA	0	
SD_CLK_slp_wpu	[3]	RW	NA	0	
SD_CLK_slp_wpd0	[2]	RW	NA	0	
SD_CLK_slp_ie	[1]	RW	NA	0	
SD_CLK_slp_oe	[0]	RW	NA	0	

3.4.2.48 SD_CMD_REG

0x000000BC	SD_CMD register(0x00008100)	SD_CMD_REG
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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															SD_CM_D_b_sr_d_rv
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_CMD_bs_r_drv	Reserve d	SD_CM_D_b_sr_wpu s	SD_CM_D_b_sr_se	Reserved		SD_CM_D_f un_wpu	SD_CM_D_f un_wpd o	SD_CMD_fun_sel			SD_CM_D_sl_p_w pu	SD_CM_D_sl_p_w pdo	SD_CM_D_sl_p_ie	SD_CM_D_sl_p_o e	
Type	RW		RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

SD_CMD register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 17]	RO	NA	0	
SD_CMD_bsr_drv	[16: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
SD_CMD_bsr_wp_us	[12]	RW	NA	0	
SD_CMD_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
SD_CMD_fun_wp_u	[8]	RW	NA	0x1	
SD_CMD_fun_wp_do	[7]	RW	NA	0	
SD_CMD_fun_sel	[6: 4]	RW	NA	0	
SD_CMD_slp_wp_u	[3]	RW	NA	0	
SD_CMD_slp_wp_do	[2]	RW	NA	0	
SD_CMD_slp_ie	[1]	RW	NA	0	

SD_CMD_slp_oe	[0]	RW	NA	0	
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3.4.2.49 GNSS_LNA_EN_REG

0x000000C0				GNSS_LNA_EN register(0x00008130)												GNSS_LNA_EN_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	GNSS_LNA_EN_bsr_drv	Reserve d	GNS_S_L_NA_EN_bsr_wpus	GNS_S_L_NA_EN_bsr_se	Reserved		GNS_S_L_NA_EN_fun_wpu	GNS_S_L_NA_EN_fun_wpdo	GNSS_LNA_EN_funsel				GNS_S_L_NA_EN_slp_wpu	GNS_S_L_NA_EN_slp_wpdo	GNS_S_L_NA_EN_slp_ie	GNS_S_L_NA_EN_slp_oe				
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW				
Reset	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0				

GNSS_LNA_EN register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
GNSS_LNA_EN_bs_r_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
GNSS_LNA_EN_bs_r_wpus	[12]	RW	NA	0	
GNSS_LNA_EN_bs_r_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
GNSS_LNA_EN_fu_n_wpu	[8]	RW	NA	0x1	
GNSS_LNA_EN_fu_n_wpdo	[7]	RW	NA	0	
GNSS_LNA_EN_fu_n_sel	[6: 4]	RW	NA	0x3	

GNSS_LNA_EN_si p_wpu	[3]	RW	NA	0	
GNSS_LNA_EN_si p_wpdo	[2]	RW	NA	0	
GNSS_LNA_EN_si p_ie	[1]	RW	NA	0	
GNSS_LNA_EN_si p_oe	[0]	RW	NA	0	

3.4.2.50 U1TXD_REG

0x000000C4				U1TXD register(0x00008000)												U1TXD_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	U1TXD_bsr_drv	Reserve d	U1T XD_bsr_wpus	U1T XD_bsr_se	Reserved		U1T XD_fun_wpu	U1T XD_fun_wpdo	U1TXD_fun_sel				U1T XD_slp_wpu	U1T XD_slp_wpdo	U1T XD_slp_ie	U1T XD_slp_oe				
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW				
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

U1TXD register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
U1TXD_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
U1TXD_bsr_wpus	[12]	RW	NA	0	
U1TXD_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
U1TXD_fun_wpu	[8]	RW	NA	0	
U1TXD_fun_wpdo	[7]	RW	NA	0	

U1TXD_fun_sel	[6: 4]	RW	NA	0	
U1TXD_slp_wpu	[3]	RW	NA	0	
U1TXD_slp_wpdo	[2]	RW	NA	0	
U1TXD_slp_ie	[1]	RW	NA	0	
U1TXD_slp_oe	[0]	RW	NA	0	

3.4.2.51 U1RXD_REG

0x000000C8			U1RXD register(0x00008100)												U1RXD_REG				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	U1RXD_bsr_drv	Reserve d	U1R XD_bsr_wpus	U1R XD_bsr_se	Reserved		U1R XD_fun_wpu	U1R XD_fun_wpd o	U1RXD_fun_sel			U1R XD_slp_wpu	U1R XD_slp_wpd o	U1R XD_slp_ie	U1R XD_slp_oe				
Type	RW		RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW			
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0			

U1RXD register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
U1RXD_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
U1RXD_bsr_wpus	[12]	RW	NA	0	
U1RXD_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
U1RXD_fun_wpu	[8]	RW	NA	0x1	
U1RXD_fun_wpd o	[7]	RW	NA	0	

U1RXD_fun_sel	[6: 4]	RW	NA	0	
U1RXD_slp_wpu	[3]	RW	NA	0	
U1RXD_slp_wpdo	[2]	RW	NA	0	
U1RXD_slp_ie	[1]	RW	NA	0	
U1RXD_slp_oe	[0]	RW	NA	0	

3.4.2.52 U1RTS_REG

0x0000000CC			U1RTS register(0x00008000)												U1RTS_REG					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	U1RTS_bsr_drv	Reserve d	U1R TS_bsr_wpus	U1R TS_bsr_se	Reserved		U1R TS_f un_wpu	U1R TS_f un_wpdo	U1RTS_fun_sel			U1R TS_s lp_wpu	U1R TS_s lp_wpdo	U1R TS_s lp_i e	U1R TS_s lp_o e					
Type	RW		RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW				
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

U1RTS register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
U1RTS_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
U1RTS_bsr_wpus	[12]	RW	NA	0	
U1RTS_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
U1RTS_fun_wpu	[8]	RW	NA	0	
U1RTS_fun_wpdo	[7]	RW	NA	0	

U1RTS_fun_sel	[6: 4]	RW	NA	0	
U1RTS_slp_wpu	[3]	RW	NA	0	
U1RTS_slp_wpdo	[2]	RW	NA	0	
U1RTS_slp_ie	[1]	RW	NA	0	
U1RTS_slp_oe	[0]	RW	NA	0	

3.4.2.53 U1CTS_REG

0x000000D0			U1CTS register(0x00008100)												U1CTS_REG					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	U1CTS_bsr_drv	Reserve d	U1CTS_bsr_wpus	U1CTS_bsr_se	Reserved		U1CTS_ts_f un_wpu	U1CTS_ts_f un_wpd o	U1CTS_fun_sel			U1CTS_ts_lp_wpu	U1CTS_ts_lp_wpd o	U1CTS_ts_lp_i e	U1CTS_ts_lp_o e	U1CTS_ts_lp_o e				
Type	RW	RO	RW	RW	RO		RW	RW	RW			RW	RW	RW	RW	RW	RW			
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0			

U1CTS register

Field Name	Bit	Type	Set/Cle ar	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
U1CTS_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
U1CTS_bsr_wpus	[12]	RW	NA	0	
U1CTS_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
U1CTS_fun_wpu	[8]	RW	NA	0x1	
U1CTS_fun_wpdo	[7]	RW	NA	0	

U1CTS_fun_sel	[6: 4]	RW	NA	0	
U1CTS_slp_wpu	[3]	RW	NA	0	
U1CTS_slp_wpdo	[2]	RW	NA	0	
U1CTS_slp_ie	[1]	RW	NA	0	
U1CTS_slp_oe	[0]	RW	NA	0	

3.4.2.54 PCIE_CLKREQ_L_REG

0x000000D4		PCIE_CLKREQ_L register(0x00008100)												PCIE_CLKREQ_L_REG					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	Reserved																		
Type	RO																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	PCIE_CLKREQ_L_bsr_drv	Reserve d	PCIE_CLKREQ_L_bsr																
Type	RW	RO	RW	RW	RO	RW													
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0		

PCIE_CLKREQ_L register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
PCIE_CLKREQ_L_bsr_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
PCIE_CLKREQ_L_bsr_wpus	[12]	RW	NA	0	
PCIE_CLKREQ_L_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	

PCIE_CLKREQ_L_f un_wpu	[8]	RW	NA	0x1	
PCIE_CLKREQ_L_f un_wpdo	[7]	RW	NA	0	
PCIE_CLKREQ_L_f un_sel	[6: 4]	RW	NA	0	
PCIE_CLKREQ_L_s lp_wpu	[3]	RW	NA	0	
PCIE_CLKREQ_L_s lp_wpdo	[2]	RW	NA	0	
PCIE_CLKREQ_L_s lp_ie	[1]	RW	NA	0	
PCIE_CLKREQ_L_s lp_oe	[0]	RW	NA	0	

3.4.2.55 PCIE_RST_L_REG

0x000000D8				PCIE_RST_L register(0x00008080)												PCIE_RST_L_REG								
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16								
Name	Reserved																							
Type	RO																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Name	PCIE_RST_L_bsr_drv	Reserve d	PCIE_RS_T_L_bsr_wpus	PCIE_RS_T_L_bsr_se	Reserved		PCIE_RS_T_L_fun_wpu	PCIE_RS_T_L_fun_wpdo	PCIE_RST_L_fun_sel				PCIE_RS_T_L_slp_wpu	PCIE_RS_T_L_slp_wpdo	PCIE_RS_T_L_slp_ie	PCIE_RS_T_L_slp_oe								
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW								
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0								

PCIE_RST_L register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
PCIE_RST_L_bsr_drv	[15: 14]	RW	NA	0x2	

reserved	[13]	RO	NA	0	
PCIE_RST_L_bsr_wpus	[12]	RW	NA	0	
PCIE_RST_L_bsr_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
PCIE_RST_L_fun_wpu	[8]	RW	NA	0	
PCIE_RST_L_fun_wpdo	[7]	RW	NA	0x1	
PCIE_RST_L_fun_sel	[6: 4]	RW	NA	0	
PCIE_RST_L_slp_wpu	[3]	RW	NA	0	
PCIE_RST_L_slp_wpdo	[2]	RW	NA	0	
PCIE_RST_L_slp_ie	[1]	RW	NA	0	
PCIE_RST_L_slp_oe	[0]	RW	NA	0	

3.4.2.56 PCIE_WAKE_L_REG

0x0000000DC		PCIE_WAKE_L register(0x00008100)															PCIE_WAKE_L_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Reserved																			
Type	RO																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	PCIE_WAKE_L_bsr_drv	Reserve d	PCIE_WAKE_L_bsr_wpus	PCIE_WAKE_L_bsr_se	Reserved		PCIE_WAKE_L_fun_wpu	PCIE_WAKE_L_fun_wpdo	PCIE_WAKE_L_fun_sel				PCIE_WAKE_L_slp_wpu	PCIE_WAKE_L_slp_wpdo	PCIE_WAKE_L_slp_ie	PCIE_WAKE_L_slp_oe				
Type	RW	RO	RW	RW	RO		RW	RW	RW				RW	RW	RW	RW				
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0				

PCIE_WAKE_L register

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
PCIE_WAKE_L_bs_r_drv	[15: 14]	RW	NA	0x2	
reserved	[13]	RO	NA	0	
PCIE_WAKE_L_bs_r_wpus	[12]	RW	NA	0	
PCIE_WAKE_L_bs_r_se	[11]	RW	NA	0	
reserved	[10: 9]	RO	NA	0	
PCIE_WAKE_L_fu_n_wpu	[8]	RW	NA	0x1	
PCIE_WAKE_L_fu_n_wpdo	[7]	RW	NA	0	
PCIE_WAKE_L_fu_n_set	[6: 4]	RW	NA	0	
PCIE_WAKE_L_slp_wpu	[3]	RW	NA	0	
PCIE_WAKE_L_slp_wpdo	[2]	RW	NA	0	
PCIE_WAKE_L_slp_ie	[1]	RW	NA	0	
PCIE_WAKE_L_slp_oe	[0]	RW	NA	0	

3.5 Strapping Pins

Cell Name	Substrate Name	Power	Strapping pin
SPSCBC2_8X_HL	RF_CTL5	VIO1V8	arm_boot_md0
SPSCBC2_8X_HL	RF_CTL6	VIO1V8	arm_boot_md1
SPSCBC2_8X_HL	RF_CTL7	VIO1V8	arm_boot_md2

3.6 PAD Information

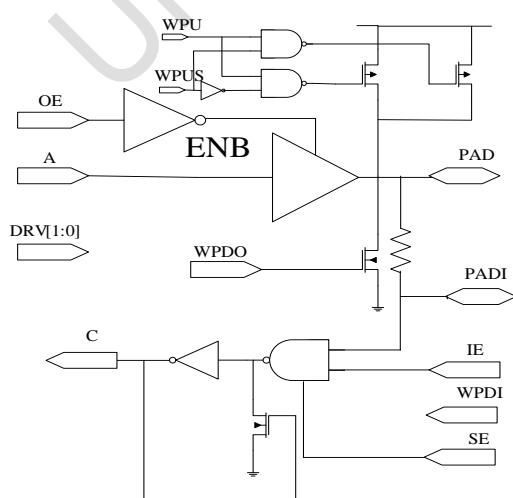
Digital Pad Type Description

Table 3-7 Digital Pad Type Description

Pin Type	Description
SPSCBC2_8X_VL/HL	Bi-direction Pad with Enable Controlled Pull-Down & Pull-Up Resistor. Programmable Driver Strength 2mA/4mA/6mA/8mA. No tolerance function. The Schmitt trigger input function can be control by the SE signal. SE=1, Schmitt input enable. SE=0 Schmitt input disable. Programmable soft pull up resistor 20K/4.7K.
SPSCBC2_24X_VL/HL	Bi-direction Pad with Enable Controlled Pull-Down & Pull-Up Resistor. Programmable Driver Strength. No tolerance function. The Schmitt trigger input function can be control by the SE signal. SE=1, Schmitt input enable. SE=0 Schmitt input disable.

SPSCBC2_8X

Bi-direction Pad with Enable Controlled Pull-Down & Pull-Up Resistor. Programmable Driver Strength. No tolerance function. The Schmitt trigger input function can be control by the SE signal. SE=1, Schmitt input enable. SE=0 Schmitt input disable.



Area:

28umX85um

Pin Name:

Pin Name	Description
VDD	Core Power Supply.
VSS	Core Ground Supply.
VDDIO	IO post driver Power Supply.
VSSIO	IO post driver Ground Supply.
WPDO	Soft Pull-Down Enable, Active=1
WPDI	In 40nm process, Input VDDIO/VDD interface note pull-down enable. Active=1. When VDDIO power down and Core VDD power on, set WPDI=1 to prevent leakage current caused by the floating node. But in 28nm process ,it not for use ,the pin floating.
WPU	Soft Pull-Up Enable, Active=1
WPUS	Soft Pull-Up select signa.0 for big res, and 1 for small res.
A	Input pin
PAD	Bonding PAD pin
PADI	PAD signal after the second protection resistor. Can be used for analog signal.
C	Output pin
DRV[1]	Driver Strength Select pin, 1bit
DRV[0]	Driver Strength Select pin, 0 bit
OE	Output Enable, Active=1
IE	Input Enable, Active=1
SE	Schmitt trigger Input Enable, Active=1

Truth Table: Input function C=PAD&IE, Output function: PAD=A&OE

	A	PAD	C	IE	OE	WPU	WPUS	WPDO	WPDI
Input	X	0	0	1	0	0	X	0	0
	X	1	1	1	0	0	X	0	0
Output	0	0	0	0	1	0	X	0	0
	1	1	0	0	1	0	X	0	0
Inout	0	0	0	1	1	0	X	0	0
	1	1	1	1	1	0	X	0	0
Tri State	X	HZ	0	0	0	0	X	0	0
	X	HZ	0	0	0	0	X	0	0
Pull up	X	1	0	0	0	1	0: 20K(1.8V) 1:4.7K(1. 8V)	0	0
Pull Down	X	0	0	0	0	0	X	1	0
IO Power-down	X	X	1	X	X	X	X	X	1

Driver Strength Select Function:

DRV[1]	DRV[0]	
0	0	2mA
0	1	4mA
1	0	6mA
1	1	8mA

DC Parameter:

		SS	TT	FF
--	--	----	----	----

V_{T+}	Schmitt trig. Low to High threshold point (1.2V)	X	0.80V	X
V_{T-}	Schmitt trig. High to low threshold point (1.2V)	X	0.39V	X
V_{T+}	Schmitt trig. Low to High threshold point (1.8V)	X	1.20V	X
V_{T-}	Schmitt trig. High to low threshold point (1.8V)	X	0.64V	X
RPU	Pull-up resistor(1.8V)	30K/6K	22K/4.6K	16K/3.5K
RPD	Pull-down resistor(1.8V)	30K	40K	60K
Iavg	Active Current@100MHZ,FF Corner,30pf loading	X	X	4mA
Ist	Standby Current	X	X	<0.1uA
IoZ	Tri-state output leakage current @Vo=3V or 0V	X	X	<0.1uA

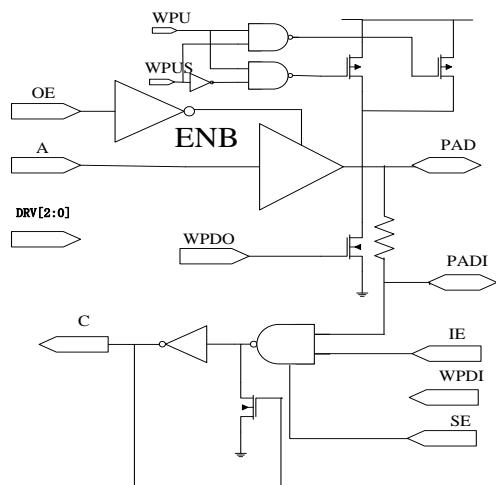
AC Parameter:

The data simulation is SS corner, Cloading=0.3pf, Cpad=30pf/15pf, VDDIO=1.8V, Temp=125C,

Delay Path		Rise Time(ns)	Fall Time(ns)	Rise Delay(ns)	Fall Delay(ns)
PAD->C		0.193	0.198	0.437	0.327
A-PAD	2mA	4.911	4.766	3.379	3.54
	4mA	2.569	2.491	2.452	2.51
	6mA	1.829	1.778	2.168	2.193
	8mA	2.609	2.548	2.491	2.521

SPSCBC2_24X

Bi-direction Pad with Enable Controlled Pull-Down & Pull-Up Resistor.Programmable Driver Strength.
No tolerance function.The Schmitt trigger input function can be control by the SE signal.SE=1,
Schmitt input enable.SE=0 Schmitt input disable.Using for EMMC/SD interface(VDDIO=1.2V/1.8V).



Area:

40umX85um

Pin Name:

Pin Name	Description
VDD	Core Power Supply.
VSS	Core Ground Supply.
VDDIO	IO post driver Power Supply.
VSSIO	IO post driver Ground Supply.
WPDO	Soft Pull-Down Enable, Active=1
WPDI	In 40nm process, Input VDDIO/VDD interface note pull-down enable. Active=1. When VDDIO power down and Core VDD power on, set WPDI=1 to prevent leakage current caused by the floating node. But in 28nm process ,it not for use ,the pin floating.
WPU	Soft Pull-Up Enable, Active=1
WPUS	Soft Pull-Up select signa.0 for big res, and 1 for small res.
A	Input pin
PAD	Bonding PAD pin
C	Output pin
DRV[2]	Driver Strength Select pin, bit2

DRV[1]	Driver Strength Select pin, bit1
DRV[0]	Driver Strength Select pin, bit0
OE	Output Enable, Active=1
IE	Input Enable, Active=1
SE	Schmitt trigger Input Enable, Active=1

Truth Table: Input function C=PAD&IE, Output function:PAD=A&OE

	A	PAD	C	IE	OE	WPU	WPUS	WP DO	WPDI
Input	X	0	0	1	0	0	X	0	0
	X	1	1	1	0	0	X	0	0
Output	0	0	0	0	1	0	X	0	0
	1	1	0	0	1	0	X	0	0
Inout	0	0	0	1	1	0	X	0	0
	1	1	1	1	1	0	X	0	0
Tri State	X	HZ	0	0	0	0	X	0	0
	X	HZ	0	0	0	0	X	0	0
Pull up	X	1	0	0	0	1	0: 20K(1.8V) 1:4.7K(1.8V)	0	0
Pull Down	X	0	0	0	0	0	X	1	0
IO Power-down	X	X	1	X	X	X	X	X	1

When the VDDIO=1.8V: **SS@125C**



DRV[2]	DRV[1]	DRV[0]	Nominal Id@0.5*VDDIO	Nominal Impedance@0.5*VDDIO	Note
0	0	0	4.5mA	200ohm	Option
0	0	1	9mA	100ohm	Option
0	1	0	13.6mA	66ohm	Option
0	1	1	18mA	50ohm	Mandatory
1	0	0	22.5mA	40ohm	Option
1	0	1	27.2mA	33ohm	Option
1	1	0	32mA	28ohm	Option
1	1	1	39.2mA	23ohm	Option

DC Parameter:

		SS	TT	FF
V _{T+}	Schmitt trig. Low to High threshold point (1.2V)	X	0.80V	X
V _{T-}	Schmitt trig. High to low threshold point (1.2V)	X	0.39V	X
V _{T+}	Schmitt trig. Low to High threshold point (1.8V)	X	1.20V	X
V _{T-}	Schmitt trig. High to low threshold point (1.8V)	X	0.64V	X
RPU	Pull-up resistor(1.8V)	30K/6K	22K/4.6K	16K/3.5K
RPD	Pull-down resistor(1.8V)	30K	40K	60K
Iavg	Active Current@208MHZ,FF Corner,15pf loading	X	X	13mA
Ist	Standby Current	X	X	<0.1uA
IoZ	Tri-state output leakage current @Vo=1.8V or 0V	X	X	<0.1uA

AC Parameter:

When VDDIO=1.8V ,

The data simulation is SS corner, clk=208MHz, Cloading=0.2pf, post simulation data.

, VDDIO=1.8, Temp=125C, Rise time and falling time are based in (10%~90%)VDD/VDDIO.

Delay Path		Cpad	Rise Time(ns)	Fall Time(ns)	Rise Delay(ns)	Fall Delay(ns)
PAD->C			0.15	0.19	0.61	0.40
A-PAD	100ohm	3pF	1.34	1.51	1.42	1.59
	66ohm	5pF	1.29	1.46	1.42	1.59
	50ohm	8pF	1.41	1.60	1.46	1.65
	40ohm	10pF	1.15	1.31	1.55	1.55
	33ohm	15pF	1.11	1.26	1.54	1.54
	28ohm	15pF	0.74	0.83	1.34	1.34

4 Electrical Specification

4.1 Absolute Maximum Ratings

Table 4-1 Absolute maximum ratings

Symbol	Parameter	Rating	Unit
AVDD1V2_TRX1	1.2V supply for Wi-Fi/BT RF	-0.3 to 1.8	V
AVDD1V2_TRX2	1.2V supply for FM RF	-0.3 to 1.8	V
AVDD1V2_AFE1	1.2V supply for Wi-Fi analog front end (ADC/DAC/PLL)	-0.3 to 1.8	V
AVDD1V2_AFE2	1.2V supply for GNSS/FM analog front end	-0.3 to 1.8	V
AVDD1V2_GNSS	1.2V supply for GNSS RX and VCO	-0.3 to 1.8	V
DVDD_CORE	0.9-V core LDO output	-0.3 to 1.1	V
VDDIO	1.8V supply for IO	-0.3 to 2.5	V
DVDD_IN	1.1V supply for core LDO	-0.3 to 1.8	V
AVDD3V3_PRI	3.3-V supply for Wi-Fi primary PA	-0.3 to 3.6	V
AVDD3V3_DIV	3.3-V supply for Wi-Fi diversity PA	-0.3 to 3.6	V
AVDD3V3_BT_PA	3.3-V supply for BT PA	-0.3 to 3.6	V
T _{STG}	Storage temperature	-60 to 150	°C
T _A	Operating temperature	-40 to 85	°C
ESD (HBM)	Human body model	±2000	V
ESD (CDM)	Charged-device model	±350	V

4.2 Recommended Operating Range

Table 4-2 Recommended operating range

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD1V2_TRX1	1.2V supply for Wi-Fi/BT RF	1.1	1.2	1.5	V
AVDD1V2_TRX2	1.2V supply for FM RF	1.1	1.2	1.5	V
AVDD1V2_AFE1	1.2V supply for Wi-Fi analog front end (ADC/DAC/PLL)	1.1	1.2	1.5	V
AVDD1V2_AFE2	1.2V supply for GNSS/FM analog front end	1.1	1.2	1.5	V
AVDD1V2_GNSS	1.2V supply for GNSS RX and VCO	1.1	1.2	1.5	V
VDDIO	1.8V supply for IO	1.7	1.8	1.9	V
DVDD_IN	1.1V supply for core LDO	1.08	1.1	1.5	V
AVDD3V3_PRI	3.3-V supply for Wi-Fi primary PA	3.2	3.3	3.4	V

AVDD3V3_DIV	3.3-V supply for Wi-Fi diversity PA	3.2	3.3	3.4	V
AVDD3V3_BT_PA	3.3-V supply for BT PA	3.2	3.3	3.4	V
T _j	Junction temperature	-10	25	115	°C
T _{STG}	Storage temperature	-60	25	150	°C
T _A	Operating temperature	-40	25	85	°C

4.3 Power On Sequence

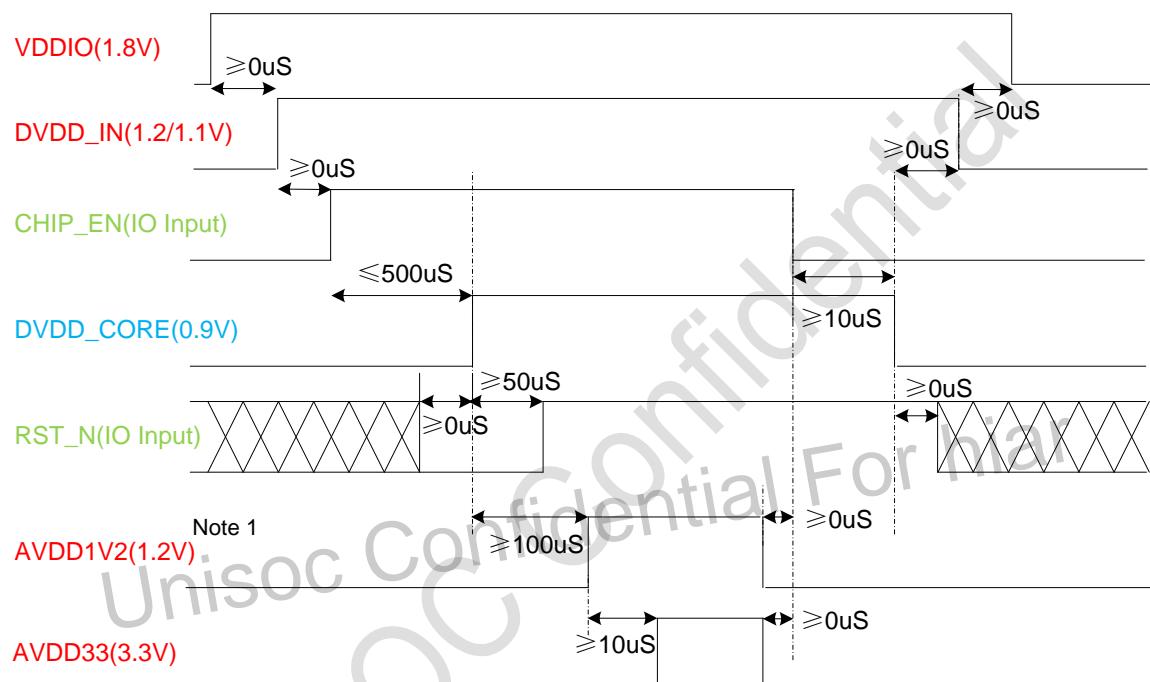


Figure 4-1 Power-On Sequence

Note.1 For limited PMIC supply, AVDD1V2 can be connected to DVDD_IN when both are 1.2v.

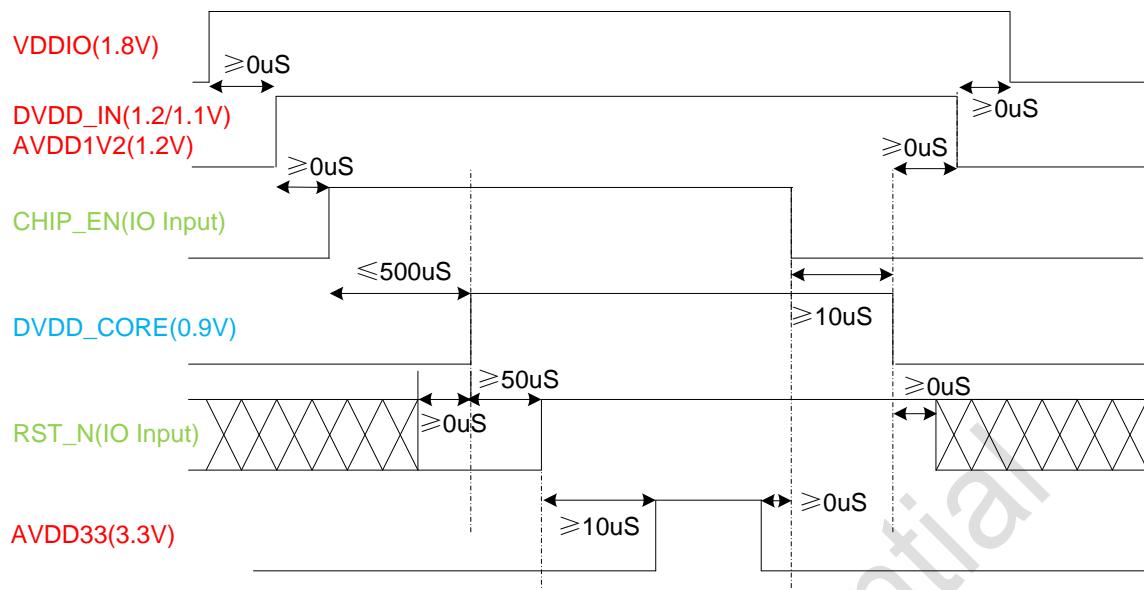


Figure 4-2 Power On Sequence (AVDD1V2 the same sequence as DVDDD_IN)

4.4 Leakage Current

Table 4-3 Deep sleep leakage current summary

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD1V2_TRX1	1.2V supply for Wi-Fi/BT RF		5		uA
AVDD1V2_TRX2	1.2V supply for FM RF		5		uA
AVDD1V2_AFE1	1.2V supply for Wi-Fi analog front end (ADC/DAC/PLL)		2		uA
AVDD1V2_AFE2	1.2V supply for GNSS/FM analog front end		2		uA
AVDD1V2_GNSS	1.2V supply for GNSS RX and VCO		1		uA
VDDIO	1.8V supply for IO		TBD		uA
DVDD_IN	1.1V supply for core LDO		TBD		uA
AVDD3V3_PRI	3.3-V supply for Wi-Fi primary PA		50		uA
AVDD3V3_DIV	3.3-V supply for Wi-Fi diversity PA		1		uA
AVDD3V3_BT_PA	3.3-V supply for BT PA		1		uA

5 IO Interface Timing Specification

5.1 SDIO Interface Timing

Please refer to SDIO chapter for SDIO timing details

5.1.1 SDIO Default Speed Timing

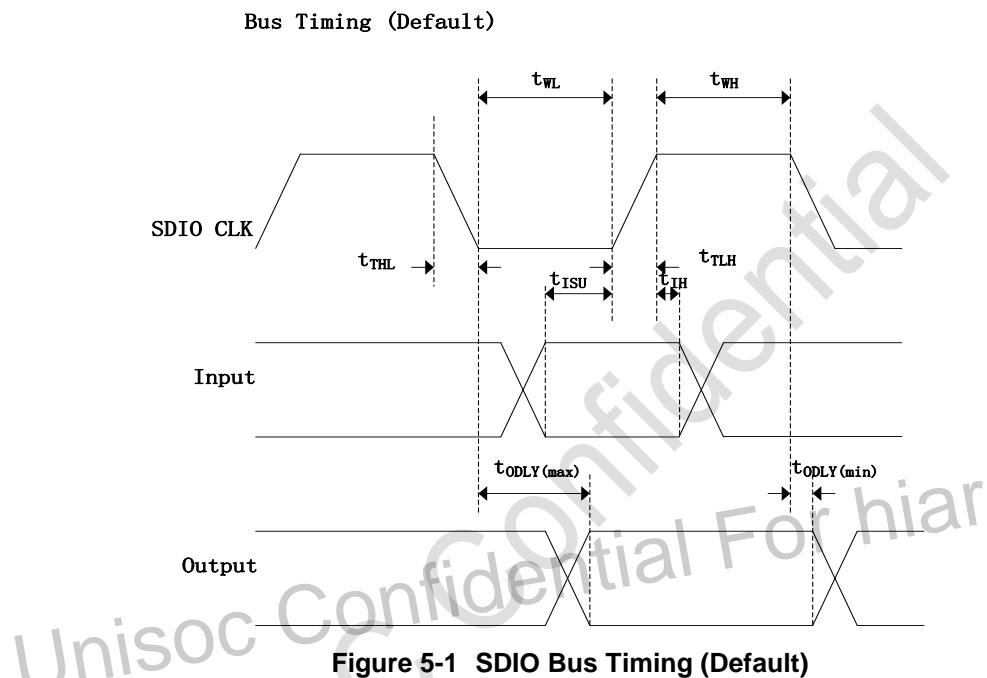


Figure 5-1 SDIO Bus Timing (Default)

Table 5-1 SDIO Bus Timing – Parameter Values (Default)

Parameter	Symbol	Min.	Max.	Unit
Clock CLK(All values are referred to min(V_{IH}) and max (V_{IL}))				
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz
Clock frequency Identification Mode	f_{OD}	0	400	kHz
Clock low time	t_{WL}	10	-	ns
Clock high time	t_{WH}	10	-	ns
Clock rise time	t_{TLH}		10	ns
Clock fall time	t_{THL}		10	ns
Inputs CMD, DATA (referenced to CLK)				

Input set-up time	t_{ISU}	5	-	ns
Input hold time	t_{IH}	5	-	ns
Outputs CMD, DATA (referenced to CLK)				
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns
Output Delay time during Data Identification Mode	t_{ODLY}	0	50	ns

*Timing parameter is based on $C_L \leq 40\text{pF}$ (1 card)

5.1.2 SDIO High Speed Mode Timing

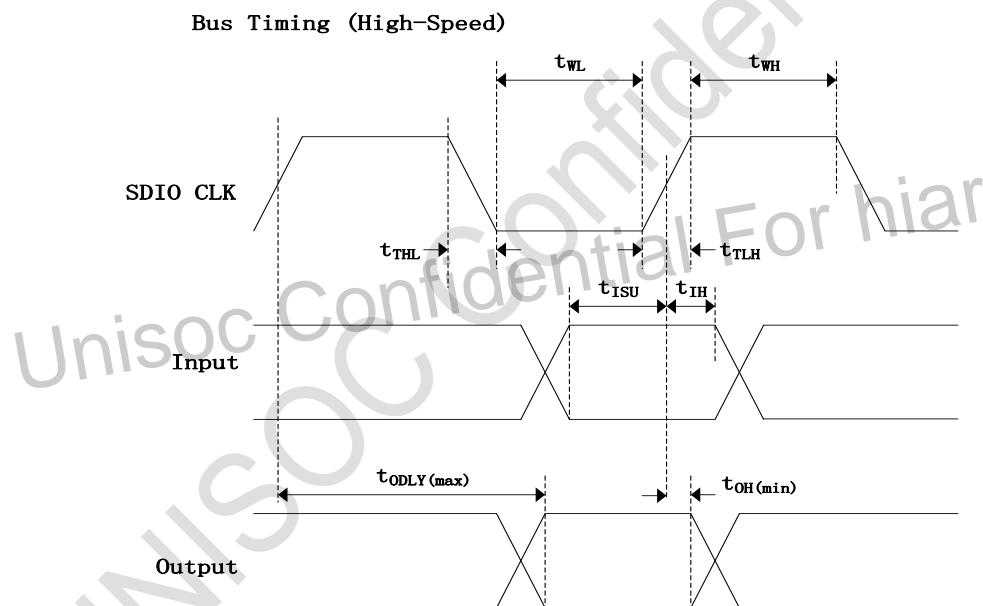


Figure 5-2 SDIO Bus Timing (High Speed)

Table 5-2 SDIO Bus Timing – Parameter Values (High Speed)

Parameter	Symbol	Min.	Max.	Unit
Clock CLK(All values are referred to min(V_{IH}) and max (V_{IL}))				
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz
Clock low time	t_{WL}	7	-	ns

Clock high time	t_{WH}	7	-	ns
Clock rise time	t_{TLH}		3	ns
Clock fall time	t_{THL}		3	ns
Inputs CMD, DATA (referenced to CLK)				
Input set-up time	t_{ISU}	6	-	ns
Input hold time	t_{IH}	2	-	ns
Outputs CMD, DATA (referenced to CLK)				
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns
Output Hold Time	t_{OH}	2.5	-	ns

*Timing parameter is based on $C_L \leq 40\text{pF}$ (1 card) for each line

5.1.3 SDIO UHS (SDR12, SDR25, SDR50, SDR104) Speed Mode Timing

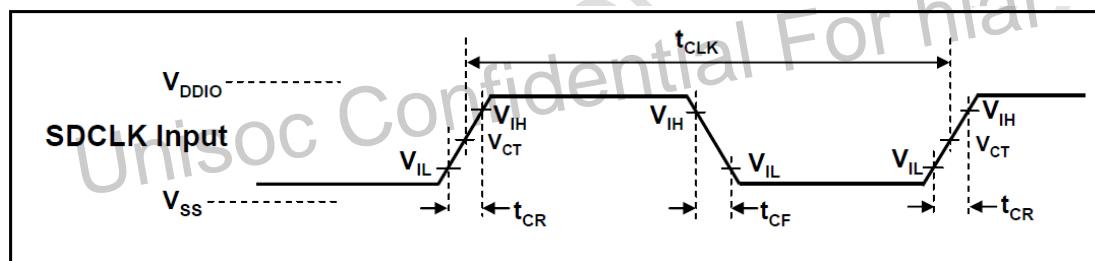


Figure 5-3 SDIO UHS Clock Timing

Table 5-3 SDIO Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, $V_{CT} = 0.975V$
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 0.96\text{ns}$ (max.) at 208MHz, $C_{CARD}=10\text{pF}$ $t_{CR}, t_{CF} < 2.00\text{ns}$ (max.) at 100MHz, $C_{CARD}=10\text{pF}$ The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

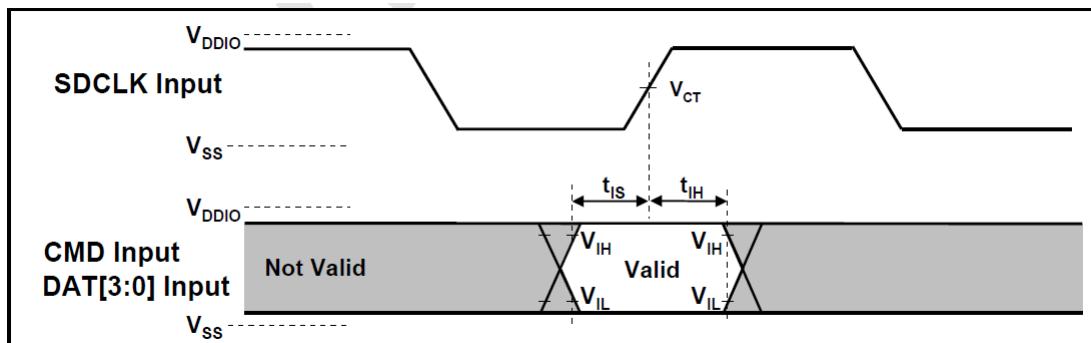


Figure 5-4 SDIO Card Input Timing

Table 5-4 SDIO SDR50 and SDR104 Input Timing

Symbol	Min.	Max.	Unit	SDR104 mode
t_{IS}	1.40	-	ns	$C_{CARD} = 10\text{pF}$, $V_{CT} = 0.975\text{V}$
t_{IH}	0.80	-	ns	$C_{CARD} = 5\text{pF}$, $V_{CT} = 0.975\text{V}$
Symbol	Min.	Max.	Unit	SDR12, SDR25 and SDR50 modes
t_{IS}	3.00	-	ns	$C_{CARD} = 10\text{pF}$, $V_{CT} = 0.975\text{V}$
t_{IH}	0.80	-	ns	$C_{CARD} = 5\text{pF}$, $V_{CT} = 0.975\text{V}$

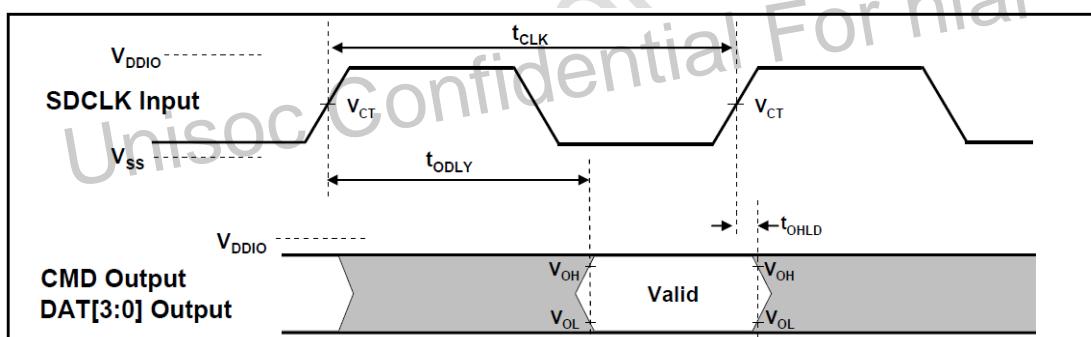


Figure 5-5 SDIO Output Timing of Fixed Data Window (SDR12, SDR25, SDR50)

Table 5-5 SDIO Output Timing of Fixed Data Window(SDR12, SDR25, SDR50)

Symbol	Min.	Max.	Unit	Remark
t_{ODLY}	-	7.5	ns	$t_{CLK} \geq 10.0\text{ns}$, $C_L = 30\text{pF}$, using driver Type B, for SDR50,
t_{ODLY}		14	ns	$t_{CLK} \geq 20.0\text{ns}$, $C_L = 40\text{pF}$, using driver Type B, for SDR25 and SDR12,
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), $C_L = 15\text{pF}$

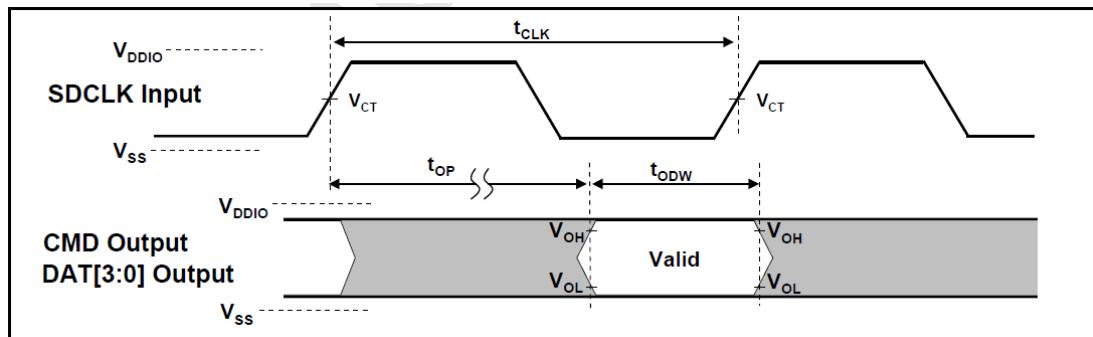


Figure 5-6 SDIO Output Timing of Fixed Data Window (SDR104)

Table 5-6 SDIO Output Timing of Fixed Data Window(SDR104)

Symbol	Min.	Max.	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	$t_{ODW}=2.88\text{ns}$ at 208MHz

5.1.4 SDIO UHS (DDR50) Speed Mode Timing

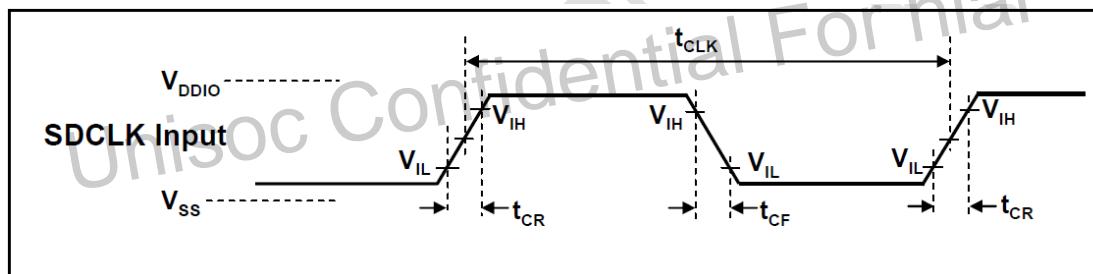


Figure 5-7 SDIO DDR50 Clock Timing

Table 5-7 SDIO DDR50 Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00\text{ns}$ (max.) at 50MHz, $C_{CARD}=10\text{pF}$
Clock Duty	45	55	%	

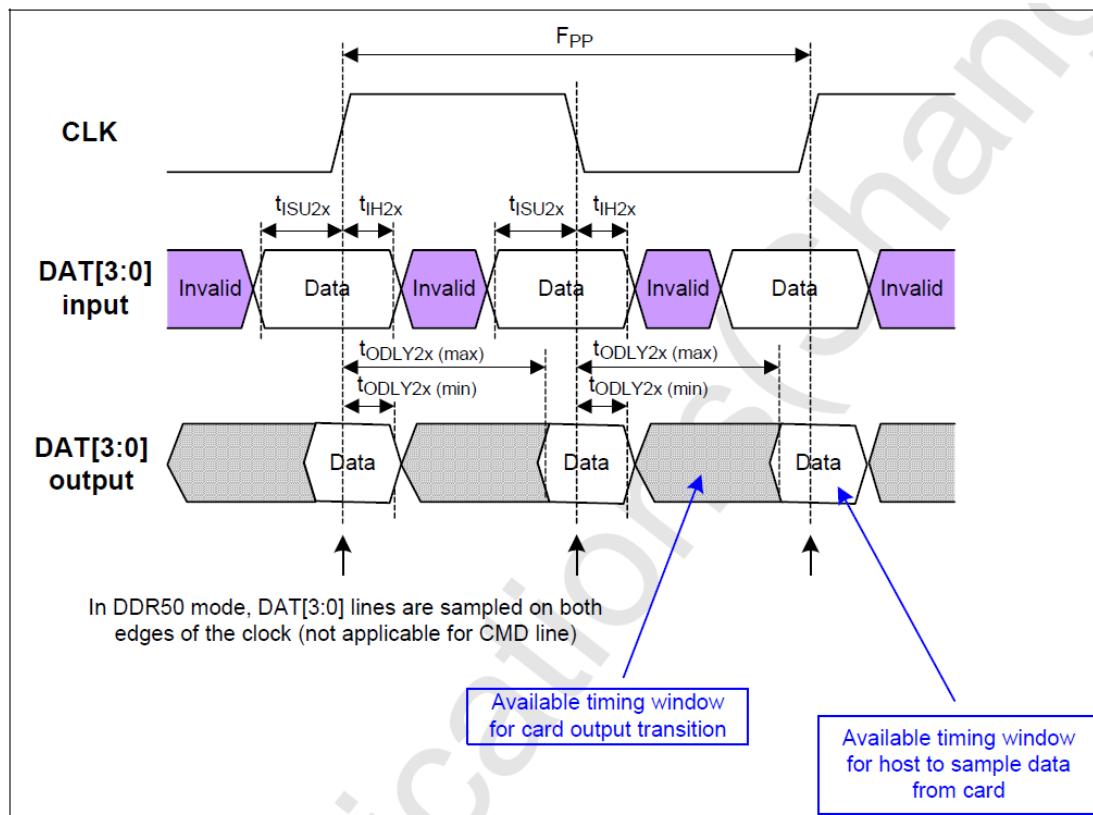


Figure 5-8 SDIO Input/Output Timing of DDR50

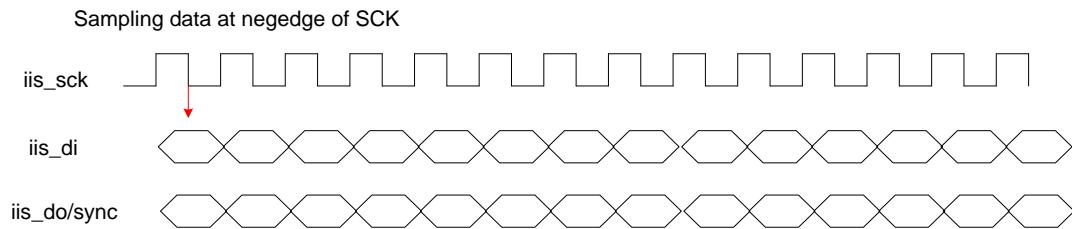
Table 5-8 SDIO Input/Output Timing of DDR50

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	$C_{CARD} \leq 10 \text{ pF}$ (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{CARD} \leq 10 \text{ pF}$ (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	$C_L \leq 30 \text{ pF}$ (1 card)
Output hold time	t_{OH}	1.5	-	ns	$C_L \geq 15 \text{ pF}$ (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	$C_{CARD} \leq 10 \text{ pF}$ (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{CARD} \leq 10 \text{ pF}$ (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq 25 \text{ pF}$ (1 card)
Output hold time	t_{OH2x}	1.5	-	ns	$C_L \geq 15 \text{ pF}$ (1 card)

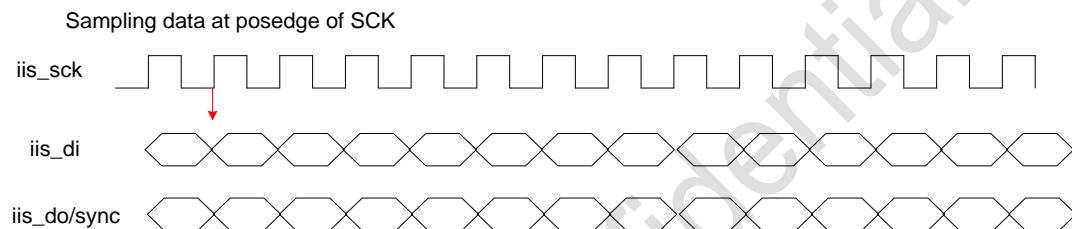
5.2 IIS/PCM Interface Timing

5.2.1 IIS Interface Timing

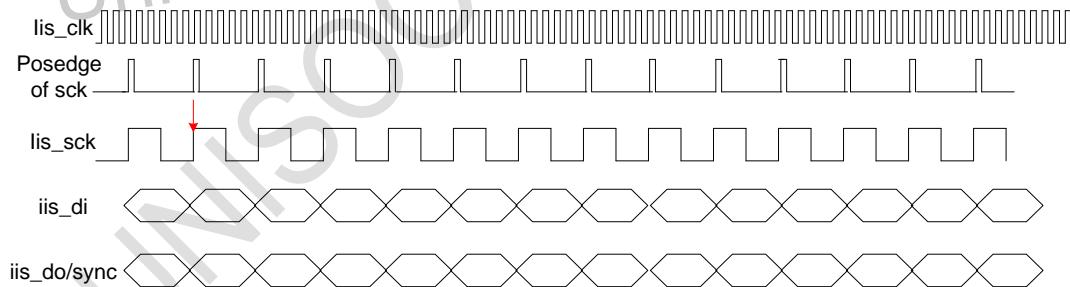
In default mode, iis output signals, like iis_do, iis_sync(for master) signal, are sent at the rising edge of iis_sck. And input signals like iis_di, iis_sync(for slave), are sampled at the falling edge of iis_sck.

**Figure 5-9 Sampling data at falling edge of IIS_SCK**

Output signals can be set as sent edge at falling edge and sampling edge at rising edge, as shown in below fError! Reference source not found..

**Figure 5-10 Sampling data at rising edge of IIS_SCK**

The implementation of sampling edge is as following.

**Figure 5-11 implementation of sampling data at falling edge of IIS_SCK**

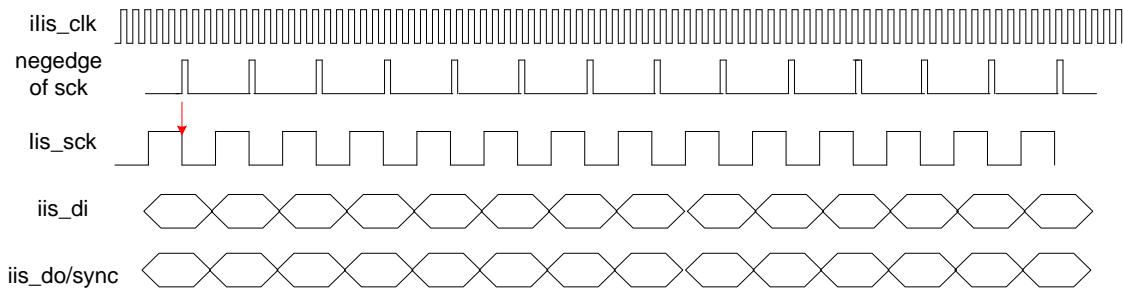


Figure 5-12 Implementation of sampling data at rising edge of IIS_SCK

5.2.2 Setup time and hold time

If we assume that max input delay is 10ns and min input delay is 0ns for **iis_di** to **iis_sck**, max output delay is 10ns and min output delay is 5ns for **iis_do/iis_lrck** to **iis_sck**. The clock period time is 50ns for **iis_sck**.

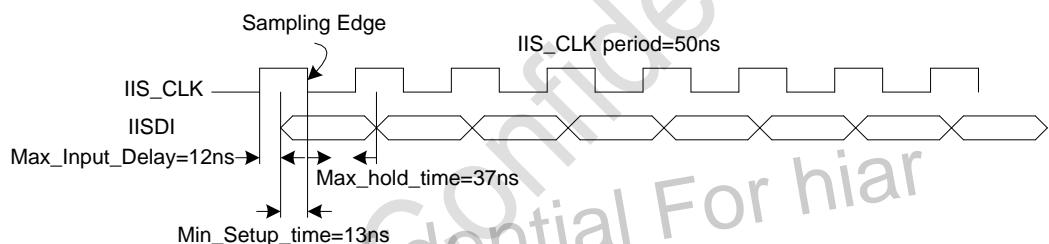


Figure 5-13 Implementation of sampling data at falling edge of IIS_SCK

Then for **iis_di**, the setup time range is $13\text{ns} < \text{setup_time} < 25\text{ns}$, and the hold time range is $25\text{ns} < \text{hold_time} < 37\text{ns}$. For **iis_do/iis_lrck**, the setup time range is $13\text{ns} < \text{setup_time} < 25\text{ns}$, and the hold time range is $25\text{ns} < \text{hold_time} < 37\text{ns}$

5.3 UART Interface Timing

As shown in below figure, the UART interface for **UART_TXD/UART_RXD** conforms to standard baud rate.

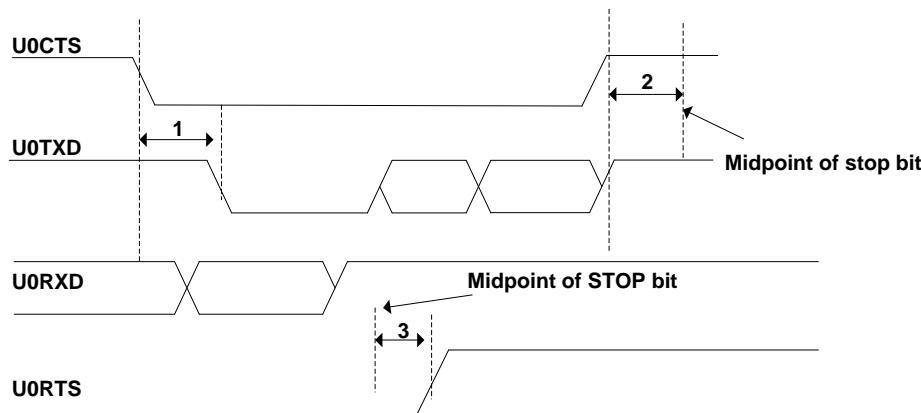


Figure 5-14UART Interface Timing (Default)

Table 5-9 UART Bus Timing – Parameter Values (Default)

RefNO.	Characteristics	Min.	Typical	Max.	Unit
1	Delay time, U0CTS low to U0TXD valid	-	-	1.5	Bit periods
2	Setup time, U0CTS high before midpoint of stop bit	-	-	-	Bit periods
3	Delay time, midpoint of stop bit to U0RTS high	-	-	0.5	Bit periods

For T2 timing, If $T2 \geq 0.5$ bit time (U0CTS high active before the stop bit), next TX data will not send; else, the next TX data will send out, and the data after the next one will not send.

5.4 I2C Interface Timing

5.4.1 Timing Parameters

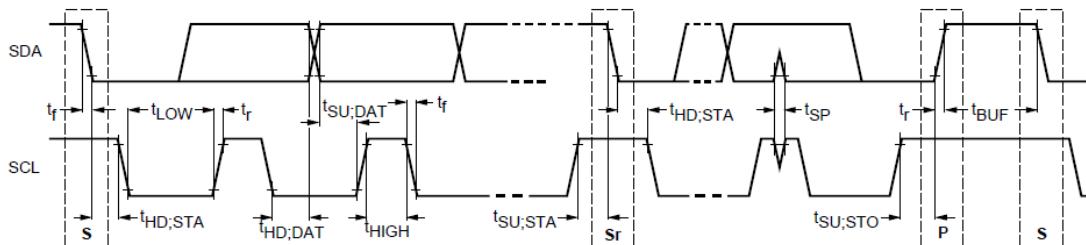


Figure 5-15 I2C timing diagram

Table 5-10 I2C interface timing parameters

Parameter	Description	Standard mode		Fast mode	
		Min	Max	Min	Max
fSCL	SCL clock frequency	0 kHz	100 kHz	0 kHz	400 kHz
tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0 us	-	0.6 us	-
tLOW	LOW period of the SCL clock	4.7 us	-	1.3 us	-
tHIGH	HIGH period of the SCL clock	4.0 us	-	0.6 us	-
tSU;STA	Set-up time for a repeated START condition	4.7 us	-	0.6 us	-
tHD;DAT	Data hold time	0 us	3.45 us	0	0.9 us
tSU;DAT	Data set-up time	250 ns	-	100 ns	-
tr	Rise time of both SDA and SCL signals	-	1000 ns	20 + 0.1Cb	300 ns
tf	Fall time of both SDA and SCL signals	-	300 ns	20 + 0.1Cb	300 ns
tSU;STO	Set-up time for STOP condition	4.0 us	-	0.6 us	-
tBUF	Bus free time between a STOP and START condition	4.7 us	-	1.3 us	-
C _b	Capacitive load for each bus line	-	400 pF	-	400 pF

5.5 SFC Interface Timing

5.5.1 Timing Parameter

SFC support 4bit data.

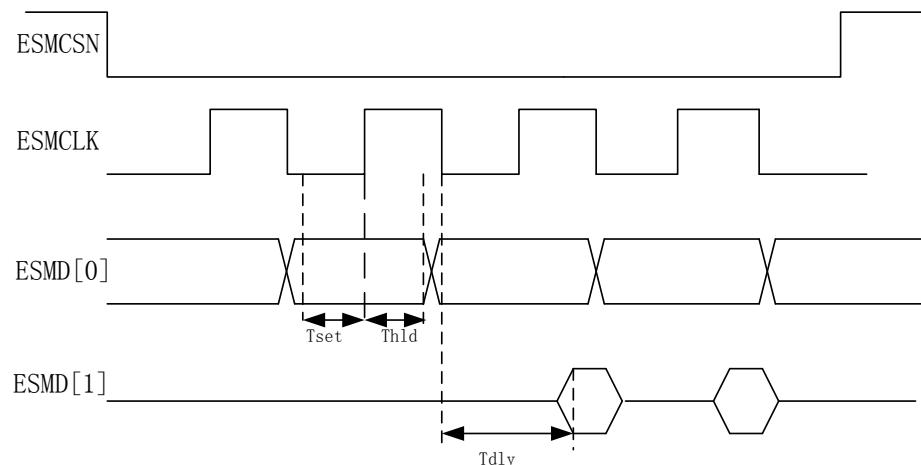


Figure 5-16 SFC Timing Chart

Table 5-11 SFC interface timing parameters

Symbol	Parameter	Min	Max
fESMCLK	SFC output clock frequency		208MHz
Tset	SFC output data setup time	3ns	
Thld	SFC output data hold time	3ns	
Tdly	Flash output delay		4.5ns

5.6 PCIE Interface Timing

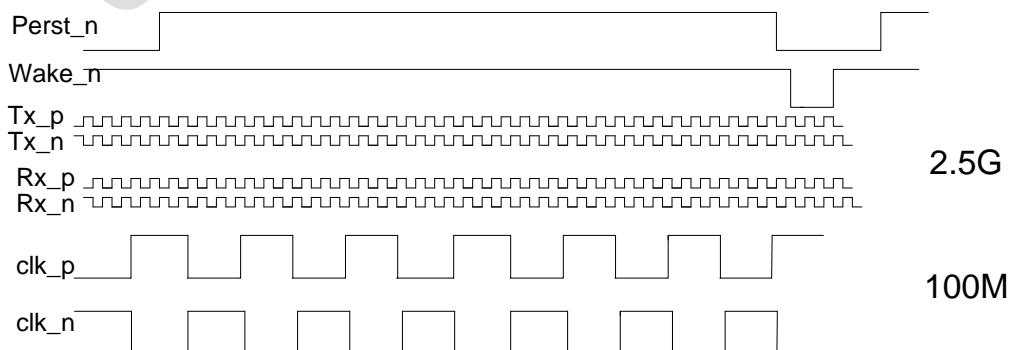


Figure 5-17 PCIe Timing Diagram