



SC2703P Device Specification

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1 General description

SC2703P is a complex Power Management IC (PMIC) that incorporates charger, flash driver, core buck, White Light Emitting Diode backlight driver (WLED) and display bias/ power supply generation for TFT display technologies. An I²C compatible 2-wire interface, an interrupt port is provided for the device control.

SC2703P contains an integrated Power Management Controller (PMC) for the multiple power supplies generated by the device. The PMC allows for configurable sequencing and output voltage configuration defined in OTP or Software controlled from the host by register allowing high flexibility to fit customer applications.

The SC2703P is available in a small WLCSP 4.120mm× 4.493mm, with no back side coating.

1.1 Charger Key features

- 4.3 to 13.5V input voltage
- 20V withstand on input voltage
- 8KV HBM on V_{BUS} and V_{BAT} pins
- 3.5 A charging current
- 90+% peak efficiency
- Reverse boost mode with 2 A output current
- 470 nH inductor
- Low-profile external components (\leq 1 mm)
- Fixed switching frequency
- Battery isolation mode
- Autonomous CCCV charging
- Integrated low Ohmic battery switch
- High accuracy
 - $\pm 0.5\%$ battery voltage regulation accuracy
 - $\pm 5\%$ charging current regulation accuracy
 - Programmable input current limit
- Reverse current protection
- Junction temperature monitoring
- Integrated 8-bit ADC
- Safety timer

1.2 Flash Driver

- Dual Flash LED source driver
- 0 to 1 A per channel
- Torch in 25mA steps
- Flash in 50mA steps
- Programmable current ramp up/down rate
- Flash and torch mode support
- Supplied by charger in reverse boost mode
- $\pm 6.5\%$ current accuracy
- Automatic open / short detection
- Programmable safety timers

1.3 Core Buck

- Output Voltage 0.35 to 1.57V
- Output Current 5A
- Efficiency 90+% at 1A (with high quality inductor)
- $\pm 15mV$ accuracy (static, at Vout <1V)
- Load transient response -4% / +6% at 3A/1μs (Vout <1V, Cload > 22uF)
- Remote sensing at point of load

- Programmable Soft start

1.4 WLED Key features

- Single channel controller
- $\pm 2\%$ Current accuracy
- $\pm 2\%$ Current linearity
- Maximum Vout 26V
- 8 bit Idac
- External Schottky diode
- Peak efficiency 88+% (Vout 19.8V, V_{BAT} 3.8V, a 2P6S configuration with diode voltage 3.3V)
- Support CABC control
- Programmable max current up to 40mA
- Programmable Vout limit

1.5 Display Supply Key features

- 88% Efficiency at Iout 40 mA
- Positive Output Voltage Range : 4.0 V to 6.0V in 100mV steps
- Negative Output Voltage Range: -6.0 V to -4.0 V in 100mV steps
- $\pm 1\%$ Output Voltage Accuracy.
- Programmable Power-Up and Power-Down Sequencing
- Programmable Active Discharge
- Supports LCD TFT with single inductor
- Maximum Output Current: 80 mA
- Positive and negative voltage are independently and adjustable

1.6 Differentiator features between SC2703L

- High voltage quick charge support
- 1.5A Flash on single channel
- WLED overdrive

1.7 Applications

- Smartphones
- Tablets
- Portable navigation devices

1.8 Terms and definitions

Define acronyms and abbreviations used in the document.

ATE - Automated Test Equipment

AP – application processor

EMI – electro-magnetic interference

ATB – analogue test bus

DTB – digital test bus

1.9 Block diagram

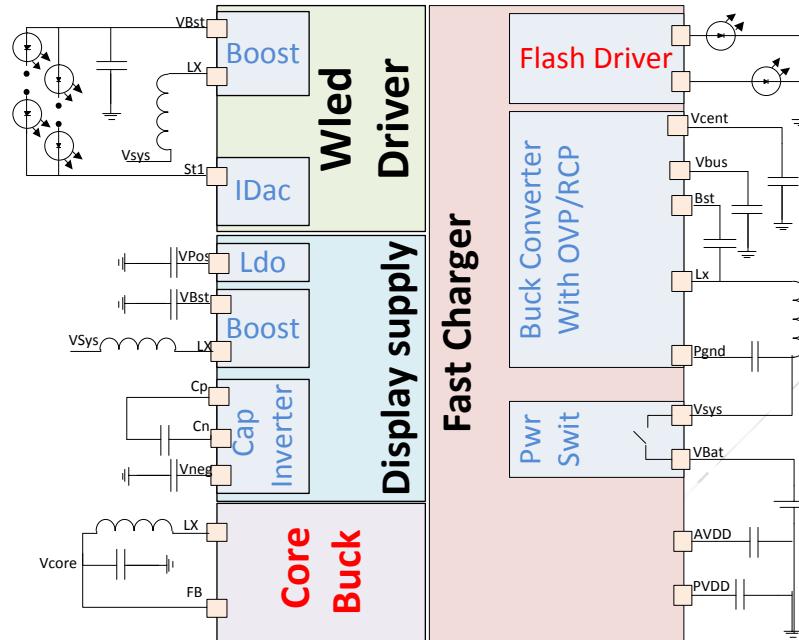


Figure 1: SC2703P block diagram

1.10 Charger description

SC2703P includes a high-efficiency charger capable of delivering **3.5A** in to a single-cell Lithium-ion battery. The supported input voltage range is 4.3V to 13.5V.

The efficiency of SC2703P is a true 90+% at 2.5 A charging current, measured from the input to the positive battery terminal. This best-in-class efficiency is achieved while retaining small PCB footprint and low component height (1 mm height).

The high efficiency allows a higher charging current compared to existing solutions.

SC2703P features a programmable input current limit and an automatic input power reduction feature which ensures safety during fast charging. Accurate charging current regulation is provided without the need of an external shunt resistor.

The charger utilizes the constant current-constant voltage charging method and fully autonomous charging control.

The power path management takes care of supplying the system from the two available power sources (V_{BUS} or V_{BATT}) and seamlessly switching between them. SC2703P can also operate without a battery, or with a deeply discharged battery. The system is always supplied from the external supply if one is available.

The DC-DC converter can operate in reverse boost mode thus enabling USB on-the-go functionality and Flash support.

An 8-bit ADC enables monitoring several charging parameters.

1.11 Flash driver description

The flash driver is a two channel current source for the flash LEDs supplied from the Vcentre rail of the charger block. Two channels are capable of sourcing 1A each. Both channels can be simultaneous operated, with a maximum load to the OTG boost of 2A. The two channels can be programmed independently to allow multiple user modes to be implemented such as camera flash, torch or even message indicator. While the max current sourced in the flash mode is $1A \times 2 = 2A$, this mode, by nature, is intended to work in short pulse. SC2703P has the capability of sourcing upto 1.5A of channel1 if channel2 is set to source 0.5A or less (total current sourced $\leq 2A$). A programmable safety timer is incorporated into the design to limit operation time and prevent damage to the external LED due to power dissipation; the driver also includes a thermal trip to disable the flash if the die temperature becomes dangerously high due to high power dissipation. Each channel can be programmed in 50mA steps for the flash mode and 25mA in the torch mode (both channels can support Torch operation). The accuracy is controlled within $\pm 6.5\%$ of the current setting. As the maximum flash current can be 2A, the power supplying the LEDs and sourced in the flash driver is provided by the charger block operating in a reverse boost mode, instead of an external charger adapter whose capacity can be a concern. However the Flash driver can operate in torch mode when Vcenter is supplied via an external V_{BUS} supply. If the V_{BUS} voltage rises above 6V in this mode of operation, the RCP/OVP switches will open and the charger will switch to reverse boost operation to support the torch. This will result in a momentary suspension of torch operation while the charger transitions from Buck to boost operation.

Current load on the Vcenter rail will be ramped up and down at programmable rate, to the target current, to ensure load transients and inrush current are controlled. Open and short LED is monitored and handled as a fault event.

1.12 Core Buck description

The Buck is suitable for the supply of CPUs, GPUs, DDR memory rails in smartphones, tablets and other handhelds applications.

The buck function, using a small external 0.10 μ H inductor is capable of delivering up to 5A continuous output current at an output voltage in the range 0.35 - 1.57 V.

To guarantee the highest accuracy and support multiple PCB routing scenarios without loss of performance, a remote sensing capability is implemented.

The pass devices are fully integrated, so no external FETs or Schottky diodes are needed.

A programmable soft start-up can be enabled, which limits the inrush current from the input node and secures a slope controlled activation of the rail.

The Dynamic Voltage Control (DVC) supports adaptive adjustment of the supply voltage dependent on the processor load, via direct register write through the communication interface (I²C).

1.13 WLED driver description

The WLED driver is a dual string driver incorporating a high efficiency high voltage boost converter, with efficiency above 88%, and a current sink IDAC that is unary linear mapping digitally to an exponential profile.

The boost works at a programmable fixed frequency using current mode architecture. The IDAC is an exponential 8 bits current DAC with dither at low current settings to improve the DNL below 2.7mA. It fits with the WLED backlight requirements in terms of human eye accommodation to light change. The implementation provides the needed accuracy with a reasonable complexity. It is a

combination of a pure linear current DAC and an exponential time sequence, digitally generated (Patent Pending).

The output of the boost is connected with a maximum 2 strings of LEDs. Each string could support up to 7+ LEDs connected in series, limited by the maximum output voltage.

A configurable overvoltage circuit monitors the boost output to a maximum of 26V. Output clamp function can be enabled to pull down the boost output when WLED_IDAC pin voltage (sink voltage) is 0.4V higher than the target.

Open and short LED is monitored and the WLED driver would automatically take action when the fault event is triggered. CABC is supported via a PWM input pin that can accept duty detect inputs from a source with a frequency range of 25 KHz to 35 KHz. The duty of this PWM input signal can be resolved into 256 steps which are then mapped to the WLED IDAC to give either a linear response or exponential response, depending on user settings.

1.14 Display power generation description

The display power supply consists of an inductive boost converter and a capacitive charge pump inverter. The boost converter runs in forced PWM mode to ensure the ripple on the Vpos supply is a constant frequency and much higher than the display line scan rate, to ensure the ripple doesn't cause display artefacts. Switching frequency is configurable to optimize the transient response and inrush current during power on. An LDO called display LDO whose input is connected to the booster output is used to supply display Vpos in TFT mode.

The charge pump inverter output is separately regulated via pulse skipping but as it uses the boost converter output to charge its flying cap the negative voltage cannot be set more negative than the Vpos voltage is positive. Inrush current and output ripple can be adjusted by register / OTP setting.

Both the boost converter and charge pump support over voltage, under voltage and short circuit protection with configurable deglitch time.

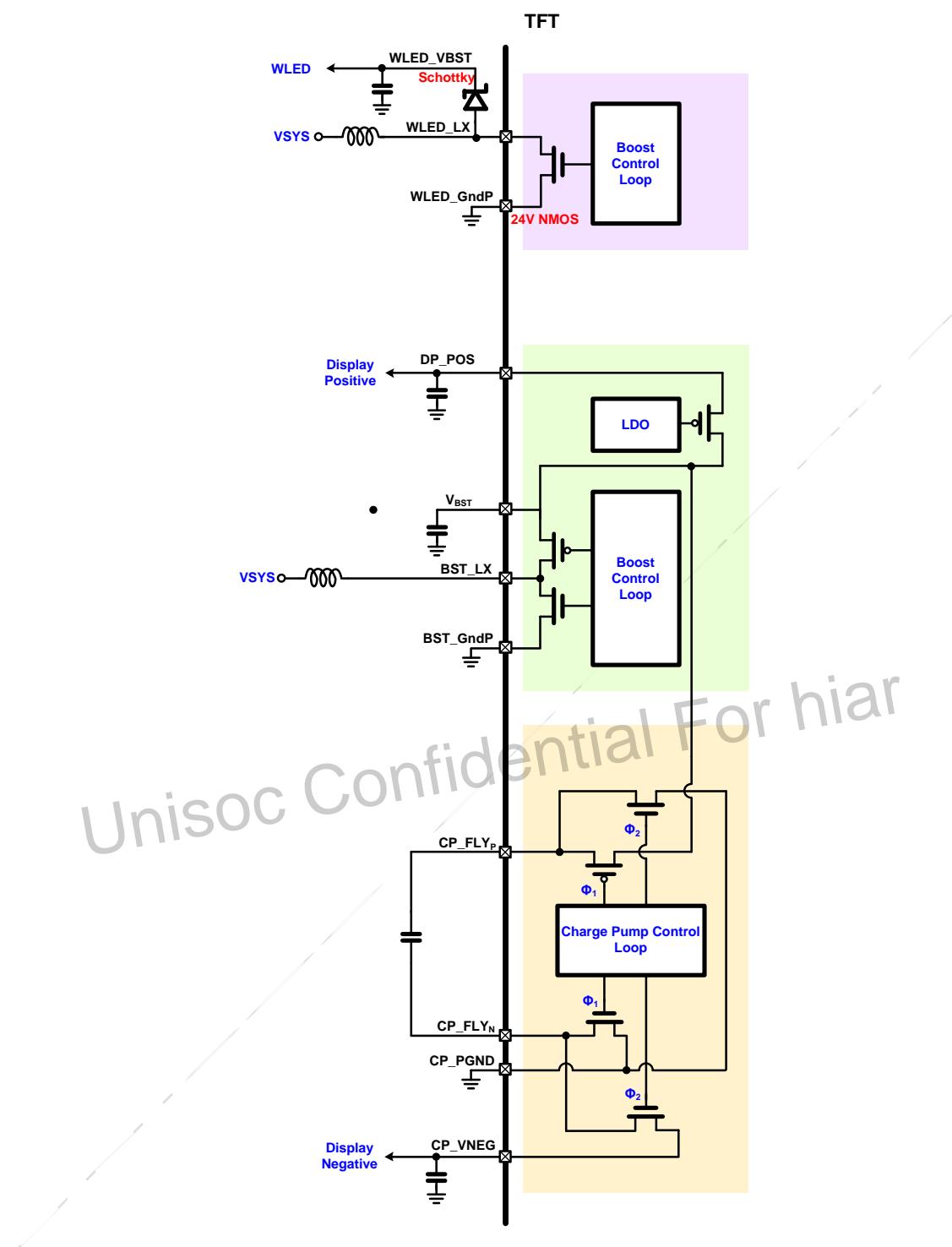


Figure 2: Display Bias Configuration

2 Absolute maximum ratings

Table 1 lists the absolute maximum ratings of the device. Exceeding these ratings may cause permanent damage to the device. Device functionality is only guaranteed under the conditions listed

in sections 3 and 4. Operating the device in conditions exceeding those listed in sections 3 and 4, but compliant with the absolute maximum ratings listed in Table 1, for extended periods of time, may affect device reliability.

Table 1: Absolute maximum ratings

Parameter	Symbol	Note	Min	Max	Unit
Storage temperature			-60	+150	°C
Operating temperature	T _A		-40	+85	°C
Terminal voltage (referenced to PGND, unless otherwise noted)	V _{BUS}	The device is not operational above V _{Bus_OVLO} .	-0.3	20	V (DC)
		Charger operational		V _{BUSOVLO}	
	SW		-0.3	V _{BUSOVLO}	V (DC)
	Vcentre		-0.3	V _{BUSOVLO}	V (DC)
	BT		-0.3	SW+V _{PVDD}	V (DC)
	V _{BATT}	Referenced to AGND	-0.3	6	V (DC)
	All other terminals	Referenced to AGND	-0.3	V _{AVDD} +0.3	V (DC)
ESD tolerance		HBM (all non-exposed pins)		2	kV
		HBM (VBUS, VBAT) to Local Gnd		8	kV
		CDM		500	V

3 Recommended operating conditions

Table 2: Recommended operating conditions

Parameter	Symbol	Conditions	Min	Max	Unit
Operating temperature	T _A		-25	85	°C
Input supply voltage	V _{BUS}		4.3	13.5	V
Battery voltage	V _{BATT}			4.6	V
Battery discharge current	I _{BATT}	Average		6	A
		Peak (up to 1 s)		9	A

4 Electrical characteristics

Unless otherwise noted, the parameters listed in Table 3–Table 25 are valid for T_A = -25°C to +85°C, V_{BUS} = 4.3 V – 13.5 V, V_{BATT} = 2.6 V – 4.4 V

4.1 Current Consumption

Table 3: Charger Current Consumption

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent current	I _{BATT}	ULP mode, V _{BATT} =3.8 V		35	50	µA
		IDLE mode, V _{BATT} =3.8 V		120		µA
Current draw from V _{BATT}	I _{BATT_IDLE}	BATT_BOOST mode, V _{BUS_REV} =5 V, I _{BUS_REV} =0 A, V _{BATT} =3.8 V		6.8		mA
Current draw from V _{BUS}	I _{BUS_IDLE}	V _{BUS} =5 V, IDLE mode, average over 1 s		450		µA
		V _{BUS} =5 V, VIN_BUCK mode, I _{SYS} =0 A, average over 1 s		8		mA

4.2 Voltage monitoring

4.2.1 POR

Table 4: POR

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power on reset threshold	V _{POR}	Rising threshold of V _{AVDD}	2.043	2.27	2.497	V
Power on hysteresis	V _{POR_HYST}			40		mV
Power on accuracy	V _{POR_ACC}		-10		+10	%

4.2.2 V_{BUS}

Table 5: V_{BUS}

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V _{bus} overvoltage threshold	V _{bus_OVLO}	Rising threshold	13.5		14.5	V
V _{bus} overvoltage hysteresis	V _{bus_OVLO_HYS}			3		%
V _{bus} overvoltage deglitch time	t _{D_Vbus_OVLO}			10		µs
V _{bus} under voltage threshold	V _{bus_UVLO_FALL}	Falling threshold, pulse width greater than 3 µs		3.8		V
	V _{bus_UVLO_RISE}	Rising threshold, pulse width greater than 3 µs	4.3	4.4	4.5	V
V _{bus} short threshold	V _{bus_SHORT}	Falling threshold, active only during OTG Mode	3.6	3.8	4.0	V
V _{bus} drop threshold	V _{bus_DROP}	Falling threshold, V _{bus_DROP} = 0x9A		12		V
		Falling threshold, V _{bus_DROP} = 0x00		4.3		V
V _{bus} drop accuracy	V _{bus_DROP_ACC}		-3.5		+3.5	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V _{bus} monitoring deglitch time (applies to V _{bus_UVLO} , V _{bus_SHORT} , V _{bus_DROP})	t _{D_Vbus}			3		μs
Input limit Enable Delay	t _{INLIM_START}	Start-up delay from VBUS insertion to OVP+RCP Enable		100		ms
Buck Warmup Delay	t _{BUCK_WARM}	Start-up delay from V _{CENTURE} to Buck Enable		100		ms
Buck Enable Delay	t _{BUCK_START}	Start-up delay from Buck Enable to SYS regulating		100		ms
BAT Insertion Start-up Delay	t _{BAT_DLY}	Start-up delay from Battery insertion to I ₂ C ready		5		ms

4.2.3 V_{BAT}

Table 6: V_{BAT}

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Overvoltage threshold	V _{BAT_OV}	Rising threshold V _{BATT_OV} = 0x? (select 4.6V setting)		4.6		V
		Rising threshold VBATT_OV = 0x0		4.0		V
V _{BATT_OV} monitoring deglitch delay	t _{D_VBAT_OV}		3			μs
Under voltage threshold	V _{BAT_UV}	Falling threshold VBATT_UV = 0xF		2.95		V
		Falling threshold VBATT_UV = 0x0		2.2		V
Short detection threshold	V _{BAT_SHORT}	Falling threshold		2.0		V
Dead battery threshold	V _{BAT_DEAD}	Rising threshold		2.0		V
V _{BATT} monitoring hysteresis	V _{BAT_MON_HYS}			3		%
Monitoring accuracy	V _{BAT_ACC}	V _{BATT} range 2.5 V–5 V IC level and cannot account for PCB parasitic	-5		+5	%
V _{BATT} monitoring deglitch delay (applies to V _{BATT_UV} , V _{BATT_SHORT})	t _{D_VBAT}			3		μs

4.2.4 V_{SYS}

Table 7: V_{SYS}

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Minimum system voltage monitoring threshold	V _{SYS_MIN}	Rising threshold, VSYS_MIN=0xF		3.9		V
		Rising threshold, VSYS_MIN=0x0		3.0		V
V _{SYS} accuracy	V _{SYS_ACC}		-5		+5	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Overvoltage lockout threshold	V _{SYS_OV}	Rising threshold		5.3		V
V _{SYS} POR threshold	V _{SYS_POR}	Falling threshold		2.75		V
V _{SYS} monitoring deglitch delay	t _{D_VSYS}			TBD		μs
V _{SYS} Under voltage threshold	V _{SYS_UV}	Rising threshold	2	2.2	2.4	V
System voltage regulation at charger FULL state	V _{SYS_FULL_REG}			V _{BAT_CHG} + 100 mV		V
V _{SYS} headroom	V _{SYS_HDRM}	Delta to V _{SYS_MIN}		200		mV

4.2.5 VBUS2BATT

Table 8: V_{BUS2BAT}

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VBUS2BAT threshold	V _{BUS2BAT}	V _{BUS} -V _{BAT} falling threshold	25	85	145	mV
	V _{BUS2BAT_RISE}	V _{BUS} -V _{BAT} rising threshold		200		mV
VBUS2BAT monitoring deglitch delay	t _{D_VIN2BAT}			TBD		μs

4.2.6 VBAT2SYS

Table 9: V_{BAT2SYS}

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Battery switch turn-on threshold (supplement entry threshold)	V _{BAT2SYS_SW}	V _{BAT} -V _{SYS} , rising threshold		75		mV
Battery switch turn-on deglitch delay	t _{D_VBAT2SYS}			3		μs
Supplement exit threshold	I _{SUP_EXIT}	Current measured from BAT to SYS		60		mA
Minimum time for BAT2SYS Short	V _{SYS_COMP}	How quickly can we go from V _{BUS} to BAT to prevent SYS brownout		1		μs
SYS Pull-up Resistance	R _{SYS_PU}	When SYS is < V _{BAT_SHORT}		70		Ω

4.3 Temperature monitoring

4.3.1 T_{JUNC}

Table 10: T_{JUNC}

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
POR temperature threshold	T _{JUNC_POR}	Rising threshold		150		°C
Critical temperature threshold	T _{JUNC_CRIT}	Rising threshold		140		°C
Warning temperature threshold	T _{JUNC_WARN}	Rising threshold, TJUNC_WARN="11"		125		°C

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
		Rising threshold, TJUNC_WARN="00"		70		°C
TJUNC monitoring deglitch delay (applies to TJUNC_POR and TJUNC_CRIT)	tD_TJUNC			3		μs

4.4 Charger DC-DC converter

The parameters listed in Table 12 are valid with the following component values, unless otherwise notes.

Table 11: Charger external components

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitor	C _{IN}	(Note 1)		1		μF
	C _{centre}			22		μF
ESR of C _{IN}	R _{ESR_CIN}			3		mΩ
Output capacitor	C _{OUT}	Nominal (local – derated)	40		<200	μF
Boot strap capacitors	C _{BOOT}	Nominal		100		nF
Inductance	L	Nominal		0.470		μH
Inductor resistance	R _{LDCR}	Nominal		20		mΩ
Charging cable inductance	L _{CABLE}		0.1		2	μH
Charging cable resistance	R _{CABLE}		50		2000	mΩ

Note 1 The maximum V_{BUS} load that can be placed at the downstream end of a USB cable is 10 μF. In addition the minimum and maximum value of the capacitance is bound by the USB On-The-Go specification [1][2].

Table 12: Charger DCDC Converter

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage range	V _{Bus}		4.3		V _{BUS_OVLO}	V
Battery voltage range	V _{BATT}	V _{BUS} at nominal USB level	2.5		4.6	V
		V _{BUS} at 5.4V			4.8	
Converter maximum duty cycle	D _{MAX}	See Note Frequency Foldback	99.5			%
Leakage current to V _{IN}	I _{Bus_LKG}	V _{IN} grounded, IDLE mode, V _{BATT} =4.4 V			70	μA
Input Resistance	R _{VBUS-CENTER}			35		mΩ
Average V _{Bus} current limit	I _{Bus_LIM}	I _{Bus_LIM} = "111"			3000	mA
		I _{Bus_LIM} = "000"			100	mA
Accuracy of V _{IN} current limit [note1]	I _{Bus_LIM_ACC}	500 mA ≤ I _{Bus} ≤ 3.0 A	-10		0	%
		200 mA ≤ I _{Bus} < 500 mA	-30		0	
		100 mA ≤ I _{Bus} < 200 mA	-40		0	

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Rate of the input power reduction	K _{IN_PWR}			25		mA/μs
Charging current	I _{BATT_CHG}	I _{BATT_CHG} = 0x3C		3.5		A
		I _{BATT_CHG} = 0x00		500		mA
Charging current regulation accuracy [note1]	I _{BATT_CHG_ACC}	1.5 A ≤ I _{BATT_CHG} ≤ 3.5 A, VBATT=3.8V, VMINSYS=3.4V	-5		+5	%
		I _{BATT_CHG} < 1.5 A, VBATT=3.8V, VMINSYS=3.4V	-10		+10	%
Battery voltage	V _{BATT_CHG}	Rising threshold VBATT_CHG = 0x32		4.8		V
		Rising threshold VBATT_CHG = 0x0		3.8		V
Battery voltage regulation accuracy [note1]	V _{BATT_CHG_ACC}		-0.5		-0.5	%
Minimum system voltage regulation	V _{SYS_MIN_REG}	V _{SYS_MIN} =0xF		3.9		V
		V _{SYS_MIN} =0x0		3.0		V
System voltage regulation at charger FULL state	V _{SYS_FULL_REG}			V _{BATT_CHG}		
System voltage regulation accuracy	V _{SYS_MIN_ACC}		-3		+3	%
Charger efficiency [note2]	η _{CHG}	V _{IN} = 9 V, V _{BATT} = 4.4 V, I _{CHG} = 3.5 A, I _{SYS} =0 A, measured from V _{BUS} to V _{BATT_P}		90+		%
		V _{BUS} = 9 V, V _{BATT} = 4.4 V, I _{CHG} = 3 A, I _{SYS} =0 A, measured from V _{BUS} to V _{BATT_P}		90+		
		V _{BUS} = 9 V, FULL state, V _{BATT} =4.4, V _{SYS} = V _{SYS_FULL_REG} , I _{CHG} = 0 A, I _{SYS} =20 mA, measured from V _{BUS} to V _{SYS}		70+		
		V _{IN} = 5 V, V _{BAT} = 4.4 V, I _{CHG} = 2.5 A, I _{SYS} =0 A, measured from V _{BUS} to V _{BAT}		92		%
		V _{IN} = 5 V, V _{BAT} = 3.8 V, I _{CHG} = 2.5 A, I _{SYS} =0 A, measured from V _{BUS} to V _{BAT}		90+		
		V _{BUS} = 5 V, FULL state, V _{BAT} =3.8, V _{SYS} = V _{SYS_FULL_REG} , I _{CHG} = 0 A, I _{SYS} =20 mA, measured from V _{BUS} to V _{SYS}		TBD		

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pulse skipping entry threshold current	I_SKIP_Entry			100		mA
Pulse skipping exit threshold current	I_SKIP_Exit			350		mA
Charger DCDC switching frequency		DCDC_FSW="01"		1.5		kHz
		DCDC_FSW="00"		1		kHz
On-resistance of the high voltage switches	R_DSON_HV			15		mΩ
On-resistance of the low voltage switches	R_DSON_LV			15		mΩ
Peak current limit	I_LIM_PEAK	PEAK_ILIM="11"		9		A
		PEAK_ILIM="00"		6		A
Peak current limit accuracy	I_LIM_PEAK_ACC		-20		+20	%

Note 1 Temperature range for these items is 0C to 85C

4.4.1 Charger Reverse boost

Table 13: Charger DCDC Reverse Boost

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage range	V _{SYS}	min{V _{SYS_MIN} } to max{V _{BATT_CHG} }	3.0		4.6	V
Output voltage	V _{BST_OTG}			5		V
	V _{BST_FLASH}	DCDC_REV_VOUT="1101" DCDC_REV_VOUT="0000"		6 4.8		V
Output overvoltage	V _{BST_OTG_OV}	Rising threshold		6		
Accuracy of output voltage regulation	V _{IN_REV_ACC}	Including ripple, static line and static load regulation	-5		+5	%
Maximum output current	I _{BST_MAX}		2			A
Reverse peak current limit	I _{Bus_REV_PEAK_LIM}	DCDC_REV_PEAK_LIM="11"		7		A
		DCDC_REV_PEAK_ILIM="00"		4		
Reverse current limit	I _{Bus_REV_LIM}	I _{Bus_REV_LIM} "111"	2000		2400	mA
		I _{Bus_REV_LIM} "000"	500		600	mA
Maximum duration of a reverse current limit condition	t _{REV_LIM_MAX}	T_REV_ILIM_MAX="11"		100		ms
		T_REV_ILIM_MAX="10"		10		
		T_REV_ILIM_MAX="01"		1		
		T_REV_ILIM_MAX="00"		∞		
Efficiency	η _{REV}	V _{BATT} =3.8 V, I _{REV} = 2A		89		%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		$V_{BATT}=3.8\text{ V}$, $I_{REV} = 1\text{ A}$		88		
PFM mode entry current	$I_{BST_OTG_PFM_ENTRY}$			200		mA
PFM mode exit current	$I_{BST_OTG_PFM_EXIT}$			400		mA
Switching frequency	f_{SW_REV}			1.5		MHz
Transient load regulation	V_{TR_LD}	$V_{BATT}=3.8\text{ V}$, $I_{BST_OTG}=0\text{ A}$ to $I_{BST_OTG_MAX}$, 100 mA/ μs	-500			mV
	$V_{TR_LD_REL}$	$V_{BATT}=3.8\text{ V}$, $I_{BST_OTG}=I_{BST_OTG_MAX}$ to 0 A, 100 mA/ μs			+500	mV

4.5 Charger

Table 14: Charger

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Re-charge threshold	V_{BATT_RECHG}	Falling threshold $V_{BAT_RECHG} = "11"$		$V_{BAT_CHG} - 240\text{ mV}$		
		Falling threshold $V_{BAT_RECHG} = "00"$		$V_{BAT_CHG} - 100\text{ mV}$		
Re-charge threshold deglitch time	$t_{D_BATT_RECHG}$			100		ms
Charge termination current threshold	I_{BATT_TERM}	$IBATT_TERM = "111"$		450		mA
		$IBATT_TERM = "000"$		100		mA
Termination current deglitch delay	$t_{D_BATT_TERM}$			50		ms
Charge termination current accuracy	$I_{BATT_TERM_ACC}$	$IBATT_TERM = "111"$	360		540	mA
End-of-charge (EOC) detection time	t_{EOC}	$T_{EOC} = "111"$		70		min
		$T_{EOC} = "001"$		10		
Pre-charge timeout	t_{OUT_PRE}	$TIMEOUT_PRE = "11"$		60		min
		$TIMEOUT_PRE = "00"$		15		
CC charging timeout	t_{OUT_CCCV}	$TIMEOUT_CCCV = "111"$		18		h
		$TIMEOUT_CCCV = "000"$		2		
Watchdog Timer	T_{WD}	$CHG_TIMER_CTRL_B = 0xFF$		4		min

4.6 Charger Pre-charge current source

Table 15: Pre-charge

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Dead-batt current	I _{BAT_{_dead}}	0 < V _{BAT} < V _{BAT_short}		50		mA
Pre-charge current	I _{BATT_PRE}	I _{BAT_{_PRE}} ="11"		500		mA
		I _{BAT_{_PRE}} ="00"		50		
Pre-charge current regulation accuracy	I _{BATT_PRE_ACC}	I _{BATT_{_PRE}} ="1", V _{SYS_MIN_REG} = 3.5 V, V _{BATT} =3.25 V	-20		+20	%

4.7 Charger Battery switch

Table 16: Battery Switch

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Battery switch on resistance	R _{DSON_BATT_SW}	Measured pin-to-pin, V _{BUS} =5 V, V _{BATT} =3.8 V		6.5		mΩ
Battery isolation duration	t _{BATT_ISO_SHORT}			750		ms
Battery isolation entry delay	t _{PRE_BATT_ISO}	T _{PRE_BATT_ISO} ="11"		10		s
		T _{PRE_BATT_ISO} ="01"		500		ms

4.8 Flash LED driver

Table 17: Flash Driver

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Source ²	I _{source}	Per Channel	0		1	A
Current accuracy	I _{sink_acc}	Vcentre to FDRV >1.2V		±8.5		%
Open circuit protection	V _{op_LED}	Vcentre to FLASH_LED*	206		1120	mV
Short circuit protection	V _{sc_LED}	FLASH_LED* to GND	-10%	900	+10%	mV
Current setting LSB ^{1&2}	I _{DAC}	5 Bit I DAC (flash setting) max 0x14		50		mA
		5 Bit I DAC (torch setting, max 0x14)		25		mA
Current accuracy	I _{acc}		-8.5		8.5	%
Current source headroom		Vcentre to FLASH_LED1/2 pin at 1A	1.2			V
Safety timer	T _{FL_SAFE}		10		1000	ms

Note 1) Both channels are switched between modes at the same time, it is not possible to have channels in different modes at the same time i.e. it is not possible to set channel 1 to torch mode and channel 2 to flash mode at the same time.

Note 2) Channel 1 can be set to a DAC value of 0x1E (1.5A) if channel 2 has a setting of ≤ 0x0A

4.9 WLED & Boost

Table 18: WLED & Boost

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Cout ³			-30%	2.2	+30%	μF
ESR _{COUT}				10		mΩ
Inductor				4.7		μH
C _z (compensation Cap)				1		nF
Sink voltage for both strings ¹	V _{sink}	Vref_fb<1:0> 2bit setting Forced IDAC selection, VSYS=3.8V, Iout =10mA	-5%	0.4 0.6 0.8 1.0	+20%	V
Over Voltage protection	OVP	Vref_ovp<0> 1bit setting	-5%	31 26	+5%	V
Over current protection	OCP	Vref_ocp<1:0> 2bit setting	-25%	1.5 1.8 1.9 2.1	+25%	A
Current accuracy (typical)	IDAC _{ACC}	VSYS = 3.8V, Tj =25°C, Iout = 10mA to 40mA	-2		2	%
Current accuracy (supply) ²	IDAC _{ACC}	VSYS = 3V to 4.6V, Tj =25°C, Iout = 10mA to 40mA	-3.5		3.5	%
Current accuracy (temperature) ²	IDAC _{ACC}	VSYS = 3.8V, Tj =-40°C to 125°C, Iout = 10mA to 40mA	-3.5		3.5	%
Current accuracy	IDAC _{ACC}	VSYS = 3.6V to 4.6V, Tj =25°C to 85°C, Iout = 10mA to 40mA	tbd		tbd	%
Boost efficiency		VSYS=3.8V, Vout=19.8V Iout _{total} = 40mA		88		%
PWM control input frequency			25		35	K Hz
Max current sink	IDAC _{MAX}			40		mA

Note 1) Vsink includes the voltage drop of PWM switch, which is not sensed by the Booster

Note 2) Supply/Temperature range introduces 1.5% deviation on absolute current accuracy

Note 3) This is not a normal mode of operation and care must be taken in inductor and schottky diode selection to ensure the peak current can be supported without saturation within the over current protection range. The Boost output capacitance must also be increased.

4.10 Display Bias/Supply

Table 19: Display Boost

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Positive Output	VBST	Boost converter running (Vsyst ≤ VBST-0.6)	4.3	5.3	6.4	V
Output setting step size				100		mV
Output current	IBST				200	mA
Line regulation	VBST _{line}	Vsys=3.8V to 4.6V, Vpos=5.4V, Iout = 40mA, forced PWM		3		mV



Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output load regulation	VBST _{load}	Vsys=3.8V, Vpos=5.4V, ΔIout = 80mA, forced PWM		3.5		%/A
Vpos discharge resistors	VBST _{Rd}			40		Ω
Boost current limit	Ilim _{BST}	3 bit register setting	0.5			A
			0.75			
			1			
			1.25			
			1.375			
			1.5			
			1.625			
			1.75			
Boost switching freq	F _{SWbst}			1		MHz

Table 20: Display Negative Charge Pump

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Negative charge pump Output	DNEG		-6.0	-5.0	-4.0	V
VCPneg accuracy	DNEG _{acc}	VBST=5.8V, VCPneg=-5.4V, Iout=40mA	-1	1		%
VCPneg voltage step	DNEG _{STEP}			100		mV
VCPneg output current	I _{neg}			40	80	mA
VCPneg line regulation	DNEG _{line}	V _{SYS} = 3.6V to 4.6V, VBST=5.3V, VCPneg= -5.0V, Iout = 40mA		4		mV
VCPneg load regulation	DNEG _{load}	Vsys 3.8V, VBST=5.3V, VCPneg= -5.0V, ΔIout =1mA to 40mA		6		%/A
VCPneg discharge resistors	DNEG _{Rd}			40		Ω
Negative charge pump switching frequency	F _{cp}			1		MHz
Display bias efficiency		Vsys=3.8V, Vpos=5.0V, Vneg=-5.0V, Iout 40mA between Vpos & Vneg		88		%

Table 21: Display LDO

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Display Positive Supply (LDO output voltage)	DPOS	connected after Boost V _{boost} > V _{LDO}	4.0	5.0	6.0	V
Output voltage setting step	DPOS _{step}			100		mV
Output Voltage accuracy	DPOS _{acc}	V _{SYS} =3.8V, V _{out} =5.4V, I _{out} =40mA	-1		1	%
Line regulation	DPOS _{LINE}	V _{SYS} =3V to 4.6V, I _{out} =40mA		3		mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Load regulation	DPOS _{LOAD}	V _{sys} =3.8V, ΔI _{out} =0mA to 40mA		3.5		mV
Output discharge resistor	DPOS _{RD}			40		Ω
Current limit	DPOS _{Ilim}			0.2		A

4.11 Core Buck

Table 22: Core Buck

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output capacitor	C _{OUT}	Including voltage and temperature coefficient	-40%	22	+30%	µF
Output capacitor ESR	C _{ESR}	f > 100 kHz		2		mΩ
Inductor value ¹	L _{PHASE}	Including current & temperature dependence Inductor range 0.1µH to 0.33µH	-50%	0.22	+20%	µH
Inductor resistance	L _{DCR}			30	50	mΩ
Buck output voltage ²	V _{BUCK}	I _{OUT} = 0 mA to I _{MAX}	0.3		1.57	V
Output voltage accuracy	V _{OACC}	incl. static line/load reg V _{OUT} ≥ 1 V	-1.5		+1.5	%
		incl. static line/load reg V _{OUT} < 1 V	-15		15	mV
Load regulation transient ³	VTR _{LOAD}	I _{OUT} = 0 to 5 A, dI/dt = 3A/1 µs PWM, V _{OUT} = 1 V		-4% /+6%		%
Line regulation transient	VTR _{LINE}	V _{SYS} = 3 to 3.6V, dt = 1us I _{OUT} = I _{MAX}		10		mV
Max resistance PCB for remote sensing	R _{PCB}	to sense connection at point of load			10	mΩ
Max inductance PCB for remote sensing	L _{PCB}	to sense connection at point of load			10	nH
Output current capability	I _{MAX}		5			A
Current limit (programmable)	I _{LIM}	BUCKx_ILIM=1000 (default)		8.4		A
Quiescent current in synchronous rectification mode	I _{QPWM}	No load, V _{SYS} = 3.7V		TBD		mA
Switching frequency	f _{SW}	after trimming		4		MHz
Turn on time	T _{ON}	After BUCKx_EN = high		50		µs
Output pull down resistor	R _{PD}	the LX node @0.5 V, (see BUCKx_PD_DIS)		150		Ω
PMOS on-resistance	R _{ON_PMOS}	V _{SYS} = 3.7V		25		mΩ
NMOS on-resistance	R _{ON_NMOS}	V _{SYS} = 3.7V		10		mΩ
Efficiency in synchronous rectification mode	η _{PWM}	I _{OUT} = 5% to 80% I _{MAX} V _{SYS} = 3.6V, V _{OUT} = 1 V With recommended inductor		TBD		%
PFM Mode						
Quiescent Current in PFM mode	I _{QPFM}	No load, V _{SYS} = 3.7V (Including service blocks)		88		µA
Efficiency in PFM mode	η _{PFM}	I _{OUT} = 10 mA, V _{SYS} = 3.6V V _{OUT} = 1 V		80		%

Note 1) Buck configuration setting changes are required for alternative inductor values

Note 2) Programmable in 10mV increments

Note 3) Additional to the dc accuracy. For Vdd=3.7V. The value is intended measured directly at COUT. In case of remote sensing, parasitic of PCB and external components may affect this value.

Note: Core buck performance figures quoted in Table 22 assume a 0.22 μ H Inductance.

4.12 Internal supplies

4.12.1 AVDD

Table 23: AVDD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal supply	V_{AVDD}	$V_{IN} > V_{IN_UVLO}$		4.0		V
		$V_{IN} < V_{IN_UVLO},$ $V_{BATT} > V_{BATT_UV}$		$V_{BATT} - V_{DROPOUT}$		
Output capacitance	C_{AVDD}	Effective capacitance, including DC-bias and temperature variation		4.7		μF

4.13 Digital I/O

Table 24: I/O

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage (SCL, SDA, nCE)	V_{IH}		1.26			V
Input low voltage (SCL, SDA, nCE)	V_{OL}				0.54	V
Output low voltage (nIRQ, SDA)	V_{OL}	Sink current 5 mA			0.3	V
Input capacitance (SCL, SDA, nCE)	C_{IN}				10	pF
SDA sink current	I_{SDA_SINK}	V_{IL}		20		mA

Note 2 nIRQ must not be pulled above VDDIO by the external pullup to prevent leakage.

4.14 2-wire interface timing

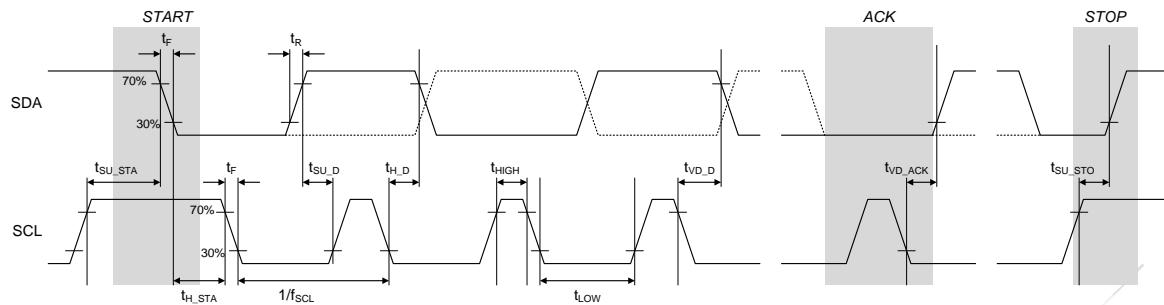


Figure 3: 2-wire interface timing

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85^\circ\text{C}$, $V_{IN} = 4.3$ to 11 V , $V_{BAT} = 2.6$ to 4.4 V

Table 25: 2-wire interface electrical characteristics

Parameter	Symbol	Test conditions	Min	Max	Unit
Bus free time from STOP to START condition	t_{BUF}		0.5		μs
Standard, fast, and Fast-plus modes					
Bus line capacitive load	C_B			150	pF
SCL clock frequency	f_{SCL}	Note 3	0	1000	kHz
Start condition setup time	t_{SU_STA}		0.26		μs
Start condition hold time	t_{H_STA}		0.26		μs
SCL low time	t_{W_CL}		0.5		μs
SCL high time	t_{W_CH}		0.26		μs
2-wire SCL and SDA rise time	t_R			120	ns
2-wire SCL and SDA fall time	t_F			120	ns
Data setup time	t_{SU_D}		50		ns
Data hold-time	t_{H_D}		0		ns
Stop condition setup time	t_{SU_STO}		0.26		μs
Data valid time	$t_{V_D_D}$			0.45	μs
Data valid acknowledge time	$t_{V_D_ACK}$			0.45	μs
Spike suppression (SCL, SDA)	t_{SP}	Fast/fast+ mode		50	ns

Note 3 Minimum clock frequency is 10 kHz if 2WIRE_TO is enabled

5 Package WLCSP (With no back side coating)

5.1 Ball out

	10	9	8	7	6	5	4	3	2	1	
A	CHG_VCENT	CHG_LX	CHG_LX	CHG_LX	CHG_LX	CHG_LX	CHG_LX	CHG_LX	CHG_LX	CHG_PGND	A
B	CHG_VCENT	CHG_VCENT	CHG_VCENT	CHG_VCENT	CHG_LX	CHG_LX	CHG_PGND	CHG_PGND	CHG_PGND	CHG_PGND	B
C	CHG_VCENT	CHG_VCENT	CHG_AGND	CHG_PVDD	CHG_BT	CHG_AVDD	CHG_AGND	CHG_PVPP	CHG_VSYS	CHG_VSYS	C
D	CHG_VBUS	CHG_VBUS	CHG_AGND	CHG_AGND	CHG_AGND	CHG_AGND	CHG_AGND	CHG_AGND	CHG_BAT	CHG_VSYS	D
E	CHG_VBUS	CHG_VBUS	CHG_AGND	CHG_AGND	CHG_AGND	CHG_AGND	CHG_AGND	CHG_BAT	CHG_BAT	CHG_VSYS	E
F	CHG_nCE	CHG_AGND	VDDIO	CHG_nIRQ	CHG_AGND	CHG_AGND	CHG_GPIO2	CHG_BAT	CHG_BAT	CHG_BAT	F
G	SCL	SDA	CHG_nONKEY	CHG_AGND	CHG_AGND	CHG_AGND	CHG_AGND	CHG_BAT	CHG_BAT	CHG_BAT	G
H	FLASH_LED2	FLASH_IN	FLASH_TRIG	DISP_AGND	DISP_AGND	WLED_PGND	BUCK_nIRQ	BUCK_FBP	BUCK_FBN	WLED_COMP	H
J	FLASH_LED1	FLASH_IN	WLED_PWM	DISP_VSYA	DISP_VSYSP	WLED_PGND	DISP_nIRQ	BUCK_PGND	BUCK_PGND	BUCK_PGND	J
K	DISP_OUTN	CP_PGND	DISP_OUTP	WLED_IDAC	WLED_SNS	WLED_LX	BUCK_EN	BUCK_LX	BUCK_LX	BUCK_LX	K
L	CP_CFLYN	CP_CFLYN	CP_CFLYP	BOOST_OUT	BOOST_LX	BOOST_PGND	BUCK_nRST	BUCK_LX	BUCK_VSYSP	BUCK_VSYSP	L
	10	9	8	7	6	5	4	3	2	1	

(BOTTOM View)

Figure 4: WLCSP Ball out

Table 26: Ball out pin description

Ball No.	Pin name	Type	Max V (V)	Max I (A)	Description
A1	CHG_PGND	VSS	0.5	0.6	Charger power ground
A2	CHG_LX	AI0	16	0.3	Charger switching node
A3	CHG_LX	AI0	16	0.3	Charger switching node
A4	CHG_LX	AI0	16	0.3	Charger switching node

Ball No.	Pin name	Type	Max V (V)	Max I (A)	Description
A5	CHG_LX	AIO	16	0.3	Charger switching node
A6	CHG_LX	AIO	16	0.3	Charger switching node
A7	CHG_LX	AIO	16	0.3	Charger switching node
A8	CHG_LX	AIO	16	0.3	Charger switching node
A9	CHG_LX	AIO	16	0.3	Charger switching node
A10	CHG_VCENT	AIO	16	0.5	Input to the DC-DC converter. Bypass to CHG_PGND with C _{CENTER} . Output of the DC-DC in Flash Mode / OTG.
B1	CHG_PGND	VSS	0.5	0.6	Charger power ground
B2	CHG_PGND	VSS	0.5	0.6	Charger power ground
B3	CHG_PGND	VSS	0.5	0.6	Charger power ground
B4	CHG_PGND	VSS	0.5	0.6	Charger power ground
B5	CHG_LX	AIO	16	0.3	Charger switching node
B6	CHG_LX	AIO	16	0.3	Charger switching node
B7	CHG_VCENT	AIO	16	0.5	Input to the DC-DC converter. Bypass to CHG_PGND with C _{CENTER} . Output of the DC-DC in Flash Mode / OTG.
B8	CHG_VCENT	AIO	16	0.5	Input to the DC-DC converter. Bypass to CHG_PGND with C _{CENTER} . Output of the DC-DC in Flash Mode / OTG.
B9	CHG_VCENT	AIO	16	0.5	Input to the DC-DC converter. Bypass to CHG_PGND with C _{CENTER} . Output of the DC-DC in Flash Mode / OTG.
B10	CHG_VCENT	AIO	16	0.5	Input to the DC-DC converter. Bypass to CHG_PGND with C _{CENTER} . Output of the DC-DC in Flash Mode / OTG.
C1	CHG_VSYS	AIO	6	0.8	Internal battery switch connection. Connect to Output of DC-DC converter VSYS. Bypass to CHG_PGND with C _{OUT} .
C2	CHG_VSYS	AIO	6	0.8	Internal battery switch connection. Connect to Output of DC-DC converter VSYS. Bypass to CHG_PGND with C _{OUT} .
C3	CHG_PVPP	PS	9	0.1	Internal supply. Bypass to CHG_BAT with C _{PVPP} .
C4	CHG_AGND	VSS	0.5	0.1	Analog ground
C5	CHG_AVDD	PS	6	0.5	Charge analog supply
C6	CHG_BT	AI	22	0.1	Gate driver supply of the DC-DC converter, Bypass to CHG_LX with C _{BT}
C7	CHG_PVDD	PS	6	0.5	Internal supply. Bypass to PGND with C _{PVDD} .



Ball No.	Pin name	Type	Max V (V)	Max I (A)	Description
C8	CHG_AGND	VSS	0.5	0.1	Analog ground
C9	CHG_VCENT	AIO	16	0.5	Input to the DC-DC converter. Bypass to CHG_PGND with C _{CENTER} . Output of the DC-DC in Flash Mode / OTG.
C10	CHG_VCENT	AIO	16	0.5	Input to the DC-DC converter. Bypass to CHG_PGND with C _{CENTER} . Output of the DC-DC in Flash Mode / OTG.
D1	CHG_VSYS	AIO	6	0.8	Internal battery switch connection. Connect to Output of DC-DC converter VSYS. Bypass to CHG_PGND with C _{OUT} .
D2	CHG_BAT	AIO	6	0.6	Battery connection
D3	CHG_AGND	VSS	0.5	0.1	Analog ground
D4	CHG_AGND	VSS	0.5	0.1	Analog ground
D5	CHG_AGND	VSS	0.5	0.1	Analog ground
D6	CHG_AGND	VSS	0.5	0.1	Analog ground
D7	CHG_AGND	VSS	0.5	0.1	Analog ground
D8	CHG_AGND	VSS	0.5	0.1	Analog ground
D9	CHG_VBUS	PS	20	0.8	Input supply. Bypass to PGND with C _{IN} . Reverse boost/OTG load.
D10	CHG_VBUS	PS	20	0.8	Input supply. Bypass to PGND with C _{IN} . Reverse boost/OTG load.
E1	CHG_VSYS	AIO	6	0.8	Internal battery switch connection. Connect to Output of DC-DC converter VSYS. Bypass to CHG_PGND with C _{OUT} .
E2	CHG_BAT	AIO	6	0.6	Battery connection
E3	CHG_BAT	AIO	6	0.6	Battery connection
E4	CHG_AGND	VSS	0.5	0.1	Analog ground
E5	CHG_AGND	VSS	0.5	0.1	Analog ground
E6	CHG_AGND	VSS	0.5	0.1	Analog ground
E7	CHG_AGND	VSS	0.5	0.1	Analog ground
E8	CHG_AGND	VSS	0.5	0.1	Analog ground
E9	CHG_VBUS	PS	20	0.8	Input supply. Bypass to PGND with C _{IN} . Reverse boost/OTG load.
E10	CHG_VBUS	PS	20	0.8	Input supply. Bypass to PGND with C _{IN} . Reverse boost/OTG load.
F1	CHG_BAT	AIO	6	0.6	Battery connection
F2	CHG_BAT	AIO	6	0.6	Battery connection

Ball No.	Pin name	Type	Max V (V)	Max I (A)	Description
F3	CHG_GPIO2	DIO	6	0.1	Charger General Purpose I/O
F4	CHG_AGND	VSS	0.5	0.1	Analog ground
F5	CHG_AGND	VSS	0.5	0.1	Analog ground
F6	CHG_AGND	VSS	0.5	0.1	Analog ground
F7	CHG_nIRQ	DO	6	0.1	Active low. Interrupt request line to host for charger
F8	VDDIO	PS	6	0.1	Supply for digital I/O interfaces
F9	CHG_AGND	VSS	0.5	0.1	Analog ground
F10	CHG_nCE	DI	6	0.1	Active low. Charger chip enable
G1	CHG_BAT	AIO	6	0.6	Battery connection
G2	CHG_AGND	VSS	0.5	0.1	Analog ground
G3	CHG_AGND	VSS	0.5	0.1	Analog ground
G4	CHG_AGND	VSS	0.5	0.1	Analog ground
G5	CHG_AGND	VSS	0.5	0.1	Analog ground
G6	CHG_AGND	VSS	0.5	0.1	Analog ground
G7	CHG_AGND	VSS	0.5	0.1	Analog ground
G8	CHG_nONKEY	DI	6	0.1	On-key. Active-low. Tie CHG_nONKEY to VDDIO if not in use
G9	SDA	DIO	6	0.1	I2C data input/output
G10	SCL	DI	6	0.1	I2C clock input
H1	WLED_COMP	AIO	6	0.1	WLED compensation
H2	BUCK_FBN	AI	0.5	0.1	Negative feedback for core buck
H3	BUCK_FBP	AI	6	0.1	Positive feedback for core buck
H4	BUCK_nIRQ	DO	6	0.1	Active low. Interrupt request line to host for core buck
H5	WLED_PGND	VSS	0.5	0.5	Power ground of WLED
H6	DISP_AGND	VSS	0.5	0.1	Analog ground
H7	DISP_AGND	VSS	0.5	0.1	Analog ground
H8	FLASH_TRIG	DI	6	0.1	Trigger real flash
H9	FLASH_IN	AI	6	1	Flash driver input, route to CHG_VCENT on PCB
H10	FLASH_LED2	AI	6	1	Flash led idac current source, route to LED2 (warm) anode

Ball No.	Pin name	Type	Max V (V)	Max I (A)	Description
J1	BUCK_PGND	VSS	0.5	1.25	Power ground of core buck
J2	BUCK_PGND	VSS	0.5	1.25	Power ground of core buck
J3	BUCK_PGND	VSS	0.5	1.25	Power ground of core buck
J4	DISP_nIRQ	DO	6	0.1	Active low. Interrupt request line to host for display
J5	WLED_PGND	VSS	0.5	0.5	Power ground of WLED
J6	DISP_VSYSP	PS	6	0.1	Power supply for display
J7	DISP_VSYSA	PS	6	0.1	Analog power for display
J8	WLED_PWM	DI	6	0.1	Pwm dimming control input for WLED
J9	FLASH_IN	AI	6	1	Flash driver input, route to CHG_VCENT on PCB
J10	FLASH_LED1	AI	6	1	Flash led idac current source, route to LED1 (cold) anode
K1	BUCK_LX	AIO	6	1.25	Core buck switching node
K2	BUCK_LX	AIO	6	1.25	Core buck switching node
K3	BUCK_LX	AIO	6	1.25	Core buck switching node
K4	BUCK_EN	DI	6	0.1	Enable core buck.
K5	WLED_LX	AIO	29	0.7	Switch node of WLED boost rail
K6	WLED_SNS	AI	29	0.1	WLED boost rail output voltage sense
K7	WLED_IDAC	AI	6	0.1	WLED string current sink terminal
K8	DISP_OUTP	AO	4.2	0.2	Positive display LDO Output
K9	CP_PGND	VSS	0.5	0.2	Power ground of Charge Pump rail
K10	DISP_OUTN	AO	-4.2	0.2	Negative Charge Pump Output
L1	BUCK_SYSP	PS	6	1.8	Power supply for core buck
L2	BUCK_SYSP	PS	6	1.8	Power supply for core buck
L3	BUCK_LX	AIO	6	1.25	Core buck switching node
L4	BUCK_nRST	DI	6	0.1	Active low. Triggers a soft shutdown and OTP re-load for core buck
L5	BOOST_PGND	VSS	0.5	0.5	Power ground of boost
L6	BOOST_LX	AIO	4.4	0.5	Boost switching node
L7	BOOST_OUT	AO	4.4	0.5	Boost rail output voltage
L8	CP_CFLYP	AIO	4.2	0.2	Positive terminal of Charge Pump flying capacitor

Ball No.	Pin name	Type	Max V (V)	Max I (A)	Description
L9	CP_CFLYN	AIO	-4.2	0.1	Negative terminal of Charge Pump flying capacitor
L10	CP_CFLYN	AIO	-4.2	0.1	Negative terminal of Charge Pump flying capacitor
A1	CHG_PGND	VSS	0.5	0.6	Charger power ground

Table 27: Pin type definition

Pin type	Description	Pin type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PS	Power supply		
VSS	Ground		

5.2 Package outline

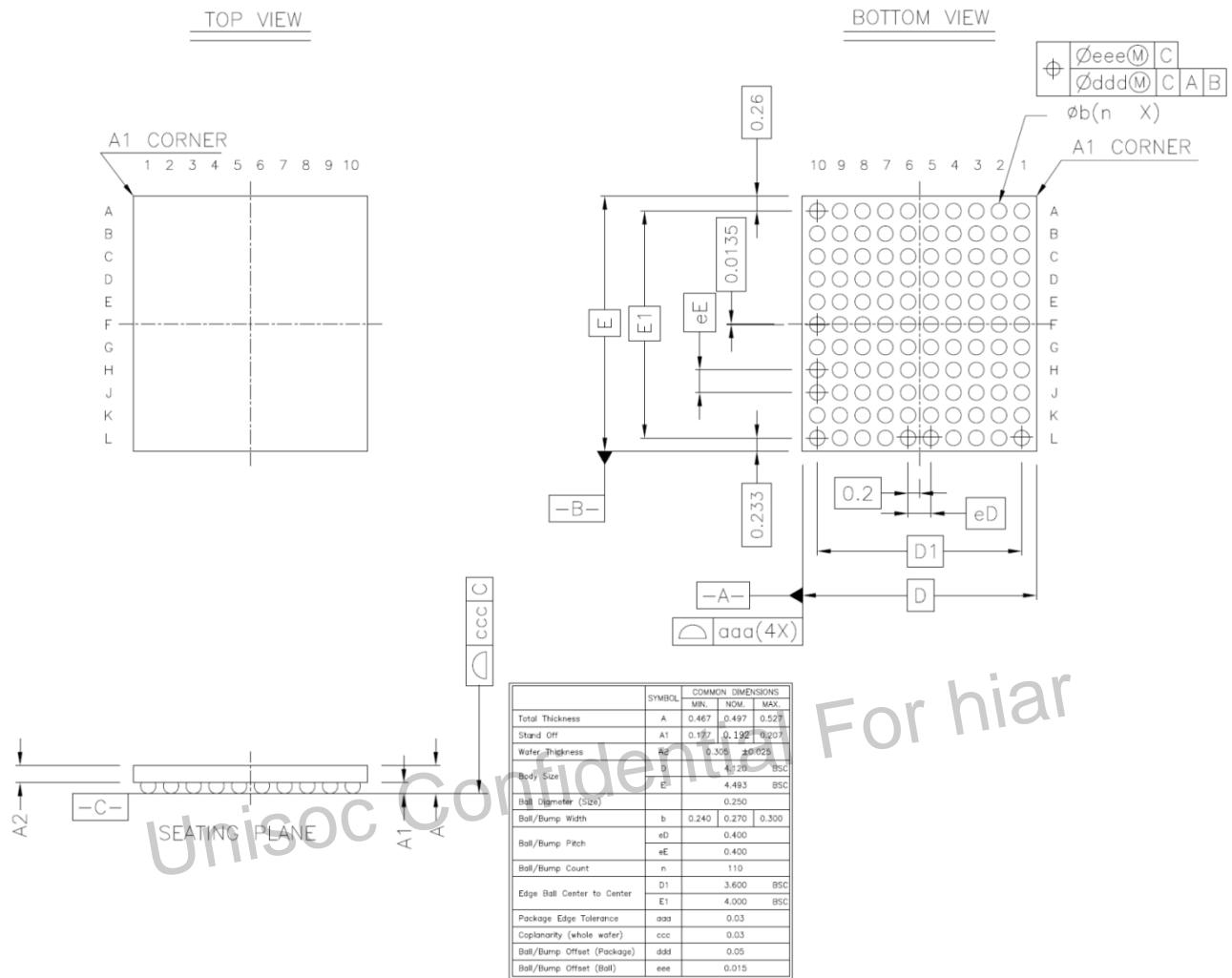


Figure 5: Package outline

5.3 List of external components

Module	Pin names	Quantity	Component	Nominal value	Unit	Package size	Rating	Note
DLDI	DISP_OUTP	1	cap	4.7	uF	0603	10V	
Charge Pump	DISP_OUTN	1	cap	4.7	uF	0603	10V	Old: 10uF; Cost down
	CP_FLYP to CP_FLYN	1	cap	2.2	uF	0603	10V	
B	BOOST_OUT	1	cap	0.1	uF	0201	16V	place closest to IC route on PCB top layer

Module	Pin names	Quantity	Component	Nominal value	Unit	Package size	Rating	Note
		1	cap	4.7	uF	0603	10V	
	BST_LX_IN	1	cap	4.7	uF	0603	10V	
	BOOST_LX	1	ind	4.7	uH	2520	1.3A	
WLED	WLED_SNS	1	cap	2.2	uF	0603	50V	2.2uF x 3 for overdrive and external-R sink modes
	WLED_LX_IN	1	cap	4.7	uF	0603	10V	10uF x 2 for overdrive and external-R sink modes
	WLED_LX	1	ind	4.7	uH	2520	1.5A	
	WLED_LX	1	SBD	1	A	SOD323HE	40V	3A for overdrive and external-R sink modes
	WLED_COMP	1	cap	1	nF	0201	6.3V	
Core Buck	BUCK_OUT	2	cap	22	uF	0603	6.3V	place closest to VDDARMO of WhaleK prefer X5R MLCC & 3-terminal cap
	BUCK_LX	1	ind	0.22	uH	2520	6.6A	Recommended! 0.33uH also can be used.
	BUCK_VSYSP	1	cap	0.1	uF	0201	10V	place closest to IC, route on PCB top layer route on PCB top layer
		1	cap	10	uF	0603	10V	prefer X5R MLCC
Flash Driver	FLASH_IN	1	cap	10	uF	0603	16V	10V to account for derating
Charger	CHG_LX	1	Ind	0.47	uH	2520	6A	
	CHG_VSYS	2	Cap	10	uF	0402	6.3V	
	CHG_BAT	1	Cap	1	uF	0402	6.3V	
	CHG_VCENT	1	Cap	22	uF	0805	16V	16V to account for derating
	CHG_PVDD	1	Cap	1	uF	0402	6.3V	
	CHG_AVDD	1	Cap	4.7	uF	0402	6.3V	
	CHG_PVPP	1	Cap	0.01	uF	0201	10V	
	CHG_VBUS	1	Cap	1	uF	0603	25V	
	CHG_BT	1	Cap	0.1	uF	0402	10V	
IO	DISP_nIRQ	1	Res	10	kΩ	0201	-	Pull-up Resistors
	BUCK_nIRQ	1	Res	10	kΩ	0201	-	Pull-up Resistors
	CHG_nIRQ	1	Res	10	kΩ	0201	-	Pull-up Resistors
	SCL	1	Res	10	kΩ	0201	-	Pull-up Resistors
	SDA	1	Res	10	kΩ	0201	-	Pull-up Resistors

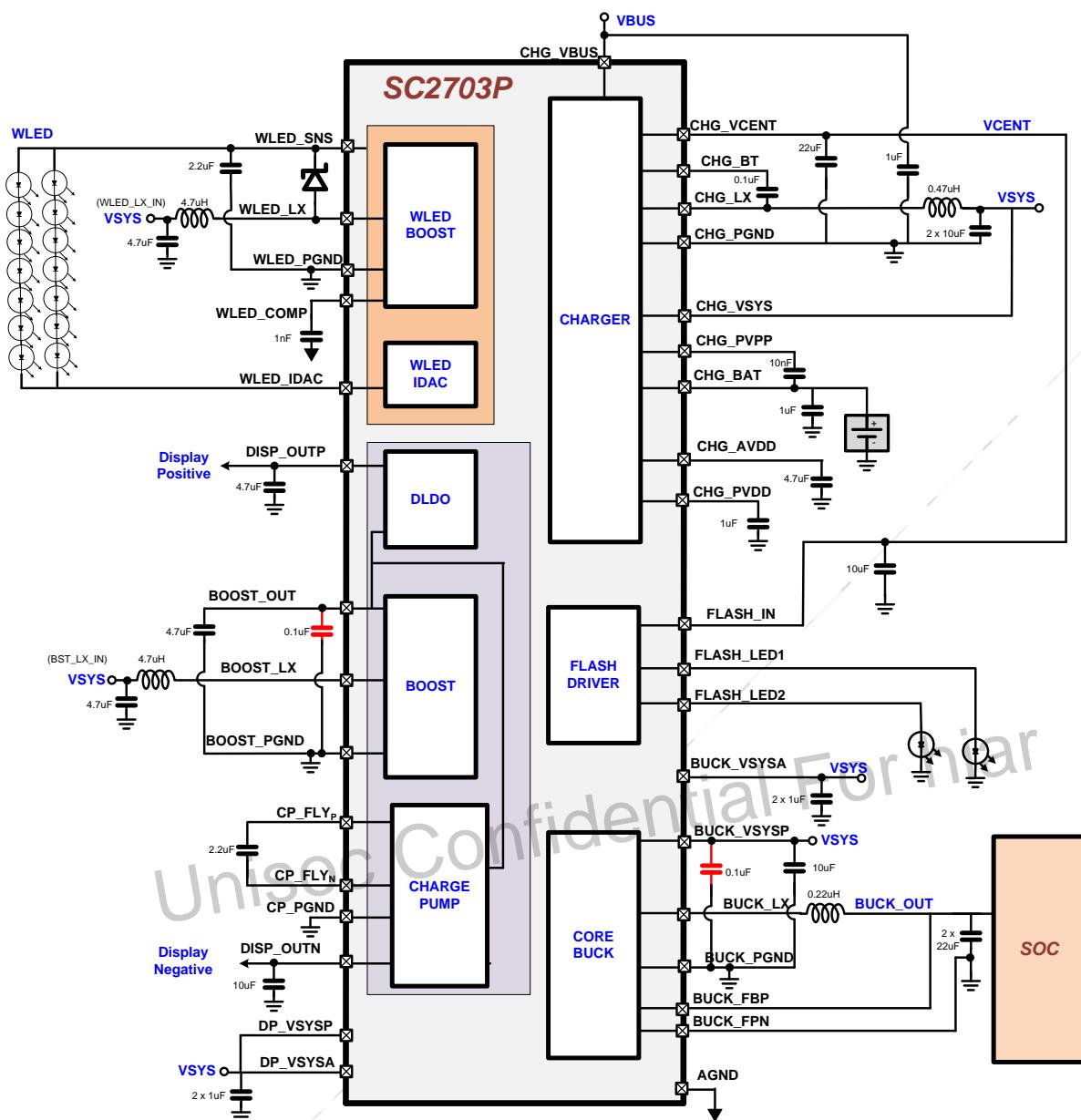


Figure 6: Application Schematic

6 Charger functional description

SC2703P is a switching charger for single-cell lithium-ion batteries. It supports input voltages up to V_{BUS_OVLO} which allows fast charging over the whole battery voltage range. In addition, SC2703P includes an advanced power path management system and input current limit.

The power path management takes care of supplying the system from the two available power sources (V_{BUS} or V_{BATT}) and seamlessly switching between them. SC2703P can also operate without a battery, or with a deeply discharged battery. In normal conditions, the system is always supplied from the external supply if one is available. If the system load is less than the input power, the surplus power is used for charging the battery. By contrast, if the system load is greater than the input power, the battery provides the difference, provided that the battery is not discharged. In the pre-charge phase system is only supplied by the DC-DC converter.

The charger uses the fast and reliable constant current (CC) and constant voltage (CV) method for charging single-cell Lithium-ion batteries, with maximum charging current of 3.5A. A new charging cycle is automatically started when a power supply is attached and the whole cycle is handled autonomously by the charger. The buck converter can operate in reverse mode, which enables SC2703P to supply 5V to V_{BUS} when USB OTG functionality is desired. In addition, when operating in reverse mode (boost mode), it can supply power to a down-stream flash driver.

6.1 Charger Flash/Torch support

Note : when supplied from the Reverse Boost mode of the charger in the Torch mode, the user settings for LED current (max 500mA) will be used to automatically switch the boost from skip (low power mode) to CCM (full power) mode around TBDmA.

Table 28: Charger Flash/Torch support

	Charging		Battery Only	
Condition	$V_{BUS} < 6V$	$V_{BUS} > 6V$	$V_{BAT} > 3V$	$V_{BAT} < 3V$ (E_LOWBAT)
FLASH_BOOST_EN (I2C)	Stop Charging (RCP/OVP OFF) Enable Boost Priority = sys/flash/charge		Enable Boost Priority = sys/flash	E_LOWBAT fault Clear FLASH_BOOST_EN
FLASH_EN (I2C & GPI)	Enable the actual flash event (only for flash events, torch will be enabled with TORCH_EN)			
TORCH_EN (I2C)	Continue Charging Priority = torch/sys/charge	Stop Charging (RCP/OVP OFF) Enable Boost Priority = torch/sys/charge	Enable Boost Enable Torch Priority = sys/torch	E_LOWBAT fault Clear TORCH_EN
OTG_EN (I2C)	Stop Charging Enable Boost Priority = sys/OTG		Enable Boost Priority = sys/OTG	E_LOWBAT fault Clear OTG_EN

The expected nine uses case scenarios are summaries below:-

- 1) **OTG Mode Only**
 - Driving peripheral OTG device

- Up to 2A
- 2) **Flash/Torch Mode Only**
- 2A of Flash/Torch load support
- 3) **OTG Mode -> OTG + Flash Mode**
- Concurrent OTG + Flash Operation
 - Automatic throttle of OTG ILIM to 500mA
 - 500mA OTG + up to 1.5A Flash (Total 2A Boost)
 - If Flash current set higher than 1.5A the OTG support will terminate and the device will only support Flash (uses case 2).
- 4) **OTG Mode -> OTG + Torch Mode**
- Concurrent OTG + Torch Operation
 - Automatic throttle of OTG ILIM to 1500mA
 - 1.5A OTG + up to 500mA Torch (Total 2A Boost)
- 5) **Flash/Torch Mode -> Flash/Torch + OTG Mode**
- Same as 3 and 4
- 6) **Torch Mode-> Torch + Charge Mode**
- Only for V_{BUS} < 6V
 - Concurrent Torch + Charge operation
 - Up to 500mA Torch + 3A Charging
 - It is important to note that in this scenario Torch takes higher priority than V_{SYS} if a Vindrop or Inlim event occurs.
- 7) **Charge Mode -> Charge + Torch Mode**
- Same as 6
- 8) **Charge Mode -> Flash Mode -> Charge Mode**
- Automatic transition between Charge & Flash Mode
 - Buck->Boost->Buck transition
- 9) **Charge + Torch Mode -> Torch Mode**
- On adapter unplug, LED current will be momentarily suspended before the Boost mode is enabled to support torch

6.2 Charger DC-DC converter

SC2703P features a high-efficiency step-down switching converter. The converter operates at a constant frequency, for a given input V_{BUS} voltage. All switches of the converter are integrated. The DC-DC can be supplied either from V_{BUS} or V_{BAT} and it can also operate without the battery.

The DC-DC converter features five operating modes:

- Input current regulation
- Charge current regulation
- Battery voltage regulation
- V_{SYS} regulation
- Reverse boost

During charging, the input current loop, the battery current loop, and the battery voltage loop are all active simultaneously. However, only the one resulting in the lowest converter duty cycle is effective at a time. For example, during the constant current phase of charging, the charge current regulation loop is normally the effective loop.

The V_{SYS} regulation is only used in pre-charge and when the charging cycle completes.

A programmable peak current limit protects the embedded devices and the inductor. Exceeding the limit, causes the DC-DC converter to limit its duty cycle and an event is triggered.

The DC-DC converter runs under the control of the state machine. There are two control bits that affect the usage of the DC-DC converter: CHG_EN and DCDC_EN. If CHG_EN is asserted but DCDC_EN is de-asserted the DC-DC converter is only enabled when charging is active. Correspondingly, if charging is disabled but DCDC_EN is still asserted, the DC-DC converter is enabled to supply the system. Typically, DCDC_EN should be asserted. The operation of the CHG_EN and DCDC_EN is explained in detail in section 12.3.

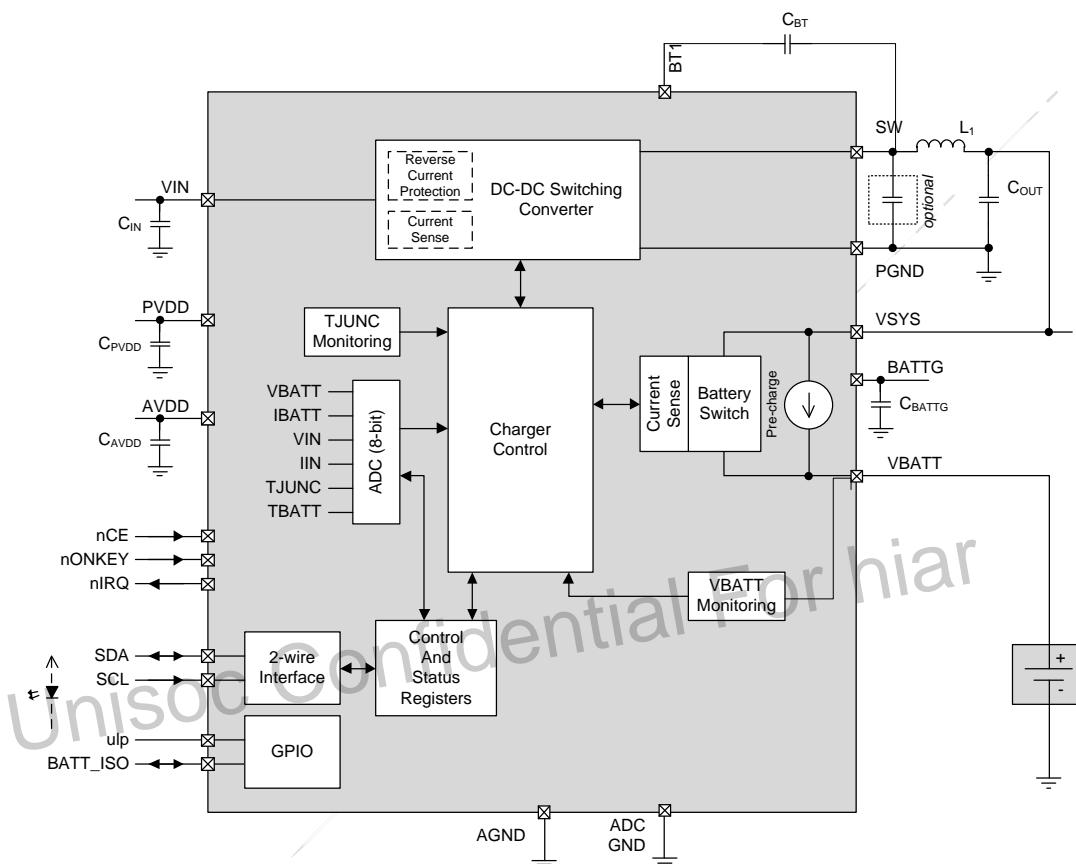


Figure 7: Charger Block diagram

6.2.1 Switching frequency

The nominal switching frequency of the DC-DC converter can be selected with the DCDC_FSW register.

The switching frequency can be dynamically adapted to the operation conditions. This means that during charging, while the battery voltage increases, the switching frequency can be automatically reduced based on the difference of V_{BUS} and V_{SYS} . The automatic adaptation is enabled from the DCDC_FSW_AUTO register.

6.2.2 Light load operation

A skip mode is implemented that further improves the efficiency below I_{SKIP_ENTRY} . When the load current drops below I_{SKIP_ENTRY} the converter automatically enters pulse skipping mode. Normal switching is resumed automatically when the current increases above I_{SKIP_EXIT} .

6.2.3 Input current limit

An average input current limit is provided to control the input power. The current limit can be set based on the capabilities of the wall-plug adaptor or the current rating of the adaptor cable. For example, in a system following the USB battery charging specification (BCS) the input current limit is set from 100 mA to 1.5 A, whereas in a system using USB Type-C connectors and cables the current limit can be set as high as 3A [2][3].

The input current limit is programmed in the IIN_LIM0 and IIN_LIM1 registers. The effective input current limit is selected from the IIN_LIM_SEL register. A block diagram depicting the input current limit is depicted in Figure 8. The DC-DC converter has a built-in sensing element that provides a measure of the input current. This is compared to the input current limit setting. If the input current limit is exceeded, the DC-DC continues to run normally but its duty cycle is limited. Also when the limit is exceeded, an event is triggered. When the input current limit is exceeded, the DC-DC converter moves to input current regulation mode, where the battery current or the battery voltage are not regulated by the DC-DC. They are determined by the system load and the impedance of the battery. However, as soon as the battery current regulation loop or the battery voltage regulation loop results in a lower duty cycle than the input current regulation loop, they will automatically become the effective regulation loop.

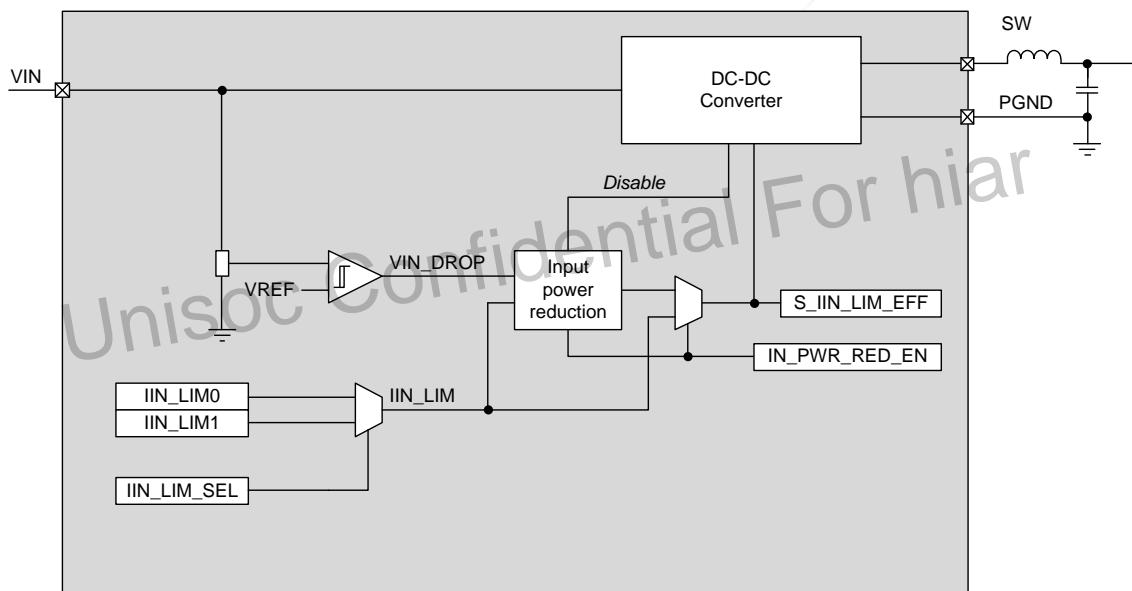


Figure 8: Structure of the input current limit block

6.2.3.1 Slew rate control

The input current limit is associated with a programmable slew rate control. Whenever the DC-DC converter is enabled or the input current limit setting is changed, the input current changes in a controlled manner in accordance to the slew rate programmed in the IBUS_LIM_SLEW register.

If the output power of the DC-DC converter is less than the programmed input current limit allows, the DC-DC converter never crosses the input current limit during the slew. For example, the battery current regulation loop might become effective before the slew completes.

6.2.3.2 Input power reduction

In normal operation, the input current limit ensures that the input power drawn by SC2703P does not exceed the capabilities of the travel adaptor or the cable and connectors. However, it is possible

that the input current limit is programmed too high. SC2703P is equipped with an automatic input power reduction feature that can handle such a situation and ensure safety during charging.

The input power reduction is an extension to the normal under- and overvoltage monitoring. A drop in V_{BUS} indicates that the V_{BUS} supply is weaker than expected or the charging cable has higher impedance than expected. When V_{BUS} drops below the V_{BUS_DROP} threshold, an event is triggered (E_VBUS_DROP), and the input power of the DC-DC converter is automatically reduced by adjusting the input current limit. A block diagram depicting the input current limit is depicted in Figure 8. The input current limit reduction will force the DC-DC converter in to the input current regulation mode described in section 6.2.3.

The input current limit is reduced until V_{BUS} rises back above V_{BUS_DROP} . The reduction rate can be controlled from the IBUS_DROP_AMOUNT and IBUS_DROP_INTERVAL registers. The reduced input current limit is then maintained until the V_{BUS} supply is removed. If the I_{in_LIM} reduction is not fast enough and V_{BUS} drops below V_{BUS_UVLO} , the DC-DC converter is disabled and an event is triggered (E_VBUS_UVLO). It is expected that after disabling the DC-DC converter V_{BUS} will rise back above the V_{BUS_UVLO} threshold. Thereupon, the state machine reacts normally to the insertion of the V_{BUS} and the DC-DC converter is re-enabled but the I_{BUS_LIM} is set to the previous effective value, i.e., the value after the reduction. If the V_{BUS_UVLO} is hit also on the consecutive re-start, the I_{BUS_LIM} will be reduced by at least one step. The re-start cycle continues until the minimum value of the I_{in_LIM} is reached.

The input power reduction is enabled by setting the IBUS_PWR_RED_EN. If the function is not enabled, the DC-DC converter will be disabled when V_{BUS} drops below the V_{IN_DROP} threshold.

The status register S_IBUS_LIM_EFF reflects the effective input current limit after the input power reduction. If the input power reduction feature is disabled (IN_PWR_RED_EN=0), the register gives the value chosen with the IBUS_LIM_SEL register.

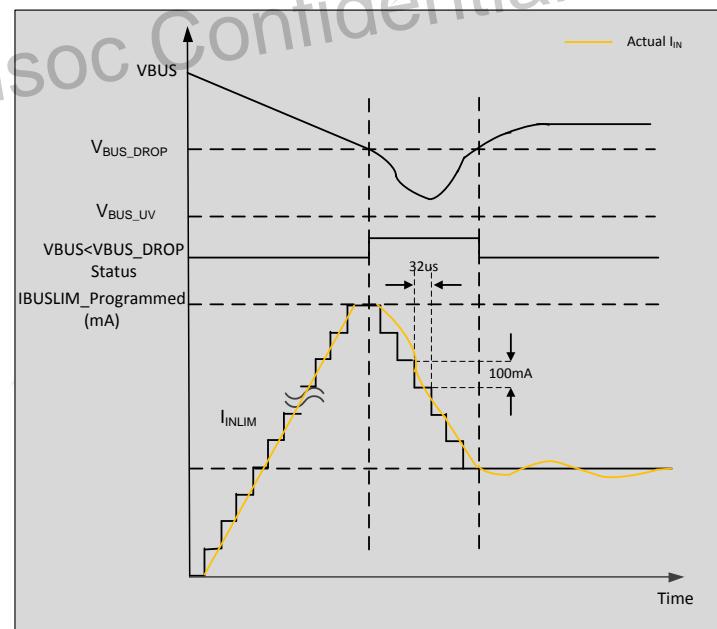


Figure 9: Expected current limit operation with a resistive cable

6.2.4 Charge current regulation

During constant current phase of charging (see section 6.3.1.2), the DC-DC converter regulates the current flowing in to the battery. The desired current is programmed in the IBATT_CHG register and

it should be set according to the capacity of the battery. The integrated battery switch is used for sensing the battery charge current.

6.2.4.1 Slew rate control

In the charge current regulation mode whenever the charge current setting is changed, the current is ramped to the target value at a rate defined in the IBATT_CHG_SLEW register. When the DC-DC is enabled, the slew rate control of the input current limit takes care of limiting the in-rush current. The slew rate control of the charging current is applied also to pre-charge current changes and changes caused by automatic junction temperature regulation.

6.2.5 Battery voltage regulation

During constant voltage phase of charging (see section 6.3.1.2), the DC-DC converter regulates the battery voltage. The battery voltage is sensed with differential inputs, as described in section 6.6. The target battery voltage is programmed in the VBATT_CHG register.

6.2.6 VSYS regulation

When the battery switch is open, the DC-DC regulates the voltage at the VSYS pin. This happens in the CHG_PRE state (see section 6.3.1.1), CHG_FULL state (see section 6.3.1.3), and if a L1_FAULT occurs during charging (see section 6.3.3). The target system voltage is programmed in the VSYS_MIN register. This voltage should be set to the minimum level where the system can operate normally.

6.2.7 Reverse boost operation

The DC-DC converter is capable of operating in a reverse boost mode, where V_{IN} is supplied from the battery. This lends itself to the USB OTG operation [2].

The reverse boost operation can only be enabled when the V_{BUS} is not supplied ($V_{BUS} < V_{BUS_SHORT}$) and the battery voltage is above V_{SYS_MIN} . Apart from the V_{BUS} monitor, SC2703P does not include any functionality for detecting if something is connected to V_{BUS} , such as attach detection protocol. This is left to the responsibility of the host processor. The boost is enabled by asserting the DCDC_OTG_BOOST register.

The reverse boost also features a soft-start feature that limits the output voltage slew rate (VBUS_REV_SLEW).

The peak current limit is operational also in the reverse boost mode of the DC-DC converter. The peak current limit setting is programmed in the DCDC_REV_PEAK_ILIM register. Exceeding the limit, causes the DC-DC converter to limit its duty cycle and an event is triggered.

The reverse boost also features a programmable OTG current limit. This feature is not required by the USB OTG standard but it is offered to enhance the safety of the target system. The desired limit is programmed in the IBUS_OTG_LIM register. When the OTG current limit is exceeded, the OVP and RCP FETs prevent the OTG current from increasing and, an event is triggered (E_IBUS_OTG_LIM). If the overcurrent condition persists for longer than $t_{OTG_LIM_MAX}$, the OVP and RCP FETs are automatically disabled and an event E_IIN_REV_LIM_MAX is triggered. The timer measuring the overcurrent condition starts automatically every time the OVP and RCP FETs enters the OTG current limit mode and resets automatically whenever the OTG current limit is no longer exceeded.

When in reverse boost mode, V_{BUS} is monitored against overvoltage ($V_{BUS_OTG_OV}$). If V_{BUS_OTG} exceeds the overvoltage for less than $t_{D_VBUS_OV}$ the DCDC_OTG_BOOST will pause switching. If V_{BUS_OTG} exceeds the overvoltage for longer than $t_{D_VBUS_OV}$ DCDC_OTG_BOOST_EN is cleared

which stops the DC-DC, and an event is triggered (E_VBUS_OTG_OV). Similarly, if the V_{BUS} is shorted during the OTG boost operation and it drops below V_{BUS_SHORT} and event E_VBUS_OTG_SHORT is triggered and the OVP and RCP FETs are disabled.

The light load efficiency of the reverse boost is improved with a pulse frequency modulation (PFM) mode. The converter switches automatically to the PFM mode when the load current drops below IBUS_OTG_PFM_TH. Normal switching is resumed automatically when the current increases above IBUS_OTG_PFM_TH+IBUS_OTG_PFM_HYS.

Light load efficiency mode is controlled by an internally generated FLASH_LP_EN signal when in Flash/Torch mode. This signal is asserted when the Flash/Torch current is programmed < 200mA to lower boost Iq. Output current capability is limited to 350mA when FLASH_LP_EN is high.

6.3 Charger

The charging algorithm used by SC2703P is the constant current-constant voltage (CCCV) charging method. The different charging phases are illustrated in Figure 11. The charging cycle is fully autonomous. If enabled via CHG_EN register, the charging starts automatically when an external supply with sufficient power is attached. The CHG_EN register can also be controlled with the nCE input as described in section 6.10.1. The charging runs until an end-of-charge is detected, the power supply is removed, or a charging fault occurs.

The state of the battery charger can be continuously monitored in the CHG_STAT status register. Whenever the status changes, an E_CHG event is triggered. A pre-requisite for starting charging is that SC2703P is in the CHG state. A safety timer is running whenever current is flowing into the battery and it will stop the charging in a case where a normal end-of-charge is not reached. Two separate timeout value can be programmed for pre-charge (TIMEOUT_PRE), and constant current, constant voltage phases (TIMEOUT_CCCV).

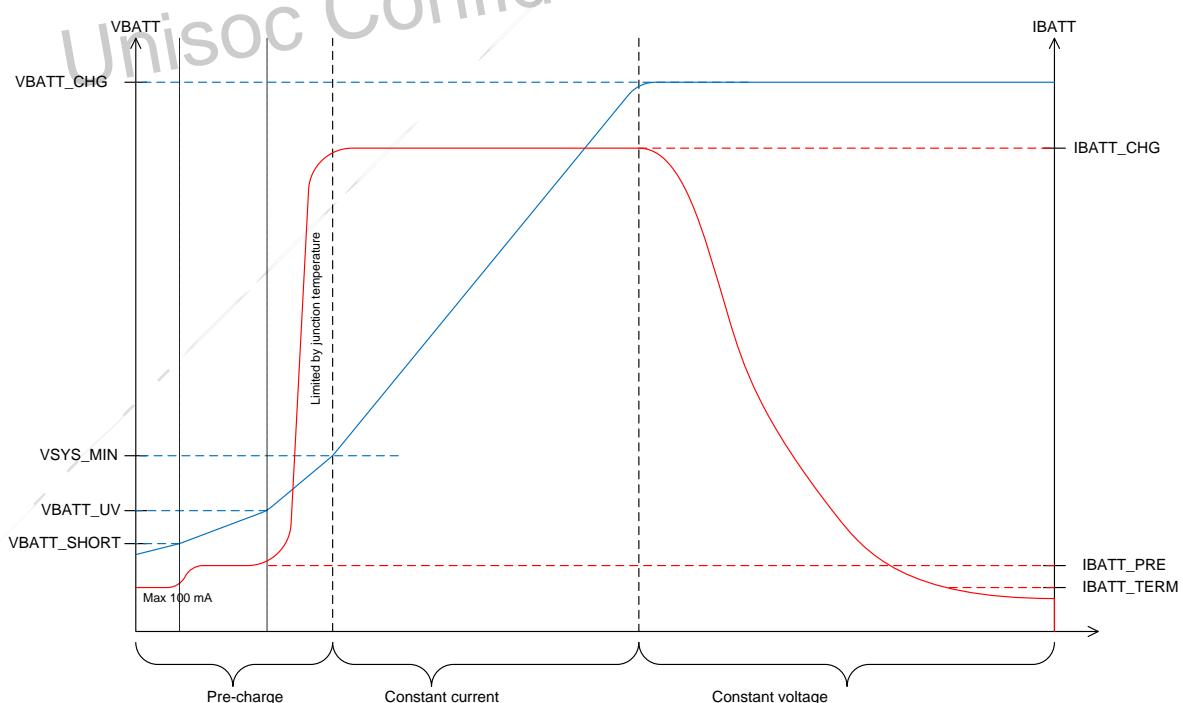


Figure 10: Constant current-constant voltage charging

6.3.1 Charging cycle

The charging state diagram is depicted in Figure 11. The main state machine of SC2703P is covered in section 12.3.

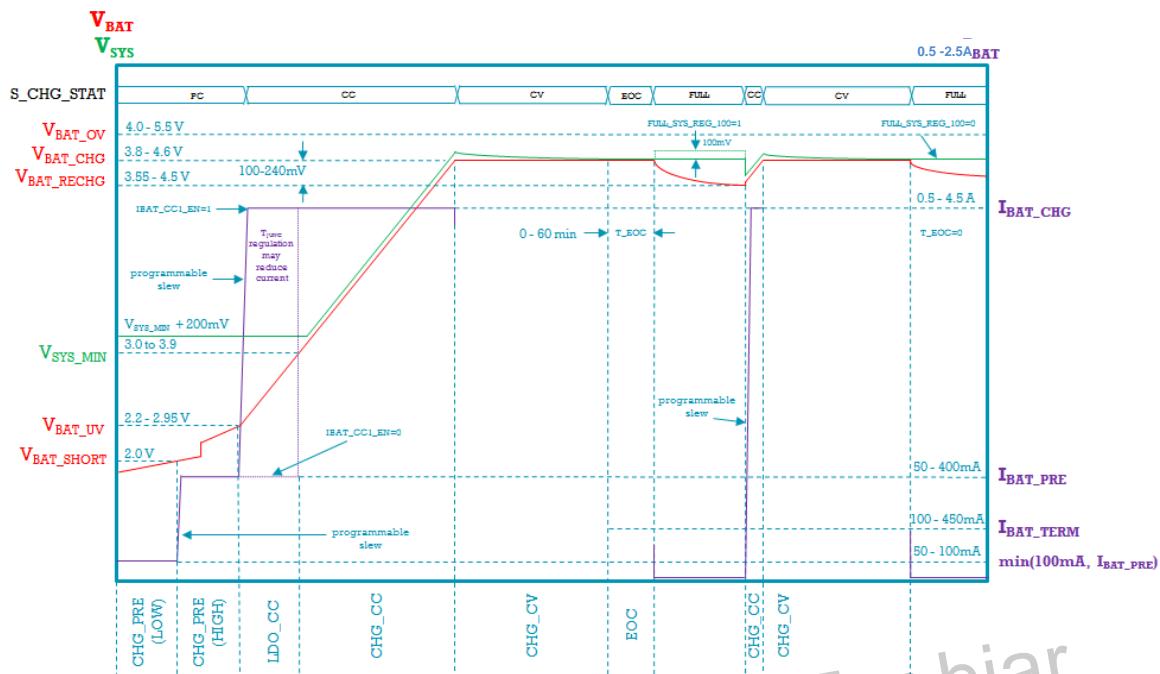


Figure 11: Charge Profile

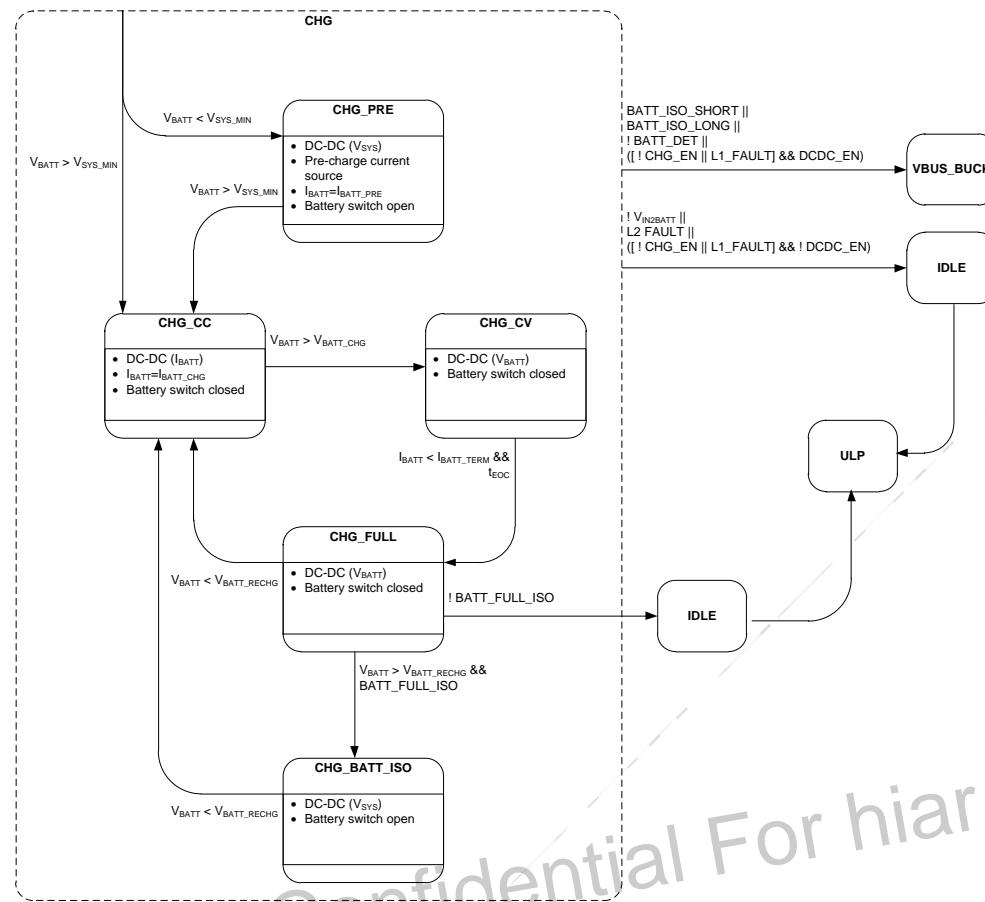


Figure 12: Charging state diagram.

Note: RDY and VBUS_BUCK states are covered in section 6.2.

6.3.1.1 Pre-charge

SC2703P ensures battery lifetime by implementing a pre-charge phase. When Li-Ion batteries get deeply discharged, so far that the battery pack protection circuitry has disconnected, they should not be recharged with full current from the very beginning. First, the battery should be charged with a low current (typically 10% of the normal CC rate) until the battery chemistry has been recovered and the protection switch has connected again.

During the pre-charge phase, the DC-DC operates in VSYS regulation mode with VSYS set to VSYS_MIN_REG. A current source, supplied from VSYS, regulates the pre-charge current IBATT_PRE. If VBATT is below VBATT_SHORT, the pre-charge current is limited to 100 mA. When the VBATT_UV is reached, the protection switches in the battery back are assumed be closed. After this, the charging current can be increased. However, VBATT_UV is not high enough to supply the system (VBATT_UV < VBATT < VSYS_MIN). In order to speed-up the pre-charge phase, SC2703P features a transition period from pre-charge to constant current phase during which the DC-DC converter still operates in the VSYS regulation mode but the pre-charge current is increased at a rate defined in the IBATT_CHG_SLEW register towards the CC current configured in IBATT_CHG register. The current ramp continues until the junction temperature reaches TJUNC_WARN, the charger current reaches IBATT_CHG, or the pre-charge current source goes to dropout. If the automatic junction temperature regulation is enabled (TJUNC_REG=1), it will automatically reduce the charging current to keep the junction temperature below TJUNC_CRIT. If the junction temperature regulation is disabled (TJUNC_REG=0) crossing the warning threshold TJUNC_WARN causes the pre-charge current fold back to the value programmed in IBATT_PRE. The automatic junction temperature regulation limits the charging current to a level

that the temperature stays below T_{JUNC_CRIT} (see section 6.9). During the transition phase the efficiency of the charging is temporarily low. As the transition phase is short, the effect to the total charging efficiency is very low. The transition phase can be disabled by setting $IBATT_PRE_HIGH_EN=0$. This will force the pre-charge phase to run with the normal $IBATT_PRE$ setting all the way to constant current phase. The different pre-charge current are summarized in Table 29.

Table 29: Pre-charge current.

	$IBATT_PRE_HIGH_EN=0$	$IBATT_PRE_HIGH_EN=1$
$V_{BATT} < V_{BATT_SHORT}$	$\min\{100 \text{ mA}, IBATT_PRE\}$	$\min\{100 \text{ mA}, IBATT_PRE\}$
$V_{BATT_SHORT} < V_{BATT} < V_{BATT_UV}$	$IBATT_PRE$	$IBATT_PRE$
$V_{BATT_UV} < V_{BATT} < V_{SYS_MIN}$	$IBATT_PRE$	$IBATT_CHG$ (limited by T_{JUNC_WARN})

The pre-charge phase runs until V_{BATT} rises above V_{SYS_MIN} . The battery switch is fully closed and the DC-DC will move to charge current regulation mode and ramp the charging current as configured in $IBATT_CHG_SLEW$ register.

6.3.1.2 Constant current and constant voltage

In constant current (CC) mode the DC-DC operates in battery current regulation mode with the charging current I_{BATT_CHG} . The system voltage V_{SYS} is defined by the charging current and the on-resistance of the battery switch.

During constant current charging, the battery current can also be affected by the input current limit, by the junction temperature regulation. If all of these features are enabled simultaneously, the effective battery current will be the smallest one.

The CC mode runs until the V_{BATT} rises above V_{BATT_CHG} or a charging fault occurs. Then the charger moves automatically to the constant voltage (CV) mode.

During the CV mode the DC-DC operates in battery voltage regulation mode with the target voltage V_{BATT_CHG} . While the battery voltage is kept at V_{BATT_CHG} , the battery current will inherently decrease. The CV phase runs until the battery current has dropped below the I_{BATT_TERM} threshold and stayed below the threshold for t_{EOC} . The end-of-charge detection period diminishes the effect of varying system load to the end-of-charge condition.

6.3.1.3 Full

If the battery isolation feature is enabled, the battery switch is opened after reaching the full state and the DC-DC moves to V_{SYS} regulation mode with the target voltage set to $V_{SYS_FULL_REG}$. If the battery voltage drops below a re-charge threshold V_{BATT_RECHG} a new charge cycle is automatically started. However, if the V_{BUS} supply is removed, a new charge cycle will start normally when it is re-inserted. The battery switch control ensures that during increased system load the battery provides supplement current. This is described in section 6.6.

6.3.2 Safety timer

A safety timer is running whenever SC2703P is in one of the charging states. The purpose of the safety timer is to detect a condition where the battery does not react to charging as expected. For example, if the voltage of the battery does not rise during pre-charge or constant current charging it is likely that the battery is damaged. This condition is detected by the safety timer.

A separate timeout value is provided for pre-charge and constant current phases (t_{OUT_PRE} , t_{OUT_CCCV}). The timer will reload automatically when a transition between pre-charge and constant current phase is detected. The constant current timeout (t_{OUT_CCCV}) covers also the constant voltage phase, i.e., the timer is not reset when the transition occurs.

A timeout will stop the charging process and trigger an event (E_CHG_TIMEOUT). The safety timer itself does not have to be cleared after a timeout. Initiating a new charging cycle after a safety timeout requires that the timeout event is cleared.

6.3.3 Charging faults

There are two levels of charging faults. The more severe faults (L2_FAULT) will disable the DC-DC converter immediately:

- Junction over temperature ($T_{JUNC} > T_{JUNC_CRIT}$)
- System voltage ($V_{SYS} > V_{SYS_OV}$)
- Battery voltage ($V_{BATT} > V_{BATT_OV}$)
- Input voltage ($V_{BUS} < V_{BUS_UVLO}$, $V_{BUS} > V_{BUS_OV}$)

The other faults (L1_FAULT) will either stop the DC-DC, or they will only stop charging, depending on the combination of the CHG_EN and DCDC_EN registers:

- Safety timeout
- WD timeout

If one of the charging faults occurs during charging, the CHG_STAT register is updated to indicate a fault and an event is triggered (E_CHG). The charging fault has to disappear and the event cleared before charging can be resumed.

Table 30: Charger Faults / IRQ

Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EVENT_A	E_IN_PWR_BLOCK	E_VBAT_OV E_VBAT_OV	E_VBAT_UV	E_VBUS_OV	E_VBUS_DROP	E_VBUS_UV	E_VBUS2BAT	E_AD_PDET
EVENT_B	E_BATDET	Reserved	Reserved	Reserved	Reserved	E_TJUNC_POR	E_TJUNC_CRT E_TJUNC_CRT E_TJUNC_CRT	E_TJUNC_WARM
EVENT_C	E_IBUS_LIM	E_ADC_DON_E	E_LOWBAT	E_IBUS_REV_LIM_MAX	E_IBUS_REV_LIM	E_DCDC_REV_BOOST_FAULT	E_VBUS_REV_OV E_VBUS_REV_OV	E_VBUS_REV_SHORT
EVENT_D	E_TIMEOUT_T_CCCV	E_TIMEOUT_PRE	E_WD	E_SYS_OV	E_VSYS_POR	Reserved	Reserved	E_CHG_STAT
EVENT_E	Reserved	Reserved	Reserved	E_VSYS_UV	Reserved	Reserved	Reserved	Reserved

L1 Faults (less Severe; Disable Charging)

L2 Faults (More Severe; Disable Buck)

OTG/Flash Faults

System Information

6.4 ON/OFF CONTROLLER

The ON/OFF Controller state diagram is shown in **Figure 14: ON/OFF Controller state diagram** below. The start-up timing diagram is shown below.

By studying the full detailed on/off controller state, one can see that many system events will force L1FAULT=1 or L2FAULT=1. For simplicity, all of the events that drive these states have been summarized in the following bulleted list:

Inserting battery only:

The following outline what happens when a dedicated charger is applied to VBUS but SC2703P is otherwise unpowered device as can be seen in:

- 1) Initial conditions:
 - a. Power applied to end product(i.e. battery)
 - b. The SC2703P is in the IDLE state.
- 2) A 5V dedicated charger is applied to VBUS.
 - a. Default charger input current = 0.5A. This allows the charger to start. Battery switch is fully enabled.
 - b. S_ADPADET =1, E_ADPADET = 1, to indicate adaptor inserted.
 - c. Internal 1MHz oscillator and AVDD would have been alive. AVDD is the best of supply from VCENTER and Battery. After the initial de-bounce time, $T_{D_VBUS2BAT}$, and a deglitch time of T_{INLIM_START} , VCENTER charges up to VBUS voltage.
 - d. Buck will then be enabled and after T_{BUCK_WARM} and T_{BUCK_START} , with CHG_EN =1 by default, charger will start running and charge current will be ramped up to its programmed charge current.

Installing an adaptor only from a full shutdown state:

The following outline what happens when a dedicated charger is applied to VBUS but SC2703P is otherwise unpowered device:

- 1) Initial conditions:
 - a. No power applied to the end product (i.e. no battery)
 - b. The SC2703P is in the hard reset state.
- 2) A 5V dedicated charger is applied to VBUS:
 - a. Default charger input current =0.5A. This allows the charger to start.
 - b. A crude supply regulator wakes up immediately which enables the internal charge-pump to enable the input limiter switch. With VCENTER present, AVDD awakes which enables the internal oscillator.
 - c. After a de-bounce time of $T_{Startup}$, BUCK_EN=1 to regulate SYS to MINSYS.
 - d. S_ADPADET =1, E_ADPADET=1 to indicate adaptor inserted. SC2703P sits in Warmup_Bck state.

Software full restart and software power-down register reset:

Factory Test mode:

Factory test mode for SC2703P is similar to installing an adaptor only from a full shutdown state.

Ship mode:

Ship mode is used as the last step in OEM manufacturing assembly

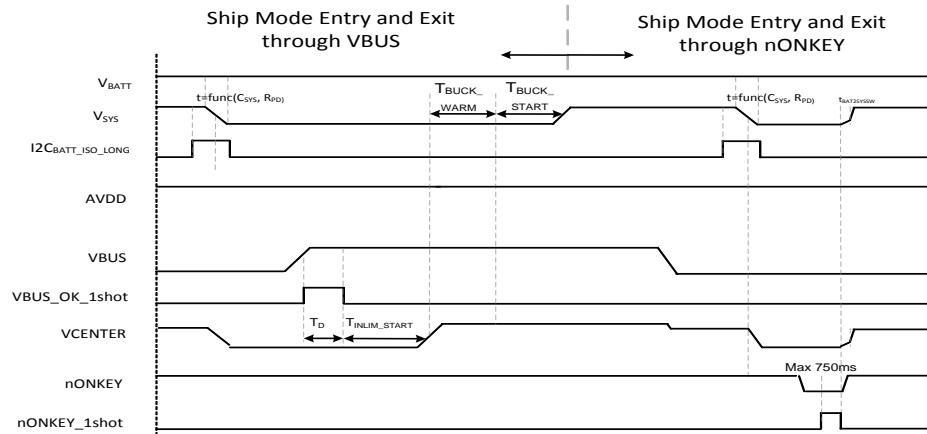


Figure 13: Ship mode entry and exit through VBUS

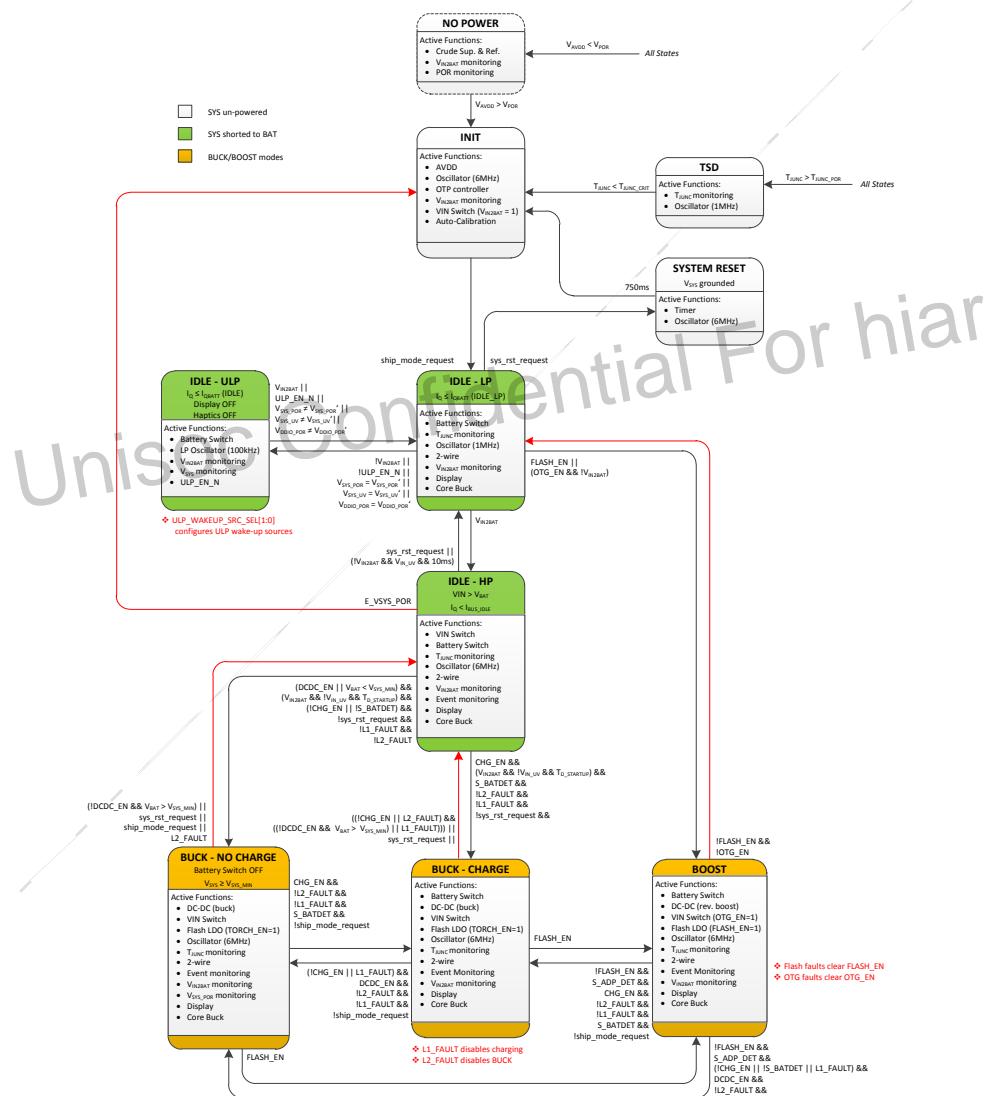


Figure 14: ON/OFF Controller state diagram

SC2703P Startup from VBUS with no battery

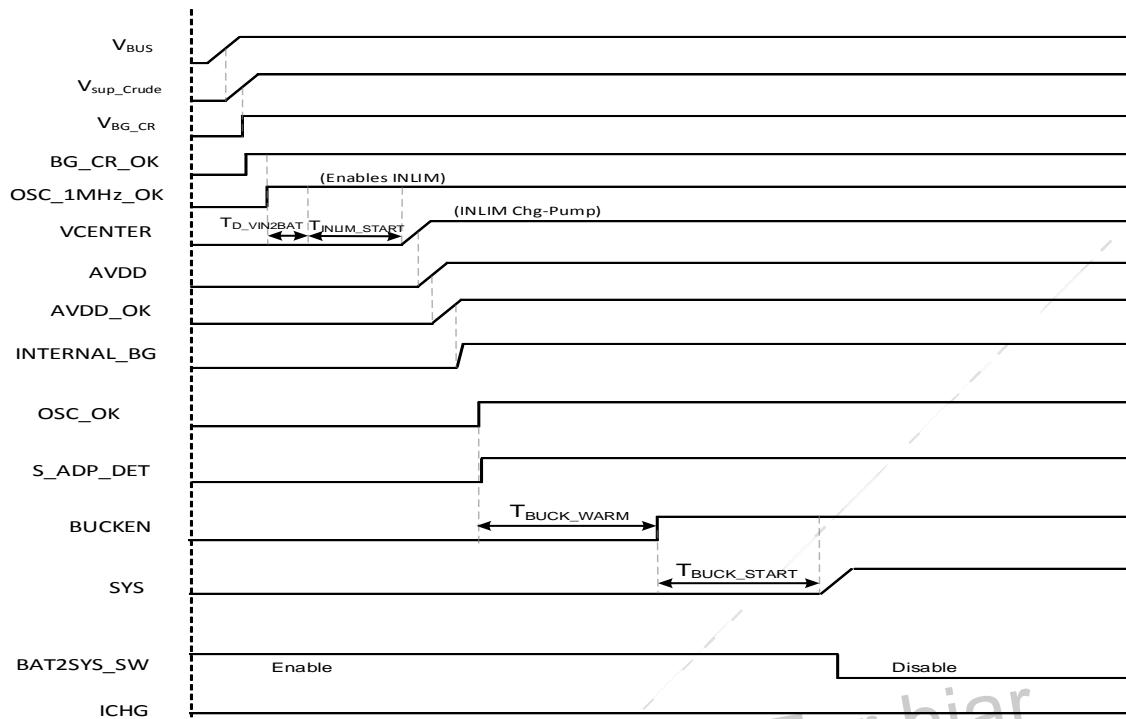


Figure 15: Start-up without battery

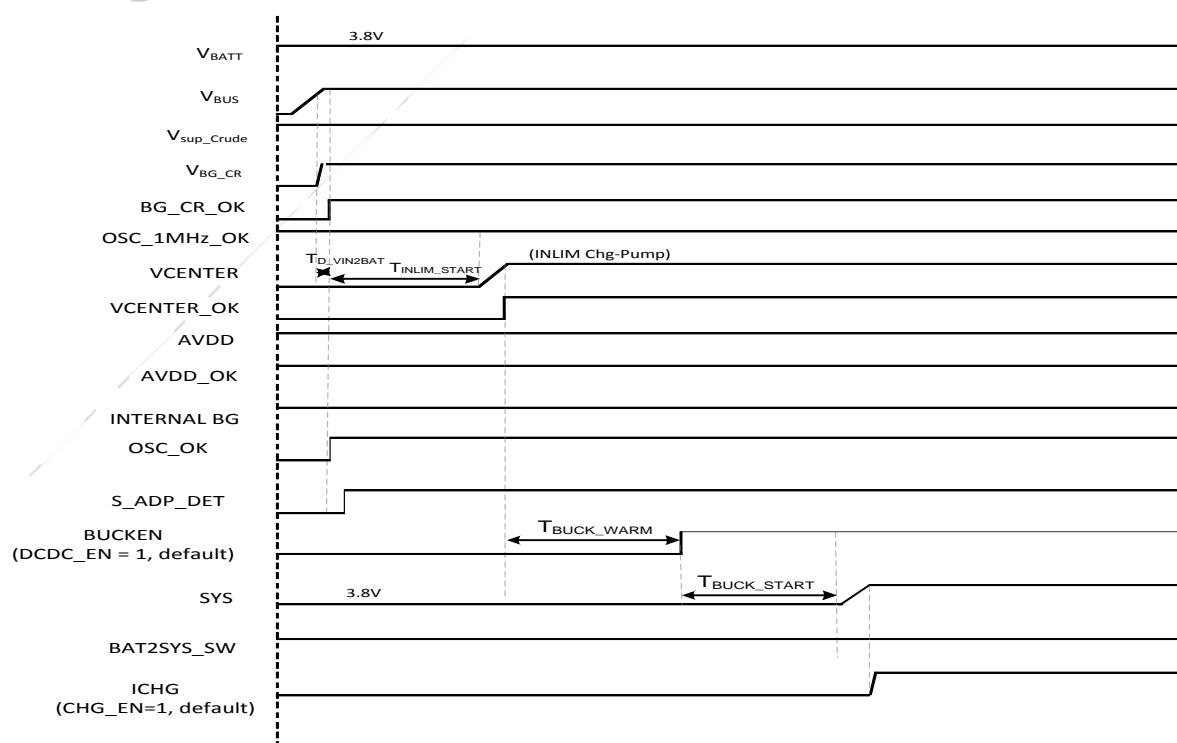
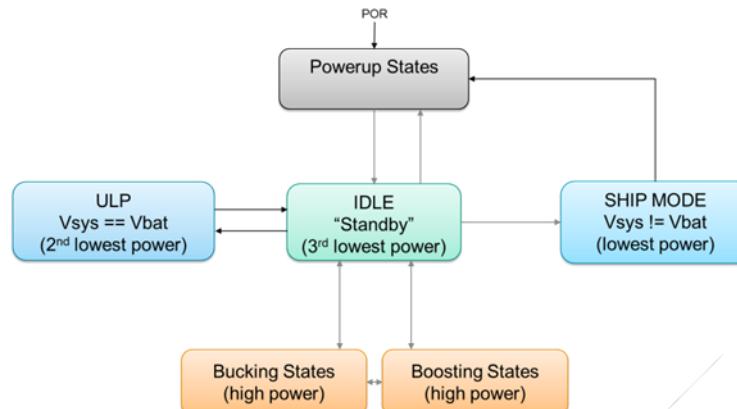


Figure 16: Start-up with battery

6.4.1 Ultra-Low Power (ULP) mode

SC2703P has an additional Ultra low power mode (ULP) that can be entered from the “idle” condition, if the display bias / Wled are shutdown.

**Figure 17: ULP state diagram**

The ULP mode can be entered and exited via I²C or Vbus insertion depending on the configuration selected, as shown in Table 31. If a system source causes ULP mode to be exited the state machine will re-enter the ULP state once the event has been serviced.

Table 31: ULP Exit

		ULP_WAKEUP_SRC_SEL[1:0]			
		0 (default)	1	2	3
User Source	GPIO2.ulp_en_n	GPIO2.ulp_en_n			GPIO2.ulp_en_n
	VBUS	VBUS	VBUS	VBUS	VBUS
		SCL	SCL	SCL	SCL
System Source	VSYS_POR	VSYS_POR	VSYS_POR	VSYS_POR	VSYS_POR
	VSYS_UV	VSYS_UV	VSYS_UV	VSYS_UV	VSYS_UV
	VDDIO_POR	VDDIO_POR	VDDIO_POR	VDDIO_POR	VDDIO_POR

6.5 Voltage monitoring

The voltage monitoring and V_{BUS} and V_{BATT} voltage monitoring levels are illustrated in Figure 19. All voltage monitoring functions have an event associated with them, which is triggered whenever the comparator trips.

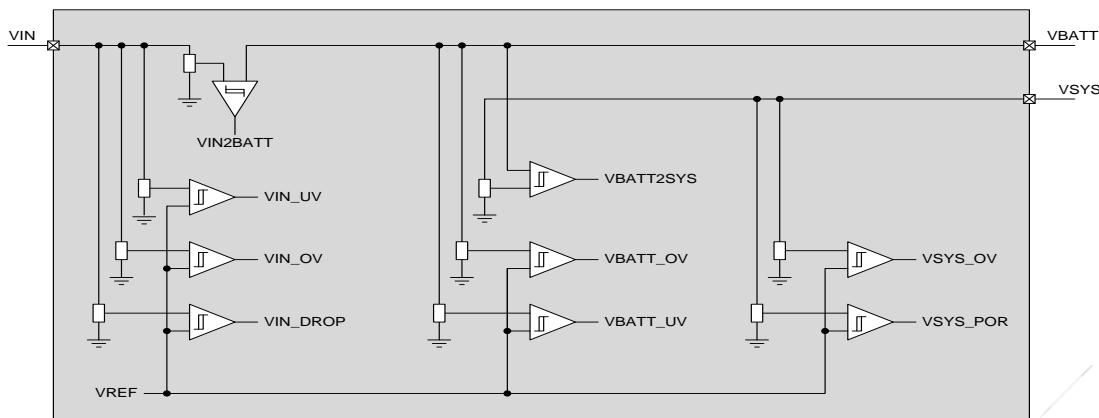


Figure 18: Voltage monitoring.

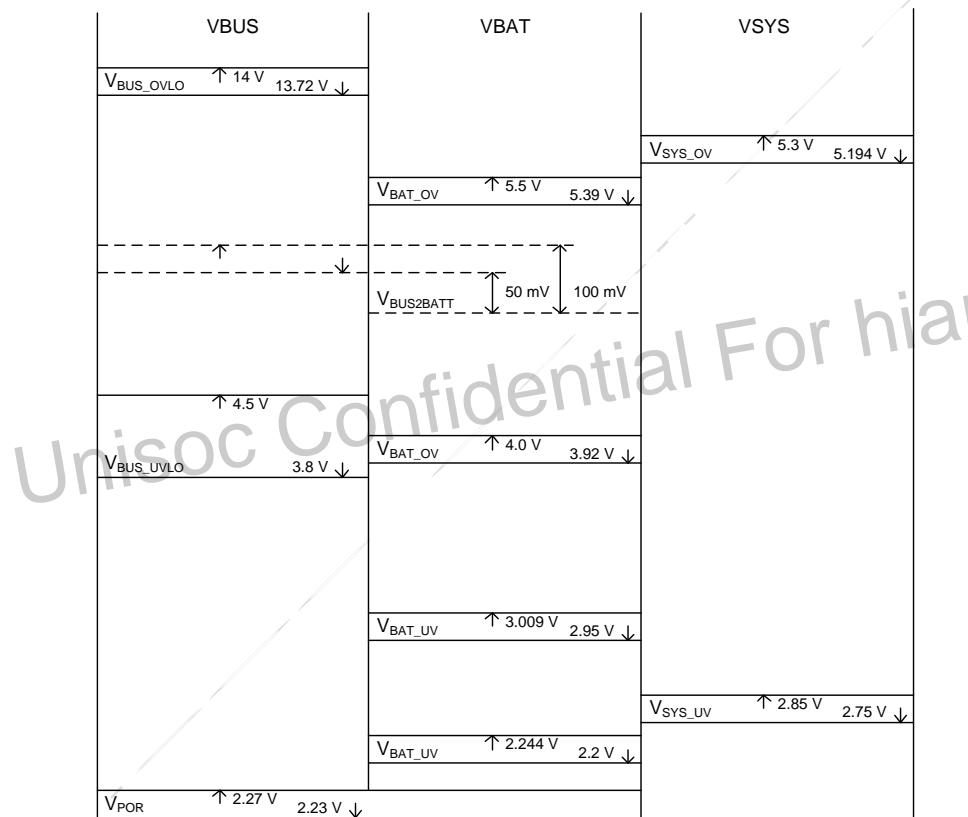


Figure 19: Voltage monitoring levels

6.5.1 VBUS

The V_{BUS_UVLO} monitor is used for detecting a valid power supply. A valid power supply is needed to charge the battery and to supply the system rail. Charging can only be started if the $V_{BUS2BATT}$ condition is true. The V_{BUS_OVLO} monitor is used for disabling the DC-DC converter when V_{BUS} rises too high. The V_{BUS_SHORT} monitor is used for detecting a short during reverse boost operation of the DC-DC converter and it is also used to check that V_{BUS} is not supplied before enabling the reverse boost mode. This is covered in section 6.2.7.

6.5.2 VINDROP

The purpose of the $V_{BUSDROP}$ monitor is to detect weak power supplies. It works in conjunction with the input current limit function of the DC-DC converter to implement the automatic input power reduction feature described in section 6.2.3.2.

6.5.3 VBATT

The battery voltage is monitored during charging to detect the target battery voltage, and to detect overvoltage and under voltage.

If overvoltage or under voltage is detected, an event is generated (E_{VBATT_OV} , E_{VBATT_UV}). V_{BATT_OV} causes a charge fault condition. V_{BATT_UV} is the battery voltage above which the protection switches in the battery pack are assumed closed.

The V_{BATT_SHORT} threshold is used to detect a short between the battery terminals.

6.5.4 VIN2BATT

The main purpose of the $V_{BUS2BATT}$ monitor is to trigger an exit the battery isolation mode. The $V_{BUS2BATT}$ monitoring is also needed to determine if the input voltage is high enough to start charging when SC2703P moves to the CHG mode, as described in section 12.3.

6.5.5 VBAT2SYS

When the battery switch is open after a completed charging cycle, the battery switch control has to detect if the V_{BUS} supply is not strong enough to supply the system and V_{SYS} drops below V_{BATT} (see section 6.3.1.3).

6.5.6 VSYS

The V_{SYS_POR} threshold is used for initiating an automatic initialization of SC2703P. The comparator is active whenever SC2703P supplies the system with the DC-DC converter, i.e., in the CHG and VIN_BUCK states. If V_{SYS} drops below V_{SYS_POR} SC2703P moves automatically to INIT state and executes a reset sequence. The event bit E_{VSYS_POR} is not reset.

The V_{SYS_OV} monitor is active whenever the DC-DC converter is running. If V_{SYS} rises above the V_{SYS_ov} , the DC-DC converter is immediately disabled.

6.5.7 Event / Status

Table 32 summarizes the events which will cause the battery FET or the reverse boost FET turn off.

Table 32: Event and Status Summary

Event/Status	Conditions	BAT FET turns off	VBUS FET turns off
E_{VSYS_POR}	$V_{SYS} < 2.8V$ (CHG, BAT_ISO_FULL, BAT_ISO_FLT states)	Yes	NO
E_{VBUS_OV}	$V_{BUS} > 10.5V$	NO	NO
Surge Fault	$V_{BUS} > 12.0V$	NO	YES
E_{VBUS_UV}	$V_{BUS} < 3.8V$	NO	YES
$E_{VBUS2BAT}$	$V_{BUS} < V_{BAT}$	NO	YES
E_{TJUNC_POR}	$T_{JUNC} > 150^{\circ}C$	YES	NO
E_{TJUNC_CRIT}	$T_{JUNC} > 140^{\circ}C$	NO	NO

SYS_RST	Various entry methods	YES	YES
E_BATDET	Battery removal (S_ADPADET=1)	YES	NO
E_VBUS_REV_SHORT*	VBUS < ~4.4V	NO	YES
E_VBUS_REV_OV*	VBUS > 4.0V	NO	YES
E_DCDC_REC_BOOST_FAULT*	OTG Activation attempted VBUS >2.0V	NO	YES
E_IBUS_REV_LIM_MAX*	Current limit for too long	NO	YES
E_LOWBAT*	VBAT < VSYS_MIN	NO	YES
E_BOOST_STARTUP_OV*	VCENT > ~4.4V	NO	YES

*OTG Mode Only - This fault doesn't affect the switches in charge states (when S_ADPADET=1)

6.6 Battery switch, Power-path and supplement mode

SC2703P features SYS soft-start when battery is initially inserted. When battery is inserted, SYS is pulled-up with a resistor R_{SYS_PU} , until SYS voltage crosses 2V threshold and at which point, SYS will be quickly brought up to equal battery voltage.

SC2703P features an integrated battery switch. The switch is closed (conductive) whenever V_{BATT} is the only supply, and during charging in constant current and constant voltage phases. The switch can be configured to be open (non-conductive) when the charging cycle completes or when V_{BUS} is the only supply of the system, but the default is to remain closed. A block diagram of the battery switch control circuit is depicted in Figure 20.

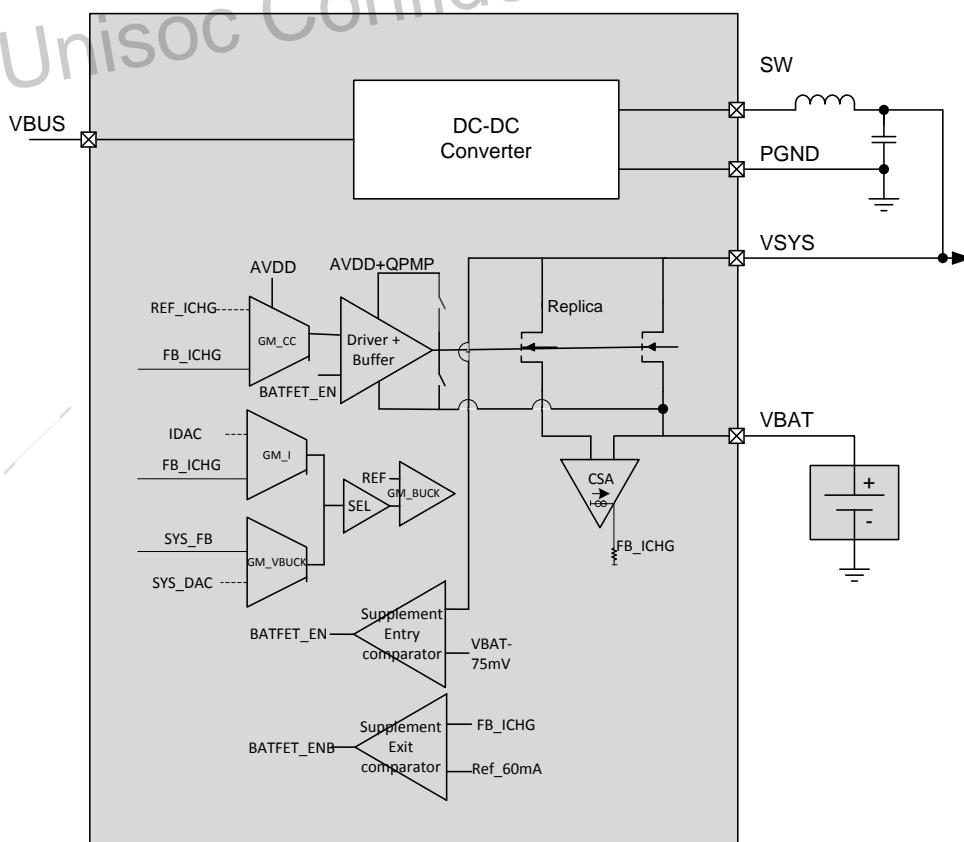
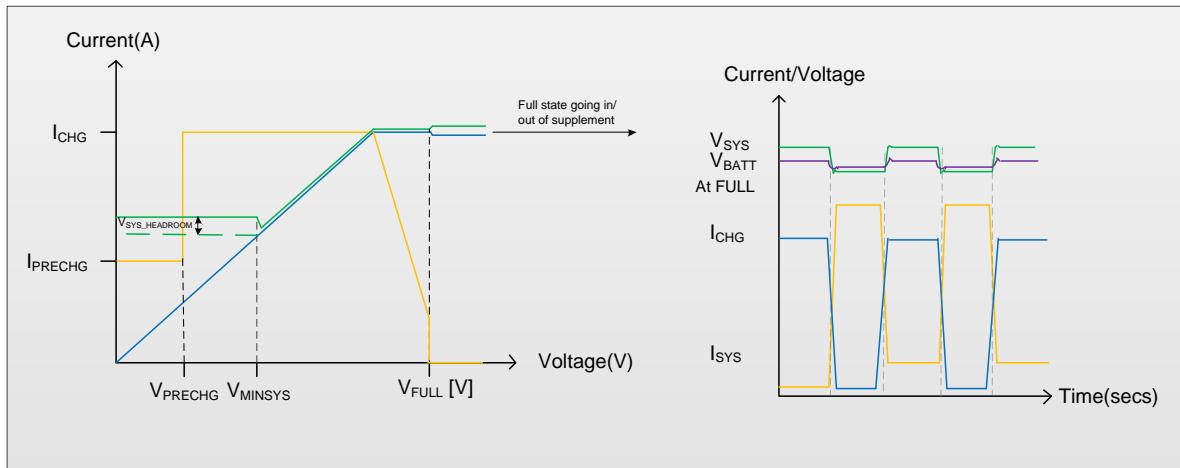


Figure 20: Battery switch control.**Figure 21: Power path current vs. voltage waveform**

The battery switch is opened when a power supply is attached and V_{BATT} is below V_{BATT_UV} . This allows the DC-DC converter to supply the system rail while the battery is pre-charged, as described in section 6.3.1.1. The battery switch is closed when the charger starts the constant current phase. During pre-charge, the battery switch does not function in supplement mode, i.e., battery is not discharged even if the DC-DC crosses the input current limit. If the input current limit is reached in the pre-charge phase, the battery current regulation is disabled in order to direct all available input power to the system.

During Constant current phase, the battery switch is fully closed and the resistance between V_{BATT} and V_{SYS} is R_{DSON_BATTSW} .

After a complete charging cycle, the battery is isolated from the system rail, as described in section 6.3.1.2. The switch remains open as long as V_{BUS} is supplied and the system load does not exceed the available input power. When the system load exceeds the available input power, V_{SYS} will drop below the battery voltage a comparator monitors the voltage delta between SYS and BATT and when SYS voltage drops 75mV BAT, the battery switch will be slowly enabled so battery can supplement the missing current. Similarly if the charge current flowing across the battery switch reduces to 60mA, the battery switch will be disabled. The battery switch voltage and current waveform is illustrated in Figure 21.

The battery switch can be also opened under software control. This can be used to minimize battery discharge during transit from the production line to the end customer or when a full power cycle of the system is required. The application processor will initiate the battery isolation by writing in the BATT_ISO_LONG register (see section 12.3.7). The battery switch will be reconnected either automatically as a response to an external event (nCE or V_{BUS}). In addition, a complete power cycle of the system can be initiated by writing into the BATT_ISO_SHORT.

6.7 Battery current sensing

SC2703P features integrated battery current sensing that does not require an external shunt resistor.

6.8 Battery detection

Battery detection is done prior to starting charging to ensure safety.

In normal conditions the battery detection can be done solely based on the battery voltage. However, if the battery is deeply discharged, or when the protection switches in the battery pack are opened, the battery voltage does not provide reliable information of the battery. It is assumed that the host or fuel gauge will provide battery detection in such situations.

6.9 Junction temperature monitoring

To protect SC2703P from damage due to excessive power dissipation the junction temperature is monitored continuously. The monitoring is split into three temperature ranges T_{JUNC_WARN} (125°C), T_{JUNC_CRIT} (140°C), and T_{JUNC_POR} (150°C).

If the junction temperature rises above the first threshold (T_{JUNC_WARN}), the event $E_{_TJUNC}$ is asserted. If the event is not masked, this will fire an interrupt. This first level of temperature supervision is intended for non-invasive temperature control, where the necessary measures for cooling the system down are left to the host software. The status of the T_{JUNC_WARN} comparator can be read from $S_{_TJUNC_WARN}$. An interrupt is generated when the temperature crosses the threshold from low to high, or from high to low. After the interrupt, the application processor can read out the comparator status to detect when the temperature drops below the threshold.

If the junction temperature continues to rise and crosses the second threshold (T_{JUNC_CRIT}), an event is fired ($E_{_TJUNC}$), the CHG_EN is de-asserted. Resuming normal operation requires that T_{JUNC} drops below T_{JUNC_CRIT} and the event is cleared.

There is also a third temperature threshold (T_{JUNC_POR}) which causes SC2703P to enter the reset mode. SC2703P stays in the reset mode as long as the junction temperature is above T_{JUNC_CRIT} .

6.9.1 Automatic junction temperature regulation

The above mentioned safety measures ensure that the host processor has the required tools to adjust the charging current according to the die temperature. However, SC2703P features an automatic current regulation mode where the charging parameters are automatically adjusted to keep the junction temperature below T_{JUNC_CRIT} . The automatic regulation can be enabled from the TJUNC_REG register. The regulation is not operational in the reverse boost mode of the DC-DC converter.

If enabled, the automatic junction temperature regulation operates in all charging phases. Each current reduction is done at a rate defined in the IBATT_CHG_SLEW register.

6.10 Control interface

All the output signals of SC2703P are driven with an open drain output stage. The signals have to be pulled-up with external resistors to an IO supply.

6.10.1 nCE

nCE is an edge sensitive, active low charge enable signal. It works in conjunction with the CHG_EN register. A falling edge of nCE sets the CHG_EN register and a rising edge clears it.

If SC2703P is in the IDLE mode, charging can be started by asserting the nCE pin or by writing to the CHG_EN register. Charging can be stopped by de-asserting the nCE pin or by writing to the CHG_EN register.

6.10.2 nIRQ

nIRQ is a level sensitive active low interrupt signal and must not be pulled above VDDIO by any external pull up resistor.

nIRQ is asserted when an un-masked event is asserted. The nIRQ will not be released until all event registers have been cleared. New events that occur during reading an event register will be held until the event register has been cleared, ensuring that the host processor does not miss them. By default all mask bits are asserted.

Some events can be generated from several sources, as depicted in Figure 22. After receiving an interrupt, the source can be detected by reading the associated status registers.

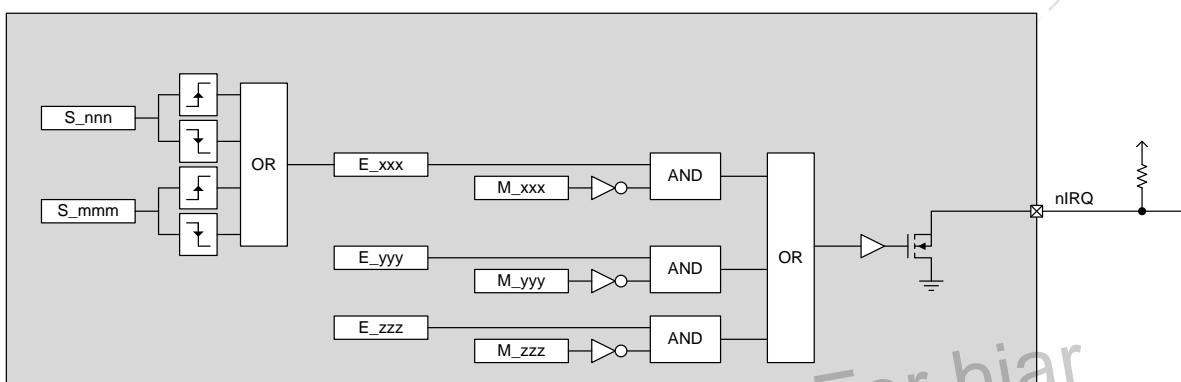


Figure 22: SC2703P interrupt logic

6.10.2.1 BATT_ISO

The BATT_ISO signal triggers an entry to the BATT_ISO_LONG mode in which the battery is isolated from the system supply. Once the battery isolation is effective and the system loses all power, it is expected that the BATT_ISO signal is no longer valid. Therefore, the BATT_ISO signal is not evaluated after the transition to the battery isolation state is started. As described in section 12.3.7, the only way to exit the BATT_ISO_LONG state is to assert the nCE or insert a valid V_{BUS} supply.

The BATT_ISO signal is provided to support systems where the final steps of a power down sequence are controlled by a microcontroller that does not have access to the 2-wire bus. After the assertion of the signal there is a delay $t_{PRE_BATT_ISO}$ before the battery switch is actually opened which allows the host processor to safely complete its power off sequence.

7 Flash Driver description

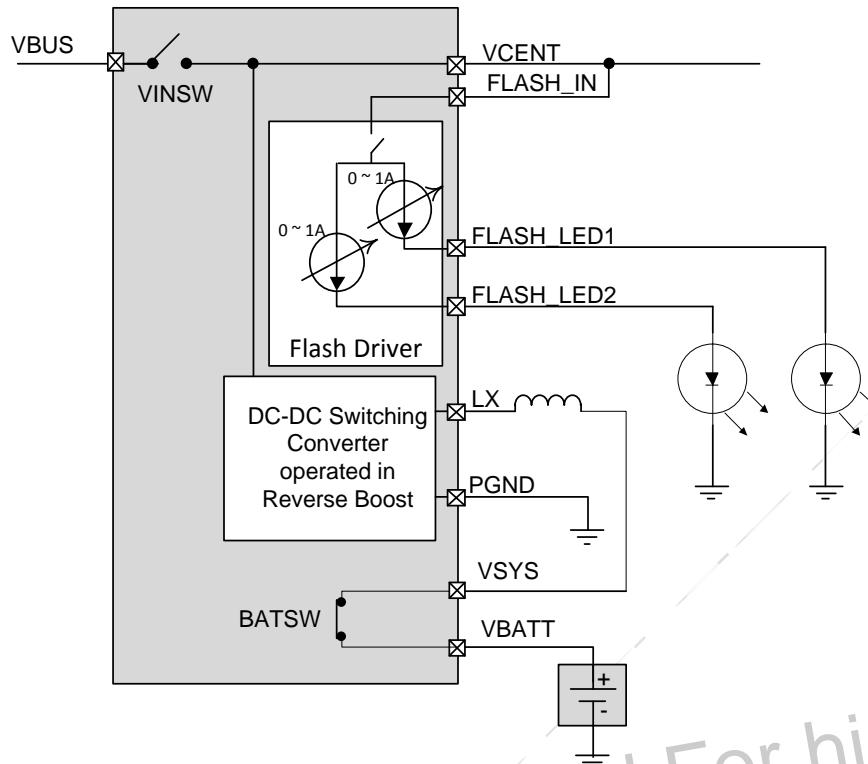


Figure 23: Flash driver in the flash mode

The Flash driver is a current source configuration, with the supply for the Flash LED coming from the Vcentre rail of the charger. If the Vcentre rail for the flash driver I being supplied by an external VBUS supply, the flash function will be disabled if the Vcentre voltage exceeds 6V. The current drawn by the Flash driver cannot exceed the input current limit set in the charger and the digital will flag an error and prevent the flash current being set above this limit. When enabled the flash current is stepped up from zero to its target current at a programmable rate, however the maximum rate is determined by the charger OTG boost transient response and so limited to TBD. Once finished driving for the programmed period the flash current is ramped down to zero at the same rate. A safety timer is included that will automatically disable the flash LED current if its duration is exceeded. In torch mode, with the current set at 500mA or less this timer is not enabled. A simple diode temperature sensor is also laid out with the current sources and if the local die temperature exceeds the safe limit the LED current source will also be disabled and an error flagged.

The forward voltage of the Flash LED must be less than or equal to Vcentre – current source Vds to insure the correct target current is sourced into the LED. If the LED selected has a high forward voltage the current source will run into drop out at high current and the sourced current will be reduced.

The maximum current that can be sourced per channel is 1A in Flash mode (total of 1A+1A for both channels) or 0.5A in torch mode (total for both channels operating in torch mode or per channels if only one channel is active). The sourced current can be programmed in 25mA steps in torch mode for both channels or 50mA steps in flash mode.

However if the current sourced from channel2 is 0.5A or less, it is possible to source up to 1.5A from channel1 (channel 2 can only source a maximum of 1A regardless of the setting applied to channel 1), the total current sourced from both channels cannot exceed the maximum total of 2A.

Refer to section 6.1 and table **Table 28** for information on the cooperation of the charger and flash driver and the limitations thus imposed. **Figure 24** shows expected uses case operation of the Flash/Torch driver in conjunction with the charger.



It should be noted that when in combined charge and torch operation mode the charging current to the battery will be reduced if a VBUS drop or input limit event occurs, but if this event persists beyond the point where the charge current has dropped to zero the torch current will not be reduced and there is a possibility that if the charger is in CC_Ido mode the system voltage could drop and cause a system fault event.

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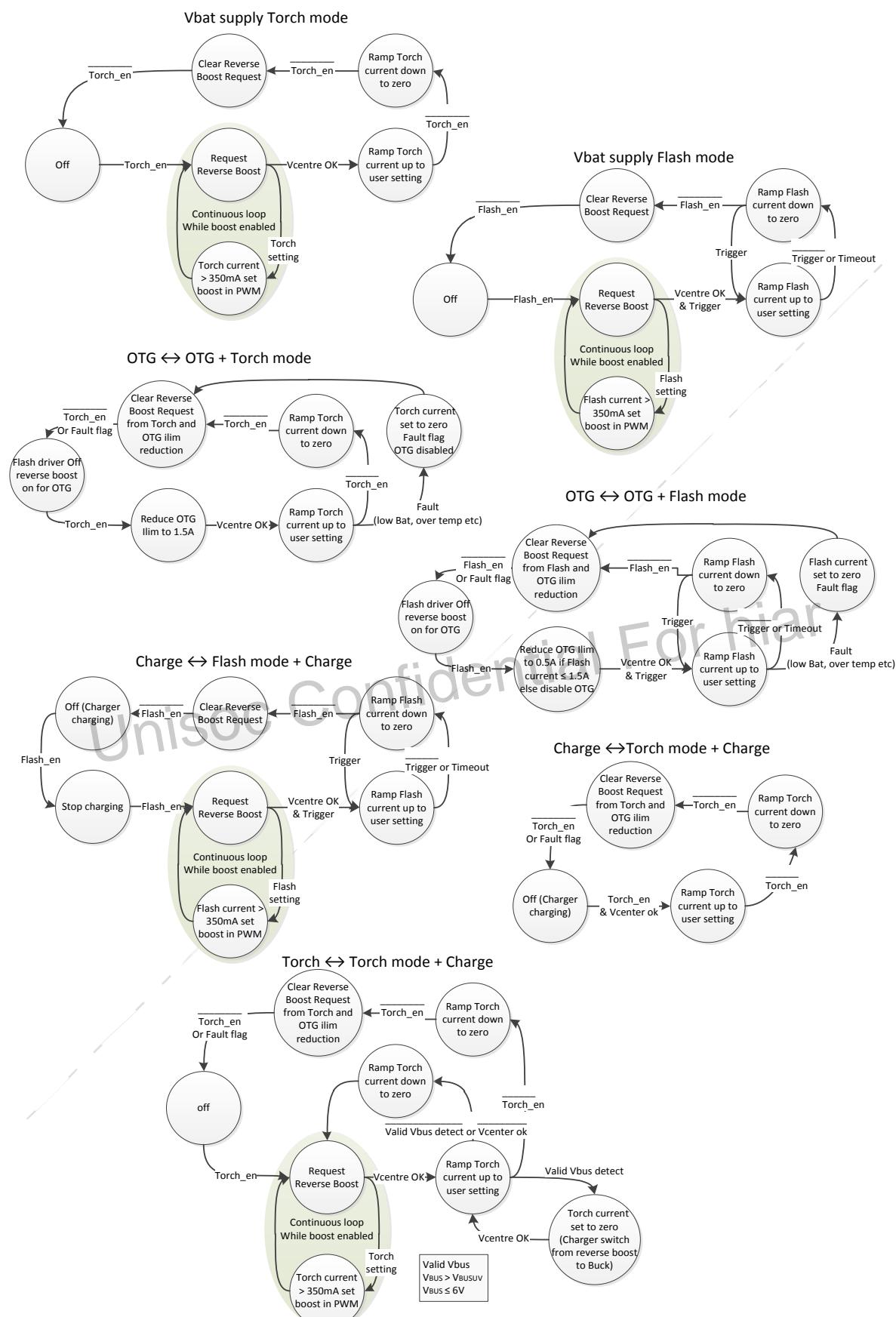
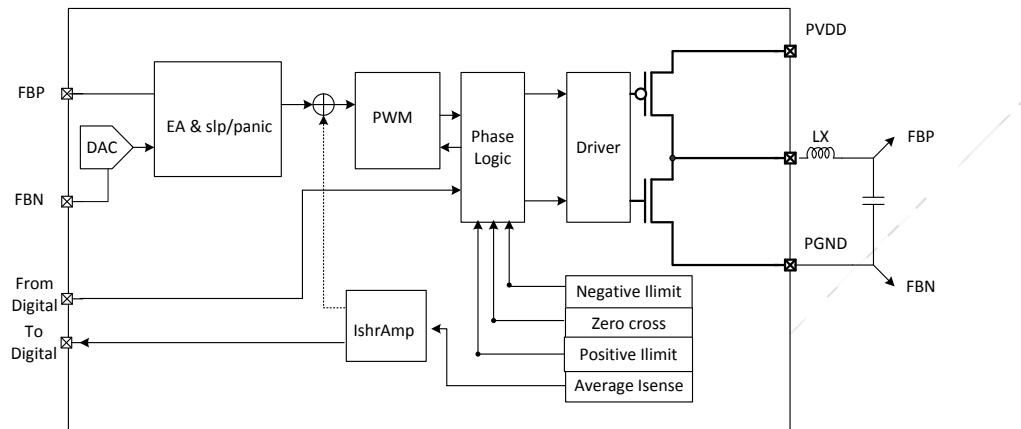


Figure 24: Flash use case operation

8 Core Buck description

**Figure 25: Core Buck**

The Core Buck is enabled / disabled via I²C and can only be enabled when the charger is in its idle mode, or other higher power states (reference and clock available). During start up, as part of the soft start to reduce inrush current, the buck will operate in DCM mode until it reaches 300mV at which point it will automatically switch to CCM mode and continue to ramp to the target output voltage, at the register controlled rate.

Although the buck can be forced to operate in PWM mode, via register command, its default configuration is to automatically switch between modes depending on the prevailing load it is presented with at any point in time, hysteresis between mode switching point ensures the device does not switch erratically between modes when the load is in the region of mode transition.

The core buck function is suitable for the supply of CPUs, GPUs, DDR memory rails in smartphones, tablets and other handhelds applications.

DVS voltage step information is located within one 8bit register. This register does not contain any other uncorrelated information. The voltage step register is unique.

DCDC turn on voltage (initial target output voltage) is configurable by OTP. However after a power down / power up sequence the DCDC output target voltage can recover to either reset default voltage, if a reset event has occurred, or the voltage set prior to the last turn off.

The Core Buck can be enabled or disabled directly via the Buck_EN pin. In addition a reset signal via the RST_B pin will trigger a shutdown sequence and OTP reload (restoring the buck's default target voltage).

9 Wled

The Boost circuit of the Wled driver will generate an output voltage that is sufficient to sustain the current drawn through the external LED's by the Idac.

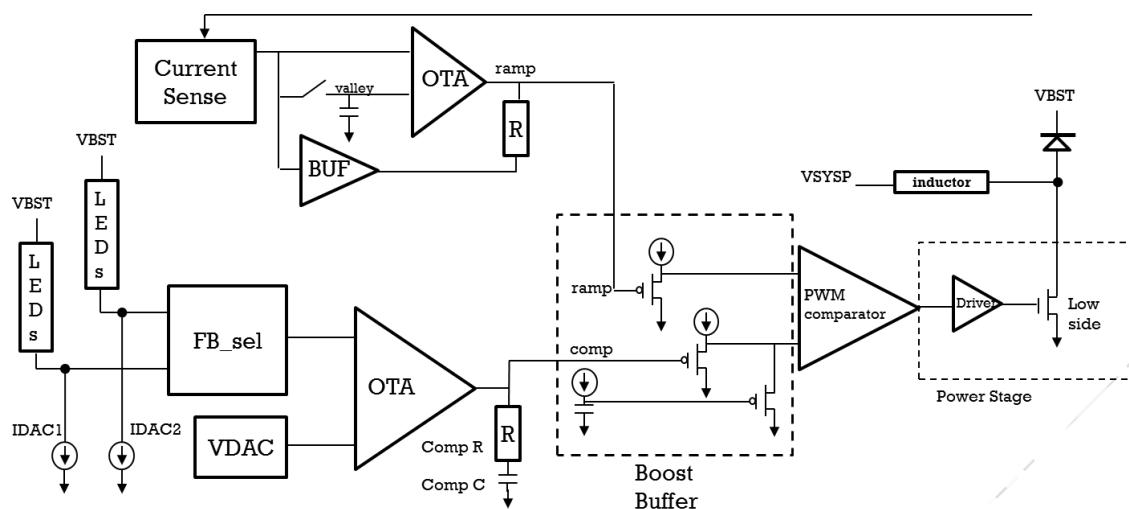


Figure 26: Wled and boost block diagram

9.1 Wled key digital features

8-bits IDAC code generation.

IDAC dimming can be done by referring to the duty of external PWM input signal or programmable register setting.

Support two modes of IDAC current, non-linear and linear mode.

Support external PWM input signal for dimming control.

External WLED_PWM input signal frequency range : 25KHz ~35KHz.

Lower frequencies the boost output voltage ripple increases, causing a non-linear response from the PWM duty cycle to the average LED current.

Duty Detection resolution: 1/256

PWM dimming output to analog.

Duty can be controlled by external PWM input signal or programmable register setting.

Support frequency range: 20KHz ~34KHz (8 settings in 2KHz steps)

PWM dimming resolution: 1/256

Support dimming duty : 0% ~ 100%.

Direct PWM dimming and analog dimming.

fully controlled by separate programmable registers setting.

OC/OV/UV_SCP Fault event Handling.

External PWM input signal duty detection.

9.2 Wled Operation Modes

There are two kinds of WLED driver dimming control, one is called PWM dimming which WLED driver's dimming level is controlled by PWM, and another one is called analog dimming which WLEDs dimming level is controlled by idac current. SC2703P provides duty detect mixed operation mode to use analog and PWM diming for high and low IDAC current, respectively.

Note:

1. *IDAC_TARGET_H, IDAC_TARGET_L, PWM_OUT_FREQ_STEP and PWM_IN_DUTY_THRESHOLD are all internal programmable registers.*
2. *"Duty (wled_pwm_data_in)" means the duty of PWM input from wled_pwm_data_in pin.*
3. *"Frequency (wled_pwm_data_in)" means the frequency of PWM input from wled_pwm_data_in pin.*

9.2.1 Duty Detect Mixed Mode:

The combination of duty detect PWM mode and duty detect analog mode. Switch point has to be determined in the beginning. If external PWM input signal's duty is greater than switch point, duty detect analog mode is performed, otherwise, enable duty detect PWM mode.

```

if( duty(wled_pwm_data_in) > PWM_IN_DUTY_THRESHOLD )
    pwm_out_frequency = 0
    pwm_out_duty = 100%
    if(IDAC_LINEAR=1):
        wled_idac_code_o = duty(wled_pwm_data_in)*256
    else
        wled_idac_code_o = LUT(duty(wled_pwm_data_in)*256)
else
    pwm_out_frequency = PWM_OUT_FREQ_STEP*2 + 20, (KHz). [20K~34KHz]
    pwm_out_duty = duty(wled_pwm_data_in)*256/ PWM_IN_DUTY_THRESHOLD
    if(IDAC_LINEAR=1):
        wled_idac_code_o = PWM_IN_DUTY_THRESHOLD
    else
        wled_idac_code_o = LUT(PWM_IN_DUTY_THRESHOLD)

```

9.3 IDAC Current Control

- Timing control and code generation for analogue IDAC.
- When enable ramping, ramps up/down 160uA per step, one step at a time.
- Controllable ramp rate when the current changes.

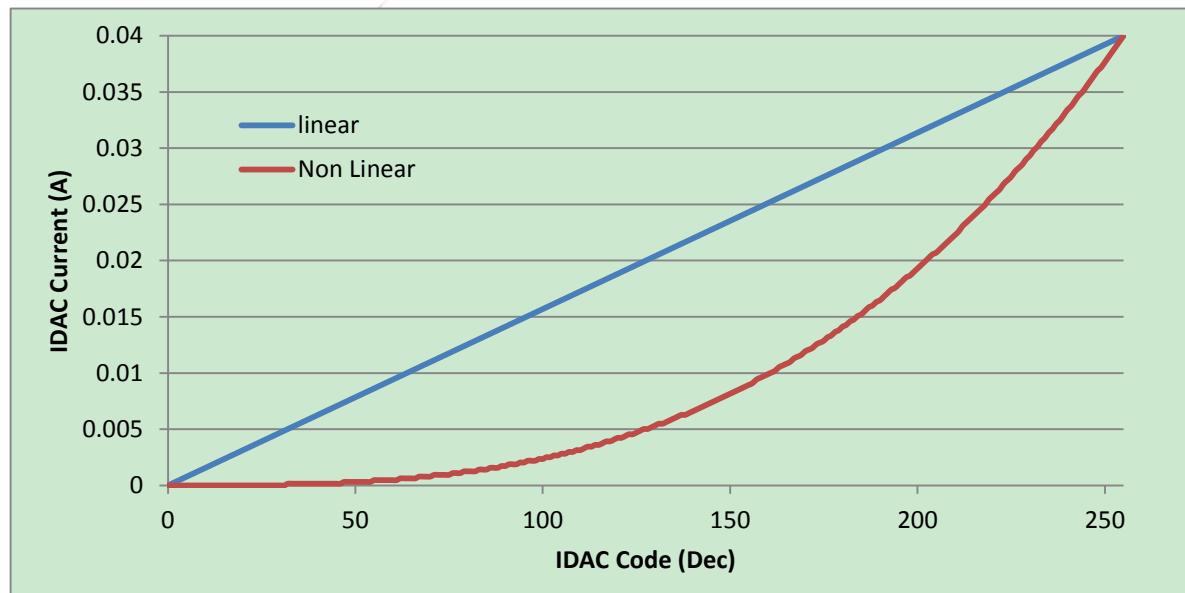
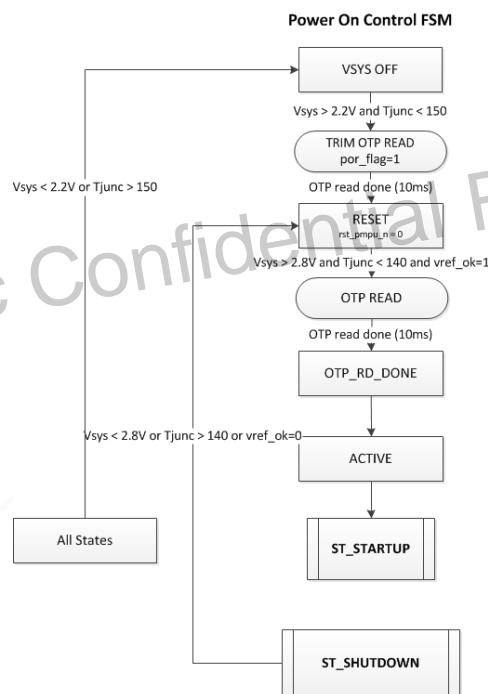


Table 33: WLED IDAC Control

Register Controls	Description
en	IDAC enable input (active HI)
data_lut<7:0>	8 bit input digital code to program WLED current value
pwm	idac_pwm input pulse coming from digital to toggle WLED current between programmed value and zero at set frequency and duty cycle.

10 Display Bias/Supply

The display bias function consists of four sub blocks, required to supply the bias voltages of a display module. The switch on and shut down of these rails is controlled by a digital state machine. The sequence of the power up and power down, the delays between each step in the sequence are configurable via I2C register writes (a predetermined sequence and delay settings are stored in OTP if the end user does not wish to modify the settings).

**Figure 27: Display function POR sequence**

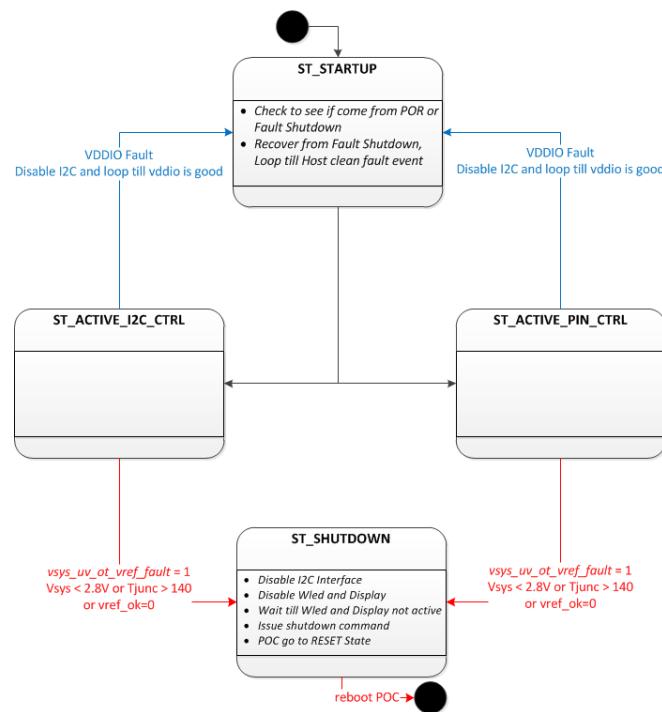


Figure 28: Display standby / active sequence

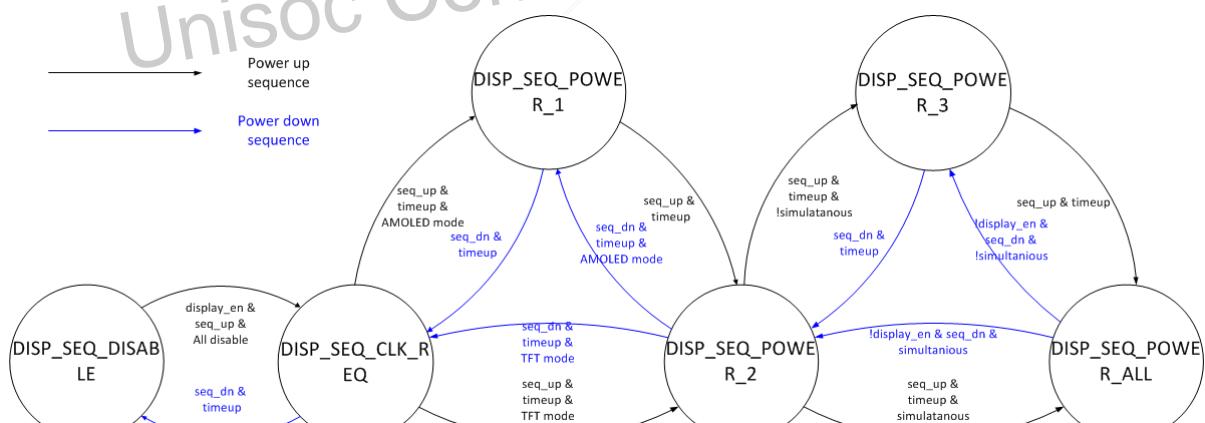


Figure 29: Display State Transition

The sequence state machine controls the enable sequence of the display bias rail generation blocks:

- vroot->vplus->vpos->vneg
- Vpos and vneg sequence can be switched or simultaneous on/off.

The default mapping:

- Pos: Boost/LDO

- Neg: CP

10.1 Enable Sequence

The sequence of Vpos and Vneg is adjustable, with each delay adjustable up to 16ms

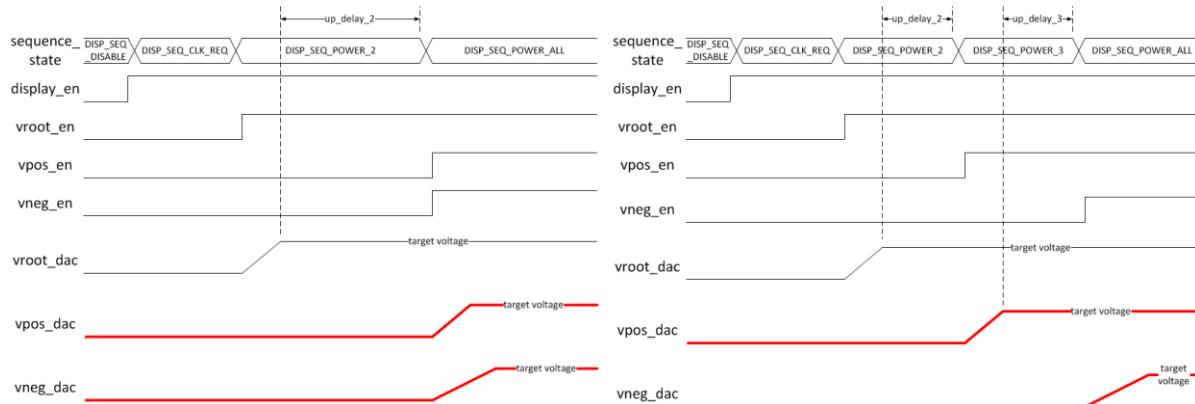


Figure 30: Enable Sequence

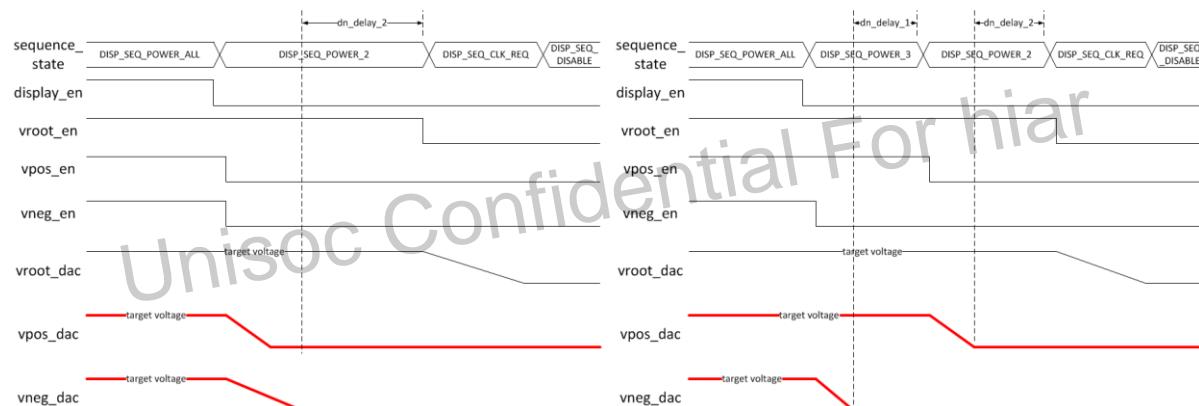


Figure 31: Disable Sequence

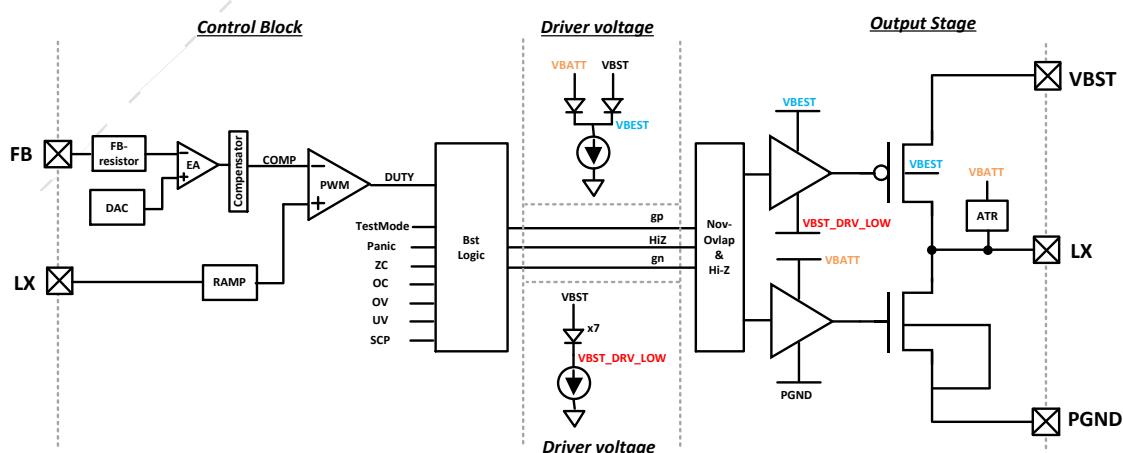


Figure 32: Boost block diagram

11 2-wire interface

The 2-wire interface provides access to control and status registers. The interface supports operations compatible to standard, fast and fast-plus mode of the I²C bus specification Rev. 3 [6].

Communication on the 2-wire bus is always between two devices, one acting as the master and the other as the slave. SC2703P will only operate as a slave.

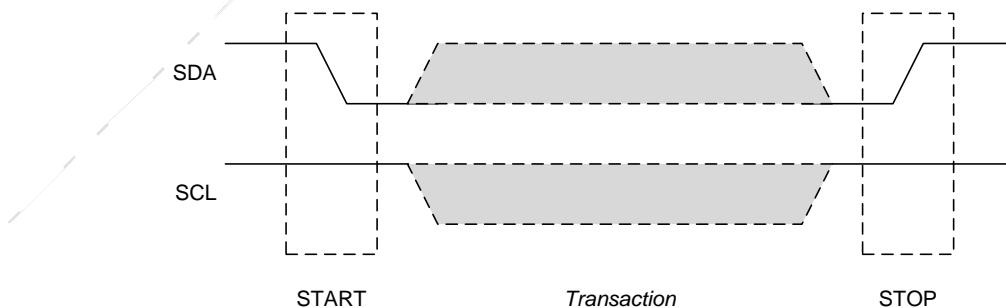
I²C register address must be 8bit to be compatible with the L3 host and thus the maximum number of registers that can be supported for a unique I²C device address is 256

SCL carries the 2-wire clock and SDA carries the bi-directional data. The 2-wire interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2–20 kΩ). These are often shared between multiple devices connected to the interface. The attached devices only drive the bus lines low by connecting them to ground. As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and it does not have any relation to the SC2703P internal clock signals. SC2703P will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow down. An automatic interface reset can be triggered in case the clock signal ceases to toggle for >35 ms (controlled in 2W_TO).

11.1 Details of the 2-wire protocol

All data is transmitted across the 2-wire bus in 8-bit groups. To send a bit the SDA line is driven at the intended state while the SCL is low. Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one address byte and one data byte. Data and address transfer is transmitted MSB first for both read and write operations. All transmission begins with the START condition from the master during which the bus is in IDLE state (the bus is free). It is initiated by a high-to-low transition on the SDA line while the SCL is in the high state. A STOP condition is indicated by a low-to-high transition on the SDA line while the SCL is in the high state. The START and STOP conditions are illustrated in Figure 33.

**Figure 33: Timing of the START and STOP conditions**

The 2-wire bus will be monitored by SC2703P for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. This is acknowledged by pulling the SDA line low during the following clock cycle (white blocks marked with 'A' in the following figures).

The protocol for a register write from master to slave consists of a START condition, a slave address, a read/write-bit, 8-bit address, 8-bit data, and a STOP condition. SC2703P responds to all bytes with an ACK. A register write operation is illustrated in Figure 34.

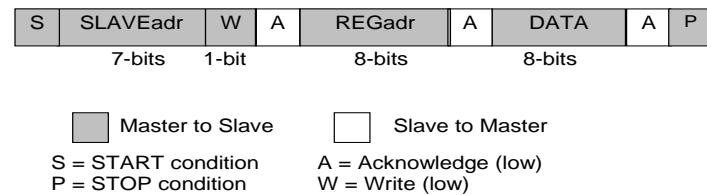


Figure 34: Byte write operation

When the host reads data from a register it first has to write-access SC2703P the target register address and then read-access SC2703P with a repeated START or alternatively a second START condition. After receiving the data, the host sends NACK and terminates the transmission with a STOP condition. This is illustrated in Figure 35.

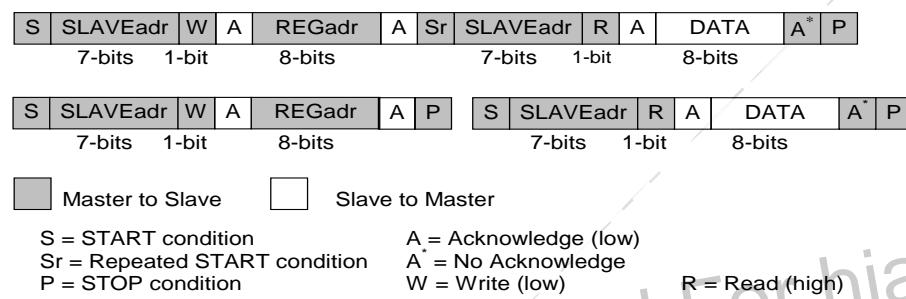


Figure 35: Examples of byte read operations

Consecutive (page) read-out mode is initiated from the master by sending an ACK instead of NACK after receiving a byte, see Figure 36. The 2-wire control block then increments the address pointer to the next register addresses and sends the data to the master. This enables an unlimited read of data bytes until the master sends a NACK directly after receiving the data, followed by a subsequent STOP condition. If a non-existent 2-wire address is read out then the SC2703P will return code zero.

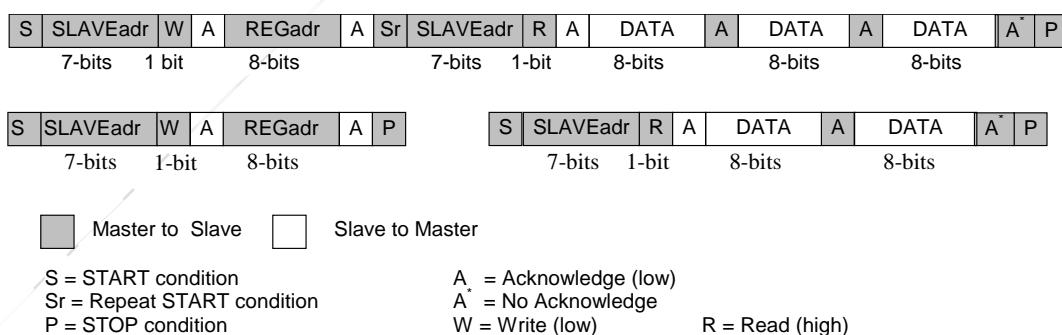


Figure 36: 2-wire page read

The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes following a slave register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data, and sends an ACK until the master sends a STOP condition. The page write mode is illustrated in Figure 37.



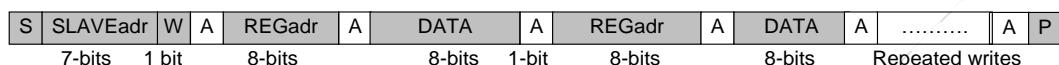
Master to Slave Slave to Master

S = START condition
Sr = Repeat START condition
P = STOP condition

A_{*} = Acknowledge (low)
A' = No Acknowledge
W = Write (low) R = Read (high)

Figure 37: 2-wire page write

Via control WRITE_MODE, a repeated write mode can be enabled. In this mode, the master can execute back-to-back write operations to non-consecutive addresses. This is achieved by transmitting register address and data pairs. The data will be stored in the address specified by the preceding byte. The repeated write mode is illustrated in Figure 38.



Master to Slave Slave to Master

S = START condition
Sr = Repeat START condition
P = STOP condition

A_{*} = Acknowledge (low)
A' = No Acknowledge
W = Write (low) R = Read (high)

Figure 38: 2-wire repeated write

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

12 Internal supplies

SC2703P features an internal node V_{DDHI} which is always connected to the higher of the two external supplies: V_{BATT} and V_{BUS}. V_{DDHI} is the supply for the internal supplies described in the following sections and for the power on reset circuitry. The V_{DDHI} structure is illustrated in Figure 39.

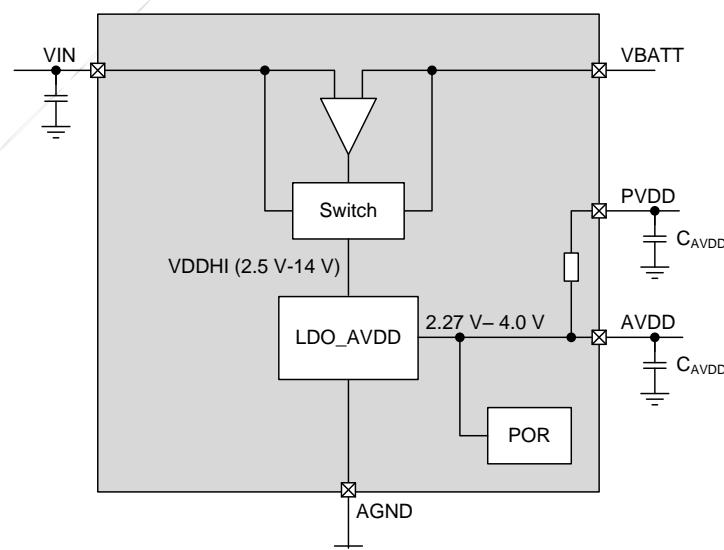


Figure 39: VDDHI and POR circuitry

12.1 AVDD (Internal Supply)

The V_{AVDD} regulator is the power supply for digital and analogue circuitry for the charger part of SC2703P. The input to the V_{AVDD} is V_{DDHI} as described in the previous section. If the $VBUS$ is not supplied, the output of the V_{AVDD} regulator $V_{BATT}-V_{DROPOUT}$. The AVDD and PVDD pins are only intended for external bypass capacitors and should not be loaded.

12.2 Internal Oscillator

The internal high-speed oscillator generates a signal at f_{osc} , the internal 12 MHz clock reference.

12.3 Power modes of Charger

The power modes of SC2703P charger are illustrated in Figure 17

The following transitions are considered as high priority and will override other transitions in the diagram:

- Critical junction temperature ($T_{JUNC} > T_{JUNC_CRIT}$)
 - Transition to INIT state
- Missing supply ($V_{AVDD} < V_{POR}$)
 - Transition to NOPOWER state
- System under voltage
 - Transition to INIT state

12.3.1 NOPOWER

V_{AVDD} is below the V_{POR} threshold. When $VBUS$ or V_{BATT} is attached the internal supply V_{AVDD} is automatically enabled. When V_{AVDD} rises above the “power on reset threshold” V_{POR} , SC2703P moves to the INIT mode.

12.3.2 INIT

When $VBUS$ or V_{BATT} rises above the V_{POR} threshold, SC2703P moves to the INIT state. In this mode, the internal reference, oscillator and clock generator are enabled and the control logic goes through reset. SC2703P goes through a full initialization including an OTP read. After the initialization is complete, the status registers and events are updated to match the status of the analog. The junction temperature is checked, and if T_{JUNC} is below the critical level (T_{JUNC_CRIT}), SC2703P moves to the IDLE state.

12.3.3 ULP (Ultra Low Power)

In the ULP mode all function not required to detect a wake up or maintain the battery FET are disabled to enter the lowest functional power state. In this state the Display bias and core buck are not enabled. The Display bias and buck require the reference and clock from the charger block and so if enabled will hold the charger block in the idle state until it is signalled to power down. Once the display bias or buck blocks have powered down they will release their “hold off” on the charger block and the charger block will drop back to the ULP state if still being requested.

12.3.4 IDLE

In the IDLE state SC2703P is supplied either from the battery or from V_{BUS} . SC2703P is fully operational as long as V_{AVDD} is above V_{POR} .

The main function in the IDLE state is to keep the battery switch closed. The $V_{BUS2BATT}$ monitor and the 2-wire interface are also enabled.

If the input supply is attached ($V_{BUS2BATT}$), SC2703P enables monitoring features and evaluates the conditions for charging:

- Battery detection (BATT_DET)
- Junction over temperature ($T_{JUNC} < T_{JUNC_CRIT}$)
- System voltage ($V_{SYS} < V_{SYS_OV}$)
- Battery voltage ($V_{BATT} < V_{BATT_OV}$)
- Input voltage ($V_{IN_UVLO} < V_{IN} < V_{IN_OV}$)

If the conditions are met, the input power reduction is not blocking the DC-DC enable (IN_PWR_BLOCK), and charging is enabled (CHG_EN=1), SC2703P moves to CHG state.

The reverse boost mode is started when the host processor sets the DCDC_REV_BOOST_EN register. The following conditions are evaluated in the IDLE state before the DC-DC can be started in the reverse boost mode:

- Battery is above the minimum system voltage ($V_{BATT} > V_{SYS_MIN}$)
- Junction temperature ($T_{JUNC} < T_{JUNC_CRIT}$)
- V_{BUS} is not already supplied ($V_{BUS} < V_{BUS_SHORT}$)

12.3.5 VBUS_BUCK

In the VBUS_BUCK state, the DC-DC converter supplies the system while the battery switch is open.

When SC2703P is in VBUS_BUCK state, and a transition to CHG state is triggered, it evaluates the junction temperature and the charging faults:

- Junction over temperature ($T_{JUNC} < T_{JUNC_CRIT}$)
- Battery voltage ($V_{BATT} < V_{BATT_RECHG}$)
- Battery overvoltage (V_{BATT_OV})

If none of the fault conditions is true, and charging is enabled (CHG_EN=1), SC2703P will move to CHG state.

Removing the V_{BUS} supply, while in VBUS_BUCK state, causes a transition to IDLE state. However, if VBUS_BUCK state has been entered after a battery isolation command (BATT_ISO_SHORT, BATT_ISO_LONG), removing the VBUS supply will complete the isolation procedure and SC2703P will move to BATT_ISO_SHORT or BATT_ISO_LONG state.

12.3.6 BATT_BOOST

In the BATT_BOOST mode, the DC-DC converter operates in the reverse boost mode (see section 6.2.7).

This mode is entered from the IDLE mode when the DCDC_REV_BOOST_EN register is set via the 2-wire interface and the following conditions are true:

- Battery is above the minimum system voltage ($V_{BATT} > V_{SYS_MIN}$)

- Junction temperature ($T_{JUNC} < T_{JUNC_CRIT}$)
- V_{IN} is not already supplied ($V_{BUS} < V_{BUS_SHORT}$)

The reverse boost is disabled by clearing the DCDC_REV_BOOST_EN bit. The following conditions will also automatically clear the DCDC_REV_BOOST_EN bit:

- Battery is below the minimum system voltage ($V_{BATT} < V_{SYS_MIN}$)
- Junction temperature ($T_{JUNC} > T_{JUNC_CRIT}$)
- V_{IN_REV} is shorted ($V_{IN_REV} < V_{IN_SHORT}$)
- V_{IN_REV} overvoltage ($V_{BUS_REV} > V_{BUS_REV_OV}$)
- I_{IN_REV} overcurrent ($E_{IIN_REV_LIM_MAX}$)

Note that the V_{BUS_SHORT} condition is used both to enter and exit the BATT_BOOST mode. Therefore, the condition is masked during the start-up of the DC-DC converter in order to prevent unintended exit from the BATT_BOOST mode.

12.3.7 BATT_ISO_LONG

In the BATT_ISO_LONG state, SC2703P disconnects the battery from the system rail. This is done to minimize battery discharge when system does not need to run at all, e.g., during transit from a production line to the end customer. Most of the functions are disabled in the BATT_ISO mode to minimize battery discharge. Only the nCE circuitry and $V_{BUS2BATT}$ monitor are active.

The BATT_ISO_LONG is entered by writing to the BATT_ISO_LONG register. If the isolation is initiated while V_{BUS} is supplied (VBUS_BUCK or CHG state), entry to BATT_ISO_LONG happens after the V_{BUS} supply is removed and a delay $t_{PRE_BATT_ISO}$.

If the battery isolation is initiated while V_{BUS} is not supplied (IDLE state), the entry to the BATT_ISO_LONG state will happen after a $t_{PRE_BATT_ISO}$ delay. This allows the host processor to complete its power down sequence.

The isolation persists until the nCE for t_{BATT_ISO} is asserted or V_{BUS} supply is detected.

12.3.8 BATT_ISO_SHORT

In the BATT_ISO_SHORT state, SC2703P disconnects the battery from the system rail for $t_{BATT_ISO_SHORT}$. This is done to execute a full power cycle to the system.

The BATT_ISO_SHORT is entered by asserting BATT_ISO_SHORT register or by asserting the nCE for longer than t_{ON_LONG} . If the battery isolation is initiated through the register, the entry to the BATT_ISO_SHORT state will happen after a $t_{PRE_BATT_ISO}$ delay. This allows the host processor to complete its power down sequence.

After $t_{BATT_ISO_SHORT}$ SC2703P will automatically move to the INIT state.

12.3.9 CHG

The CHG state contains several sub-states that correspond to the different charging phases presented in section 6.3. The following description applies to all the CHG sub-states.

If the V_{BUS} supply is removed ($V_{BUS2BATT}$), SC2703P moves to the IDLE state. If the charging is disabled by de-asserting the CHG_EN, SC2703P moves either to VBUS_BUCK or IDLE states depending on the value of the DCDC_EN register. If only charging is disabled (CHG_EN=0, DCDC_EN=1), SC2703P moves to VBUS_BUCK state. This means that the battery is isolated and the system will be supplied by the DC-DC converter. If both charging and the DC-DC converter are

disabled (CHG_EN=0, DCDC_EN=0), SC2703P moves to IDLE state. In this case the battery switch is closed and the system is supplied by the battery.

A charging fault will automatically clear the CHG_EN register. This will cause SC2703P to move either to VBUS_BUCK or IDLE states depending on the level of the charging fault. The more severe faults (L2_FAULT) will disable the DC-DC converter immediately. The other faults (L1_FAULT) will either stop the DC-DC, or they will only stop charging, depending on the combination of the CHG_EN and DCDC_EN registers. The charging faults were introduced in section 6.3.3.

12.4 Watchdog timer

SC2703P features a watchdog timer that is intended to monitor the host software during charging, and disable the charger in the event of system malfunction. Some of the automatic charge features of SC2703P[can be disabled and implemented in software instead. Moving the control to software requires tighter supervision than what is provided by the charging timer (section 6.3.2) and therefore, a separate watchdog timer is provided.

Whenever the charger is enabled, the watchdog timer is loaded with a pre-programmed value (TIMER_LOAD) and it starts decrementing. In normal operation the application processor should periodically re-initialize the safety timer by writing a new value to the TIMER_LOAD register. The value of the counter can be read from the TIMER_COUNT register. However, if the timer reaches zero an event is asserted, and the charger is automatically disabled.

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13 Charger Register map

Register	Ad dr	Status and Event							
		7	6	5	4	3	2	1	0
STATUS_A	0x00	Reserved	S_VBAT_OV	S_VBAT_UV	S_VIN_OV	S_VIN_DR OP	S_VIN_UV	S_VIN2BAT	S_ADP_DET
STATUS_B	0x01	S_BATDET	Reserved	Reserved	Reserved	Reserved	Reserved	S_TJUNC_C RIT	S_TJUNC_W ARN
STATUS_C	0x02	S_IIN_LIM	Reserved	S_LOWBAT	Reserved	S_IIN_REV _LIM	Reserved	S_VIN_REV _OV	S_VIN_REV _SHORT
STATUS_D	0x03	Reserved	Reserved	Reserved	S_VSYS_OV	Reserved	S_CHG_STAT<2:0>		
STATUS_E	0x04	S_IDLE_LP	S_TORCH_ON	S_BOOST_STA RTUP_OV	S_VSYS_UV	S_GPI3	S_GPI2	S_GPI1	S_GPIO
STATUS_F	0x05	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	S_LOWBAT_BOOST	S_TORCH_CHG_OV
STATUS_G	0x06	S_IIN_LIM_EFF<7:0>							
STATUS_H	0x07	S_IBAT_CHG_EFF<7:0>							
STATUS_I	0x08	S_VBAT_CHG_EFF<7:0>							
EVENT_A	0x09	Reserved 0	E_VBAT_OV	E_VBAT_UV	E_VIN_OV	E_VIN_DR OP	E_VIN_UV	Reserved 0	E_ADP_DET
EVENT_B	0x0A	E_BATDET	Reserved	Reserved	Reserved	Reserved	E_TJUNC_POR	E_TJUNC_C RIT	E_TJUNC_W ARN

EVENT_C	0x0B	E_IIN_LIM	E_ADC_DONE	E_LOWBAT	E_IIN_REV_LIM_MAX	E_IIN_REV_LIM	E_DCDC_REV_BOOST_FAULT	E_VIN_REV_OV	E_VIN_REV_SHORT
EVENT_D	0x0C	E_TIMEOUT_CCCV	E_TIMEOUT_PRE	E_WD	E_VSYS_OV	E_VSYS_POR	Reserved	Reserved	E_CHG_STAT
EVENT_E	0x0D	Reserved	Reserved	E_BOOST_STA_RTUP_OV	E_VSYS_UV	E_GPI3	E_GPI2	E_GPI1	E_GPIO
EVENT_F	0x0E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	E_LOWBAT_BOOST	E_TORCH_CHG_OV
MASK_A	0x12	Reserved 1	M_VBAT_OV	M_VBAT_UV	M_VIN_OV	M_VIN_DR_OP	M_VIN_UV	Reserved 0	M_ADP_DET
MASK_B	0x13	M_BATDET	Reserved	Reserved	Reserved	Reserved	M_TJUNC POR	M_TJUNC_C_RIT	M_TJUNC_WARN
MASK_C	0x14	M_IIN_LIM	M_ADC_DONE	M_LOWBAT	M_IIN_REV_LIM_MAX	M_IIN_REV_LIM	M_DCDC_REV_BOOST_FAULT	M_VIN_REV_OV	M_VIN_REV_SHORT
MASK_D	0x15	M_TIMEOUT_CCCV	M_TIMEOUT_PRE	M_WD	M_VSYS_OV	M_VSYS_POR	Reserved	Reserved	M_CHG_STAT
MASK_E	0x16	Reserved	Reserved	M_BOOST_STA_RTUP_OV	M_VSYS_UV	M_GPI3	M_GPI2	M_GPI1	M_GPIO
MASK_F	0x17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	M_LOWBAT_BOOST	M_TORCH_CHG_OV
MASK_G	0x18	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
MASK_H	0x19	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
MASK_I	0x1A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Voltage Monitoring									
Register	Ad dr	7	6	5	4	3	2	1	0

VIN_CTRL_A	0x1B	VIN_DROP<7:0>									
VBAT_CTRL_A	0x1C	VBAT_OV<3:0>				VBAT_UV<3:0>					
DC-DC											
Register	Ad dr	7	6	5	4	3	2	1	0		
DCDC_CTRL_A	0x1D	Reserved	Reserved	DCDC_FSW<1:0>		DCDC_FS W_AUTO	OTG_EN	DCDC_EN	CHG_EN		
DCDC_CTRL_B	0x1E	IN_PWR_RE D	IIN_REV_LIM<2:0>			DCDC_REV_PEAK_ILIM<1:0>		DCDC_PEAK_ILIM<1:0>			
DCDC_CTRL_C	0x1F	T_REV_ILIM_MAX<1:0>		IIN_LIM_SLEW<1:0>		DCDC_REV_BOOST_FSW<1:0>		Reserved	IIN_LIM_SEL		
DCDC_CTRL_D	0x20	Reserved	IIN_LIM1<2:0>			Reserved	IIN_LIM0<2:0>				
DCDC_CTRL_E	0x21	VSYS_SLEW<1:0>		VIN_REV_SLEW<1:0>		IIN_DROP_AMOUNT<1:0>		IIN_DROP_INTERVAL<1:0 >			
DCDC_CTRL_F	0x22	CHG_RST ART	Reserved	Reserved	FORCE_BOO ST_SKIP	DCDC_REV_VOUT<3:0>					
Charger											
Register	Ad dr	7	6	5	4	3	2	1	0		
CHG_CTRL_A	0x23	VBAT_RECHG<1:0>		VBAT_CHG<5:0>							
CHG_CTRL_B	0x24	IBAT_CC1_E N	Reserved 0	IBAT_CHG<5:0>							
CHG_CTRL_C	0x25	Reserved	Reserved	IBAT_CHG_SLEW<1:0>		VSYS_MIN<3:0>					

CHG_CTRL_D	0x26	T_EOC<2:0>				IBAT_TERM<2:0>			IBAT_PRE<1:0>	
CHG_CTRL_E	0x27	CHG_STAT_EVENT_SEL<1:0>			VBAT_WARM<1:0>			VBAT_COLD<1:0>		IBAT_WARM
Battery Switch										
Register	Ad dr	7	6	5	4	3	2	1	0	
BATSW_CTR_L_A	0x28	Reserved	Reserved	T_PRE_BAT_ISO<1:0>			BAT_ISO_GPI	BAT_ISO_FULL	BAT_ISO_SHORT	BAT_ISO_LONG
Junction Temperature										
Register	Ad dr	7	6	5	4	3	2	1	0	
TJUNC_CTR_L_A	0x2A	Reserved	Reserved	Reserved	Reserved	Reserved	TJUNC_REG	TJUNC_WARN<1:0>		
ADC										
Register	Ad dr	7	6	5	4	3	2	1	0	
ADC_CTRL_A	0x2B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ADC_CNVR_T	
ADC_RES_0	0x2C	ADC_RES_VIN<7:0>								
ADC_RES_1	0x2D	ADC_RES_VBAT<7:0>								
ADC_RES_2	0x2E	ADC_RES_IIN<7:0>								
ADC_RES_3	0x2F	ADC_RES_IBAT<7:0>								
ADC_RES_4	0x30	ADC_RES_TJUNC<7:0>								

ADC_RES_5	0x31	Reserved															
I/O																	
Register	Ad dr	7	6	5	4	3	2	1	0								
GPIO_CONF_A	0x32	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved								
GPIO_CONF_B	0x33	Reserved	Reserved	Reserved	GPIO2_OUT	GPIO2_INT_EDGE	GPIO2_PIN<1:0>										
TWI_CTRL_A	0x34	TWI_ADDR<6:0>								Reserved							
TWI_CTRL_B	0x35	PP_EN	SDA_EXTRA_THOLD_DELAY	SCL_DEGLITCH_HSPEED	SCL_DEGLITCH_EN	TWI_WR_MODE	SDA_DEGLITCH_HSPEED	SDA_DEGLITCH_TCH_EN	TWI_TO								
Safety Timer																	
Register	Ad dr	7	6	5	4	3	2	1	0								
CHG_TIMER_CTRL_A	0x36	CHG_TIMER_EN	Reserved	TIMEOUT_PRE<1:0>	Reserved	TIMEOUT_CCCV<2:0>											
CHG_TIMER_CTRL_B	0x37	TIMER_LOAD<7:0>															
CHG_TIMER_CTRL_C	0x38	TIMER_COUNT<7:0>															
Configuration																	
Register	Ad dr	7	6	5	4	3	2	1	0								
CONF_A	0x40	ULP_EN	ULP_WAKEUP_SRC_SEL<1:0>	BAT_DET_CTRL	BAT_DET_SRC<1:0>			WD_EN	ONKEY_DET_EN								
CONF_B	0x41	IDLE_LP_MODE_DIS	SPSP_ENABLE	SPSP_TUNE_ENABLE	SPSP_TUNE<4:0>												

13.1 Status and Event

13.1.1 Register STATUS_A

Address	Name	POR value	Status Register A								
0x00	STATUS_A	0x00	7	6	5	4	3	2	1	0	
Reserved	S_VBAT_OV	S_VBAT_UV	S_VIN_OV	S_VIN_DROP	S_VIN_UV	S_VIN2BAT	S_ADP_DET				
Field name	Bits	Type	POR	Description							
S_VBAT_OV	[6]	RO	0x0	VBAT overvoltage comparator status							
S_VBAT_UV	[5]	RO	0x0	VBAT undervoltage comparator status.							
S_VIN_OV	[4]	RO	0x0	VIN overvoltage comparator status							
S_VIN_DROP	[3]	RO	0x0	VIN DROP comparator status							
S_VIN_UV	[2]	RO	0x0	VIN undervoltage comparator status							
S_VIN2BAT	[1]	RO	0x0	VIN2BAT comparator status							
S_ADP_DET	[0]	RO	0x0	Charger attach/detach status							

13.1.2 Register STATUS_B

Address	Name	POR value	Status Register B								
0x01	STATUS_B	0x00	7	6	5	4	3	2	1	0	
S_BATDET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	S_TJUNC_CRIT	S_TJUNC_WARN		
Field name	Bits	Type	POR	Description							
S_BATDET	[7]	RO	0x0	Battery detection status							

S_TJUNC_CRIT	[1]	RO	0x0	TJUNC CRIT comparator status				
S_TJUNC_WARN	[0]	RO	0x0	TJUNC_WARN comparator status				

13.1.3 Register STATUS_C

Address	Name	POR value	Status Register C							
0x02	STATUS_C	0x00	7	6	5	4	3	2	1	0
S_IIN_LIM	Reserved	S_LOWBAT	Reserved	S_IIN_REV_LIM	Reserved	S_VIN_REV_OV	S_VIN_REV_SHORT			
Field name	Bits	Type	POR	Description						
S_IIN_LIM	[7]	RO	0x0	Input current limit status.						
S_LOWBAT	[5]	RO	0x0	Low battery (below VSYS_MIN) status in Buck operation						
S_IIN_REV_LIM	[3]	RO	0x0	Reverse boost input current limit comparator status.						
S_VIN_REV_OV	[1]	RO	0x0	VIN overvoltage comparator status in reverse boost mode.						
S_VIN_REV_SHORT	[0]	RO	0x0	VIN below VIN_SHORT comparator status in reverse boost mode.						

13.1.4 Register STATUS_D

Address	Name	POR value	Status Register D													
0x03	STATUS_D	0x00	7	6	5	4	3	2	1	0						
Reserved	Reserved	Reserved	S_VSYS_OV	Reserved	S_CHG_STAT<2:0>											
Field name	Bits	Type	POR	Description												
S_VSYS_OV	[4]	RO	0x0	VSYS_OV comparator status												

Charging Status					
				Value	Description
S_CHG_STAT	[2:0]	RO	0x0	0x0 (POR)	DCDC off (OFF)
				0x1	Pre-charge (PC)
				0x2	Constant Current (CC)
				0x3	Constant Voltage (CV)
				0x4	Top-Off (TO)
				0x5	Full (FULL)
				0x6	L1 Fault (L1)
				0x7	L2 Fault (L2)

13.1.5 Register STATUS_E

Address	Name	POR value	Status Register E								
0x04	STATUS_E	0x00									
7	6	5	4	3	2	1	0				
S_IDLE_LP	S_TORCH_ON	S_BOOST_STARTUP_OV	S_VSYS_UV	S_GPI3	S_GPI2	S_GPI1	S_GPI0				
Field name	Bits	Type	POR	Description							
S_IDLE_LP	[7]	RO	0x0	Low Power in Idle system status							
S_TORCH_ON	[6]	RO	0x0	Torch is Enabled status							
S_BOOST_STARTUP_OV	[5]	RO	0x0	During boost startup, the Vcenter node is over its acceptable voltage.							
S_VSYS_UV	[4]	RO	0x0	VSYS below VSYS_UV threshold (nominal 2.2V)							
S_GPI3	[3]	RO	0x0	GPI3 Pin Value. Reflects the value of pin when configured as GPI. Reads '0' when in any other configuration.							

S_GPIO2	[2]	RO	0x0	GPI2 Pin Value. Reflects the value of pin when configured as GPIO. Reads '0' when in any other configuration.
S_GPIO1	[1]	RO	0x0	GPI1 Pin Value. Reflects the value of pin when configured as GPIO. Reads '0' when in any other configuration.
S_GPIO0	[0]	RO	0x0	GPI0 Pin Value. Reflects the value of pin when configured as GPIO. Reads '0' when in any other configuration.

13.1.6 Register STATUS_F

Address	Name	POR value	Status Register F							
7	6	5	4	3	2	1	0			
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	S_LWBAT_BOOST	S_TORCH_CHG_OV			
Field name	Bits	Type	POR	Description						
S_LWBAT_BOOST	[1]	RO	0x0	Low battery (below VSYS_MIN) status in Boost operation						
S_TORCH_CHG_OV	[0]	RO	0x0	Torch/Charge Overvoltage status						

13.1.7 Register STATUS_G

Address	Name	POR value	Status Register G							
7	6	5	4	3	2	1	0			
S_IIN_LIM_EFF<7:0>										
Field name	Bits	Type	POR	Description						

				Effective input current limit when input power reduction is in action. The maximum value is 3000 mA. $S_{_IIN_LIM_EFF} = 25 + N \times 25 \text{ mA}$																																																
S_IIN_LIM_EFF	[7:0]	RO	0x00	<table border="1"><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>0x00 (POR)</td><td>25 mA</td></tr><tr><td>0x01</td><td>50 mA</td></tr><tr><td>0x02</td><td>75 mA</td></tr><tr><td>0x03</td><td>100 mA</td></tr><tr><td>0x04</td><td>125 mA</td></tr><tr><td>0x05</td><td>150 mA</td></tr><tr><td>0x06</td><td>175 mA</td></tr><tr><td>0x07</td><td>200 mA</td></tr><tr><td>0x08</td><td>225 mA</td></tr><tr><td>0x09</td><td>250 mA</td></tr><tr><td>0x0A</td><td>275 mA</td></tr><tr><td>0x0B</td><td>300 mA</td></tr><tr><td>0x0C</td><td>325 mA</td></tr><tr><td>0x0D</td><td>350 mA</td></tr><tr><td>0x0E</td><td>375 mA</td></tr><tr><td>0x0F</td><td>400 mA</td></tr><tr><td>0x10</td><td>425 mA</td></tr><tr><td>0x11</td><td>450 mA</td></tr><tr><td>0x12</td><td>475 mA</td></tr><tr><td>0x13</td><td>500 mA</td></tr><tr><td>0x14</td><td>525 mA</td></tr><tr><td>0x15</td><td>550 mA</td></tr><tr><td>0x16</td><td>575 mA</td></tr></tbody></table>	Value	Description	0x00 (POR)	25 mA	0x01	50 mA	0x02	75 mA	0x03	100 mA	0x04	125 mA	0x05	150 mA	0x06	175 mA	0x07	200 mA	0x08	225 mA	0x09	250 mA	0x0A	275 mA	0x0B	300 mA	0x0C	325 mA	0x0D	350 mA	0x0E	375 mA	0x0F	400 mA	0x10	425 mA	0x11	450 mA	0x12	475 mA	0x13	500 mA	0x14	525 mA	0x15	550 mA	0x16	575 mA
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0x1A	675 mA
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0x1C	725 mA
0x1D	750 mA
0x1E	775 mA
0x1F	800 mA
0x20	825 mA
0x21	850 mA
0x22	875 mA
0x23	900 mA
0x24	925 mA
0x25	950 mA
0x26	975 mA
0x27	1000 mA
0x28	1025 mA
0x29	1050 mA
0x2A	1075 mA
0x2B	1100 mA
0x2C	1125 mA
0x2D	1150 mA
0x2E	1175 mA
0x2F	1200 mA
0x30	1225 mA

0x31	1250 mA
0x32	1275 mA
0x33	1300 mA
0x34	1325 mA
0x35	1350 mA
0x36	1375 mA
0x37	1400 mA
0x38	1425 mA
0x39	1450 mA
0x3A	1475 mA
0x3B	1500 mA
0x3C	1525 mA
0x3D	1550 mA
0x3E	1575 mA
0x3F	1600 mA
0x40	1625 mA
0x41	1650 mA
0x42	1675 mA
0x43	1700 mA
0x44	1725 mA
0x45	1750 mA
0x46	1775 mA
0x47	1800 mA
0x48	1825 mA
0x49	1850 mA
0x4A	1875 mA

0x4B	1900 mA
0x4C	1925 mA
0x4D	1950 mA
0x4E	1975 mA
0x4F	2000 mA
0x50	2025 mA
0x51	2050 mA
0x52	2075 mA
0x53	2100 mA
0x54	2125 mA
0x55	2150 mA
0x56	2175 mA
0x57	2200 mA
0x58	2225 mA
0x59	2250 mA
0x5A	2275 mA
0x5B	2300 mA
0x5C	2325 mA
0x5D	2350 mA
0x5E	2375 mA
0x5F	2400 mA
0x60	2425 mA
0x61	2450 mA
0x62	2475 mA
0x63	2500 mA
0x64	2525 mA

				0x65	2550 mA
				0x66	2575 mA
				0x67	2600 mA
				0x68	2625 mA
				0x69	2650 mA
				0x6A	2675 mA
				0x6B	2700 mA
				0x6C	2725 mA
				0x6D	2750 mA
				0x6E	2775 mA
				0x6F	2800 mA
				0x70	2825 mA
				0x71	2850 mA
				0x72	2875 mA
				0x73	2900 mA
				0x74	2925 mA
				0x75	2950 mA
				0x76	2975 mA
				0x77	3000 mA

13.1.8 Register STATUS_H

Address	Name	POR value	Status Register H							
0x07	STATUS_H	0x00								
7	6	5	4	3	2	1	0			

S_IBAT_CHG_EFF<7:0>																																														
Field name	Bits	Type	POR	Description																																										
Effective charging current when junction temperature regulation and/or battery temperature profiels are in action. The Maximum value is 3500 mA. S_IBATT_CHG_EFF = 25+N*25 mA																																														
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S_IBAT_CHG_EFF	[7:0]	RO	0x00																																											

0x14	525 mA
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0x26	975 mA
0x27	1000 mA
0x28	1025 mA
0x29	1050 mA
0x2A	1075 mA
0x2B	1100 mA
0x2C	1125 mA
0x2D	1150 mA

0x2E	1175 mA
0x2F	1200 mA
0x30	1225 mA
0x31	1250 mA
0x32	1275 mA
0x33	1300 mA
0x34	1325 mA
0x35	1350 mA
0x36	1375 mA
0x37	1400 mA
0x38	1425 mA
0x39	1450 mA
0x3A	1475 mA
0x3B	1500 mA
0x3C	1525 mA
0x3D	1550 mA
0x3E	1575 mA
0x3F	1600 mA
0x40	1625 mA
0x41	1650 mA
0x42	1675 mA
0x43	1700 mA
0x44	1725 mA
0x45	1750 mA
0x46	1775 mA
0x47	1800 mA

0x48	1825 mA
0x49	1850 mA
0x4A	1875 mA
0x4B	1900 mA
0x4C	1925 mA
0x4D	1950 mA
0x4E	1975 mA
0x4F	2000 mA
0x50	2025 mA
0x51	2050 mA
0x52	2075 mA
0x53	2100 mA
0x54	2125 mA
0x55	2150 mA
0x56	2175 mA
0x57	2200 mA
0x58	2225 mA
0x59	2250 mA
0x5A	2275 mA
0x5B	2300 mA
0x5C	2325 mA
0x5D	2350 mA
0x5E	2375 mA
0x5F	2400 mA
0x60	2425 mA
0x61	2450 mA

0x62	2475 mA
0x63	2500 mA
0x64	2525 mA
0x65	2550 mA
0x66	2575 mA
0x67	2600 mA
0x68	2625 mA
0x69	2650 mA
0x6A	2675 mA
0x6B	2700 mA
0x6C	2725 mA
0x6D	2750 mA
0x6E	2775 mA
0x6F	2800 mA
0x70	2825 mA
0x71	2850 mA
0x72	2875 mA
0x73	2900 mA
0x74	2925 mA
0x75	2950 mA
0x76	2975 mA
0x77	3000 mA
0x78	3025 mA
0x79	3050 mA
0x7A	3075 mA
0x7B	3100 mA

				0x7C	3125 mA
				0x7D	3150 mA
				0x7E	3175 mA
				0x7F	3200 mA
				0x80	3225 mA
				0x81	3250 mA
				0x82	3275 mA
				0x83	3300 mA
				0x84	3325 mA
				0x85	3350 mA
				0x86	3375 mA
				0x87	3400 mA
				0x88	3425 mA
				0x89	3450 mA
				0x8A	3475 mA
				0x8B	3500 mA

13.1.9 Register STATUS_I

Address	Name	POR value	Status Register I								
0x08	STATUS_I	0x00	7	6	5	4	3	2	1	0	
S_VBAT_CHG_EFF<7:0>											
Field name	Bits	Type	POR	Description							

				Effective charging voltage when battery temperature profiles are in action. The maximum value is 4800 mV. S_VBAT_CHG_EFF = 20+N*20 mV.																																																
S_VBAT_CHG_EFF	[7:0]	RO	0x00	<table border="1"><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>0x00 (POR)</td><td>20 mV</td></tr><tr><td>0x01</td><td>40 mV</td></tr><tr><td>0x02</td><td>60 mV</td></tr><tr><td>0x03</td><td>80 mV</td></tr><tr><td>0x04</td><td>100 mV</td></tr><tr><td>0x05</td><td>120 mV</td></tr><tr><td>0x06</td><td>140 mV</td></tr><tr><td>0x07</td><td>160 mV</td></tr><tr><td>0x08</td><td>180 mV</td></tr><tr><td>0x09</td><td>200 mV</td></tr><tr><td>0x0A</td><td>220 mV</td></tr><tr><td>0x0B</td><td>240 mV</td></tr><tr><td>0x0C</td><td>260 mV</td></tr><tr><td>0x0D</td><td>280 mV</td></tr><tr><td>0x0E</td><td>300 mV</td></tr><tr><td>0x0F</td><td>320 mV</td></tr><tr><td>0x10</td><td>340 mV</td></tr><tr><td>0x11</td><td>360 mV</td></tr><tr><td>0x12</td><td>380 mV</td></tr><tr><td>0x13</td><td>400 mV</td></tr><tr><td>0x14</td><td>420 mV</td></tr><tr><td>0x15</td><td>440 mV</td></tr><tr><td>0x16</td><td>460 mV</td></tr></tbody></table>	Value	Description	0x00 (POR)	20 mV	0x01	40 mV	0x02	60 mV	0x03	80 mV	0x04	100 mV	0x05	120 mV	0x06	140 mV	0x07	160 mV	0x08	180 mV	0x09	200 mV	0x0A	220 mV	0x0B	240 mV	0x0C	260 mV	0x0D	280 mV	0x0E	300 mV	0x0F	320 mV	0x10	340 mV	0x11	360 mV	0x12	380 mV	0x13	400 mV	0x14	420 mV	0x15	440 mV	0x16	460 mV
Value	Description																																																			
0x00 (POR)	20 mV																																																			
0x01	40 mV																																																			
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0x03	80 mV																																																			
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0x08	180 mV																																																			
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0x0B	240 mV																																																			
0x0C	260 mV																																																			
0x0D	280 mV																																																			
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0x11	360 mV																																																			
0x12	380 mV																																																			
0x13	400 mV																																																			
0x14	420 mV																																																			
0x15	440 mV																																																			
0x16	460 mV																																																			

0x17	480 mV
0x18	500 mV
0x19	520 mV
0x1A	540 mV
0x1B	560 mV
0x1C	580 mV
0x1D	600 mV
0x1E	620 mV
0x1F	640 mV
0x20	660 mV
0x21	680 mV
0x22	700 mV
0x23	720 mV
0x24	740 mV
0x25	760 mV
0x26	780 mV
0x27	800 mV
0x28	820 mV
0x29	840 mV
0x2A	860 mV
0x2B	880 mV
0x2C	900 mV
0x2D	920 mV
0x2E	940 mV
0x2F	960 mV
0x30	980 mV

0x31	1000 mV
0x32	1020 mV
0x33	1040 mV
0x34	1060 mV
0x35	1080 mV
0x36	1100 mV
0x37	1120 mV
0x38	1140 mV
0x39	1160 mV
0x3A	1180 mV
0x3B	1200 mV
0x3C	1220 mV
0x3D	1240 mV
0x3E	1260 mV
0x3F	1280 mV
0x40	1300 mV
0x41	1320 mV
0x42	1340 mV
0x43	1360 mV
0x44	1380 mV
0x45	1400 mV
0x46	1420 mV
0x47	1440 mV
0x48	1460 mV
0x49	1480 mV
0x4A	1500 mV

0x4B	1520 mV
0x4C	1540 mV
0x4D	1560 mV
0x4E	1580 mV
0x4F	1600 mV
0x50	1620 mV
0x51	1640 mV
0x52	1660 mV
0x53	1680 mV
0x54	1700 mV
0x55	1720 mV
0x56	1740 mV
0x57	1760 mV
0x58	1780 mV
0x59	1800 mV
0x5A	1820 mV
0x5B	1840 mV
0x5C	1860 mV
0x5D	1880 mV
0x5E	1900 mV
0x5F	1920 mV
0x60	1940 mV
0x61	1960 mV
0x62	1980 mV
0x63	2000 mV
0x64	2020 mV

0x65	2040 mV
0x66	2060 mV
0x67	2080 mV
0x68	2100 mV
0x69	2120 mV
0x6A	2140 mV
0x6B	2160 mV
0x6C	2180 mV
0x6D	2200 mV
0x6E	2220 mV
0x6F	2240 mV
0x70	2260 mV
0x71	2280 mV
0x72	2300 mV
0x73	2320 mV
0x74	2340 mV
0x75	2360 mV
0x76	2380 mV
0x77	2400 mV
0x78	2420 mV
0x79	2440 mV
0x7A	2460 mV
0x7B	2480 mV
0x7C	2500 mV
0x7D	2520 mV
0x7E	2540 mV

0x7F	2560 mV
0x80	2580 mV
0x81	2600 mV
0x82	2620 mV
0x83	2640 mV
0x84	2660 mV
0x85	2680 mV
0x86	2700 mV
0x87	2720 mV
0x88	2740 mV
0x89	2760 mV
0x8A	2780 mV
0x8B	2800 mV
0x8C	2820 mV
0x8D	2840 mV
0x8E	2860 mV
0x8F	2880 mV
0x90	2900 mV
0x91	2920 mV
0x92	2940 mV
0x93	2960 mV
0x94	2980 mV
0x95	3000 mV
0x96	3020 mV
0x97	3040 mV
0x98	3060 mV

0x99	3080 mV
0x9A	3100 mV
0x9B	3120 mV
0x9C	3140 mV
0x9D	3160 mV
0x9E	3180 mV
0x9F	3200 mV
0xA0	3220 mV
0xA1	3240 mV
0xA2	3260 mV
0xA3	3280 mV
0xA4	3300 mV
0xA5	3320 mV
0xA6	3340 mV
0xA7	3360 mV
0xA8	3380 mV
0xA9	3400 mV
0xAA	3420 mV
0xAB	3440 mV
0xAC	3460 mV
0xAD	3480 mV
0xAE	3500 mV
0xAF	3520 mV
0xB0	3540 mV
0xB1	3560 mV
0xB2	3580 mV

0xB3	3600 mV
0xB4	3620 mV
0xB5	3640 mV
0xB6	3660 mV
0xB7	3680 mV
0xB8	3700 mV
0xB9	3720 mV
0xBA	3740 mV
0xBB	3760 mV
0xBC	3780 mV
0xBD	3800 mV
0xBE	3820 mV
0xBF	3840 mV
0xC0	3860 mV
0xC1	3880 mV
0xC2	3900 mV
0xC3	3920 mV
0xC4	3940 mV
0xC5	3960 mV
0xC6	3980 mV
0xC7	4000 mV
0xC8	4020 mV
0xC9	4040 mV
0xCA	4060 mV
0xCB	4080 mV
0xCC	4100 mV

0xCD	4120 mV
0xCE	4140 mV
0xCF	4160 mV
0xD0	4180 mV
0xD1	4200 mV
0xD2	4220 mV
0xD3	4240 mV
0xD4	4260 mV
0xD5	4280 mV
0xD6	4300 mV
0xD7	4320 mV
0xD8	4340 mV
0xD9	4360 mV
0xDA	4380 mV
0xDB	4400 mV
0xDC	4420 mV
0xDD	4440 mV
0xDE	4460 mV
0xDF	4480 mV
0xE0	4500 mV
0xE1	4520 mV
0xE2	4540 mV
0xE3	4560 mV
0xE4	4580 mV
0xE5	4600 mV
0xE6	4620 mV

				0xE7	4640 mV
				0xE8	4660 mV
				0xE9	4680 mV
				0xEA	4700 mV
				0xEB	4720 mV
				0xEC	4740 mV
				0xED	4760 mV
				0xEE	4780 mV
				0xEF	4800 mV

13.1.10 Register EVENT_A

Address	Name	POR value	Event Register A (Event fields are set by hardware. Write 1 to the field to clear.)												
0x09	EVENT_A	0x00	7	6	5	4	3	2	1	0					
Reserved 0	E_VBAT_OV	E_VBAT_UV	E_VIN_OV	E_VIN_DROP	E_VIN_UV	Reserved 0	E_AD_P_DET								
Field name															
Bits															
Field name															
E_VBAT_OV	[6]	EVENT	0x0	VBAT overvoltage event											
E_VBAT_UV	[5]	EVENT	0x0	VBAT undervoltage event											
E_VIN_OV	[4]	EVENT	0x0	VIN overvoltage event											
E_VIN_DROP	[3]	EVENT	0x0	VIN dropped below the VIN_DROP threshold											
E_VIN_UV	[2]	EVENT	0x0	VIN undervoltage event											
E_AD_P_DET	[0]	EVENT	0x0	An adaptor was inserted or removed											

13.1.11 Register EVENT_B

Address	Name	POR value	Event Register B (Event fields are set by hardware. Write 1 to the field to clear.)							
0x0A	EVENT_B	0x00	7	6	5	4	3	2	1	0
E_BATDET	Reserved	Reserved	Reserved	Reserved	Reserved	E_TJUNC_POR	E_TJUNC_CRIT	E_TJUNC_WARN		
Field name	Bits	Type	POR	Description						
E_BATDET	[7]	EVENT	0x0	The battery detection status changed.						
E_TJUNC_POR	[2]	EVENT	0x0	Junction temperature above TJUNC_POR threshold event. Reset only in NOPOWER state (VAVDD POR).						
E_TJUNC_CRIT	[1]	EVENT	0x0	The junction temperature status changed (S_TJUNC_CRIT)						
E_TJUNC_WARN	[0]	EVENT	0x0	The junction temperature status changed (S_TJUNC_WARN)						

13.1.12 Register EVENT_C

Address	Name	POR value	Event Register C (Event fields are set by hardware. Write 1 to the field to clear.)							
0x0B	EVENT_C	0x00	7	6	5	4	3	2	1	0
E_IIN_LIM_M	E_ADC_DONE_E	E_LOWBA_T	E_IIN_REV_LIM_MA_X	E_IIN_REV_LI_M	E_DCDC_REV_BOOST_FAUL_T	E_VIN_REV_O_V	E_VIN_REV_SHORT			
Field name	Bits	Type	POR	Description						
E_IIN_LIM	[7]	EVENT	0x0	The input current crossed the IIN_LIM limit.						
E_ADC_DONE	[6]	EVENT	0x0	The ADC measurement was completed.						
E_LOWBAT	[5]	EVENT	0x0	The battery voltage dropped below VSYS_MIN during Buck operation						
E_IIN_REV_LIM_MAX	[4]	EVENT	0x0	The output current of the reverse boost stayed above the IIN_REV_LIM limit for longer than T_REV_ILIM_MAX[1:0].						

E_IIN_REV_LIM	[3]	EVENT	0x0	The output current of the reverse boost crossed the IIN_REV_LIM limit.
E_DCDC_REV_BOOST_FAULT	[2]	EVENT	0x0	The reverse boost mode of the DC-DC converter was blocked (VIN > VIN_SHORT).
E_VIN_REV_OV	[1]	EVENT	0x0	The output voltage of the reverse boost crossed the VIN_REV_OV threshold.
E_VIN_REV_SHORT	[0]	EVENT	0x0	The output voltage of the reverse boost dropped below VIN_SHORT.

13.1.13 Register EVENT_D

Address	Name	POR value	Event Register D (Event fields are set by hardware. Write 1 to the field to clear.)								
0x0C	EVENT_D	0x00	7	6	5	4	3	2	1	0	
Field name	Bits	Type	POR	Description							
E_TIMEOUT_CCCV	[7]	EVENT	0x0	E_TIMEOUT_CCCV	E_TIMEOUT_PRE	E_WD	E_VSYS_OV	E_VSYS_POR	Reserved	Reserved	E_CHG_STAT
E_TIMEOUT_CCCV	[7]	EVENT	0x0	The charging timer expired (CC/CV).							
E_TIMEOUT_PRE	[6]	EVENT	0x0	The charging timer expired (precharge).							
E_WD	[5]	EVENT	0x0	The watchdog timer expired.							
E_VSYS_OV	[4]	EVENT	0x0	The system voltage crossed the VSYS_OV threshold.							
E_VSYS_POR	[3]	EVENT	0x0	VSYS dropped below the VSYS_POR threshold. Reset only in NOPOWER state (VAVDD POR).							
E_CHG_STAT	[0]	EVENT	0x0	The status of the charger (CHG_STAT) changed, based on CHG_STAT_EVENT_SEL selection.							

13.1.14 Register EVENT_E

Address	Name	POR value	Event Register E (Event fields are set by hardware. Write 1 to the field to clear.)								
0x0D	EVENT_E	0x00	7	6	5	4	3	2	1	0	

Reserved	Reserved	E_BOOST_STARTUP_OV	E_VSYS_UV	E_GPI3	E_GPI2	/ E_GPI1	E_GPIO
Field name	Bits	Type	POR	Description			
E_BOOST_STARTUP_OV	[5]	EVENT	0x0	During boost startup, the Vcenter node was over its acceptable voltage.			
E_VSYS_UV	[4]	EVENT	0x0	VSYS went below the VSYS_UV_N threshold (typical 2.2V).			
E_GPI3	[3]	EVENT	0x0	GPI3 input pin change event.			
E_GPI2	[2]	EVENT	0x0	GPI2 input pin change event.			
E_GPI1	[1]	EVENT	0x0	GPI1 input pin change event.			
E_GPIO	[0]	EVENT	0x0	GPIO0 input pin change event.			

13.1.15 Register EVENT_F

Address	Name	POR value	Event Register F (Event fields are set by hardware. Write 1 to the field to clear.)														
0x0E	EVENT_F	0x00	7	6	5	4	3	2	1	0							
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	E_LWBAT_BOOST	E_TORCH_CHG_OV	Field name								
								Description									
E_LWBAT_BOOST	[1]	EVENT	0x0	The battery voltage dropped below VSYS_MIN during Boost operation													
E_TORCH_CHG_OV	[0]	EVENT	0x0	VIN > 6V occurred during Vsys regulating states. Flash_Ido_en is disabled													

13.1.16 Register MASK_A

Address	Name	POR value	Mask Register A								
0x12	MASK_A	0xFC	7	6	5	4	3	2	1	0	

Reserved 1	M_VBAT_OV	M_VBAT_UV	M_VIN_OV	M_VIN_DROP	M_VIN_UV	Reserved 0	M_ADP_DET
Field name	Bits	Type	POR	Description			
M_VBAT_OV	[6]	RW OTP	0x1	Mask bit for E_VBAT_OV			
M_VBAT_UV	[5]	RW OTP	0x1	Mask bit for E_VBAT_UV			
M_VIN_OV	[4]	RW OTP	0x1	Mask bit for E_VIN_OV			
M_VIN_DROP	[3]	RW OTP	0x1	Mask bit for E_VIN_DROP			
M_VIN_UV	[2]	RW OTP	0x1	Mask bit for E_VIN_UV			
M_ADP_DET	[0]	RW OTP	0x0	Mask bit for E_ADP_DET			

13.1.17 Register MASK_B

Address	Name	POR value	Mask Register B								
0x13	MASK_B	0xFF	7	6	5	4	3	2	1	0	
M_BATDET	Reserved	Reserved	Reserved	Reserved	Reserved	M_TJUNC_POR	M_TJUNC_CRIT	M_TJUNC_WARN			
Field name	Bits	Type	POR	Description							
M_BATDET	[7]	RW OTP	0x1	Mask bit for E_BATDET							
M_TJUNC_POR	[2]	RW OTP	0x1	Mask bit for E_TJUNC_POR							

M_TJUNC_CRIT	[1]	RW OTP	0x1	Mask bit for E_TJUNC_CRIT			
M_TJUNC_WARN	[0]	RW OTP	0x1	Mask bit for E_TJUNC_WARN			

13.1.18 Register MASK_C

Address	Name	POR value	Mask Register C								
0x14	MASK_C	0xFF	7	6	5	4	3	2	1	0	
M_IIN_LI M	M_ADC_DONE E	M_LOWBA T	M_IIN_REV_LIM_MA X	M_IIN_REV_LI M	M_DCDC_REV_BOOST_FAU LT	M_VIN_REV_O V	M_VIN_REV_SHOR T				
Field name		Bits	Type	POR	Description						
M_IIN_LIM			[7]	RW OTP	0x1	Mask bit for E_IIN_LIM					
M_ADC_DONE			[6]	RW OTP	0x1	Mask bit for E_ADC_DONE					
M_LOWBAT			[5]	RW OTP	0x1	Mask bit for E_LOWBAT					
M_IIN_REV_LIM_MAX			[4]	RW OTP	0x1	Mask bit for E_IIN_REV_LIM_MAX					
M_IIN_REV_LIM			[3]	RW OTP	0x1	Mask bit for E_IIN_REV_LIM					
M_DCDC_REV_BOOST_FAULT			[2]	RW OTP	0x1	Mask bit for E_DCDC_REV_BOOST_FAULT					
M_VIN_REV_OV			[1]	RW OTP	0x1	Mask bit for E_VIN_REV_OV					

M_VIN_REV_SHORT	[0]	RW OTP	0x1	Mask bit for E_VIN_REV_SHORT	
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13.1.19 Register MASK_D

Address	Name	POR value	Mask Register D								
0x15	MASK_D	0xF9	7	6	5	4	3	2	1	0	
M_TIMEOUT_CCCV	M_TIMEOUT_PRE	M_WD	M_VSYS_OV	M_VSYS_POR	Reserved	Reserved	M_CHG_STAT				
Field name	Bits	Type	POR	Description							
M_TIMEOUT_CCCV	[7]	RW OTP	0x1	Mask bit for E_TIMEOUT_CCCV							
M_TIMEOUT_PRE	[6]	RW OTP	0x1	Mask bit for E_TIMEOUT_PRE							
M_WD	[5]	RW OTP	0x1	Mask bit for E_WD							
M_VSYS_OV	[4]	RW OTP	0x1	Mask bit for E_VSYS_OV							
M_VSYS_POR	[3]	RW OTP	0x1	Mask bit for E_VSYS_POR							
M_CHG_STAT	[0]	RW OTP	0x1	Mask bit for E_CHG_STAT							

13.1.20 Register MASK_E

Address	Name	POR value	Mask Register E							
0x16	MASK_E	0x3F	7	6	5	4	3	2	1	0
Reserved	Reserved		M_BOOST_STARTUP_OV	M_VSYS_UV	M_GPI3	M_GPI2	M_GPI1	M_GPI0		
Field name		Bits	Type	POR	Description					
M_BOOST_STARTUP_OV		[5]	RW OTP	0x1	Mask bit for E_BOOST_STARTUP_OV					
M_VSYS_UV		[4]	RW OTP	0x1	Mask bit for E_VSYS_UV_N					
M_GPI3		[3]	RW OTP	0x1	Mask bit for E_GPI3					
M_GPI2		[2]	RW OTP	0x1	Mask bit for E_GPI2					
M_GPI1		[1]	RW OTP	0x1	Mask bit for E_GPI1					
M_GPI0		[0]	RW OTP	0x1	Mask bit for E_GPI0					

13.1.21 Register MASK_F

Address	Name	POR value	Mask Register F							
0x17	MASK_F	0x03	7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	M_LOWBAT_BOOST	M_TORCH_CHG_OV		
Field name		Bits	Type	POR	Description					

M_LOWBAT_BOOST	[1]	RW OTP	0x1	Mask bit for E_LOWBAT_BOOST					
M_TORCH_CHG_OV	[0]	RW OTP	0x1	Mask bit for E_TORCH_CHG_OV					

13.1.22 Register MASK_G

Address	Name	POR value	Mask Register G								
0x18	MASK_G	0x00	7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
Field name	Bits	Type	POR	Description							

13.1.23 Register MASK_H

Address	Name	POR value	Mask Register H								
0x19	MASK_H	0x00	7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
Field name	Bits	Type	POR	Description							

13.1.24 Register MASK_I

Address	Name	POR value	Mask Register I								
0x1A	MASK_I	0x00	7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
Field name	Bits	Type	POR	Description							

13.2 Voltage Monitoring

13.2.1 Register VIN_CTRL_A

Address	Name	POR value	Input Voltage Control Register A								
0x1B	VIN_CTRL_A	0x00	7	6	5	4	3	2	1	0	
VIN_DROP<7:0>											
Field name	Bits	Type	POR	Description							
VIN_DROP	[7:0]	RW OTP	0x00	VIN drop threshold. Any value greater than the maximum will be stored in the register but limited to the maximum at the output. $VIN_DROP=4.3+(N*0.05) V$							
Value	Description										
0x00 (POR)	4.30 V										
0x01	4.35 V										
0x02	4.40 V										
0x03	4.45 V										

0x04	4.50 V
0x05	4.55 V
0x06	4.60 V
0x07	4.65 V
0x08	4.70 V
0x09	4.75 V
0x0A	4.80 V
0x0B	4.85 V
0x0C	4.90 V
0x0D	4.95 V
0x0E	5.00 V
0x0F	5.05 V
0x10	5.10 V
0x11	5.15 V
0x12	5.20 V
0x13	5.25 V
0x14	5.30 V
0x15	5.35 V
0x16	5.40 V
0x17	5.45 V
0x18	5.50 V
0x19	5.55 V
0x1A	5.60 V
0x1B	5.65 V
0x1C	5.70 V
0x1D	5.75 V

0x1E	5.80 V
0x1F	5.85 V
0x20	5.90 V
0x21	5.95 V
0x22	4.00 V
0x23	4.05 V
0x24	4.10 V
0x25	4.15 V
0x26	4.20 V
0x27	4.25 V
0x28	4.30 V
0x29	4.35 V
0x2A	4.40 V
0x2B	4.45 V
0x2C	4.50 V
0x2D	4.55 V
0x2E	4.60 V
0x2F	4.65 V
0x30	4.70 V
0x31	4.75 V
0x32	4.80 V
0x33	4.85 V
0x34	4.90 V
0x35	4.95 V
0x36	5.00 V
0x37	5.05 V

0x38	5.10 V
0x39	5.15 V
0x3A	5.20 V
0x3B	5.25 V
0x3C	5.30 V
0x3D	5.35 V
0x3E	5.40 V
0x3F	5.45 V
0x40	5.50 V
0x41	5.55 V
0x42	5.60 V
0x43	5.65 V
0x44	5.70 V
0x45	5.75 V
0x46	5.80 V
0x47	5.85 V
0x48	5.90 V
0x49	5.95 V
0x4A	6.00 V
0x4B	6.05 V
0x4C	6.10 V
0x4D	6.15 V
0x4E	6.20 V
0x4F	6.25 V
0x50	6.30 V
0x51	6.35 V

0x52	6.40 V
0x53	6.45 V
0x54	6.50 V
0x55	6.55 V
0x56	6.60 V
0x57	6.65 V
0x58	6.70 V
0x59	6.75 V
0x5A	6.80 V
0x5B	6.85 V
0x5C	6.90 V
0x5D	6.95 V
0x5E	9.00 V
0x5F	9.05 V
0x60	9.10 V
0x61	9.15 V
0x62	9.20 V
0x63	9.25 V
0x64	9.30 V
0x65	9.35 V
0x66	9.40 V
0x67	9.45 V
0x68	9.50 V
0x69	9.55 V
0x6A	9.60 V
0x6B	9.65 V

0x6C	9.70 V
0x6D	9.75 V
0x6E	9.80 V
0x6F	9.85 V
0x70	9.90 V
0x71	9.95 V
0x72	10.00 V
0x73	10.05 V
0x74	10.10 V
0x75	10.15 V
0x76	10.20 V
0x77	10.25 V
0x78	10.30 V
0x79	10.35 V
0x7A	10.40 V
0x7B	10.45 V
0x7C	10.50 V
0x7D	10.55 V
0x7E	10.60 V
0x7F	10.65 V
0x80	10.70 V
0x81	10.75 V
0x82	10.80 V
0x83	10.85 V
0x84	10.90 V
0x85	10.95 V

				0x86	9.00 V
				0x87	9.05 V
				0x88	9.10 V
				0x89	9.15 V
				0x8A	9.20 V
				0x8B	9.25 V
				0x8C	9.30 V
				0x8D	9.35 V
				0x8E	9.40 V
				0x8F	9.45 V
				0x90	9.50 V
				0x91	9.55 V
				0x92	9.60 V
				0x93	9.65 V
				0x94	9.70 V
				0x95	9.75 V
				0x96	9.80 V
				0x97	9.85 V
				0x98	9.90 V
				0x99	9.95 V
				0x9A	12.00 V

13.2.2 Register VBAT_CTRL_A

Address	Name	POR value	Battery Voltage Control Register A
---------	------	-----------	------------------------------------

0x1C		VBAT_CTRL_A		0xF0																
		7	6	5	4	3	2	1	0											
VBAT_OV<3:0>								VBAT_UV<3:0>												
Field name		Bits	Type	POR	Description															
Battery overvoltage threshold (4.0 V-5.5 V). VBAT_OV=4.0V + N*100 mV																				
Value								Description												
VBAT_OV	[7:4]	RW OTP	0xF		0x0	4.0 V														
					0x1	4.1 V														
					0x2	4.2 V														
					0x3	4.3 V														
					0x4	4.4 V														
					0x5	4.5 V														
					0x6	4.6 V														
					0x7	4.7 V														
					0x8	4.8 V														
					0x9	4.9 V														
					0xA	5.0 V														
					0xB	5.1 V														
					0xC	5.2 V														
					0xD	5.3 V														
					0xE	5.4 V														
					0xF	(POR)														
VBAT_UV		[3:0]	RW OTP	0x0	Battery undervoltage threshold (2.2 V-2.95 V). VBAT_UV=2.2V + N*50 mV															
Value								Description												

			0x0 (POR)	2.20 V
			0x1	2.25 V
			0x2	2.30 V
			0x3	2.35 V
			0x4	2.40 V
			0x5	2.45 V
			0x6	2.50 V
			0x7	2.55 V
			0x8	2.60 V
			0x9	2.65 V
			0xA	2.70 V
			0xB	2.75 V
			0xC	2.80 V
			0xD	2.85 V
			0xE	2.90 V
			0xF	2.95 V

13.3 DC-DC

13.3.1 Register DCDC_CTRL_A

Reserved	Reserved	DCDC_FSW<1:0>		DCDC_FSW_AUTO	OTG_EN	DCDC_EN	CHG_EN						
Field name	Bits	Type	POR	Description									
DCDC_FSW	[5:4]	RW OTP	0x1	Switching frequency of the DC-DC converter. Also sets the max buck frequency allowable during auto mode.									
				<table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>1.0 MHz</td> </tr> <tr> <td>0x1 (POR)</td> <td>1.5 MHz</td> </tr> <tr> <td>0x2</td> <td>2.0 MHz</td> </tr> <tr> <td>0x3</td> <td>2.5 MHz</td> </tr> </tbody> </table>				Value	Description	0x0	1.0 MHz	0x1 (POR)	1.5 MHz
Value	Description												
0x0	1.0 MHz												
0x1 (POR)	1.5 MHz												
0x2	2.0 MHz												
0x3	2.5 MHz												
Enables dynamic frequency adaptation.													
Enables reverse boost mode of the DC-DC for OTG. This bit self-clears when an OTG fault occurs.													
Enables DC-DC converter. This bit is evaluated only when VBAT > VSYS_MIN.													
CHG_EN	[0]	RW OTP	0x1	Main Charger Enable. This bit self-clears when a charger fault occurs.									

13.3.2 Register DCDC_CTRL_B

Address	Name	POR value	DC-DC Control Register B				
0x1E	DCDC_CTRL_B	0x02					
7	6	5	4	3	2	1	0
IN_PWR_RED	IIN_REV_LIM<2:0>		DCDC_REV_PEAK_ILIM<1:0>		DCDC_PEAK_ILIM<1:0>		
Field name	Bits	Type	POR	Description			

IN_PWR_RED	[7]	RW OTP	0x0	Activates the automatic input power reduction.																		
IIN_REV_LIM	[6:4]	RW OTP	0x0	DC-DC output current limit in reverse boost mode. <table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0 (POR)</td><td>500 mA</td></tr> <tr><td>0x1</td><td>900 mA</td></tr> <tr><td>0x2</td><td>1200 mA</td></tr> <tr><td>0x3</td><td>1500 mA</td></tr> <tr><td>0x4</td><td>2000 mA</td></tr> <tr><td>0x5</td><td>2000 mA</td></tr> <tr><td>0x6</td><td>2000 mA</td></tr> <tr><td>0x7</td><td>2000 mA</td></tr> </tbody> </table>	Value	Description	0x0 (POR)	500 mA	0x1	900 mA	0x2	1200 mA	0x3	1500 mA	0x4	2000 mA	0x5	2000 mA	0x6	2000 mA	0x7	2000 mA
Value	Description																					
0x0 (POR)	500 mA																					
0x1	900 mA																					
0x2	1200 mA																					
0x3	1500 mA																					
0x4	2000 mA																					
0x5	2000 mA																					
0x6	2000 mA																					
0x7	2000 mA																					
DCDC_REV_PEAK_ILIM	[3:2]	RW OTP	0x0	DC-DC peak current limit in reverse boost mode <table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0 (POR)</td><td>5000 mA</td></tr> <tr><td>0x1</td><td>6000 mA</td></tr> <tr><td>0x2</td><td>7000 mA</td></tr> <tr><td>0x3</td><td>8000 mA</td></tr> </tbody> </table>	Value	Description	0x0 (POR)	5000 mA	0x1	6000 mA	0x2	7000 mA	0x3	8000 mA								
Value	Description																					
0x0 (POR)	5000 mA																					
0x1	6000 mA																					
0x2	7000 mA																					
0x3	8000 mA																					
DCDC_PEAK_ILIM	[1:0]	RW OTP	0x2	DC-DC peak current limit. <table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td>6000 mA</td></tr> <tr><td>0x1</td><td>7000 mA</td></tr> <tr><td>0x2 (POR)</td><td>8000 mA</td></tr> <tr><td>0x3</td><td>9000 mA</td></tr> </tbody> </table>	Value	Description	0x0	6000 mA	0x1	7000 mA	0x2 (POR)	8000 mA	0x3	9000 mA								
Value	Description																					
0x0	6000 mA																					
0x1	7000 mA																					
0x2 (POR)	8000 mA																					
0x3	9000 mA																					

13.3.3 Register DCDC_CTRL_C

Address	Name	POR value	DC-DC Control Register C										
0x1F	DCDC_CTRL_C	0x08	7	6	5	4	3	2	1	0			
T_REV_ILIM_MAX<1:0>				IIN_LIM_SLEW<1:0>			DCDC_REV_BOOST_FSW<1:0>		Reserved	IIN_LIM_SEL			
Field name		Bits	Type	POR	Description								
Maximum duration of a reverse current limit condition before disabling boost.													
T_REV_ILIM_MAX		[7:6]	RW OTP	0x0	Value		Description						
					0x0 (POR)	No limit							
					0x1	1 ms							
					0x2	10 ms							
					0x3	30 ms							
					Slew rate of the input current.								
IIN_LIM_SLEW		[5:4]	RW OTP	0x0	Value		Description						
					0x0 (POR)	200 uA/us							
					0x1	100 uA/us							
					0x2	25 uA/us							
					0x3	2 mA/us							
					Switching frequency of the DC-DC converter in reverse boost mode.								
DCDC_REV_BOOST_FSW		[3:2]	RW OTP	0x2	Value		Description						
					0x0	0.375 MHz							

				0x1	0.75 MHz
				0x2 (POR)	1.5 MHz
				0x3	3.0 MHz
Input current limit selection (only valid if IIN_LIM_ISET = 0)					
Value		Description			
IIN_LIM_SEL [0]		RW OTP	0x0	0x0 (POR)	Input current limit setting is IIN_LIM0.
				0x1	Input current limit setting is IIN_LIM1.

13.3.4 Register DCDC_CTRL_D

Address	Name	POR value	DC-DC Control Register D								
0x20	DCDC_CTRL_D	0x00	7	6	5	4	3	2	1	0	
Reserved	IIN_LIM1<2:0>					Reserved	IIN_LIM0<2:0>				
Field name		Bits	Type	POR	Description						
Input current limit. This setting is active for IIN_LIM_SEL = 1											
IIN_LIM1		[6:4]	RW OTP	0x0	Value		Description				
					0x0 (POR)		0x0	100 mA			
					0x1		0x1	150 mA			
					0x2		0x2	500 mA			
					0x3		0x3	900 mA			
					0x4		0x4	1500 mA			

				0x5	2000 mA		
				0x6	2500 mA		
				0x7	3000 mA		
				Input current limit. This setting is active for IIN_LIM_SEL = 0			
Value	Description						
0x0 (POR)	100 mA						
0x1	150 mA						
0x2	500 mA						
0x3	900 mA						
0x4	1500 mA						
0x5	2000 mA						
0x6	2500 mA						
0x7	3000 mA						

13.3.5 Register DCDC_CTRL_E

Address	Name	POR value	DC-DC Control Register E													
0x21	DCDC_CTRL_E	0x35	7	6	5	4	3	2	1	0						
VSYS_SLEW<1:0>			VIN_REV_SLEW<1:0>				IIN_DROP_AMOUNT<1:0>		IIN_DROP_INTERVAL<1:0>							
Field name	Bits	Type	POR	Description												
VSYS_SLEW	[7:6]	RW OTP	0x0	Slew rate of the output voltage in VSYS regulation mode.												
Value	Description															

				0x0 (POR)	200 uV/us
				0x1	100 uV/us
				0x2	25 uV/us
				0x3	2 mV/us
Slew rate of the output voltage in reverse boost mode.					
VIN_REV_SLEW	[5:4]	RW OTP	0x3	Value	Description
				0x0	0.2 mV/us
				0x1	0.5 mV/us
				0x2	1.0 mV/us
				0x3 (POR)	2.0 mV/us
IIN Drop Amount for Input Current Reduction					
IIN_DROP_AMOUNT	[3:2]	RW OTP	0x1	Value	Description
				0x0	25 mA
				0x1 (POR)	50 mA
				0x2	100 mA
				0x3	200 mA
IIN Drop Interval for Input Current Reduction					
IIN_DROP_INTERVAL	[1:0]	RW OTP	0x1	Value	Description
				0x0	64us
				0x1 (POR)	128us
				0x2	1ms
				0x3	6.2ms

13.3.6 Register DCDC_CTRL_F

Address	Name	POR value	DC-DC Control Register F																
0x22	DCDC_CTRL_F	0x07	7	6	5	4	3	2	1	0									
CHG_RESTART	Reserved	Reserved	FORCE_BOOST_SKIP DCDC_REV_VOUT<3:0>																
Field name	Bits	Type	POR	Description															
CHG_RESTART	[7]	RW	0x0	Restarts charging when '1' is written to this field. This field will always read back '0'.															
FORCE_BOOST_SKIP	[4]	RW OTP	0x0	Force skip in Boost															
DCDC_REV_VOUT	[3:0]	RW OTP	0x7	Flash Voltage Output. $4.80V + i * 100mV$. Maximum value restricted to 4.0V.															
Value	Description																		
0x0	4.8 V																		
0x1	4.9 V																		
0x2	5 V																		
0x3	5.1 V																		
0x4	5.2 V																		
0x5	5.3 V																		
0x6	5.4 V																		
0x7 (POR)	5.5 V																		
0x8	5.6 V																		
0x9	5.7 V																		
0xA	5.8 V																		

				0xB	5.9 V
				0xC	6 V
				0xD	6 V
				0xE	6 V
				0xF	6 V

13.4 Charger

13.4.1 Register CHG_CTRL_A

Address	Name	POR value	Charger Control Register A								
0x23	CHG_CTRL_A	0x14	7	6	5	4	3	2	1	0	
VBAT_RECHG<1:0>		VBAT_CHG<5:0>									
Field name	Bits	Type	POR	Description							
VBAT_RECHG	[7:6]	RW OTP	0x0	Battery voltage re-charge threshold.							
				Value	Description						
				0x0 (POR)	VBAT_CHG-100 mV						
				0x1	VBAT_CHG-160 mV						
				0x2	VBAT_CHG-200 mV						
VBAT_CHG	[5:0]	RW OTP	0x14	Target battery voltage (3.8 to 4.6 V). VBAT_CHG=3.8+N*0.02 V.							
				Value	Description						
				0x00	3.80 V						

0x01	3.82 V
0x02	3.84 V
0x03	3.86 V
0x04	3.88 V
0x05	3.90 V
0x06	3.92 V
0x07	3.94 V
0x08	3.96 V
0x09	3.98 V
0x0A	4.00 V
0x0B	4.02 V
0x0C	4.04 V
0x0D	4.06 V
0x0E	4.08 V
0x0F	4.10 V
0x10	4.12 V
0x11	4.14 V
0x12	4.16 V
0x13	4.18 V
0x14 (POR)	4.20 V
0x15	4.22 V
0x16	4.24 V
0x17	4.26 V
0x18	4.28 V
0x19	4.30 V

0x1A	4.32 V
0x1B	4.34 V
0x1C	4.36 V
0x1D	4.38 V
0x1E	4.40 V
0x1F	4.42 V
0x20	4.44 V
0x21	4.46 V
0x22	4.48 V
0x23	4.50 V
0x24	4.52 V
0x25	4.54 V
0x26	4.56 V
0x27	4.58 V
0x28	4.60 V
0x29	4.62 V
0x2A	4.64 V
0x2B	4.66 V
0x2C	4.68 V
0x2D	4.70 V
0x2E	4.72 V
0x2F	4.74 V
0x30	4.76 V
0x31	4.78 V
0x32	4.80 V

13.4.2 Register CHG_CTRL_B

Address	Name	POR value	Charger Control Register B																								
0x24	CHG_CTRL_B	0x80	7	6	5	4	3	2	1	0																	
IBAT_CC1_EN	Reserved 0		IBAT_CHG<5:0>																								
Field name	Bits	Type	POR	Description																							
IBAT_CC1_EN	[7]	RW OTP	0x1	Enables the CC1 step of the constant current charging.																							
				<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td>CC1 is disabled. Charger runs in precharge phase (IBAT_PRE) while VBAT_UV < VBAT < VSYS_MIN.</td></tr> <tr> <td>0x1 (POR)</td><td>CC1 is enabled. Charger runs in constant current phase (IBAT_CHG, limited by TJUNC regulation) while VBAT_UV < VBAT < VSYS_MIN.</td></tr> </tbody> </table>								Value	Description	0x0	CC1 is disabled. Charger runs in precharge phase (IBAT_PRE) while VBAT_UV < VBAT < VSYS_MIN.	0x1 (POR)	CC1 is enabled. Charger runs in constant current phase (IBAT_CHG, limited by TJUNC regulation) while VBAT_UV < VBAT < VSYS_MIN.										
Value	Description																										
0x0	CC1 is disabled. Charger runs in precharge phase (IBAT_PRE) while VBAT_UV < VBAT < VSYS_MIN.																										
0x1 (POR)	CC1 is enabled. Charger runs in constant current phase (IBAT_CHG, limited by TJUNC regulation) while VBAT_UV < VBAT < VSYS_MIN.																										
IBAT_CHG	[5:0]	RW OTP	0x00	Charging current in the CC-phase (0.5 to 3.5 A). The maximum value is 3.5 A (0x3C). Any value greater than the maximum will be stored in the register but tied to the maximum internally. IBAT_CHG=500+N*50 mA. All values greater than 0x3F is reserved.																							
				<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x00 (POR)</td><td>0.50 A</td></tr> <tr> <td>0x01</td><td>0.55 A</td></tr> <tr> <td>0x02</td><td>0.60 A</td></tr> <tr> <td>0x03</td><td>0.65 A</td></tr> <tr> <td>0x04</td><td>0.70 A</td></tr> <tr> <td>0x05</td><td>0.75 A</td></tr> <tr> <td>0x06</td><td>0.80 A</td></tr> </tbody> </table>								Value	Description	0x00 (POR)	0.50 A	0x01	0.55 A	0x02	0.60 A	0x03	0.65 A	0x04	0.70 A	0x05	0.75 A	0x06	0.80 A
Value	Description																										
0x00 (POR)	0.50 A																										
0x01	0.55 A																										
0x02	0.60 A																										
0x03	0.65 A																										
0x04	0.70 A																										
0x05	0.75 A																										
0x06	0.80 A																										

0x07	0.85 A
0x08	0.90 A
0x09	0.95 A
0x0A	1.00 A
0x0B	1.05 A
0x0C	1.10 A
0x0D	1.15 A
0x0E	1.20 A
0x0F	1.25 A
0x10	1.30 A
0x11	1.35 A
0x12	1.40 A
0x13	1.45 A
0x14	1.50 A
0x15	1.55 A
0x16	1.60 A
0x17	1.65 A
0x18	1.70 A
0x19	1.75 A
0x1A	1.80 A
0x1B	1.85 A
0x1C	1.90 A
0x1D	1.95 A
0x1E	2.00 A
0x1F	2.05 A
0x20	2.10 A

0x21	2.15 A
0x22	2.20 A
0x23	2.25 A
0x24	2.30 A
0x25	2.35 A
0x26	2.40 A
0x27	2.45 A
0x28	2.50 A
0x29	2.55 A
0x2A	2.60 A
0x2B	2.65 A
0x2C	2.70 A
0x2D	2.75 A
0x2E	2.80 A
0x2F	2.85 A
0x30	2.90 A
0x31	2.95 A
0x32	3.00 A
0x33	3.05 A
0x34	3.10 A
0x35	3.15 A
0x36	3.20 A
0x37	3.25 A
0x38	3.30 A
0x39	3.35 A
0x3A	3.40 A

				0x3B	3.45 A
				0x3C	3.50 A

13.4.3 Register CHG_CTRL_C

Address	Name	POR value	Charger Control Register C											
7	6	5	4	3	2	1	0							
Reserved	Reserved	IBAT_CHG_SLEW<1:0>				VSYS_MIN<3:0>								
Field name		Bits	Type	POR	Description									
IBAT_CHG_SLEW	[5:4]	RW OTP	0x0	0x0	Slew rate control for the charging current.									
					Value		Description							
					0x0 (POR)	200 uA/us								
					0x1	100 uA/us								
					0x2	25 uA/us								
					0x3	2 mA/us								
VSYS_MIN	[3:0]	RW OTP	0x8	0x8	Minimum system voltage (3.0 to 3.9 V). VSYS_MIN=3.0+N*0.06 V									
					Value		Description							
					0x0	3.00 V								
					0x1	3.06 V								
					0x2	3.12 V								
					0x3	3.18 V								
					0x4	3.24 V								
					0x5	3.30 V								

				0x6	3.36 V
				0x7	3.42 V
				0x8 (POR)	3.48 V
				0x9	3.54 V
				0xA	3.60 V
				0xB	3.66 V
				0xC	3.72 V
				0xD	3.78 V
				0xE	3.84 V
				0xF	3.90 V

13.4.4 Register CHG_CTRL_D

Address	Name	POR value	Charger Control Register D																				
7	6	5	4	3	2	1	0																
T_EOC<2:0>					IBAT_TERM<2:0>			IBAT_PRE<1:0>															
Field name	Bits	Type	POR	Description																			
T_EOC	[7:5]	RW OTP	0x0	End of charge detection time.																			
Value	Description																						
0x0 (POR)	0 min																						
0x1	1 min																						
0x2	5 min																						

				0x3 10 min 0x4 20 min 0x5 30 min 0x6 45 min 0x7 60 min			
				Charging termination current (100 to 450 mA). IBAT_TERM=100+N*50 mA			
IBAT_TERM	[4:2]	RW OTP	0x0	Value	Description		
				0x0 (POR)	100 mA		
				0x1	150 mA		
				0x2	200 mA		
				0x3	250 mA		
				0x4	300 mA		
				0x5	350 mA		
				0x6	400 mA		
				0x7	450 mA		
IBAT_PRE	[1:0]	RW OTP	0x2	Pre-charging current (50 to 400 mA). IBAT_PRE=2^N*50 mA.			
				Value	Description		
				0x0	50 mA		
				0x1	100 mA		
				0x2 (POR)	200 mA		
				0x3	400 mA		

13.4.5 Register CHG_CTRL_E

Address	Name	POR value	Charger Control Register E														
0x27	CHG_CTRL_E	0x00	7	6	5	4	3	2	1	0							
CHG_STAT_EVENT_SEL<1:0>			Reserved			Reserved			Reserved	Reserved							
Field name	Bits	Type	POR	Description													
CHG_STAT_EVENT_SEL [7:6]	RW OTP	0x0	0x0	Selects which transitions of charge status (S_CHG_STAT) will generate an E_CHG_STAT event													
				Value	Description												
				0x0 (POR)	Event on all status transitions (except faults)												
				0x1	Event on a limited set of transitions: All Other States->FULL FULL->All Other States												
				0x2	Event on a limited set of transitions: OFF->PC/CC/CV/TO PC/CC/CV/TO-->OFF/FULL/L1/L2												
				0x3	Event on a limited set of transitions: OFF->PC/CC/CV/TO PC/CC/CV/TO-->OFF/FULL/L1/L2 All Other States->CC CC->All Other States												

13.5 Battery Switch

13.5.1 Register BATSW_CTRL_A

Address	Name	POR value	Battery Switch Control Register A													
7	6	5	4	3	2	1	0									
Reserved	Reserved	T_PRE_BAT_ISO<1:0>			BAT_ISO_GPI	BAT_ISO_FULL	BAT_ISO_SHORT	BAT_ISO_LONG								
Field name	Bits	Type	POR	Description												
T_PRE_BAT_ISO	[5:4]	RW OTP	0x0	Controls the entry delay to battery isolation												
				Value	Description											
				0x0 (POR)	No delay											
				0x1	500 ms											
				0x2	1 s											
				0x3	10 s											
BAT_ISO_GPI	[3]	RW OTP	0x0	Activates the GPIO control for the BAT_ISO_LONG. The GPIO has to be configured as an GPI for the control to work.												
BAT_ISO_FULL	[2]	RW OTP	0x1	Writing '1' to this bit will enable the charger to disconnect the battery after the charging cycle reaches the full state. This bit does not automatically reset.												
BAT_ISO_SHORT	[1]	RW	0x0	Writing '1' to this bit will cause a soft reset of all register values and the battery disconnects after a 20 ms delay. The battery is reconnected automatically after a 750 ms delay. The bit is automatically reset and cannot be cleared manually.												
BAT_ISO_LONG	[0]	RW	0x0	Writing '1' to this bit will cause a soft reset of all register values and the battery disconnects after a 20 ms delay. Reconnecting the battery will require an external event (nONKEY or VIN). The bit is automatically reset and cannot be cleared manually.												

13.6 Junction Temperature

13.6.1 Register TJUNC_CTRL_A

Address	Name	POR value	Junction Temperature Control Register A																
7	6	5	4	3	2	1	0												
Reserved	Reserved	Reserved	Reserved	Reserved	TJUNC_REG	TJUNC_WARN<1:0>													
Field name	Bits	Type	POR	Description															
TJUNC_REG	[2]	RW OTP	0x0	Enables the automatic temperature regulation.															
TJUNC_WARN	[1:0]	RW OTP	0x0	Threshold for a junction temperature warning.															
				<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0 (POR)</td><td>70°C</td></tr> <tr> <td>0x1</td><td>90°C</td></tr> <tr> <td>0x2</td><td>110°C</td></tr> <tr> <td>0x3</td><td>125°C</td></tr> </tbody> </table>						Value	Description	0x0 (POR)	70°C	0x1	90°C	0x2	110°C	0x3	125°C
Value	Description																		
0x0 (POR)	70°C																		
0x1	90°C																		
0x2	110°C																		
0x3	125°C																		

13.7 ADC

13.7.1 Register ADC_CTRL_A

Address	Name	POR value	ADC Control Register										
0x2B	ADC_CTRL_A	0x00	7	6	5	4	3	2	1	0			
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ADC_CNVRT				
Field name	Bits	Type	POR	Description									
ADC_CNVRT	[0]	RW	0x0	Triggers the ADC measurement. The enable is triggered on a write of 1 to this bit, and will always read back 0. When the measurement is done (E_ADC_DONE) the results can be read from ADC_RES_*									

13.7.2 Register ADC_RES_0

Address	Name	POR value	ADC Channel 0 Result Register								
0x2C	ADC_RES_0	0x00	7	6	5	4	3	2	1	0	
ADC_RES_VIN<7:0>											
Field name	Bits	Type	POR	Description							
ADC_RES_VIN	[7:0]	RO	0x00	Result of the previous ADC measurement for VIN (Channel 0). 1 LSB = 50mV							

13.7.3 Register ADC_RES_1

Address	Name	POR value	ADC Channel 1 Result Register							

0x2D		ADC_RES_1		0x00								
7	6	5	4	3	2	1	0					
ADC_RES_VBAT<7:0>												
Field name	Bits	Type	POR				Description					
ADC_RES_VBAT	[7:0]	RO	0x00	Result of the previous ADC measurement for VBAT (Channel 1). 1 LSB = 20mV								

13.7.4 Register ADC_RES_2

Address	Name		POR value	ADC Channel 2 Result Register									
0x2E	ADC_RES_2		0x00										
7	6	5	4	3	2	1	0						
ADC_RES_IIN<7:0>													
Field name	Bits	Type	POR				Description						
ADC_RES_IIN	[7:0]	RO	0x00	Result of the previous ADC measurement for IIN (Channel 2). 1 LSB = 25mA (OTG current is positive)									

13.7.5 Register ADC_RES_3

Address	Name		POR value	ADC Channel 3 Result Register									
0x2F	ADC_RES_3		0x00										
7	6	5	4	3	2	1	0						
ADC_RES_IBAT<7:0>													
Field name	Bits	Type	POR				Description						
ADC_RES_IBAT	[7:0]	RO	0x00	Result of the previous ADC measurement for IBAT (Channel 3). 1 LSB = 25mA									

13.7.6 Register ADC_RES_4

Address	Name	POR value	ADC Channel 4 Result Register							
0x30	ADC_RES_4	0x00	ADC_RES_TJUNC<7:0>							
7	6	5	4	3	2	1	0			
ADC_RES_TJUNC										
Field name	Bits	Type	POR	Description						
ADC_RES_TJUNC	[7:0]	RO	0x00	Result of the previous ADC measurement for TJUNC (Channel 4). 1 LSB = 1C (unsigned)						

13.8 I/O

13.8.1 Register GPIO_CONF_B

Address	Name	POR value	GPIO Configuration Register B							
0x33	GPIO_CONF_B	0x03	GPIO2_OUT							
7	6	5	4	3	2	1	0			
Reserved	Reserved	Reserved		GPIO2_OUT	GPIO2_INT_EDGE	GPIO2_PIN<1:0>				
Field name	Bits	Type	POR	Description						

GPIO2 Output Value (When configured as GPO)			
Value			Description
0x0 (POR)			GPO: Output is Driven Low (0)
0x1			GPO: Output is High Impedance (1)
GPI2 Interrupt Edge Select (When configured as GPI)			
Value			Description
0x0 (POR)			GPI: Interrupt on Rising Edge
0x1			GPI: Interrupt on Falling Edge
GPIO2 Function			
Value			Description
0x0			BATT_GOOD (output)
0x1			GPI
0x2			GPO (open drain)
0x3 (POR)			ULP_EN_N (input)

13.8.2 Register TWI_CTRL_A

Address	Name	POR value	Two-Wire Interface Control Register A							
0x34	TWI_CTRL_A	0x98								
7	6	5	4	3	2	1	0	TWI_ADDR<6:0>		
										Reserved
Field name	Bits	Type	POR	Description						

TWI_ADDR	[7:1]	RW OTP	0x4C	Two-Wire Interface Slave Address	
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13.8.3 Register TWI_CTRL_B

Address	Name	POR value	Two-Wire Interface Control Register B																
0x35	TWI_CTRL_B	0x32	7	6	5	4	3	2	1	0									
PP_E N	SDA_EXTRA_THOLD_DE LAY	SCL_DEGLITCH_HSPE ED	SCL_DEGLITCH_ EN	TWI_WR_MO DE	SDA_DEGLITCH_HSP EED	SDA_DEGLITCH_ EN	TWI_T O												
Field name																			
PP_EN	[7]	RW OTP	0x0	Configurable IO pads are in push-pull mode (1) or open-drain mode (0). Effects all pins which have configurability options.															
SDA_EXTRA_THOLD_DELAY	[6]	RW OTP	0x0	Enable an additional filter for extra delay on SDA line. Filter is RC based (typical 70ns delay).															
SCL_DEGLITCH_HSPEED	[5]	RW OTP	0x1	Select the fast RC time															
				Value	Description														
				0x0	Slow RC time selected (typical 70ns delay)														
				0x1 (POR)	Fast RC time selected (typical 20ns delay)														
SCL_DEGLITCH_EN	[4]	RW OTP	0x1	Enable the deglitch RC filter on SCL															
TWI_WR_MODE	[3]	RW OTP	0x0	Two-Wire Interface write mode behavior.															
				Value	Description														
				0x0 (POR)	Page write mode (write data to consecutive addresses)														

			0x1	Repeated write mode (write data to arbitrary addresses using address-data pairs)		
SDA_DEGLITCH_HSPEED	[2]	RW OTP	0x0	Select the fast RC time		
				<table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>Slow RC time selected (typical 70ns delay)</td> </tr> <tr> <td>0x1</td> <td>Fast RC time selected (typical 20ns delay)</td> </tr> </tbody> </table>	Value	Description
Value	Description					
0x0 (POR)	Slow RC time selected (typical 70ns delay)					
0x1	Fast RC time selected (typical 20ns delay)					
Enable the deglitch RC filter on SDA						
TWI_TO	[0]	RW OTP	0x0	Enable 35 ms timeout for the Two-Wire Interface.		

13.9 Safety Timer

13.9.1 Register CHG_TIMER_CTRL_A

Address	Name	POR value	Safety Timer Control Register A							
0x36	CHG_TIMER_CTRL_A	0x80								
7	6	5	4	3	2	1	0			
CHG_TIMER_EN	Reserved		TIMEOUT_PRE<1:0>	Reserved		TIMEOUT_CCCV<2:0>				
Field name	Bits	Type	POR	Description						
CHG_TIMER_EN	[7]	RW OTP	0x1	Enables the precharge/CCCV timer.						
TIMEOUT_PRE	[5:4]	RW OTP	0x0	Pre-charge timeout.						
Value	Description									

				0x0 (POR)	15 min
				0x1	30 min
				0x2	45 min
				0x3	60 min
Constant Current/Constant Voltage charging timeout.					
Value	Description				
0x0 (POR)	2 h				
0x1	4 h				
0x2	6 h				
0x3	8 h				
0x4	10 h				
0x5	12 h				
0x6	14 h				
0x7	18 h				

13.9.2 Register CHG_TIMER_CTRL_B

Address	Name	POR value	Safety Timer Control Register B									
0x37	CHG_TIMER_CTRL_B	0xFF										
7	6	5	4	3	2	1	0	TIMER_LOAD<7:0>				
Field name	Bits	Type	POR	Description								

TIMER_LOAD	[7:0]	RW OTP	0xff	Watchdog timer pre-load and re-load. Writing the register when the charger is not enabled sets the pre-load value. The pre-load value is automatically loaded in to TIMER_COUNT the next time the charger starts. Writing the register during charging loads the written value in to TIMER_COUNT.
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13.9.3 Register CHG_TIMER_CTRL_C

Address	Name	POR value	Safety Timer Count Register												
0x38	CHG_TIMER_CTRL_C	0x00													
7	6	5	4	3	2	1	0	TIMER_COUNT<7:0>							
Field name	Bits	Type	POR	Description											
TIMER_COUNT	[7:0]	RO	0x00	Countdown value of the watchdog timer. Decremented at 1s intervals when charging is enabled. Reading the register gives the current timer value. Writing the register has no effect.											

13.10 Configuration

13.10.1 Register CONF_A

Address	Name	POR value	Configuration Register A								
0x40	CONF_A	0x0F									
7	6	5	4	3	2	1	0				
Field name	Bits	Type	POR	Description							
ULP_EN	ULP_WAKEUP_SRC_SEL<1:0>			BAT_DET_CTRL	BAT_DET_SRC<1:0>			WD_EN	ONKEY_DET_EN		

				Enable Ultra-Low-Power Mode (Field valid only when GPIO2_PIN is NOT configured for ULP_EN_N)										
				<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0 (POR)</td><td>Device's lowest power is IDLE state.</td></tr> <tr> <td>0x1</td><td>Device's lowest power is ULP state. ULP may only be entered from IDLE state, and only wakes on I2C, VIN2BAT, and nONKEY detection. All monitoring is disabled, and shared resources to display & haptics sub-ip's are disabled. I2C can not handle back to back writes.</td></tr> </tbody> </table>	Value	Description	0x0 (POR)	Device's lowest power is IDLE state.	0x1	Device's lowest power is ULP state. ULP may only be entered from IDLE state, and only wakes on I2C, VIN2BAT, and nONKEY detection. All monitoring is disabled, and shared resources to display & haptics sub-ip's are disabled. I2C can not handle back to back writes.				
Value	Description													
0x0 (POR)	Device's lowest power is IDLE state.													
0x1	Device's lowest power is ULP state. ULP may only be entered from IDLE state, and only wakes on I2C, VIN2BAT, and nONKEY detection. All monitoring is disabled, and shared resources to display & haptics sub-ip's are disabled. I2C can not handle back to back writes.													
ULP_EN	[7]	RW OTP	0x0	<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0 (POR)</td><td>Allows the ULP wakeup to come from a selected source</td></tr> <tr> <td>0x1</td><td>GPIO2.ULP_EN_N, VBUS, VSYS_POR, VSYS_UV, VDDIO_POR</td></tr> <tr> <td>0x2</td><td>GPIO2.ULP_EN_N, VBUS, SCL, VSYS_POR, VSYS_UV, VDDIO_POR</td></tr> <tr> <td>0x3</td><td>VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR</td></tr> </tbody> </table>	Value	Description	0x0 (POR)	Allows the ULP wakeup to come from a selected source	0x1	GPIO2.ULP_EN_N, VBUS, VSYS_POR, VSYS_UV, VDDIO_POR	0x2	GPIO2.ULP_EN_N, VBUS, SCL, VSYS_POR, VSYS_UV, VDDIO_POR	0x3	VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR
Value	Description													
0x0 (POR)	Allows the ULP wakeup to come from a selected source													
0x1	GPIO2.ULP_EN_N, VBUS, VSYS_POR, VSYS_UV, VDDIO_POR													
0x2	GPIO2.ULP_EN_N, VBUS, SCL, VSYS_POR, VSYS_UV, VDDIO_POR													
0x3	VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR													
ULP_WAKEUP_SRC_SEL	[6:5]	RW OTP	0x0	<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0 (POR)</td><td>GPIO2.ULP_EN_N, VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR</td></tr> <tr> <td>0x1</td><td>GPIO2.ULP_EN_N, VBUS, SCL, VSYS_POR, VSYS_UV, VDDIO_POR</td></tr> <tr> <td>0x2</td><td>VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR</td></tr> <tr> <td>0x3</td><td>GPIO2.ULP_EN_N, VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR</td></tr> </tbody> </table>	Value	Description	0x0 (POR)	GPIO2.ULP_EN_N, VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR	0x1	GPIO2.ULP_EN_N, VBUS, SCL, VSYS_POR, VSYS_UV, VDDIO_POR	0x2	VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR	0x3	GPIO2.ULP_EN_N, VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR
Value	Description													
0x0 (POR)	GPIO2.ULP_EN_N, VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR													
0x1	GPIO2.ULP_EN_N, VBUS, SCL, VSYS_POR, VSYS_UV, VDDIO_POR													
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0x3	GPIO2.ULP_EN_N, VBUS, SCL, NONKEY, TJUNC_CRIT, TJUNC_POR, DISPLAY_CLK_REQ, VSYS_POR, VSYS_UV, VDDIO_POR													
BAT_DET_CTRL	[4]	RW OTP	0x0	Controls for the battery detection in conjunction with BAT_DET_SRC.										
BAT_DET_SRC	[3:2]	RW OTP	0x3	<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td>BAT_DET_CTRL</td></tr> <tr> <td>0x1</td><td>BAT_DET_CTRL OR VBAT</td></tr> <tr> <td>0x2</td><td>Reserved</td></tr> <tr> <td>0x3 (POR)</td><td>Reserved</td></tr> </tbody> </table>	Value	Description	0x0	BAT_DET_CTRL	0x1	BAT_DET_CTRL OR VBAT	0x2	Reserved	0x3 (POR)	Reserved
Value	Description													
0x0	BAT_DET_CTRL													
0x1	BAT_DET_CTRL OR VBAT													
0x2	Reserved													
0x3 (POR)	Reserved													
WD_EN	[1]	RW OTP	0x1	Enables the watchdog timer.										

ONKEY_DET_EN	[0]	RW OTP	0x1	Enables the detection of long key presses.
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13.10.2 Register CONF_B

Address	Name	POR value	Configuration Register A										
7	6	5	4	3	2	1	0						
0x41	CONF_B	0x00	SPSP_TUNE<4:0>										
Field name	Bits	Type	POR	Description									
IDLE_LP_MODE_DIS	[7]	RW OTP	0x0	Disables the low-power IDLE mode.									
IDLE_LP_MODE_DIS	[7]	RW OTP	0x0	Value	Description								
				0x0 (POR)	Device is in low-power mode when in IDLE.								
SPSP_ENABLE	[6]	RW OTP	0x0	Enable spread spectrum of the DC-DC converter clock.									
SPSP_TUNE_ENABLE	[5]	RW OTP	0x0	Enable to adjust the System Clock using SPSP_TUNE setting									
SPSP_TUNE	[4:0]	RW OTP	0x0	System Clock Frequency adjustment									
				Value	Description								
				0x00	no adjustment								
				0x01	1% decrease								
				0x02	2% decrease								
				0x03	3% decrease								

0x04	4% decrease
0x05	5% decrease
0x06	6% decrease
0x07	7% decrease
0x08	8% decrease
0x09	9% decrease
0x0A	10% decrease
0x0B	reserved
0x0C	reserved
0x0D	reserved
0x0E	reserved
0x0F	reserved
0x10	no adjustment
0x11	1% increase
0x12	2% increase
0x13	3% increase
0x14	4% increase
0x15	5% increase
0x16	6% increase
0x17	7% increase
0x18	8% increase
0x19	9% increase
0x1A	10% increase
0x1B	reserved
0x1C	reserved
0x1D	reserved

				0x1E	reserved		
				0x1F	reserved		

14 Display, Core Buck and Flash Driver Register map

VIRTUAL ADDRESSES									
Status registers (virtual)									
Register	Ad dr	7	6	5	4	3	2	1	0
STATUS_A (COREBUCK_STA TUS)	0x 00 00	Reserved	Reserved	VSYS_UV_OT_V REF_FLT	OVCURR1	Reserved	Reserved	Reserved	PWRGOOD1
STATUS_B (FLASH_STATUS)	0x 00 01	VCENT_DRO P	TARGET_EX CEED_MAX	FAULT_CLEAR_ EN	OT	CH2_SC	CH2_OC	CH1_SC	CH1_OC
STATUS_C (SYSCTRL_STAT US)	0x 00 02	Reserved	Reserved	Reserved	SYS_WDT_TI MEOUT	VDDIO_FLT	Reserved	VSYS_UV_OT_ VREF_FLT	Reserved
STATUS_D (DISPLAY_STATU S_A)	0x 00 03	Reserved	Reserved	CP_UVP	CP_OVP	DLDO_SC	BOOST_UVP	BOOST_OCP	BOOST_OVP
STATUS_E (WLED_STATUS)	0x 00 04	Reserved	Reserved	Reserved	Reserved	Reserved	WLED_UV	WLED_OV	WLED_OC
Event registers (virtual)									
Register	Ad dr	7	6	5	4	3	2	1	0
EVENT_A (COREBUCK_EVE NT)	0x 00 10	Reserved	Reserved	EVT_VSYS_UV_ OT_VREF_FLT	EVT_OVCUR R1	Reserved	Reserved	Reserved	EVT_PWRGOO D1
EVENT_B (FLASH_EVENT)	0x 00 11	EVT_VCEN T_DROP	EVT_TARGE T_EXCEED_ MAX	EVT_FAULT_CL EAR_EN	EVT_OT	EVT_CH2_S C	EVT_CH2_OC	EVT_CH1_SC	EVT_CH1_OC

EVENT_C (SYSCTRL_EVENT)	0x0012	Reserved	Reserved	Reserved	EVT_SYS_WDT	EVT_VDDIO_FLT	EVT_CHCR	EVT_VSYS_UV_OT_VREF_FLT	Reserved
EVENT_D (DISPLAY_EVENT_A)	0x0013	Reserved	Reserved	EVT_CP_UVP	EVT_CP_OV_P	EVT_DLDO_SC	EVT_BOOST_UVP	EVT_BOOST_OCP	EVT_BOOST_OVP
EVENT_E (WLED_EVENT)	0x0014	Reserved	Reserved	Reserved	Reserved	Reserved	EVT_WLED_UV	EVT_WLED_OV	EVT_WLED_OC
IRQ mask (virtual)									
Register	Addr	7	6	5	4	3	2	1	0
IRQ_MASK_A (COREBUCK_IRQ_MASK)	0x0020	Reserved	Reserved	M_VSYS_UV_OT_VREF_FLT	M_OVCURR1	Reserved	Reserved	Reserved	M_PWRGOOD1
IRQ_MASK_B (FLASH_IRQ_MASK)	0x0021	M_VCENT_DROP	M_TARGET_EXCEED_MAX	M_FAULT_CLEA_R_EN	M_OT	M_CH2_SC	M_CH2_OC	M_CH1_SC	M_CH1_OC
IRQ_MASK_C (SYSCTRL_IRQ_MASK)	0x0022	Reserved	Reserved	Reserved	M_SYS_WDT	M_VDDIO_FLT	M_CHCR	M_VSYS_UV_OT_VREF_FLT	Reserved
IRQ_MASK_D (DISPLAY_IRQ_MASK_A)	0x0023	Reserved	Reserved	M_CP_UVP	M_CP_OVP	M_DLDO_SC	M_BOOST_UVP	M_BOOST_OC_P	M_BOOST_OV_P
IRQ_MASK_E (WLED_IRQ_MASK)	0x0024	Reserved	Reserved	Reserved	Reserved	Reserved	M_WLED_UV	M_WLED_OV	M_WLED_OC
System (virtual)									
Register	Addr	7	6	5	4	3	2	1	0

VSYS_SYSCTRL_CHIP_ID (SYSCTRL_CHIP_ID)	0x0030	TRC<3:0>				MRC<3:0>			
VSYS_COREBUC_K_BUCK1_0 (COREBUCK_BUCK1_0)	0x0031	Reserved	CH1_A_VOUT<6:0>						
VSYS_COREBUC_K_BUCK1_1 (COREBUCK_BUCK1_1)	0x0032	Reserved	CH1_SLEW_VD<2:0>			Reserved	CH1_SLEW_VU<2:0>		
VSYS_COREBUC_K_BUCK1_2 (COREBUCK_BUCK1_2)	0x0033	Reserved	CH1_SLEW_PD<2:0>			CH1_SLEW_PU<2:0>			CH1_PD_DIS
VSYS_COREBUC_K_BUCK1_3 (COREBUCK_BUCK1_3)	0x0034	Reserved	OC1_MASK	PG1_MASK<1:0>		CH1_ILIM<3:0>			
VSYS_COREBUC_K_BUCK1_4 (COREBUCK_BUCK1_4)	0x0035	Reserved	CH1_VMAX<6:0>						
VSYS_COREBUC_K_BUCK1_5 (COREBUCK_BUCK1_5)	0x0036	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CH1_EN
VSYS_COREBUC_K_BUCK1_6	0x0037	Reserved	CH1_B_VOUT<6:0>						

(COREBUCK_BU CK1_6)														
VSYS_COREBUC K_BUCK1_7 (COREBUCK_BU CK1_7)	0x 00 38	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CH1_A_CMD<1:0>					
VSYS_FLASH_DR IVER_ACTIVE (FLASH_DRIVER_ ACTIVE)	0x 00 39	LED2_PIN_S EL_DRIVER_ EN	LED1_PIN_S EL_DRIVER_ EN	LED2_DRIVER_ EN	LED1_DRIVE R_EN	Reserved	MODE	LED2_EN	LED1_EN					
VSYS_FLASH_DR IVER_STATUS (FLASH_DRIVER_ STATUS)	0x 00 3A	Reserved	Reserved	Reserved	DRIVER_VIN _IS_PG	Reserved	Reserved	DRIVER_IS_ACTIVE<1:0>						
VSYS_FLASH_FD _CONFIG1 (FLASH_FD_CON FIG1)	0x 00 3B	BRIGHT_WIDTH_TORCH<2:0>			BRIGHT_WIDTH_FLASH<2:0>			WARMUP_TIME_SEL<1:0>						
VSYS_FLASH_FD _CONFIG2 (FLASH_FD_CON FIG2)	0x 00 3C	DEG_PROTECT<1:0>		RAMPDOWN_PROTECT<2:0>			RAMPDOWN_DISABLE<2:0>							
VSYS_FLASH_FD _CONFIG3 (FLASH_FD_CON FIG3)	0x 00 3D	Reserved	Reserved	DISABLE_FLAS H_TIMEOUT	FD_EN_PRE C	FLASH_TIMEOUT<3:0>								
VSYS_FLASH_FD _CONFIG4 (FLASH_FD_CON FIG4)	0x 00 3E	TRANSEL_TORCH<3:0>				TRANSEL_FLASH<3:0>								

VSYS_FLASH_FD_CONFIG5 (FLASH_FD_CONFIG5)	0x003F	Reserved	Reserved	Reserved	TORCH_TARGET_CH1<4:0>				
VSYS_FLASH_FD_CONFIG6 (FLASH_FD_CONFIG6)	0x0040	Reserved	Reserved	Reserved	FLASH_TARGET_CH1<4:0>				
VSYS_FLASH_FD_CONFIG7 (FLASH_FD_CONFIG7)	0x0041	Reserved	Reserved	Reserved	TORCH_TARGET_CH2<4:0>				
VSYS_FLASH_FD_CONFIG8 (FLASH_FD_CONFIG8)	0x0042	Reserved	Reserved	Reserved	FLASH_TARGET_CH2<4:0>				
VSYS_FLASH_FD_CONFIG9 (FLASH_FD_CONFIG9)	0x0043	Reserved	Reserved	TUNE_CH2<2:0>			TUNE_CH1<2:0>		
VSYS_FLASH_FD_CONFIG10 (FLASH_FD_CONFIG10)	0x0044	PREC_DELAY<1:0>		CP_BIAS_DELAY<1:0>		CP_DISCHG_DELAY<1:0>		CP_CK_DELAY<1:0>	
VSYS_FLASH_FD_FAULT_CONFIG (FLASH_FD_FAULT_CONFIG)	0x0045	TORCH_TARGET_REDUCE<1:0>		E_AUTO_REDUCE_TORCH_CURRENT	E_OT_AUTO_SHUTDOWN	E_CH2_SC_AUTO_SHUTDOWN	E_CH2_OC_AUTO_SHUTDOWN	E_CH1_SC_AUTO_SHUTDOWN	E_CH1_OC_AUTO_SHUTDOWN
VSYS_SYSCTRL_DISPLAY_ACTIVE	0x0046	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WLED_EN	DISPLAY_EN

(SYSCTRL_DISPLAY_ACTIVE)									
VSYS_SYSCTRL_DISPLAY_STATUS (SYSCTRL_DISPLAY_STATUS)	0x0047	Reserved	Reserved	WLED_IS_PG	DISPLAY_IS_PG	Reserved	Reserved	WLED_IS_ACTIVE	DISPLAY_IS_ACTIVE
VSYS_DISPLAY_CONFIG1 (DISPLAY_CONFIG1)	0x0048	Reserved 0	Reserved 0	Reserved 0	Reserved	DN_VPOS_VNEG	UP_VPOS_VNEG	SEQ_DN_SIMULTANOUS	SEQ_UP_SIMULTANOUS
VSYS_DISPLAY_CONFIG2 (DISPLAY_CONFIG2)	0x0049	UP_DELAY_SRC_SCALE					UP_DELAY_SRC<6:0>		
VSYS_DISPLAY_CONFIG3 (DISPLAY_CONFIG3)	0x004A	UP_DELAY_POS_NEG_SCALE					UP_DELAY_POS_NEG<6:0>		
VSYS_DISPLAY_CONFIG4 (DISPLAY_CONFIG4)	0x004B	DN_DELAY_SRC_SCALE					DN_DELAY_SRC<6:0>		
VSYS_DISPLAY_CONFIG5 (DISPLAY_CONFIG5)	0x004C	DN_DELAY_POS_NEG_SCALE					DN_DELAY_POS_NEG<6:0>		
VSYS_DISPLAY_CONFIG6 (DISPLAY_CONFIG6)	0x004D	MAP_SWITCH_ENABLE	Reserved	CP_MAP<1:0>		LDO_MAP<1:0>		BOOST_MAP<1:0>	

VSYS_DISPLAY_BOOST_VOLTAGE (DISPLAY_BOOST_VOLTAGE)	0x004E	BOOST_VOLTAGE<7:0>						
VSYS_DISPLAY_BOOST_SLEW_RATE (DISPLAY_BOOST_SLEW_RATE)	0x004F	Reserved	Reserved	Reserved	Reserved	Reserved	BOOST_SLEW_RATE<2:0>	
VSYS_DISPLAY_BOOST_CONFIG1 (DISPLAY_BOOST_CONFIG1)	0x0050	Reserved	Reserved 0	Reserved 0	Reserved 0	Reserved	BOOST_SEL_POC_LIMIT<2:0>	
VSYS_DISPLAY_CP_VOLTAGE (DISPLAY_CP_VOLTAGE)	0x0051	CP_VOLTAGE<7:0>						
VSYS_DISPLAY_CP_SLEW_RATE (DISPLAY_CP_SLEW_RATE)	0x0052	Reserved	Reserved	Reserved	Reserved	Reserved	CP_SLEW_RATE<2:0>	
VSYS_DISPLAY_CP_CONFIG8 (DISPLAY_CP_CONFIG8)	0x0053	CP_SEL_RON_MP1_NM<1:0>		Reserved 0	Reserved 0	CP_SEL_RON_MN2_NM<1:0>	Reserved 0	Reserved 0
VSYS_DISPLAY_CP_CONFIG9 (DISPLAY_CP_CONFIG9)	0x0054	Reserved 0	Reserved	CP_OUTN_SHRT_PNGD_N5V	Reserved	CP_DIN_SPARE<3:0>		

VSYS_DISPLAY_LDO_VOLTAGE (DISPLAY_LDO_VOLTAGE)	0x0055	LDO_VOLTAGE<7:0>							
VSYS_DISPLAY_LDO_SLEW_RATE (DISPLAY_LDO_SLEW_RATE)	0x0056	Reserved	Reserved	Reserved	Reserved	Reserved	LDO_SLEW_RATE<2:0>		
VSYS_WLED_CONFIG1 (WLED_CONFIG1)	0x0057	Reserved	Reserved 0	Reserved 0	IDAC_LINEAR	WLED_IDAC_EN	WLED_MODE<2:0>		
VSYS_WLED_CONFIG2 (WLED_CONFIG2)	0x0058	IDAC_TARGET<7:0>							
VSYS_WLED_CONFIG3 (WLED_CONFIG3)	0x0059	PWM_OUT_FREQ_STEP<2:0>			PWM_IN_FREQ_RANGE	IDAC_RAMP_RATE<3:0>			
VSYS_WLED_CONFIG4 (WLED_CONFIG4)	0x005A	PWM_IN_DUTY_THRESHOLD<7:0>							
VSYS_WLED_CONFIG5 (WLED_CONFIG5)	0x005B	PWM_OUT_DUTY<7:0>							
VSYS_WLED_CONFIG6 (WLED_CONFIG6)	0x005C	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	WLED_PANIC_EN		
VSYS_WLED_CONFIG7 (WLED_CONFIG7)	0x005D	Reserved 0	WLED_PANIC_PERIOD<1:0>		WLED_DISCHARGE_SEL<2:0>		PWM_THRESHOLD_PLUS		
							IDAC_RAMP_DIS		

VSYS_WLED_BO OST_CONTROL1 (WLED_BOOST_C ONTROL1)	0x 00 5E	VDAC_SLEW_RATE<2:0>			PANIC_FB_SEL<1:0>	SEL_OVP_TH	SEL_POC_LIMIT<1:0>		
VSYS_WLED_BO OST_CONTROL2 (WLED_BOOST_C ONTROL2)	0x 00 5F	VDAC_SEL<7:0>							
VSYS_SYSCTRL_ SEQ_MODE_CON TROL1 (SYSCTRL_SEQ_ MODE_CONTROL 1)	0x 00 61	Reserved	Reserved	Reserved	COREBUCK_ EN_CTRL_SE LECT	WLED_POW ER_CTRL_S ELECT	DISPLAY_PO WER_CTRL_S ELECT	COREBUCK_R ST_N_CTRL_S ELECT	COREBUCK_P OWER_CTRL_S ELECT
COREBUCK SLAVE									
Event									
Register	Addr	7	6	5	4	3	2	1	0
COREBUCK_EVENT	0x010 0	Reserve d	Reserved	EVT_VSYS_UV_OT_VREF_F LT	EVT_OVCURR 1	Reserve d	Reserve d	Reserve d	EVT_PWRGOOD 1
COREBUCK_STATUS	0x010 1	Reserve d	Reserved	VSYS_UV_OT_VREF_FLT	OVCURR1	Reserve d	Reserve d	Reserve d	PWRGOOD1
COREBUCK_IRQ_MAS K	0x010 2	Reserve d	Reserved	M_VSYS_UV_OT_VREF_FLT	M_OVCURR1	Reserve d	Reserve d	Reserve d	M_PWRGOOD1
Buck1									
Register	Addr	7	6	5	4	3	2	1	0
COREBUCK_BUCK1_0	0x010 3	Reserve d	CH1_A_VOUT<6:0>						
COREBUCK_BUCK1_1	0x010 4	Reserve d	CH1_SLEW_VD<2:0>				Reserve d	CH1_SLEW_VU<2:0>	

COREBUCK_BUCK1_2	0x0105	Reserve d	CH1_SLEW_PD<2:0>				CH1_SLEW_PU<2:0>			CH1_PD_DIS				
COREBUCK_BUCK1_3	0x0106	Reserve d	OC1_MAS K	PG1_MASK<1:0>				CH1_ILIM<3:0>						
COREBUCK_BUCK1_4	0x0107	Reserve d	CH1_VMAX<6:0>											
COREBUCK_BUCK1_5	0x0108	Reserve d	Reserved	Reserved		Reserved	Reserved	Reserve d	Reserve d	Reserve d CH1_EN				
COREBUCK_BUCK1_6	0x0109	Reserve d	CH1_B_VOUT<6:0>											
COREBUCK_BUCK1_7	0x010A	Reserve d	Reserved	Reserved		Reserved	Reserve d	Reserve d	CH1_A_CMD<1:0>					
FLASH DRIVER SLAVE														
Flash Driver Event														
Register	Ad dr	7	6	5	4	3	2	1	0					
FLASH_EVENT	0x0200	EVT_VCEN TDROP	EVT_TARGET_EXCEED_MAX	EVT_FAULT_CLEAR_AR_EN	EVT_OT	EVT_CH2_SC	EVT_CH2_OC	EVT_CH1_SC	EVT_CH1_OC					
FLASH_STATUS	0x0201	VCENT_DRO P	TARGET_EXCEED_MAX	FAULT_CLEAR_E N	OT	CH2_SC	CH2_OC	CH1_SC	CH1_OC					
FLASH_IRQ_MASK	0x0202	M_VCEN DROP	M_TARGET_E XCEED_MAX	M_FAULT_CLEAR _EN	M_OT	M_CH2_SC	M_CH2_OC	M_CH1_SC	M_CH1_OC					
Flash Driver Control														
Register	Ad dr	7	6	5	4	3	2	1	0					

FLASH_DRIVER_ACTIVE	0x0203	LED2_PIN_SEL_DRIVER_EN	LED1_PIN_SEL_DRIVER_EN	LED2_DRIVER_EN	LED1_DRIVER_EN	Reserved	MODE	LED2_EN	LED1_EN											
FLASH_DRIVER_STATUS	0x0204	Reserved	Reserved	Reserved	DRIVER_VIN_IS_PG	Reserved	Reserved	DRIVER_IS_ACTIVE<1:0>												
Flash Driver Configuration																				
Register	Addr	7	6	5	4	3	2	1	0											
FLASH_FD_CONFIG1	0x0205	BRIGHT_WIDTH_TORCH<2:0>			BRIGHT_WIDTH_FLASH<2:0>			WARMUP_TIME_SEL<1:0>												
FLASH_FD_CONFIG2	0x0206	DEG_PROTECT<1:0>		RAMPDOWN_PROTECT<2:0>			RAMPDOWN_DISABLE<2:0>													
FLASH_FD_CONFIG3	0x0207	Reserved	Reserved	DISABLE_FLASH_TIMEOUT	FD_EN_PREC	FLASH_TIMEOUT<3:0>														
FLASH_FD_CONFIG4	0x0208	TRANSEL_TORCH<3:0>				TRANSEL_FLASH<3:0>														
FLASH_FD_CONFIG5	0x0209	Reserved	Reserved	Reserved	TORCH_TARGET_CH1<4:0>															
FLASH_FD_CONFIG6	0x020A	Reserved	Reserved	Reserved	FLASH_TARGET_CH1<4:0>															
FLASH_FD_CONFIG7	0x020B	Reserved	Reserved	Reserved	TORCH_TARGET_CH2<4:0>															

FLASH_FD_CONFIG8	0x020C	Reserved	Reserved	Reserved	FLASH_TARGET_CH2<4:0>							
FLASH_FD_CONFIG9	0x020D	Reserved	Reserved	TUNE_CH2<2:0>			TUNE_CH1<2:0>					
FLASH_FD_CONFIG10	0x020E	PREC_DELAY<1:0>			CP_BIAS_DELAY<1:0>		CP_DISCHG_DELAY<1:0>		CP_CK_DELAY<1:0>			
FLASH_FD_FAULT_CONFIG	0x020F	TORCH_TARGET_REDUCE<1:0>			E_AUTO_REDUCE_TORCH_CURRENT	E_OT_AUTO_SHUTDOWN	E_CH2_SC_AU_TO_SHUTDOWN	E_CH2_OC_AU_TO_SHUTDOWN	E_CH1_SC_AU_TO_SHUTDOWN	E_CH1_OC_AU_TO_SHUTDOWN		
SYS SLAVE												
Event												
Register	Ad dr	7	6	5	4	3	2	1	0			
SYSCTRL_EVENT	0x0300	Reserved	Reserved	Reserved	EVT_SYS_WDT	EVT_VDDIO_FLT	EVT_CHCR	EVT_VSYS_UV_OT_VREF_FLT	Reserved			
SYSCTRL_STATUS	0x0301	Reserved	Reserved	Reserved	SYS_WDT_TIME_OUT	VDDIO_FLT	Reserved	VSYS_UV_OT_VREF_FLT	Reserved			
SYSCTRL_IRQ_MASK	0x0302	Reserved	Reserved	Reserved	M_SYS_WDT	M_VDDIO_FLT	M_CHCR	M_VSYS_UV_OT_VREF_FLT	Reserved			
System Configuration												
Register	Ad dr	7	6	5	4	3	2	1	0			
SYSCTRL_CHIP_ID	0x0303	TRC<3:0>				MRC<3:0>						
Supply Sequence Control												
Register	Ad dr	7	6	5	4	3	2	1	0			

SYSCTRL_DISPLA Y_ACTIVE	0x0 308	Rese rved	Rese rved	Reserv ed	Reserved	Reserved	Reserved	WLED_EN	DISPLAY_EN
SYSCTRL_DISPLA Y_STATUS	0x0 309	Rese rved	Rese rved	WLED_ IS_PG	DISPLAY_IS_PG	Reserved	Reserved	WLED_IS_ACTIVE	DISPLAY_IS_ACTIV E
SYSCTRL_SEQ_M ODE_CONTROL1	0x0 30A	Rese rved	Rese rved	Reserv ed	COREBUCK_EN_ CTRL_SELECT	WLED_POWER_ CTRL_SELECT	DISPLAY_POWER_ CTRL_SELECT	COREBUCK_RST_N_ CTRL_SELECT	COREBUCK_POWE R_CTRL_SELECT
DISPLAY SLAVE									
DISPLAY Event									
Register	Add r	7	6	5	4	3	2	1	0
DISPLAY_EVENT_A	0x03 40	Reserved	Reser ved	EVT_CP_UVP	EVT_CPOVP	EVT_DLDO_SC	EVT_BOOST_UVP	EVT_BOOST_OCP	EVT_BOOST_OVP
DISPLAY_STATUS_A	0x03 41	Reserved	Reser ved	CP_UVP	CP_OVP	DLDO_SC	BOOST_UV P	BOOST_OCP	BOOST_OVP
DISPLAY_IRQ_MAS K_A	0x03 42	Reserved	Reser ved	M_CP_UVP	M_CPOVP	M_DLDO_S C	M_BOOST_UVP	M_BOOST_OCP	M_BOOST_OVP
Display Main-Ctrl Configuration									
Register	Add r	7	6	5	4	3	2	1	0
DISPLAY_CONFIG1	0x03 43	Reserved 0	Reser ved 0	Reserved 0	Reserved	DN_VPOS_VNEG	UP_VPOS_VNEG	SEQ_DN_SIMUL TANOUS	SEQ_UP_SIMUL TANOUS
DISPLAY_CONFIG2	0x03 44	UP_DELAY_SRC_S CALE	UP_DELAY_SRC<6:0>						
DISPLAY_CONFIG3	0x03 45	UP_DELAY_POS_N EG_SCALE	UP_DELAY_POS_NEG<6:0>						
DISPLAY_CONFIG4	0x03 46	DN_DELAY_SRC_S CALE	DN_DELAY_SRC<6:0>						
DISPLAY_CONFIG5	0x03 47	DN_DELAY_POS_N EG_SCALE	DN_DELAY_POS_NEG<6:0>						

DISPLAY_CONFIG6	0x0348	MAP_SWITCH_ENA BLE	Reser ved	CP_MAP<1:0>	LDO_MAP<1:0>	BOOST_MAP<1:0>						
Display Boost												
Register	Add r	7	6	5	4	3	2	1	0			
DISPLAY_BOOST_V OLTAGE	0x0350			BOOST_VOLTAGE<7:0>								
DISPLAY_BOOST_S LEW_RATE	0x0351	Reserved	Reser ved	Reserved	Reserved	Reserved	BOOST_SLEW_RATE<2:0>					
DISPLAY_BOOST_C ONFIG1	0x0352	Reserved	Reser ved 0	Reserved 0	Reserved 0	Reserved	BOOST_SEL_POC_LIMIT<2:0>					
Display Charge Pump												
Register	Add r	7	6	5	4	3	2	1	0			
DISPLAY_CP_VOLT AGE	0x0360			CP_VOLTAGE<7:0>								
DISPLAY_CP_SLEW _RATE	0x0361	Reserved	Reser ved	Reserved	Reserved	Reserved	CP_SLEW_RATE<2:0>					
DISPLAY_CP_CONF IG8	0x0369	CP_SEL_RON_MP1_NM<1 :0>		Reserved 1	Reserved 1	CP_SEL_RON_MN2_N M<1:0>	Reserved 1	Reserved 1				
DISPLAY_CP_CONF IG9	0x036A	Reserved 0	Reser ved	CP_OUTN_SHRT_ PNGD_N5V	Reserved	CP_DIN_SPARE<3:0>						
Display LDO												
Register	Add r	7	6	5	4	3	2	1	0			
DISPLAY_LDO_VOL TAGE	0x0373			LDO_VOLTAGE<7:0>								
DISPLAY_LDO_SLE W_RATE	0x0374	Reserved	Reser ved	Reserved	Reserved	Reserved	LDO_SLEW_RATE<2:0>					
WLED SLAVE												

Event																
Register	Addr	7	6	5	4	3	2	1	0							
WLED_EVENT	0x0380	Reserved	Reserved	Reserved	Reserved	Reserved	EVT_WLED_UV	EVT_WLED_OV	EVT_WLED_OC							
WLED_STATUS	0x0381	Reserved	Reserved	Reserved	Reserved	Reserved	WLED_UV	WLED_OV	WLED_OC							
WLED_IRQ_MASK	0x0382	Reserved	Reserved	Reserved	Reserved	Reserved	M_WLED_UV	M_WLED_OV	M_WLED_OC							
WLED Configuration																
Register	Addr	7	6	5	4	3	2	1	0							
WLED_CONFIG1	0x0383	Reserved	Reserved 1	Reserved 0	IDAC_LINEAR	WLED_IDAC_EN	WLED_MODE<2:0>									
WLED_CONFIG2	0x0384	IDAC_TARGET<7:0>														
WLED_CONFIG3	0x0385	PWM_OUT_FREQ_STEP<2:0>			PWM_IN_FREQ_RANGE	IDAC_RAMP_RATE<3:0>										
WLED_CONFIG4	0x0386	PWM_IN_DUTY_THRESHOLD<7:0>														
WLED_CONFIG5	0x0387	PWM_OUT_DUTY<7:0>														
WLED_CONFIG6	0x0388	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	WLED_PANIC_EN	WLED_PANIC_VTH<1:0>								
WLED_CONFIG7	0x0389	Reserved 0	WLED_PANIC_PERIOD<1:0>			WLED_DISCHARGE_SEL<2:0>		PWM_THRESHOLD_PLUS	IDAC_RAMP_DIS							
WLED_BOOST_CONTROL1	0x0390	VDAC_SLEW_RATE<2:0>			PANIC_FB_SEL<1:0>		SEL_OVP_TH	SEL_POC_LIMIT<1:0>								
WLED_BOOST_CONTROL2	0x0391	VDAC_SEL<7:0>														

14.1 COREBUCK SLAVE

14.1.1 Event

14.1.1.1 Register COREBUCK_EVENT

Address	Register Name	POR Value	Reset Type(s)	Event Register				
7	6	5	4	3	2	1	0	
Reserved	Reserved	EVT_VSYS_UV_OT_VREF_FLT	EVT_OVCURR1	Reserved	Reserved	Reserved	EVT_PWRGOOD1	
Field Name		Bits	Type	POR	Description			
EVT_VSYS_UV_OT_VREF_FLT		[5]	EVENT	0x0	VSYS Fault or Over temperature or Vref not OK on the PMIC			
EVT_OVCURR1		[4]	EVENT	0x0	OVCURR1 caused event			
EVT_PWRGOOD1		[0]	EVENT	0x0	PWRGOOD1 caused event			

14.1.1.2 Register COREBUCK_STATUS

Address	Register Name	POR Value	Reset Type(s)	Status Register				
7	6	5	4	3	2	1	0	
Reserved	Reserved	VSYS_UV_OT_VREF_FLT	OVCURR1	Reserved	Reserved	Reserved	PWRGOOD1	
Field Name		Bits	Type	POR	Description			
VSYS_UV_OT_VREF_FLT		[5]	RO	0x0	VSYS Fault or Over temperature or Vref not OK on the PMIC			
OVCURR1		[4]	RO	0x0	asserted as long as buck1 current limit hitting			
PWRGOOD1		[0]	RO	0x0	asserted as long as the buck1 output voltage is in range			

14.1.1.3 Register COREBUCK_IRQ_MASK

Address	Register Name	POR Value	Reset Type(s)	IRQ Mask Register								
7	6	5	4	3	2	1	0					
Reserved	Reserved	M_VSYS_UV_OT_VREF_FLT	M_OVCURR1	Reserved	Reserved	Reserved	M_PWRGOOD1					
Field Name		Bits	Type	POR	Description							
M_VSYS_UV_OT_VREF_FLT	[5]	IRQ_MASK OTP	0x0	VSYS UV/OT/VREF fault IRQ irqmask								
M_OVCURR1	[4]	IRQ_MASK OTP	0x0	OVCURR1 IRQ mask								
M_PWRGOOD1	[0]	IRQ_MASK OTP	0x0	PWRGOOD1 IRQ mask								

14.1.2 Buck1

14.1.2.1 Register COREBUCK_BUCK1_0

Address	Register Name	POR Value	Reset Type(s)	Target Voltage								
7	6	5	4	3	2	1	0					
Reserved				CH1_A_VOUT<6:0>								
Field Name		Bits	Type	POR	Description							
M_VSYS_UV_OT_VREF_FLT	[5]	IRQ_MASK OTP	0x0	VSYS UV/OT/VREF fault IRQ irqmask								
M_OVCURR1	[4]	IRQ_MASK OTP	0x0	OVCURR1 IRQ mask								
M_PWRGOOD1	[0]	IRQ_MASK OTP	0x0	PWRGOOD1 IRQ mask								

CH1_A_VOUT	[6:0]	RW OTP	0x46	Output voltage setting A: From 0.30V (0000000) to 1.57V (1111111) in steps of 10 mV (default 1.0V)
------------	-------	-----------	------	---

14.1.2.2 Register COREBUCK_BUCK1_1

Address	Register Name			POR Value	Reset Type(s)	Description											
0x0104	COREBUCK_BUCK1_1			0x44	C: PowerOn (HW default) OtpReload RstReload (OTP value)	Channel pull-down, and power-up/down slew rates											
7	6	5	4	3	2	1	0										
Reserved	CH1_SLEW_VD<2:0>			Reserved	CH1_SLEW_VU<2:0>												
Field Name	Bits	Type	POR	Description													
CH1_SLEW_VD	[6:4]	RW OTP	0x4	Voltage slew-rate for DVC ramp-down													
				Value	Description												
				0x0	10mV/8us												
				0x1	10mV/4us												
				0x2	10mV/2us												
				0x3	10mV/us												
				0x4 (POR)	20mV/us												
				0x5	40mV/us												
				0x6	Reserved												
				0x7	Reserved												
CH1_SLEW_VU	[2:0]	RW OTP	0x4	Voltage slew-rate for DVC ramp-up													
				Value	Description												
				0x0	10mV/8us												
				0x1	10mV/4us												

				0x2	10mV/2us
				0x3	10mV/us
				0x4 (POR)	20mV/us
				0x5	40mV/us
				0x6	Reserved
				0x7	Reserved

14.1.2.3 Register COREBUCK_BUCK1_2

Address	Register Name			POR Value	Reset Type(s)								
0x0105	COREBUCK_BUCK1_2			0x48	C: PowerOn (HW default) OtpReload RstReload (OTP value)	DVC slew rates							
	7	6	5	4	3	2	1	0					
Reserved	CH1_SLEW_PD<2:0>				CH1_SLEW_PU<2:0>				CH1_PD_DIS				
Field Name	Bits	Type	POR	Description									
CH1_SLEW_PD	[6:4]	RW OTP	0x4	Voltage slew-rate during power-down									
				Value	Description								
				0x0	10mV/8us								
				0x1	10mV/4us								
				0x2	10mV/2us								
				0x3	10mV/us								
				0x4 (POR)	20mV/us								
				0x5	40mV/us								
				0x6	Reserved								

				0x7	Immidiate power-down
CH1_SLEW_PU	[3:1]	RW OTP	0x4	Voltage slew-rate during startup	
				Value	Description
				0x0	10mV/8us
				0x1	10mV/4us
				0x2	10mV/2us
				0x3	10mV/us
				0x4 (POR)	20mV/us
				0x5	40mV/us
				0x6	Reserved
				0x7	target voltage applied immediately
CH1_PD_DIS	[0]	RW OTP	0x0	Pull down while BUCK is disabled. 0: enable, 1: disable	

14.1.2.4 Register COREBUCK_BUCK1_3

Address	Register Name			POR Value	Reset Type(s)	Current limit settings				
0x0106	COREBUCK_BUCK1_3			0x09	C: PowerOn (HW default) OtpReload RstReload (OTP value)	Current limit settings				
7	6		5		4	3	2	1	0	
Reserved	OC1_MASK			PG1_MASK<1:0>		CH1_ILIM<3:0>				
Field Name	Bits	Type	POR	Description						
OC1_MASK	[6]	RW OTP	0x0	Over-current mask during DVC						

	PG1_MASK	[5:4]	RW OTP	0x0	Power-good mask	
					Value	Description
	CH1_ILIM	[3:0]	RW OTP	0x9	0x0 (POR)	No mask
					0x1	Mask LOW during DVC
					0x2	Mask HIGH during DVC
					0x3	Reserved
					Select OCP threshold	
					Value	Description
					0x0	Reserved
					0x1	5.6 A
					0x2	4.0 A
					0x3	4.4 A
					0x4	4.8 A
					0x5	5.2 A
					0x6	5.6 A
					0x7	6.0 A
					0x8	6.4 A
					0x9 (POR)	6.8 A
					0xA	9.2 A
					0xB	9.6 A
					0xC	10.0 A
					0xD	10.4 A
					0xE	10.8 A
					0xF	Disable

14.1.2.5 Register COREBUCK_BUCK1_4

Address	Register Name	POR Value	Reset Type(s)								
7	6	5	4	3	2	1	0				
Reserved	CH1_VMAX<6:0>										
Field Name	Bits	Type	POR	Description							
CH1_VMAX	[6:0]	RWT OTP	0x7f	VOUT max setting: From 0.30V (0000000) to 1.57V (1111111) in steps of 10 mV							

14.1.2.6 Register COREBUCK_BUCK1_5

Address	Register Name	POR Value	Reset Type(s)								
7	6	5	4	3	2	1	0				
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CH1_EN			
Field Name	Bits	Type	POR	Description							
CH1_EN	[0]	RW	0x0	Channel enable							

14.1.2.7 Register COREBUCK_BUCK1_6

Address	Register Name	POR Value	Reset Type(s)								
7	6	5	4	3	2	1	0				
Reserved	CH1_B_VOUT<6:0>										
Field Name	Bits	Type	POR	Description							

CH1_B_VOUT	[6:0]	RW	0x0	Output voltage setting B: (Output voltage setting A Reset/OTP Value) From 0.30V (0000000) to 1.57V (1111111) in steps of 10 mV (default 1.0V)
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14.1.2.8 Register COREBUCK_BUCK1_7

Address	Register Name			POR Value	Reset Type(s)								
0x010A	COREBUCK_BUCK1_7			0x03	C: PowerOn (HW default) OtpReload RstReload (OTP value)	Misc configuration							
7	6		5	4	3	2	1	0					
Reserved	Reserved		Reserved	Reserved	Reserved	Reserved	CH1_A_CMD<1:0>						
Field Name	Bits	Type	POR	Description									
CH1_A_CMD	[1:0]	RW OTP	0x3	Operation mode selection									
				Value	Description								
				0x0	Force PFM operation								
				0x1	Force PWM operation (full phase)								
				0x2	Force PWM operation (with phase shedding)								
				0x3 (POR)	Auto mode								

14.2 FLASH DRIVER SLAVE

14.2.1 Flash Driver Event

14.2.1.1 Register FLASH_EVENT

Address	Register Name	POR Value	Reset Type(s)	
0x0200	FLASH_EVENT	0x00	A: PowerOn	

7	6	5	4	3	2	1	0
EVT_VCENT_DROP	EVT_TARGET_EXCEED_MAX	EVT_FAULT_CLEAR_EN	EVT_OT	EVT_CH2_SC	EVT_CH2_OC	EVT_CH1_SC	EVT_CH1_OC
Field Name Bits Type POR Description							
EVT_VCENT_DROP	[7]	EVENT	0x0	Vcenter drop during flash/torch			
EVT_TARGET_EXCEED_MAX	[6]	EVENT	0x0	Sum of Flash Target or sum of Torch target exceed Max current limit			
EVT_FAULT_CLEAR_EN	[5]	EVENT	0x0	Force clear torch_en/flash_en due to VSYS < MINVSYs or Reverse Boost Fault or E_LOWBAT			
EVT_OT	[4]	EVENT	0x0	Over Temperature Fault Event			
EVT_CH2_SC	[3]	EVENT	0x0	Channel2 Short Circuit Fault Event			
EVT_CH2_OC	[2]	EVENT	0x0	Channel2 Open Circuit Fault Event			
EVT_CH1_SC	[1]	EVENT	0x0	Channel1 Short Circuit Fault Event			
EVT_CH1_OC	[0]	EVENT	0x0	Channel1 Open Circuit Fault Event			

14.2.1.2 Register FLASH_STATUS

Address	Register Name	POR Value		Reset Type(s)				
0x0201	FLASH_STATUS	0x00		D: PowerOn M fsm Error Rst Reload				
7	6	5	4	3	2	1	0	
VCENT_DROP	TARGET_EXCEED_MAX	FAULT_CLEAR_EN	OT	CH2_SC	CH2_OC	CH1_SC	CH1_OC	
Field Name Bits Type POR Description								
VCENT_DROP	[7]	RO	0x0	Vcenter drop status				
				Value	Description			
				0x0 (POR)	Vcenter Ready			
TARGET_EXCEED_MAX	[6]	RO	0x0	Sum of target exceed MAX limit				
				Value	Description			
				0x1	Vcenter Not Ready			

				0x0 (POR)	normal
				0x1	The target value is exceed limitation
				Clear torch_en/flash_en Status	
				Value	Description
FAULT_CLEAR_EN	[5]	RO	0x0	0x0 (POR)	normal
				0x1	fault_clear_en assert
				OT Fault Status	
OT	[4]	RO	0x0	Value	Description
				0x0 (POR)	normal
				0x1	Over Temperature Fault Occur
				Channel2 SC Fault Status	
CH2_SC	[3]	RO	0x0	Value	Description
				0x0 (POR)	normal
				0x1	Channel2 Short Circuit Fault Occur
				Channel2 OC Fault Status	
CH2_OC	[2]	RO	0x0	Value	Description
				0x0 (POR)	normal
				0x1	Channel2 Open Circuit Fault Occur
				Channel1 SC Fault Status	
CH1_SC	[1]	RO	0x0	Value	Description
				0x0 (POR)	normal
				0x1	Channel1 Short Circuit Fault Occur

				Channel1 OC Fault Status	
				Value	Description
CH1_OC				0x0 (POR)	normal
				0x1	Channel1 Open Circuit Fault Occur

14.2.1.3 Register FLASH_IRQ_MASK

Address	Register Name	POR Value	Reset Type(s)						
0x0202	FLASH_IRQ_MASK	0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)						
7	6	5	4	3	2	1	0		
M_VCENT_DROP	M_TARGET_EXCEED_MAX	M_FAULT_CLEAR_EN	M_OT	M_CH2_SC	M_CH2_OC	M_CH1_SC	M_CH1_OC		
Field Name	Bits	Type	POR	Description					
M_VCENT_DROP	[7]	IRQ_MASK OTP	0x0	irqmask for EVT_VCENT_DROP					
M_TARGET_EXCEED_MAX	[6]	IRQ_MASK OTP	0x0	irqmask for EVT_TARGET_EXCEED_MAX					
M_FAULT_CLEAR_EN	[5]	IRQ_MASK OTP	0x0	irqmask for EVT_FAULT_CLEAR_EN					
M_OT	[4]	IRQ_MASK OTP	0x0	irqmask for E_OT					
M_CH2_SC	[3]	IRQ_MASK OTP	0x0	irqmask for E_CH2_SC					
M_CH2_OC	[2]	IRQ_MASK OTP	0x0	irqmask for E_CH2_OC					

M_CH1_SC	[1]	IRQ_MASK OTP	0x0	irqmask for E_CH1_SC	
M_CH1_OC	[0]	IRQ_MASK OTP	0x0	irqmask for E_CH1_OC	

14.2.2 Flash Driver Control

14.2.2.1 Register FLASH_DRIVER_ACTIVE

Address	Register Name	POR Value	Reset Type(s)	Flash Driver Active Control Register																	
0x0203	FLASH_DRIVER_ACTIVE	0x00	B: PowerOn MfsmError A: PowerOn																		
				7	6	5	4	3	2	1	0										
LED2_PIN_SEL_DRIVER_EN LED1_PIN_SEL_DRIVER_EN LED2_DRIVER_EN LED1_DRIVER_EN Reserved MODE LED2_EN LED1_EN																					
Field Name	Bits	Type	POR	Description																	
LED2_PIN_SEL_DRIVER_EN	[7]	RW	0x0	Enable pin control on LED2 Driver.																	
				Value	Description																
				0x0 (POR)	Disabled																
LED1_PIN_SEL_DRIVER_EN	[6]	RW	0x0	Enable pin control on LED1 Driver.																	
				Value	Description																
				0x0 (POR)	Disabled																
LED2_DRIVER_EN																					
[5] RW 0x0				Driver Enable. Driver will start to ramp the LED2 current when this bit set to 1.																	
				Value	Description																

			0x0 (POR)	Disable						
			0x1	Enable						
LED1_DRIVER_EN	[4]	RW	0x0	Driver Enable. Driver will start to ramp the LED1 current when this bit set to 1.						
				<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0 (POR)</td><td>Disabled</td></tr> <tr> <td>0x1</td><td>Enabled</td></tr> </tbody> </table>	Value	Description	0x0 (POR)	Disabled	0x1	Enabled
Value	Description									
0x0 (POR)	Disabled									
0x1	Enabled									
Operation Mode. Only update when Flash Driver is inactive.										
<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0 (POR)</td><td>Flash Mode</td></tr> <tr> <td>0x1</td><td>Torch Mode</td></tr> </tbody> </table>	Value	Description	0x0 (POR)	Flash Mode	0x1	Torch Mode				
Value	Description									
0x0 (POR)	Flash Mode									
0x1	Torch Mode									
Enable Channel 2, Driver will start requesting charger's Vcenter if any channel is enable.										
LED2_EN	[1]	RW	0x0	<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0 (POR)</td><td>Disabled</td></tr> <tr> <td>0x1</td><td>Enabled</td></tr> </tbody> </table>	Value	Description	0x0 (POR)	Disabled	0x1	Enabled
Value	Description									
0x0 (POR)	Disabled									
0x1	Enabled									
Enable Channel 1, Driver will start requesting charger's Vcenter if any channel is enable.										
<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0 (POR)</td><td>Disabled</td></tr> <tr> <td>0x1</td><td>Enabled</td></tr> </tbody> </table>	Value	Description	0x0 (POR)	Disabled	0x1	Enabled				
Value	Description									
0x0 (POR)	Disabled									
0x1	Enabled									

14.2.2.2 Register FLASH_DRIVER_STATUS

Address	Register Name	POR Value	Reset Type(s)	Flash Driver Status Register

0x0204	FLASH_DRIVER_STATUS			0x00	D: PowerOn M fsmError RstReload					
7	6	5	4	3	2	1	0			
Reserved	Reserved	Reserved	DRIVER_VIN_IS_PG	Reserved	Reserved	Reserved	DRIVER_IS_ACTIVE<1:0>			
Field Name	Bits	Type	POR	Description						
DRIVER_VIN_IS_PG [4]	[4]	RO	0x0	Flash driver power supply (Vcenter) is ready						
				Value	Description					
				0x0 (POR)	Not-PG					
DRIVER_IS_ACTIVE [1:0]	[1:0]	RO	0x0	Flash driver is active.						
				Value	Description					
				0x0 (POR)	Disable					
				0x1	Standby (Vcenter Ready Only)					
				0x2	Torching					
				0x3	Flashing					

14.2.3 Flash Driver Configuration

14.2.3.1 Register FLASH_FD_CONFIG1

Address	Register Name	POR Value	Reset Type(s)	
0x0205	FLASH_FD_CONFIG1	0x32	C: PowerOn (HW default) OtpReload RstReload (OTP value)	

7	6	5	4	3	2	1	0
BRIGHT_WIDTH_TORCH<2:0>				BRIGHT_WIDTH_FLASH<2:0>			
				WARMUP_TIME_SEL<1:0>			
Field Name	Bits	Type	POR	Description			
BRIGHT_WIDTH_TORCH[7:5]	RW OTP	0x1	brightness level code width in torch mode(Ramp Up Speed).				
			Value	Description			
			0x0	0msec			
			0x1 (POR)	0.05msec/target step			
			0x2	1.6msec/target step			
			0x3	3.2msec/target step			
			0x4	4.4msec/target step			
			0x5	12.8msec/target step			
BRIGHT_WIDTH_FLASH[4:2]	RW OTP	0x4	brightness level code width in flash mode(Ramp Up Speed).				
			Value	Description			
			0x0	0usec			
			0x1	1usec/target step			
			0x2	2usec/target step			
			0x3	4usec/target step			
			0x4 (POR)	8usec/target step			
			0x5	16usec/target step			
WARMUP_TIME_SEL	[1:0]	RW OTP	0x2	duration between the rising edge of fd_en_ch1 and fd_led_en_ch1 (as well as fd_en_ch2 and fs_led_en_ch2)			
				Value	Description		

0x0	0usec
0x1	10us
0x2 (POR)	30us
0x3	64us

14.2.3.2 Register FLASH_FD_CONFIG2

Address	Register Name		POR Value	Reset Type(s)									
0x0206	FLASH_FD_CONFIG2		0xA4	C: PowerOn (HW default) OtpReload RstReload (OTP value)									
7	6		5	4	3	2	1	0					
DEG_PROTECT<1:0>			RAMPDOWN_PROTECT<2:0>				RAMPDOWN_DISABLE<2:0>						
Field Name	Bits	Type	POR	Description									
DEG_PROTECT	[7:6]	RW OTP	0x2	Deglitch time for short-circuit, open-circuit and over-temperature protection									
				Value	Description								
				0x0	Debounce for 4us								
				0x1	Debounce for 16us								
				0x2 (POR)	Debounce for 64us								
				0x3	Debounce for 256us								
RAMPDOWN_PROTECT		RW OTP	0x4	Brightness level code width when count down is started during protection in flash/torch mode(Fault Ramp Down Speed).									
				Value	Description								
				0x0	0usec								
				0x1	1usec/target step								

				0x2	2usec/target step
				0x3	4usec/target step
				0x4 (POR)	8usec/target step
				0x5	16usec/target step
				0x6	32usec/target step
				0x7	64usec/target step
RAMPDOWN_DISABLE	[2:0]	RW OTP	0x4	Brightness level code width when count down is started during disable in flash/torch mode(Ramp Down Speed).	
				Value	Description
				0x0	0usec
				0x1	1usec/target step
				0x2	2usec/target step
				0x3	4usec/target step
				0x4 (POR)	8usec/target step
				0x5	16usec/target step
				0x6	32usec/target step
				0x7	64usec/target step

14.2.3.3 Register FLASH_FD_CONFIG3

Address	Register Name	POR Value	Reset Type(s)	
0x0207	FLASH_FD_CONFIG3	0x1A	C: PowerOn (HW default) OtpReload RstReload (OTP value)	
7	6	5	4	3 2 1 0

Reserved	Reserved	DISABLE_FLASH_TIMEOUT	FD_EN_PREC	FLASH_TIMEOUT<3:0>																						
Field Name	Bits	Type	POR	Description																						
DISABLE_FLASH_TIMEOUT	[5]	RW OTP	0x0	Disable Flash Timeout.																						
				<table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>Enable</td> </tr> <tr> <td>0x1</td> <td>Disable</td> </tr> </tbody> </table>	Value	Description	0x0 (POR)	Enable	0x1	Disable																
Value	Description																									
0x0 (POR)	Enable																									
0x1	Disable																									
<table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Disable pre-charge function</td> </tr> <tr> <td>0x1 (POR)</td> <td>Enable pre-charge function</td> </tr> </tbody> </table>	Value	Description	0x0	Disable pre-charge function	0x1 (POR)	Enable pre-charge function																				
Value	Description																									
0x0	Disable pre-charge function																									
0x1 (POR)	Enable pre-charge function																									
FLASH_TIMEOUT	[3:0]	RW OTP	0xA	Duration for Flash. Work only when flash is not in pin control mode and DISABLE_FLASH_TIMEOUT not set.																						
				<table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>10ms</td> </tr> <tr> <td>0x1</td> <td>40ms</td> </tr> <tr> <td>0x2</td> <td>60ms</td> </tr> <tr> <td>0x3</td> <td>80ms</td> </tr> <tr> <td>0x4</td> <td>100ms</td> </tr> <tr> <td>0x5</td> <td>120ms</td> </tr> <tr> <td>0x6</td> <td>140ms</td> </tr> <tr> <td>0x7</td> <td>160ms</td> </tr> <tr> <td>0x8</td> <td>180ms</td> </tr> <tr> <td>0x9</td> <td>200ms</td> </tr> <tr> <td>0xA (POR)</td> <td>300ms</td> </tr> <tr> <td>0xB</td> <td>400ms</td> </tr> </tbody> </table>	Value	Description	0x0	10ms	0x1	40ms	0x2	60ms	0x3	80ms	0x4	100ms	0x5	120ms	0x6	140ms	0x7	160ms	0x8	180ms	0x9	200ms
Value	Description																									
0x0	10ms																									
0x1	40ms																									
0x2	60ms																									
0x3	80ms																									
0x4	100ms																									
0x5	120ms																									
0x6	140ms																									
0x7	160ms																									
0x8	180ms																									
0x9	200ms																									
0xA (POR)	300ms																									
0xB	400ms																									

			0xC	500ms
			0xD	600ms
			0xE	800ms
			0xF	1000ms

14.2.3.4 Register FLASH_FD_CONFIG4

Address	Register Name	POR Value	Reset Type(s)									
7	6	5	4	3	2	1	0					
0x0208	FLASH_FD_CONFIG4	0x22	C: PowerOn (HW default) OtpReload RstReload (OTP value)									
TRANSEL_TORCH<3:0>					TRANSEL_FLASH<3:0>							
Field Name	Bits	Type	POR	Description								
TRANSEL_TORCH	[7:4]	RW OTP	0x2	Transient improvement for torch mode								
TRANSEL_FLASH	[3:0]	RW OTP	0x2	Transient improvement for flash mode								

14.2.3.5 Register FLASH_FD_CONFIG5

Address	Register Name	POR Value	Reset Type(s)					
0x0209	FLASH_FD_CONFIG5	0x00	A: PowerOn					
7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	TORCH_TARGET_CH1<4:0>					
Field Name	Bits	Type	POR	Description				
TORCH_TARGET_CH1	[4:0]	RW	0x0	Torch Mode Brightness Target for channel 1. Max 500mA. CH1+CH2 Max 500mA				
Value			Description					

0x0 (POR)	1mA
0x1	25mA
0x2	50mA
0x3	75mA
0x4	100mA
0x5	125mA
0x6	150mA
0x7	175mA
0x8	200mA
0x9	225mA
0xA	250mA
0xB	275mA
0xC	300mA
0xD	325mA
0xE	350mA
0xF	375mA
0x10	400mA
0x11	425mA
0x12	450mA
0x13	475mA
0x14	500mA

14.2.3.6 Register FLASH_FD_CONFIG6

Address	Register Name	POR Value	Reset Type(s)					
0x020A	FLASH_FD_CONFIG6	0x00	A: PowerOn					
7	6	5	4	3	2	1	0	

Reserved	Reserved		Reserved		FLASH_TARGET_CH1<4:0>			
Field Name	Bits	Type	POR	Description				
FLASH_TARGET_CH1[4:0]	RW	0x0	Flash Mode Brightness Target for channel 1. Max 1A. CH1+CH2 Max 2A	Value				
				Description				
				0x0 (POR)	10mA			
				0x1	50mA			
				0x2	100mA			
				0x3	150mA			
				0x4	200mA			
				0x5	250mA			
				0x6	300mA			
				0x7	350mA			
				0x8	400mA			
				0x9	450mA			
				0xA	500mA			
				0xB	550mA			
				0xC	600mA			
				0xD	650mA			
				0xE	700mA			
				0xF	750mA			
				0x10	800mA			
				0x11	850mA			
				0x12	900mA			
				0x13	950mA			
				0x14	1000mA			
				0x15	1050mA			
				0x16	1100mA			

0x17	1150mA
0x18	1200mA
0x19	1250mA
0x1A	1300mA
0x1B	1350mA
0x1C	1400mA
0x1D	1450mA
0x1E	1500mA

14.2.3.7 Register FLASH_FD_CONFIG7

Address	Register Name		POR Value	Reset Type(s)					
0x020B	FLASH_FD_CONFIG7		0x00	A: PowerOn					
7	6	5	4	3	2	1	0		
Reserved	Reserved		Reserved	TORCH_TARGET_CH2<4:0>					
Field Name	Bits	Type	POR	Description					
TORCH_TARGET_CH2[4:0]	RW	0x0	0x0	Torch Mode Brightness Target for channel 2. Max 500mA. CH1+CH2 Max 500mA					
				Value	Description				
				0x0 (POR)	1mA				
				0x1	25mA				
				0x2	50mA				
				0x3	75mA				
				0x4	100mA				
				0x5	125mA				
				0x6	150mA				
				0x7	175mA				
				0x8	200mA				

				0x9	225mA
				0xA	250mA
				0xB	275mA
				0xC	300mA
				0xD	325mA
				0xE	350mA
				0xF	375mA
				0x10	400mA
				0x11	425mA
				0x12	450mA
				0x13	475mA
				0x14	500mA

14.2.3.8 Register FLASH_FD_CONFIG8

Address	Register Name		POR Value	Reset Type(s)					
0x020C	FLASH_FD_CONFIG8		0x00	A: PowerOn					
7	6	5	4	3	2	1	0		
Reserved	Reserved		Reserved	FLASH_TARGET_CH2<4:0>					
Field Name		Bits	Type	POR	Description				
FLASH_TARGET_CH2[4:0]		RW	0x0	Flash Mode Brightness Target for channel 2. Max 1A. CH1+CH2 Max 2A					
		Value	Description						
		0x0 (POR)	10mA						
		0x1	50mA						
		0x2	100mA						
		0x3	150mA						
		0x4	200mA						

				0x5	250mA
				0x6	300mA
				0x7	350mA
				0x8	400mA
				0x9	450mA
				0xA	500mA
				0xB	550mA
				0xC	600mA
				0xD	650mA
				0xE	700mA
				0xF	750mA
				0x10	800mA
				0x11	850mA
				0x12	900mA
				0x13	950mA
				0x14	1000mA

14.2.3.9 Register FLASH_FD_CONFIG9

Address	Register Name	POR Value	Reset Type(s)					
0x020D	FLASH_FD_CONFIG9	0x24	C: PowerOn (HW default) OtpReload RstReload (OTP value)					
7	6	5	4	3	2	1	0	
Reserved	Reserved	TUNE_CH2<2:0>				TUNE_CH1<2:0>		
Field Name	Bits	Type	POR	Description				

TUNE_CH2	[5:3]	RW OTP	0x4	Tune for the LED full-range current of channel 2														
				<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td>0.25A</td></tr> <tr><td>0x1</td><td>0.5A</td></tr> <tr><td>0x2</td><td>0.75A</td></tr> <tr><td>0x3</td><td>1A</td></tr> <tr><td>0x4 (POR)</td><td>1.25A</td></tr> <tr><td>0x5</td><td>1.5A</td></tr> <tr><td>0x6</td><td>1.75A</td></tr> <tr><td>0x7</td><td>NA</td></tr> </tbody> </table>	Value	Description	0x0	0.25A	0x1	0.5A	0x2	0.75A	0x3	1A	0x4 (POR)	1.25A	0x5	1.5A
Value	Description																	
0x0	0.25A																	
0x1	0.5A																	
0x2	0.75A																	
0x3	1A																	
0x4 (POR)	1.25A																	
0x5	1.5A																	
0x6	1.75A																	
0x7	NA																	
Tune for the LED full-range current of channel 1																		
<table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td>0.25A</td></tr> <tr><td>0x1</td><td>0.5A</td></tr> <tr><td>0x2</td><td>0.75A</td></tr> <tr><td>0x3</td><td>1A</td></tr> <tr><td>0x4 (POR)</td><td>1.25A</td></tr> <tr><td>0x5</td><td>1.5A</td></tr> <tr><td>0x6</td><td>1.75A</td></tr> <tr><td>0x7</td><td>NA</td></tr> </tbody> </table>	Value	Description	0x0	0.25A	0x1	0.5A	0x2	0.75A	0x3	1A	0x4 (POR)	1.25A	0x5	1.5A	0x6	1.75A	0x7	NA
Value	Description																	
0x0	0.25A																	
0x1	0.5A																	
0x2	0.75A																	
0x3	1A																	
0x4 (POR)	1.25A																	
0x5	1.5A																	
0x6	1.75A																	
0x7	NA																	

14.2.3.10 Register FLASH_FD_CONFIG10

Address	Register Name	POR Value	Reset Type(s)	
0x020E	FLASH_FD_CONFIG10	0x55	C: PowerOn (HW default) OtpReload	

				RstReload (OTP value)										
7	6		5	4	3	2	1	0						
PREC_DELAY<1:0>			CP_BIAS_DELAY<1:0>			CP_DISCHG_DELAY<1:0>		CP_CK_DELAY<1:0>						
Field Name	Bits	Type	POR	Description										
PREC_DELAY	[7:6]	RW OTP	0x1	Set the delay time of the pre-charge function										
				Value	Description									
				0x0	4usec									
				0x1 (POR)	8usec									
				0x2	16usec									
				0x3	32usec									
CP_BIAS_DELAY	[5:4]	RW OTP	0x1	Delay time between charge pump and bias core										
				Value	Description									
				0x0	16usec									
				0x1 (POR)	32usec									
				0x2	64usec									
				0x3	128usec									
CP_DISCHG_DELAY	[3:2]	RW OTP	0x1	Set the leading and lagging time between d_clk_in and d_dischg_cs										
				Value	Description									
				0x0	8usec									
				0x1 (POR)	16usec									
				0x2	32usec									
				0x3	64usec									
CP_CK_DELAY		RW OTP	0x1	Set the leading and lagging time between d_en_cp and d_clk_in										
				Value	Description									

0x0	4usec
0x1 (POR)	8usec
0x2	16usec
0x3	32usec

14.2.3.11 Register FLASH_FD_FAULT_CONFIG

Address	Register Name	POR Value	Reset Type(s)																						
7	6	5	4	3	2	1	0																		
0x020F	FLASH_FD_FAULT_CONFIG	0x80	C: PowerOn (HW default) OtpReload RstReload (OTP value)																						
TORCH_TARGET_R EDUCE<1:0>	E_AUTO_REDUCE_TO RCH_CURRENT	E_OT_AUTO_S HUTDOWN	E_CH2_SC_AUTO SHUTDOWN	E_CH2_OC_AUTO SHUTDOWN	E_CH1_SC_AUTO SHUTDOWN	E_CH1_OC_AUTO SHUTDOWN																			
Field Name			Bits	Type	POR	Description																			
TORCH_TARGET_REDUCE			[7:6]	RW OTP	0x2	Torch Mode Brightness Target for each channel when Charger request FD to reduce current																			
						Value	Description																		
						0x0	0mA																		
						0x1	25mA																		
						0x2 (POR)	50mA																		
E_AUTO_REDUCE_TORCH_CURRENT			[5]	RW OTP	0x0	Auto reduce torch current when charger vin_drop or iin_lim																			

E_OT_AUTO_SHUTDOWN	[4]	RW OTP	0x0	Auto-shutdown led when E_OT occurred
E_CH2_SC_AUTO_SHUTDOWN	[3]	RW OTP	0x0	Auto-shutdown led when E_CH2_SC occurred
E_CH2_OC_AUTO_SHUTDOWN	[2]	RW OTP	0x0	Auto-shutdown led when E_CH2_OC occurred
E_CH1_SC_AUTO_SHUTDOWN	[1]	RW OTP	0x0	Auto-shutdown led when E_CH1_SC occurred
E_CH1_OC_AUTO_SHUTDOWN	[0]	RW OTP	0x0	Auto-shutdown led when E_CH1_OC occurred

14.3 SYS SLAVE

14.3.1 Event

14.3.1.1 Register SYSCTRL_EVENT

Address	Register Name	POR Value		Reset Type(s)	Event Register						
0x0300	SYSCTRL_EVENT	0x00		A: PowerOn							
7	6	5	4	3	2	1	0				
Reserved	Reserved	Reserved		EVT_SYS_WDT	EVT_VDDIO_FLT	EVT_CHCR	EVT_VSYS_UV_OT_VREF_FLT	Reserved			
Field Name		Bits	Type	POR	Description						
EVT_SYS_WDT		[4]	EVENT	0x0	System watchdog timeout						
EVT_VDDIO_FLT		[3]	EVENT	0x0	VDDIO Fault						
EVT_CHCR		[2]	EVENT	0x0	Chip to host communication						
EVT_VSYS_UV_OT_VREF_FLT		[1]	EVENT	0x0	VSYS Fault or Over temperature or Vref not OK on the PMIC						

14.3.1.2 Register SYSCTRL_STATUS

Address	Register Name	POR Value		Reset Type(s)	Status Register

0x0301	SYSCTRL_STATUS	0x00	D: PowerOn MfsmError RstReload					
7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	SYS_WDT_TIMEOUT	VDDIO_FLT	Reserved	VSYS_UV_OT_VREF_FLT	Reserved	
Field Name	Bits	Type	POR	Description				
SYS_WDT_TIMEOUT	[4]	RO	0x0	Indicates watchdog timeout				
				Value	Description			
				0x0 (POR)	Normal			
				0x1	Watchdog Timeout			
VDDIO_FLT	[3]	RO	0x0	VDDIO Fault				
				Value	Description			
				0x0 (POR)	Fault			
				0x1	Normal			
VSYS_UV_OT_VREF_FLT	[1]	RO	0x0	VSYS Fault or Over temperature or Vref not OK on the PMIC				
				Value	Description			
				0x0 (POR)	Fault			
				0x1	Normal			

14.3.1.3 Register SYSCTRL_IRQ_MASK

Address	Register Name	POR Value	Reset Type(s)	IRQ Mask Register
0x0302	SYSCTRL_IRQ_MASK	0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)	

7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	M_SYS_WDT	M_VDDIO_FLT	M_CHCR	M_VSYS_UV_OT_VREF_FLT	Reserved	
Field Name		Bits	Type	POR	Description			
M_SYS_WDT		[4]	IRQ_MASK OTP	0x0	System Watch Dog Timer irqmask			
M_VDDIO_FLT		[3]	IRQ_MASK OTP	0x0	VDDIO Fault event irqmask			
M_CHCR		[2]	IRQ_MASK OTP	0x0	CHCR irqmask			
M_VSYS_UV_OT_VREF_FLT		[1]	IRQ_MASK OTP	0x0	VSYS UV/OT/VREF fault event irqmask			

14.3.2 System Configuration

14.3.2.1 Register SYSCTRL_CHIP_ID

Address	Register Name	POR Value		Reset Type(s)							
0x0303	SYSCTRL_CHIP_ID	0x00		C: PowerOn (HW default) OtpReload RstReload (OTP value) D: PowerOn M fsm Error RstReload	Chip ID						
7	6	5	4	3	2	1	0				
TRC<3:0>					MRC<3:0>						
Field Name		Bits	Type	POR	Description						
TRC		[7:4]	RWT OTP	0x0	Read back of OTP Trimming Release Code (TRC) - starts with code 0						

MRC	[3:0]	RO	0x0	Read back of Mask Revision Code (MRC)
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14.3.3 Supply Sequence Control

14.3.3.1 Register SYSCTRL_DISPLAY_ACTIVE

Address	Register Name			POR Value	Reset Type(s)	Power Rail Active Control Register							
0x0308	SYSCTRL_DISPLAY_ACTIVE			0x00	A: PowerOn	7	6	5	4	3	2	1	0
Reserved	Reserved		Reserved	Reserved	Reserved	Reserved	Reserved	WLED_EN	DISPLAY_EN				
Field Name		Bits	Type	POR	Description								
WLED_EN	[1]	RW	0x0	Wled Enable	Value	Description							
				0x0 (POR)	Disabled								
				0x1	Enabled								
DISPLAY_EN	[0]	RW	0x0	Display Enable	Value	Description							
				0x0 (POR)	Disabled								
				0x1	Enabled								

14.3.3.2 Register SYSCTRL_DISPLAY_STATUS

Address	Register Name			POR Value	Reset Type(s)	Power Rail Status Register			
0x0309	SYSCTRL_DISPLAY_STATUS			0x00	D: PowerOn M fsmError RstReload				

7	6	5	4	3	2	1	0
Reserved	Reserved	WLED_IS_PG	DISPLAY_IS_PG	Reserved	Reserved	WLED_IS_ACTIVE	DISPLAY_IS_ACTIVE
Field Name	Bits	Type	POR	Description			
WLED_IS_PG	[5]	RO	0x0	Wled is ready			
				Value	Description		
				0x0 (POR)	Non-PG		
DISPLAY_IS_PG	[4]	RO	0x0	Display power is ready			
				Value	Description		
				0x0 (POR)	Non-PG		
WLED_IS_ACTIVE	[1]	RO	0x0	Wled is active.			
				Value	Description		
				0x0 (POR)	Non-Active		
DISPLAY_IS_ACTIVE	[0]	RO	0x0	Display is active.			
				Value	Description		
				0x0 (POR)	Non-Active		

14.3.3.3 Register SYSCTRL_SEQ_MODE_CONTROL1

Address	Register Name	POR Value	Reset Type(s)	Power Rail Sequence Control Register

0x030A		SYSCTRL_SEQ_MODE_CONTROL1				0x0B	C: PowerOn (HW default) OtpReload RstReload (OTP value)					
7	6	5	4	3	2	1	0					
Reser ved	Reser ved	Reser ved	COREBUCK_EN_CTR L_SELECT	WLED_POWER_CTR L_SELECT	DISPLAY_POWER_CTR L_SELECT	COREBUCK_RST_N_CT RL_SELECT	COREBUCK_POWER_CTR RL_SELECT					
Field Name				Bits	Type	POR	Description					
COREBUCK_EN_CTRL_SELECT				[4]	RW OTP	0x0	COREBUCK_EN GPIO trigger select					
							Value	Description				
							0x0 (POR)	Level Trigger				
WLED_POWER_CTRL_SELECT				[3]	RW OTP	0x1	Power rail control source select. If set to '1' then I2C write to this bit will be no longer valid.					
							Value	Description				
							0x0	From I2C Access				
DISPLAY_POWER_CTRL_SELECT				[2]	RW OTP	0x0	Power rail control source select. If set to '1' then I2C write to this bit will be no longer valid.					
							Value	Description				
							0x0 (POR)	From I2C Access				
COREBUCK_RST_N_CTRL_SELECT				[1]	RW OTP	0x1	Disable the corebuck or not when corebuck_nrst assert.					
							Value	Description				
							0x0	Don't disable buck when pin assert				

				0x1 (POR)	Disable buck when pin asset		
COREBUCK_POWER_CTRL_SELECT	[0]	RW OTP	0x1	Power rail control source select. If set to '1' then I2C write to this bit will be no longer valid.			
Value	Description						
0x0	From I2C Access						
0x1 (POR)	From GPIO						

14.4 DISPLAY SLAVE

14.4.1 DISPLAY Event

14.4.1.1 Register DISPLAY_EVENT_A

Address	Register Name		POR Value	Reset Type(s)					
0x0340	DISPLAY_EVENT_A		0x00	A: PowerOn					
7	6		5	4	3	2	1	0	
Reserved	Reserved		EVT_CP_UVP	EVT_CP_OVP	EVT_DLDO_SC	EVT_BOOST_UVP	EVT_BOOST_OCP	EVT_BOOST_OVP	
Field Name	Bits	Type	POR	Description					
EVT_CP_UVP	[5]	EVENT	0x0	Event caused by CP UVP Fault					
EVT_CP_OVP	[4]	EVENT	0x0	Event caused by CP OVP Fault					
EVT_DLDO_SC	[3]	EVENT	0x0	Event caused by DLDO SC Fault					
EVT_BOOST_UVP	[2]	EVENT	0x0	Event caused by BOOST UVP Fault					
EVT_BOOST_OCP	[1]	EVENT	0x0	Event caused by BOOST OCP Fault					
EVT_BOOST_OVP	[0]	EVENT	0x0	Event caused by BOOST OVP Fault					

14.4.1.2 Register DISPLAY_STATUS_A

Address	Register Name	POR Value	Reset Type(s)

0x0341	DISPLAY_STATUS_A			0x00	D: PowerOn M fsmError RstReload					
7	6		5	4	3	2	1	0		
Reserved	Reserved		CP_UVP	CP_OVP	DLDO_SC	BOOST_UVP	BOOST_OCP	BOOST_OVP		
Field Name	Bits	Type	POR	Description						
CP_UVP	[5]	RO	0x0	CP UVP Fault Status						
				Value	Description					
				0x0 (POR)	RESET					
CP_OVP	[4]	RO	0x0	CP OVP Fault Status						
				Value	Description					
				0x0 (POR)	RESET					
DLDO_SC	[3]	RO	0x0	DLDO SC Fault Status						
				Value	Description					
				0x0 (POR)	RESET					
BOOST_UVP	[2]	RO	0x0	Boost UVP Fault Status						
				Value	Description					
				0x0 (POR)	RESET					
BOOST_OCP	[1]	RO	0x0	Boost OCP Fault Status						
				Value	Description					

				0x0 (POR)	RESET
				0x1	OFF
					Boost OVP Fault Status
				Value	Description
BOOST_OVP	[0]	RO	0x0	0x0 (POR)	RESET
				0x1	OFF

14.4.1.3 Register DISPLAY_IRQ_MASK_A

Address	Register Name			POR Value	Reset Type(s)					
0x0342	DISPLAY_IRQ_MASK_A			0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)					
7	6	5	4	3	2	1	0			
Reserved	Reserved	M_CP_UVP	M_CP_OVP	M_DLDO_SC	M_BOOST_UVP	M_BOOST_OCP	M_BOOST_OVP			
Field Name	Bits	Type	POR	Description						
M_CP_UVP	[5]	IRQ_MASK OTP	0x0	CP_UVP irqmask						
M_CP_OVP	[4]	IRQ_MASK OTP	0x0	CP_OVP irqmask						
M_DLDO_SC	[3]	IRQ_MASK OTP	0x0	DLDO_SC irqmask						
M_BOOST_UVP	[2]	IRQ_MASK OTP	0x0	BOOST_UVP irqmask						
M_BOOST_OCP	[1]	IRQ_MASK OTP	0x0	BOOST_OCP irqmask						

M_BOOST_OVP	[0]	IRQ_MASK OTP	0x0	BOOST_OVP irqmask	
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14.4.2 Display Main-Ctrl Configuration

14.4.2.1 Register DISPLAY_CONFIG1

Address	Register Name	POR Value	Reset Type(s)					
7	6	5	4	3	2	1	0	
0x0343	DISPLAY_CONFIG1	0x04	C: PowerOn (HW default) OtpReload RstReload (OTP value)					
Reserved 0	Reserved 0	Reserved 0	Reserved	DN_VPOS_VNEG	UP_VPOS_VNEG	SEQ_DN_SIMULTANOUS	SEQ_UP_SIMULTANOUS	
Field Name	Bits	Type	POR	Description				
DN_VPOS_VNEG	[3]	RW OTP	0x0	Sequence down, Vpos disable first				
				Value	Description			
				0x0 (POR)	vneg disable earlier than vpos			
UP_VPOS_VNEG	[2]	RW OTP	0x1	Sequence up, Vpos enable first				
				Value	Description			
				0x0	vneg enable earlier than vpos			
SEQ_DN_SIMULTANOUS	[1]	RW OTP	0x0	Simultaneous enable for sequence down				
				Value	Description			

				0x0 (POR)	vpos and vneg are disable by sequence
				0x1	vpos and vneg are disable at the same time
					Simultaneous enable for sequence up
				Value	Description
SEQ_UP_SIMULTANOUS	[0]	RW OTP	0x0	0x0 (POR)	vpos and vneg are enable by sequence
				0x1	vpos and vneg are enable at the same time

14.4.2.2 Register DISPLAY_CONFIG2

Address	Register Name	POR Value	Reset Type(s)																
0x0344	DISPLAY_CONFIG2	0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)																
7	6	5	4	3	2	1	0												
UP_DELAY_SRC_SCALE								UP_DELAY_SRC<6:0>											
Field Name	Bits	Type	POR																
UP_DELAY_SRC_SCALE	[7]	RW OTP	0x0	Up sequence delay scale for aux state															
Value	Description																		
0x0 (POR)	32us																		
0x1	128us																		
UP_DELAY_SRC	[6:0]	RW OTP	0x0	Up sequence delay for src state															
Value	Description																		
0x0 (POR)	UP_DELAY_SRC value																		

14.4.2.3 Register DISPLAY_CONFIG3

Address	Register Name	POR Value	Reset Type(s)											
0x0345	DISPLAY_CONFIG3	0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)											
		UP_DELAY_POS_NEG_SCALE								UP_DELAY_POS_NEG<6:0>				
Field Name		Bits	Type	POR	Description									
UP_DELAY_POS_NEG_SCALE		[7:7]	RW OTP	0x0	Up sequence delay scale for pos/neg state									
					Value		Description							
					0x0 (POR)	32us								
UP_DELAY_POS_NEG		[6:0]	RW OTP	0x0	Up sequence delay for pos/neg state									
					Value		Description							
					0x0 (POR)	UP_DELAY_POS_NEG value								

14.4.2.4 Register DISPLAY_CONFIG4

Address	Register Name	POR Value	Reset Type(s)											
0x0346	DISPLAY_CONFIG4	0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)											
		DN_DELAY_SRC_SCALE								DN_DELAY_SRC<6:0>				
DN_DELAY_SRC_SCALE		[7:7]	RW OTP	0x0	Down sequence delay scale for src state									
					Value		Description							
					0x0 (POR)	32us								

Field Name	Bits	Type	POR	Description	
DN_DELAY_SRC_SCALE	[7:7]	RW OTP	0x0	Down sequence delay scale for src state	
				Value	Description
				0x0 (POR)	32us
DN_DELAY_SRC	[6:0]	RW OTP	0x0	Down sequence delay for src state	
				Value	Description
				0x0 (POR)	DN_DELAY value for src state

14.4.2.5 Register DISPLAY_CONFIG5

Address	Register Name	POR Value		Reset Type(s)								
0x0347	DISPLAY_CONFIG5	0x00		C: PowerOn (HW default) OtpReload RstReload (OTP value)								
		7	6	5	4	3	2	1	0			
DN_DELAY_POS_NEG_SCALE		DN_DELAY_POS_NEG<6:0>										
Field Name	Bits	Type	POR	Description								
DN_DELAY_POS_NEG_SCALE	[7:7]	RW OTP	0x0	Down sequence delay scale for pos/neg state								
				Value	Description							
				0x0 (POR)	32us							
DN_DELAY_POS_NEG	[6:0]	RW OTP	0x0	Down sequence delay for pos/neg state								
				Value	Description							

			0x0 (POR)	DN_DELAY value for pos/neg state
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14.4.2.6 Register DISPLAY_CONFIG6

Address	Register Name	POR Value	Reset Type(s)															
0x0348	DISPLAY_CONFIG6	0x3A	C: PowerOn (HW default) OtpReload RstReload (OTP value)															
7		6		5		4		3		2								
MAP_SWITCH_ENABLE		Reserved		CP_MAP<1:0>			LDO_MAP<1:0>		BOOST_MAP<1:0>									
Field Name		Bits	Type	POR														
MAP_SWITCH_ENABLE[7]		RW OTP	0x0	Enable for mapping of power rail and sequence														
				Value	Description													
				0x0 (POR)	The setting of BOOST_MAP, INV_MAP, CP_MAP, and LDO_MAP is invalid													
CP_MAP		RW OTP	0x3	Charge Pump enable sequence mapping														
				Value	Description													
				0x0	Disable													
				0x1	source power enable sequence													
				0x2	positive supply enable sequence													
LDO_MAP		RW OTP	0x2	LDO enable sequence mapping														
				Value	Description													
				0x0	Disable													

				0x1	source power enable sequence
				0x2 (POR)	positive supply enable sequence
				0x3	negative supply enable sequence
BOOST_MAP				Boost enable sequence mapping	
				Value	Description
				0x0	Disable
				0x1	source power enable sequence
				0x2 (POR)	positive supply enable sequence
				0x3	negative supply enable sequence

14.4.3 Display Boost

14.4.3.1 Register DISPLAY_BOOST_VOLTAGE

Address	Register Name			POR Value	Reset Type(s)															
0x0350	DISPLAY_BOOST_VOLTAGE			0x68	C: PowerOn (HW default) OtpReload RstReload (OTP value)															
7	6	5	4	3	2	1	0	BOOST_VOLTAGE<7:0>												
Field Name	Bits	Type	POR	Description																
BOOST_VOLTAGE	[7:0]	RW OTP	0x68	Select DAC output for Display Boost (unit: 10mV). VDAC=FB=(1/5)xBOOST_OUT																
				Value	Description															
				0x0	Boost DAC=0V, Boost output=0V															

				0x1	Boost DAC=20mV, Boost output=0.1V
				0x2	Boost DAC=30mV, Boost output=0.15V
				0x3	Boost DAC=40mV, Boost output=0.2V
				0x4	Boost DAC=50mV, Boost output=0.25V
				0x5	Boost DAC=60mV, Boost output=0.3V
				0x6	Boost DAC=70mV, Boost output=0.35V

14.4.3.2 Register DISPLAY_BOOST_SLEW_RATE

Address	Register Name			POR Value	Reset Type(s)				
0x0351	DISPLAY_BOOST_SLEW_RATE			0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)				
	7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BOOST_SLEW_RATE<2:0>			
Field Name	Bits	Type	POR	Description					
BOOST_SLEW_RATE[2:0]	RW OTP	0x0	Select Vout slew rate for Boost soft start and soft shutdown.	Value		Description			
				0x0 (POR)	1.5625mV/us				
				0x1	3.125mV/us				
				0x2	4.25mV/us				
				0x3	9.375mV/us				
				0x4	12.5mV/us				
				0x5	13.625mV/us				
				0x6	16.75mV/us				

			0x7	25mV/us	
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14.4.3.3 Register DISPLAY_BOOST_CONFIG1

Address	Register Name			POR Value	Reset Type(s)	Bit Description										
0x0352	DISPLAY_BOOST_CONFIG1			0x01	C: PowerOn (HW default) OtpReload RstReload (OTP value)											
	7	6	5	4	3	2	1	0								
Reserved	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved	BOOST_SEL_POC_LIMIT<2:0>										
Field Name		Bits	Type	POR	Description											
BOOST_SEL_POC_LIMIT[2:0]		RW OTP	0x1		Control the positive over current limit.											
					Value	Description										
					0x0	490mA										
					0x1 (POR)	670mA										
					0x2	823mA										
					0x3	1A										
					0x4	1.2A										
					0x5	1.4A										
					0x6	1.6A										
					0x7	1.9A										

14.4.4 Display Charge Pump

14.4.4.1 Register DISPLAY_CP_VOLTAGE

Address	Register Name			POR Value	Reset Type(s)												
0x0360	DISPLAY_CP_VOLTAGE			0x63	C: PowerOn (HW default) OtpReload RstReload (OTP value)												
7	6	5	4	3	2	1	0										
CP_VOLTAGE<7:0>																	
Field Name	Bits	Type	POR	Description													
CP_VOLTAGE	[7:0]	RW OTP	0x63	Select DAC output for Display CP (unit: 10mV). VDAC=FB=(-1/5)xDISP_OUTN													
				Value	Description												
				0x0	Charge Pump DAC=0V, Charge Pump output=0V												
				0x1	Charge Pump DAC=20mV, Charge Pump output=-0.1V												
				0x2	Charge Pump DAC=30mV, Charge Pump output=-0.15V												
				0x3	Charge Pump DAC=40mV, Charge Pump output=-0.2V												

14.4.4.2 Register DISPLAY_CP_SLEW_RATE

Address	Register Name			POR Value	Reset Type(s)							
0x0361	DISPLAY_CP_SLEW_RATE			0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)							
7	6	5	4	3	2	1	0					
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CP_SLEW_RATE<2:0>						

Field Name	Bits	Type	POR	Description	
CP_SLEW_RATE	[2:0]	RW OTP	0x0	Select Vout slew rate for Charge Pump soft start and soft shutdown.	
				Value	Description
				0x0 (POR)	1.5625mV/us
				0x1	3.125mV/us
				0x2	4.25mV/us
				0x3	9.375mV/us
				0x4	12.5mV/us
				0x5	13.625mV/us
				0x6	16.75mV/us
				0x7	25mV/us

14.4.4.3 Register DISPLAY_CP_CONFIG8

Address	Register Name			POR Value	Reset Type(s)									
0x0369	DISPLAY_CP_CONFIG8			0x33	C: PowerOn (HW default) OtpReload RstReload (OTP value)									
	7	6	5	4	3	2	1	0						
	CP_SEL_RON_MP1_NM<1:0>		Reserved 1		Reserved 1	CP_SEL_RON_MN2_NM<1:0>		Reserved 1	Reserved 1					
Field Name	Bits	Type	POR	Description										
CP_SEL_RON_MP1_NM	[7:6]	RW OTP	0x0	Select Rdson of MP1H after DAC is settled at target value for cp_sstart_delay (normal mode)										
				Value	Description									
				0x0 (POR)	1x Ron									
				0x1	3x Ron									

				0x2	6x Ron
				0x3	50.4x Ron
CP_SEL_RON_MN2_NM[3:2]				Select Rdson of MN2H after DAC is settled at target value for cp_sstart_delay (normal mode)	
				Value	Description
				0x0 (POR)	1x Ron
				0x1	2x Ron
				0x2	5.8x Ron
				0x3	13.6x Ron

14.4.4.4 Register DISPLAY_CP_CONFIG9

Address	Register Name			POR Value	Reset Type(s)								
0x036A	DISPLAY_CP_CONFIG9			0x20	C: PowerOn (HW default) OtpReload RstReload (OTP value)								
7	6	5	4	3	2	1	0						
Reserved 0	Reserved	CP_OUTN_SHRT_PNGD_N5V	Reserved	CP_DIN_SPARE<3:0>									
Field Name			Bits	Type	POR	Description							
CP_OUTN_SHRT_PNGD_N5V[5:5]			RW	OTP	0x1	Select PGND-5V function if cp_en=1							
						Value	Description						
						0x0	Internal GND_N5V for driver are generated by regulator						
						0x1 (POR)	Always tie internal GND_N5V to DISP_OUTN as OUTN >-5.5V at steady state. (cp_vdac<1.1V)						
CP_DIN_SPARE			[3:0]	RW	0x0	cp_din_spare is defined as internal cp_en_auto_vsys_shrt_outn_p5v. As cp_vsys_shrt_outn_p5v=1, it can auto select VSYSP short to DISP_OUTN+5V or not 0: disable 1: enable							

					cp_din_spare is defined as internal cp_en_auto_vsys_shrt_outn_p5v_th. It works as cp_en_auto_vsys_shrt_outn_p5v=1 and cp_vsys_shrt_outn_p5v=1, it defines the threshold of VSYSP level to make VSYSP short to DISP_OUTN+5V.(if VSYSP>Vth_vsys) 00: Vth_vsys = 4V 01: Vth_vsys = 3.9V 10: Vth_vsys = 3.75V 11: Vth_vsys = 3.6V cp_din_spare is spare A/D interface net.
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14.4.5 Display LDO

14.4.5.1 Register DISPLAY_LDO_VOLTAGE

Address	Register Name			POR Value	Reset Type(s)	LDO_VOLTAGE<7:0>																				
7	6	5	4	3	2	1	0																			
Field Name				Bits	Type	POR	Description																			
LDO_VOLTAGE				[7:0]	RW OTP	0x63	Select DAC output for Display LDO (unit: 10mV). VDAC=FB=(1/5)xDISP_OUTP																			
				Value		Description																				
				0x0			display ldo DAC=0V, display ldo target voltage=0V																			
				0x1			display ldo DAC=20mV, display ldo target voltage=0.1V																			
				0x2			display ldo DAC=30mV, display ldo target voltage=0.15V																			
				0x3			display ldo DAC=40mV, display ldo target voltage=0.2V																			

14.4.5.2 Register DISPLAY_LDO_SLEW_RATE

Address	Register Name			POR Value	Reset Type(s)							
7	6	5	4	3	2	1	0					
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO_SLEW_RATE<2:0>						
Field Name		Bits	Type	POR	Description							
LDO_SLEW_RATE	[2:0]	RW OTP	0x0	Select Vout slew rate for Display LDO soft start and soft shutdown.	Value							
					0x0 (POR)	1.5625mV/us						
					0x1	3.125mV/us						
					0x2	4.25mV/us						
					0x3	9.375mV/us						
					0x4	12.5mV/us						
					0x5	13.625mV/us						
					0x6	16.75mV/us						
					0x7	25mV/us						

14.5 WLED SLAVE

14.5.1 Event

14.5.1.1 Register WLED_EVENT

Address	Register Name	POR Value	Reset Type(s)					
7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	Reserved	Reserved	EVT_WLED_UV	EVT_WLED_OV	EVT_WLED_OC	
Field Name	Bits	Type	POR	Description				
EVT_WLED_UV	[2]	EVENT	0x0	WLED UV Fault Event				
EVT_WLED_OV	[1]	EVENT	0x0	WLED OV Fault Event				
EVT_WLED_OC	[0]	EVENT	0x0	WLED OC Fault Event				

14.5.1.2 Register WLED_STATUS

Address	Register Name	POR Value	Reset Type(s)						
7	6	5	4	3	2	1	0		
Reserved	Reserved	Reserved	Reserved	Reserved	WLED_UV	WLED_OV	WLED_OC		
Field Name	Bits	Type	POR	Description					
WLED_UV	[2]	RO	0x0	WLED UV Fault Status					
				Value	Description				
				0x0 (POR)	normal				
				0x1	WLED UV Fault Occur				

WLED OV Fault Status				
WLED_OV	[1]	RO	0x0	Value
				Description
WLED_OC	[0]	RO	0x0	0x0 (POR)
				normal
WLED OC Fault Status				
WLED_OC	[0]	RO	0x0	Value
				Description
WLED_OC	[0]	RO	0x0	0x0 (POR)
				normal
WLED Over Current Fault Occur				

14.5.1.3 Register WLED_IRQ_MASK

Address	Register Name	POR Value	Reset Type(s)					
0x0382	WLED_IRQ_MASK	0x07	C: PowerOn (HW default) OtpReload RstReload (OTP value)					
7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	Reserved	Reserved	M_WLED_UV	M_WLED_OV	M_WLED_OC	
Field Name	Bits	Type	POR	Description				
M_WLED_UV	[2]	IRQ_MASK OTP	0x1	irqmask for E_WLED_UV				
M_WLED_OV	[1]	IRQ_MASK OTP	0x1	irqmask for E_WLED_OV				
M_WLED_OC	[0]	IRQ_MASK OTP	0x1	irqmask for E_WLED_OC				

14.5.2 WLED Configuration

14.5.2.1 Register WLED_CONFIG1

Address	Register Name	POR Value	Reset Type(s)										
7	6	5	4	3	2	1	0						
Reserved	Reserved 1	Reserved0	IDAC_LINEAR	WLED_IDAC_EN	WLED_MODE<2:0>								
Field Name		Bits	Type	POR	Description								
IDAC_LINEAR	[4]	RW OTP	0x1	WLED IDAC current linear									
				Value		Description							
				0x0	Non-Linear								
				0x1 (POR)	Linear								
WLED_IDAC_EN	[3]	RW OTP	0x1	Enable WLED IDAC									
				Value		Description							
				0x0	Disable IDAC								
				0x1 (POR)	Enable IDAC								
WLED_MODE	[2:0]	RW OTP	0x3	WLED mode selection									
				Value		Description							
				0x0	Bypass mode								
				0x1	N.A.								
				0x2	N.A.								
				0x3 (POR)	N.A.								
				0x4	duty detect mixed mode								
				0x5	ext_r_mode								

14.5.2.2 Register WLED_CONFIG2

Address	Register Name	POR Value	Reset Type(s)													
7	6	5	4	3	2	1	0	IDAC_TARGET<7:0>								
Field Name		Bits	Type	POR	Description											
IDAC_TARGET	[7:0]	RW OTP	0x0	set WLED IDAC current target, LSB=160uA												

14.5.2.3 Register WLED_CONFIG3

Address	Register Name	POR Value	Reset Type(s)													
7	6	5	4	3	2	1	0	IDAC_RAMP_RATE<3:0>								
Field Name		Bits	Type	POR	Description											
PWM_OUT_FREQ_STEP	[7:5]	RW OTP	0x0	WLED PWM output frequency step; PWM OUT frequency=20K+2*PWM_OUT_FREQ_STEP												
				Value	Description											
				0x0 (POR)	20KHz											
				0x1	22KHz											
				0x2	24KHz											

				0x3	26KHz
				0x4	28KHz
				0x5	30KHz
				0x6	32KHz
				0x7	34KHz
PWM_IN_FREQ_RANGE [4]	RW OTP	0x0	WLED PWM input frequency range for duty detection in detection mode		
			Value	Description	
			0x0 (POR)	PWM input frequency range 25Khz ~ 30Khz	
			0x1	PWM input frequency range 30Khz ~ 35Khz	
			WLED_IDAC RAMP CIOCK RATE		
IDAC_RAMP_RATE	[3:0]	RW OTP	0x0	Value	Description
				0x0 (POR)	2MHz
				0x1	1MHz
				0x2	500Khz
				0x3	250Khz
				0x4	125Khz
				0x5	62.5Khz
				0x6	31.25Khz
				0x7	13.625Khz
				0x8	5.825Khz
				0x9	3.90625Khz
				0xA	1.953125Khz
				0xB	1.953125Khz
				0xC	1.953125Khz
				0xD	1.953125Khz
				0xE	1.953125Khz

			0xF	1.953125KHz	
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14.5.2.4 Register WLED_CONFIG4

Address	Register Name	POR Value	Reset Type(s)	Field Name								Bits	Type	POR	Description				
0x0386	WLED_CONFIG4	0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)									7	6	5	4	3	2	1	0
PWM_IN_DUTY_THRESHOLD<7:0>																			
PWM_IN_DUTY_THRESHOLD	[7:0]	RW OTP	0x0	WLED pwm in duty threshold of analog/dimming mode in mixed mode. The threshold of PWM input Duty to determine analog/PWM dimming in mixed mode															

14.5.2.5 Register WLED_CONFIG5

Address	Register Name	POR Value	Reset Type(s)	Field Name								Bits	Type	POR	Description				
0x0387	WLED_CONFIG5	0xFF	C: PowerOn (HW default) OtpReload RstReload (OTP value)									7	6	5	4	3	2	1	0
PWM_OUT_DUTY<7:0>																			
PWM_OUT_DUTY	[7:0]	RW OTP	0xff	WLED PWM output threshold for dimming control. Used in direct mode only															

14.5.2.6 Register WLED_CONFIG6

Address	Register Name	POR Value	Reset Type(s)																		
7	6	5	4	3	2	1	0														
Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	WLED_PANIC_EN	WLED_PANIC_VTH<1:0>															
Field Name		Bits	Type	POR	Description																
WLED_PANIC_EN		[2]	RTWT OTP	0x0	WLED_PANIC_EN																
					Value		Description														
					0x0 (POR)	Disable panic comparator															
WLED_PANIC_VTH		[1:0]	RW OTP	0x2	WLED panic level threshold select																
					Value		Description														
					0x0	0.5V															
					0x1	0.6V															
					0x2 (POR)	0.7V															
					0x3	DAC															

14.5.2.7 Register WLED_CONFIG7

Address	Register Name	POR Value	Reset Type(s)				
0x0389	WLED_CONFIG7	0x40	C: PowerOn (HW default)				

				OtpReload RstReload (OTP value)					
7	6	5	4	3	2	1	0		
Reserved 0	WLED_PANIC_PERIOD<1:0>			WLED_DISCHARGE_SEL<2:0>			PWM_THRESHOLD_PLUS	IDAC_RAMP_DIS	
Description									
Field Name		Bits	Type	POR					
WLED_PANIC_PERIOD		[6:5]	RW OTP	0x2	Detect WLED panic(drv_b) period				
					Value		Description		
					0x0	5us			
					0x1	10us			
					0x2 (POR)	20us			
					0x3	30us			
WLED_DISCHARGE_SEL		[4:2]	RW OTP	0x0	Audio-skipping discharge current selection (typical discharge current when VSYS=3.8V)				
					Value		Description		
					0x0 (POR)	12.3mA			
					0x1	4.5mA			
					0x2	3.9mA			
					0x3	6.9mA			
					0x4	2.2mA			
					0x5	5.8mA			
					0x6	5.5mA			
					0x7	9.9mA			
PWM_THRESHOLD_PLUS		[1]	RW OTP	0x0	Set the WLED PWM out duty minimum bound to 1/256				
					Value		Description		
					0x0 (POR)	Minimum PWM dimming duty is 0			

				0x1	Minimum PWM dimming duty is 1/256
IDAC_RAMP_DIS	[0]	RW OTP	0x0	WLED IDAC ramp disable	
Value	Description				
0x0 (POR)	IDAC code ramp enable				
0x1	IDAC code ramp disable				

14.5.2.8 Register WLED_CONFIG9

Address	Register Name	POR Value	Reset Type(s)									
7	6	5	4	3	2	1	0					
VDAC_FULL_SCALE_EXT_R<7:0>												
Field Name	Bits	Type	POR									
VDAC_FULL_SCALE_EXT_R[7:0]	[7:0]	RW OTP	0x95	Full-scale VDAC code for WLED in ext_r_rmode, range from 0 to 1.6v, VDAC=FB=WLED_IDAC; Voltage = (VDAC_FULL_SCALE_EXT_R == 0)? 0mV : 10mV + (VDAC_FULL_SCALE_EXT_R * 10mV)								
Value	Description											
0x0	0mV											
0x1	10 + VDAC_FULL_SCALE_EXT_R * 10 unit:=mV											
0x9F	1600mV											

14.5.2.9 Register WLED_BOOST_CONTROL1

Address	Register Name	POR Value	Reset Type(s)				

0x0390	WLED_BOOST_CONTROL1			0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)																			
7	6	5	4	3	2	1	0																	
VDAC_SLEW_RATE<2:0>				PANIC_FB_SEL<1:0>		SEL_OVP_TH	SEL_POC_LIMIT<1:0>																	
Field Name Bits Type POR Description																								
VDAC RAMP SLEW RATE (LSB=10mV)																								
VDAC_SLEW_RATE	[7:5]	RW OTP	0x0	Value	Description																			
				0x0 (POR)	1.5625mV/us																			
				0x1	3.125mV/us																			
				0x2	4.25mV/us																			
				0x3	9.375mV/us																			
				0x4	12.5mV/us																			
				0x5	13.625mV/us																			
				0x6	16.75mV/us																			
				0x7	25mV/us																			
Select WLED boost FB ratio in panic comparison																								
PANIC_FB_SEL		RW OTP	0x0	Value	Description																			
				0x0 (POR)	Panic fb = WLED IDAC FB																			
				0x1	Panic fb = 0.9xWLED IDAC FB																			
				0x2	Panic fb = 0.8xWLED IDAC FB																			
				0x3	Panic fb = 0.7xWLED IDAC FB																			
SEL_OVP_TH		RW OTP	0x0	over voltage protection (OVP) threshold for WLED boost																				
Value Description																								

				0x0 (POR)	25.8V
				0x1	31.9V
					Current limit threshold for WLED boost
				Value	Description
SEL_POC_LIMIT	[1:0]	RW OTP	0x0	0x0 (POR)	2.5A
				0x1	1.5A
				0x2	2.0A
				0x3	3.0A

14.5.2.10 Register WLED_BOOST_CONTROL2

Address	Register Name			POR Value	Reset Type(s)												
0x0391	WLED_BOOST_CONTROL2			0x00	C: PowerOn (HW default) OtpReload RstReload (OTP value)												
7	6	5	4	3	2	1	0										
VDAC_SEL<7:0>																	
Field Name	Bits	Type	POR	Description													
VDAC_SEL	[7:0]	RW OTP	0x0	VDAC target for WLED boost													

The core buck register address is 8 bit. The address shown in the register map consists of [15:10] unused + [9:8] as core buck I2C device ID (slave address) + [7:0] for register address. An example is shown below.

To access COREBUCK_BUCK1_0 : 0x0103 → 0000 0001 0000 0011

Core buck device ID: 0x48 | **0x1** → 0x49

I2C command to access COREBUCK_BUCK1 : S100 1001 W/R A **0000 0011**

W/R = 0 for write, 1 for read; S: start, A: ack

Display Register Address Range	I2C Device ID	Register Block
0x0000~0x00FF	0x48	Virtual Register
0x0100~0x01FF	0x49	CoreBuck
0x0200~0x02FF	0x4A	Flash Driver

15 References

- [1] USB specification, Rev. 2.0, April 2000.
- [2] On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification, Revision 2.0 version 1.1a, Jul. 2012.
- [3] Battery Charging Specification, Revision 1.2, Dec. 2010.
- [4] USB Type-C Cable And Connector Specification, Rev. 1.0, Aug. 2014.
- [5] A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers, Japan Electronics and Information Technology Industries Association and Battery Association of Japan, Apr. 2007.
- [6] I2C Bus Specification And User Manual, Revision 3, Jun. 2007.

Revision History

Version	Date	Owner	Notes
V1.0	2018-03-27	Hardware	Created
V1.1	2018-05-04	Hardware	Update: 5.2 Package outline
V1.2	2018-07-02	Hardware	Update: Page7: add General description Page8: 3.5 A charging current; Page9: 4.0 V to 6.0V in 100mV steps; -6.0 V to -4.0V in 100mV steps Page38: with maximum charging current of 3.5A
V1.3	2018-08-24	Hardware	Update: 1.10 3.5A; 4.22 Max 14.5 4.6 IBAT_dead 0<Vbat<VBAT_short; 4.7 6.5 mΩ 4.8 ±8.5 -8.5 8.5 4.10 Max 6.4 Table20: Min -6.0 Table21: Max 6.0 4.11 ILIM 8.4 A 5.1 add: (BOTTOM View); 5.2 update Figure 5; 5.3 DISP_OUTN: change to 4.7uF ; CHG_BT: change to 10V
V1.4	2019-02-27	Hardware	Update: 1. FLASH_FD_CONFIG5/6/7/8 discription 2. WLED max vout fix to 26V 3. Remove WLED Overdrive mode
V1.5	2019-06-17	Hardware	Update: Remove I2C high speed mode descriptions.

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