UCP1301 Device Specification

Confidential and Proprietary

Revision History

Version	Data	Note
1.0	2019/11/26	First draft
1.1	2020/03/16	Update and correct package information to MSL1

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1 System Overview

1.1 General Description

UCP1301 is a high performance, low noise, analog audio 8.5V Smart Amplifier with current and voltage sensing ADC inside, which specialized in music and audio applications with speaker temperature and membrane excursion protection to avoid speaker damage by Unisoc FB-*SmarAmp*™ running on host.

The current and voltage feedback, so-called IV sensing feedback, will be transferred from analog signal to digital signal by ADCs, then to PDM data format output to the Host.

1.2 UCP1301 Features

- Current and Voltage sensing feedback for Smart Amplifier application
- Boost voltage: Typical=8.5V ,Max=9.5V
- Low noise: 9uV in Receiver Mode
  37uV in SPK Mode
- High SNR: 103dB
- THD+N: 0.01%
- Multi-level AGC: True-RMS base
- Output power: 4.2W@8Ω
- Speaker/receiver amplifier for 2-in-1 speaker application
- High PSRR:>90dB@217Hz
- Efficiency:
  - >80%(ClassK 2.1W PVDD =8.5V)
  - >83.6%(ClassK 2.1W PVDD =6.5V)
- Ultralow pop noise:<500uV
- Current and Voltage sensing feedback for FB-SmarAmpV3.0 application
- Support analog differential/single-end input, analog differential output
- Support cut-off frequency <30Hz for Cin and Rin @18dB~24dB gain
- Boost switching frequency >=1.6MHz
- Support Class-AB driver in receiver mode
- Support Class-D / Class-AB driver in speaker boost mode (Class-K)
- Support boost bypass mode to VBAT
- Support Class-D switching frequency customized
- Support Boost switching frequency customized
- PDM interface for IV sensing feedback
- Digital I2C control
- All digital IO support 1.8V/3.3V
- Support OVP / OCP / OTP / SCP / UVP
- Package information: 3.08x2.08mm^2 WLCSP

UCP1301

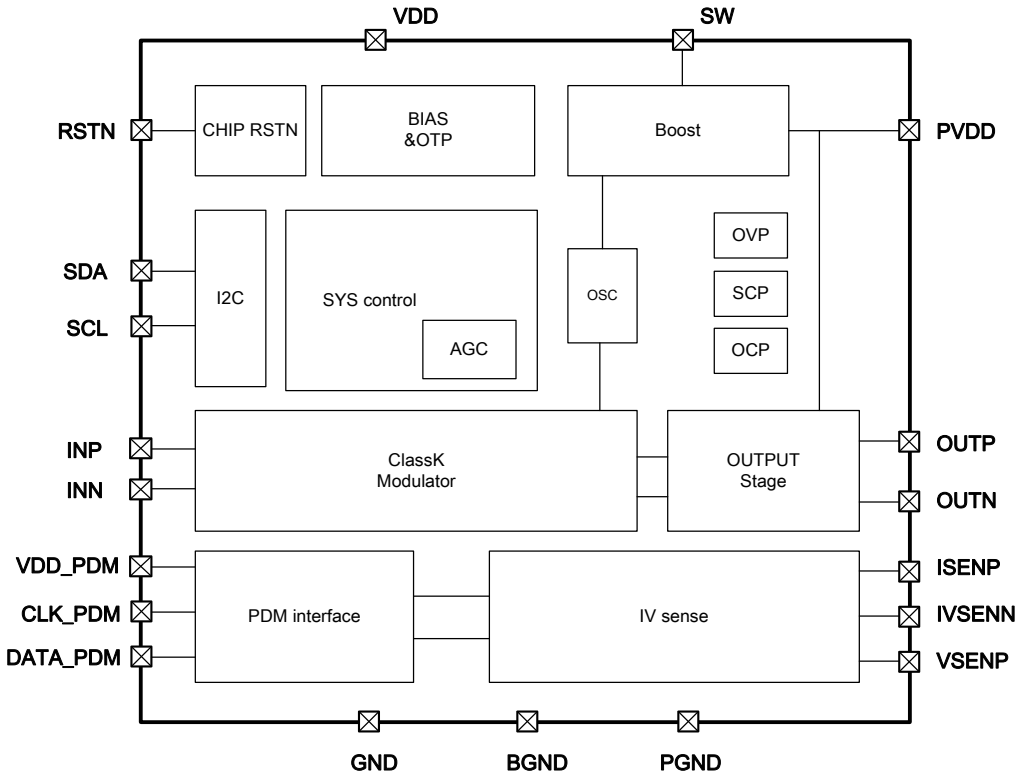


Figure 1-1 Block diagram

2 Package Information

Plastic-encapsulated surface mount packages are sensitive to damage induced by absorbed moisture and temperature. All of the UCP1301 chips are MSL 1, which had been marked on the label for every package.

2.1 Top Marking Definition

UCP1301

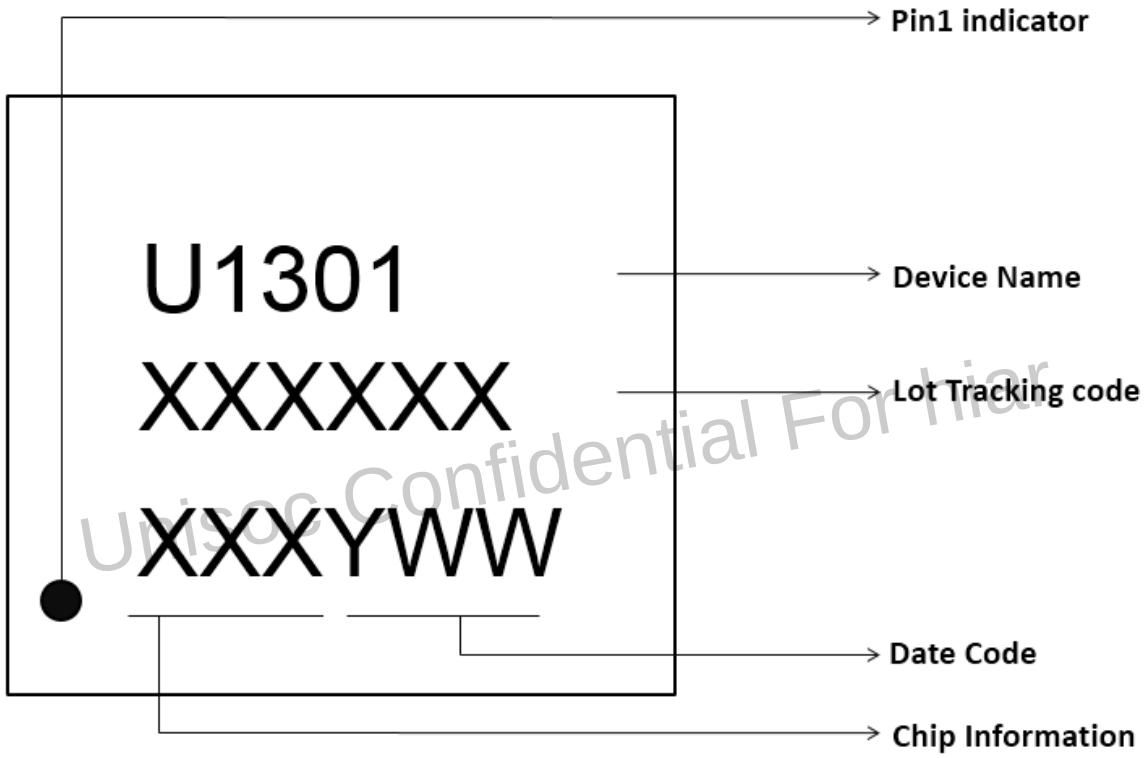


Figure 2-1 Top Marking Definition

2.2 BGA Pinout

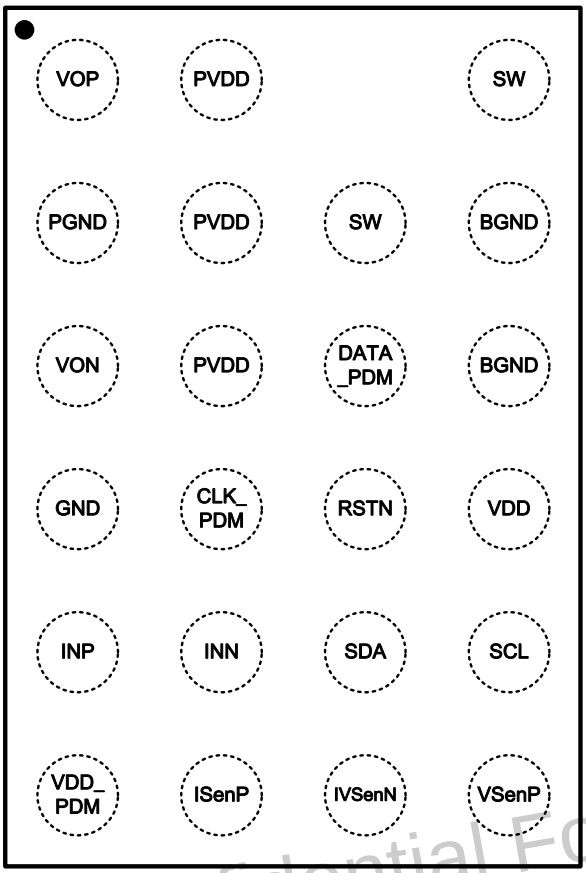
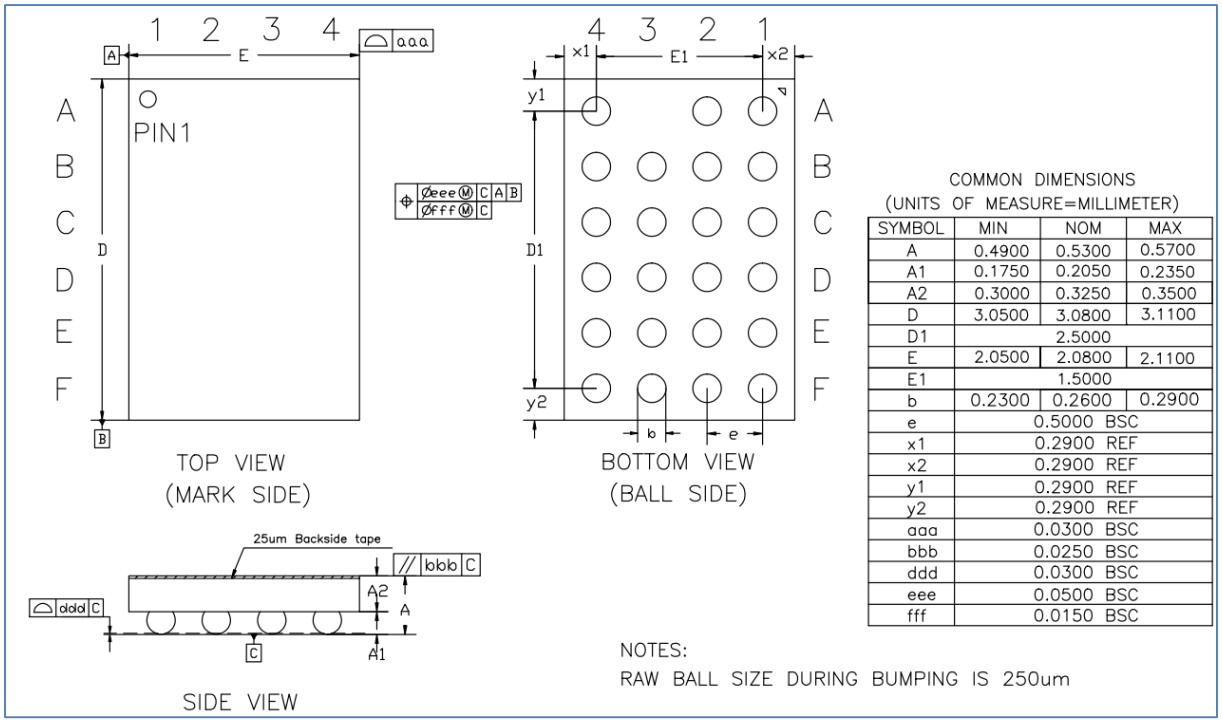


Figure 2-2 UCP1301 Pin Assignment and device marking

2.3 Package Outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.4900	0.5300	0.5700
A1	0.1750	0.2050	0.2350
A2	0.3000	0.3250	0.3500
D	3.0500	3.0800	3.1100
D1		2.5000	
E	2.0500	2.0800	2.1100
E1		1.5000	
b	0.2300	0.2600	0.2900
e		0.5000 BSC	
x1		0.2900 REF	
x2		0.2900 REF	
y1		0.2900 REF	
y2		0.2900 REF	
aaa		0.0300 BSC	
bbb		0.0250 BSC	
ddd		0.0300 BSC	
eee		0.0500 BSC	
fff		0.0150 BSC	

Figure 2-3 Package Outline

2.4 Reflow Profile

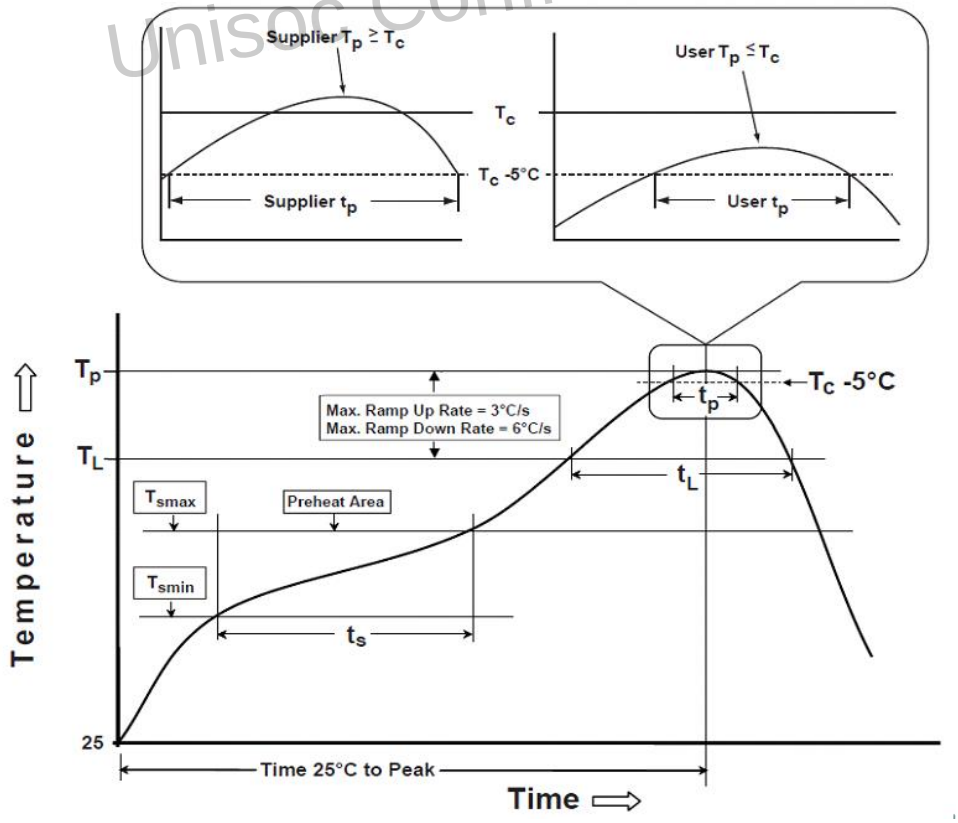


Figure 2-4 Recommended reflow profile

Table 2-1 JEDEC Classification reflow profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 2-2. For suppliers T_p must equal or exceed the Classification temp in Table 2-2.	For users T_p must not exceed the Classification temp in Table 2-3. For suppliers T_p must equal or exceed the Classification temp in Table 2-3.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 2-4 .	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.		

Note: The above recommended reflow profiles from IPC/JEDEC J-STD-020 are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on the specific process needs and board designs and shall not exceed the parameters in IPC/JEDEC J-STD-020.

Table 2-2 SnPb Eutectic Process - Classification Temperatures (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2-3 Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

3 Pin Information

3.1 Pin List

Table3-1 Pin Information

UCP1301

PIN NO	NAME	TYPE	DESCRIPTION
A1	VOP	IO	PA output P
A2，B2，C2	PVDD	Power	Boost output
A4，B3	SW	IO	Boost switching node
B1	PGND	Ground	PA Ground
B4，C4	BGND	Ground	Boost Ground
C1	VON	IO	PA output N
C3	DATA_PDM	IO	PDM data
D1	GND	Ground	Ground
D2	CLK_PDM	IO	PDM clock
D3	RSTN	IO	Reset pin. Low effective. Low for reset High for power on
D4	VDD	Power	Power
E1	INP	IO	Audio input P
E2	INN	IO	Audio input N
E3	SDA	IO	IIC interface, data
E4	SCL	IO	IIC interface, clock
F1	VDD_PDM	Power	Power input of PDM interface
F2	ISENP	IO	Speaker current sense P
F3	IVSENN	IO	Speaker current/voltage sense N
F4	VSENP	IO	Speaker voltage sense P

3.2 Control Registers

3.2.1 Memory Map

Base address 0x00

0x0030	PIN_REG0	PIN_REG0
0x0031	PIN_REG1	PIN_REG1

3.2.2 Register Description

3.2.2.1 PIN_REG0

0x00000030			PIN_REG0(0x000011CC)									PIN_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCL_FUNC_DRV		SCL_WPU	SCL_WPDO	SDA_FUNC_DRV		SDA_WPU	SDA_WPDO
Type									RW		RW	RW	RW		RW	RW
Reset									1	1	0	0	1	1	0	0

PIN_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description (IO Voltage=1.8V)
reserved	[31: 16]	RO	NA	0	
SCL_FUNC_DRV	[7: 6]	RW	NA	0x3	SCL pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
SCL_WPU	[5]	RW	NA	0	SCL pad pull up enable 0: disable 1: enable
SCL_WPDO	[4]	RW	NA	0	SCL pad pull down enable 0: disable 1: enable
SDA_FUNC_DRV	[3: 2]	RW	NA	0x3	SDA pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
SDA_WPU	[1]	RW	NA	0	SDA pad pull up enable 0: disable 1: enable
SDA_WPDO	[0]	RW	NA	0	SDA pad pull down enable 0: disable 1: enable

3.2.2.2 PIN_REG1

0x00000031			PIN_REG1(0x000000CC)									PIN_REG1				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INP_FUNC_DRV		INP_WPU	INP_WPDO	INN_FUNC_DRV		INN_WPU	INN_WPDO	CLK_PDM_FUNC_DRV		CLK_PDM_WPU	CLK_PDM_WPDO	DATA_PDM_FUNC_DRV		DATA_PDM_WPU	DATA_PDM_WPDO
Type	RW		RW	RW	RW		RW	RW	RW		RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0

PIN_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description(IO Voltage=1.8V)
reserved	[31: 16]	RO	NA	0	
INP_FUNC_DRV	[15: 14]	RW	NA	0	INP pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
INP_WPU	[13]	RW	NA	0	INP pad pull up enable 0: disable 1: enable
INP_WPDO	[12]	RW	NA	0	INP pad pull down enable 0: disable 1: enable
INN_FUNC_DRV	[11: 10]	RW	NA	0	INN pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
INN_WPU	[9]	RW	NA	0	INN pad pull up enable 0: disable 1: enable
INN_WPDO	[8]	RW	NA	0	INN pad pull down enable 0: disable 1: enable
CLK_PDM_FUNC_DRV	[7: 6]	RW	NA	0x3	CLK_PDM pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
CLK_PDM_WPU	[5]	RW	NA	0	CLK_PDM pad pull up enable 0: disable 1: enable
CLK_PDM_WPD	[4]	RW	NA	0	CLK_PDM pad pull down enable

O					0: disable 1: enable
DATA_PDM_FUNC_DRV	[3: 2]	RW	NA	0x3	DATA_PDM pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
DATA_PDM_WPU	[1]	RW	NA	0	DATA_PDM pad pull up enable 0: disable 1: enable
DATA_PDM_WPDO	[0]	RW	NA	0	DATA_PDM pad pull down enable 0: disable 1: enable

4 Electrical Specification

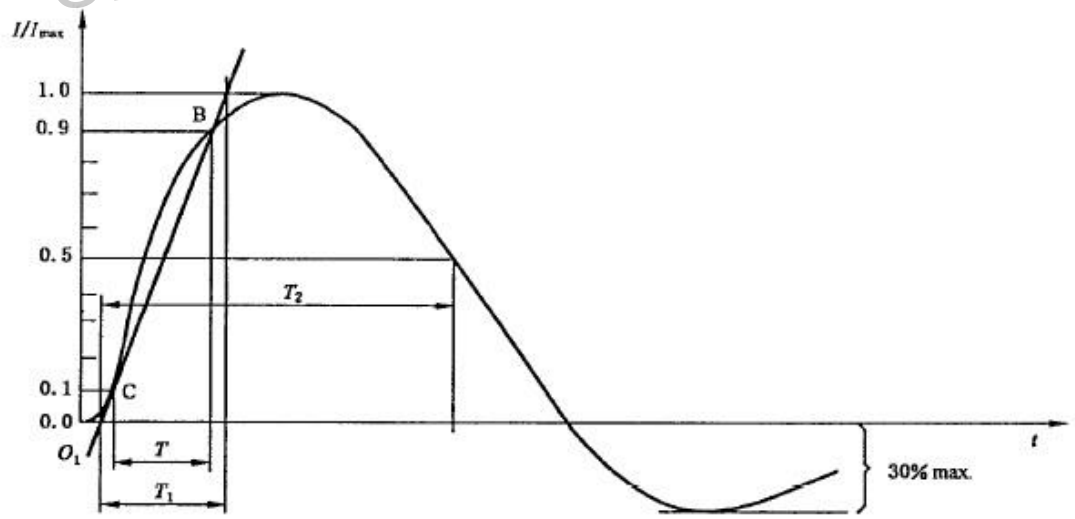
4.1 Absolute maximum ratings

The functionality of UCP1301 is subject to the absolute maximum/minimum values listed in following table. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Absolute maximum ratings of UCP1301

Symbol	Parameter	Min	Max	Unit
VDD	Supply voltage	-0.3	5.5	V
VDD_PDM	Supply voltage of PDM interface	-0.3	5.5	V
Vinn/Vinp	Input voltage of INN/INP pin	-0.3	VDD	
$V_{max, ESD}$	Maximum ESD stress voltage, Human Body Model, any pin to any supply pin, either polarity or any pin to all non-supply pins together, either polarity. Three stresses maximum.		2,000	V
$T_{storage}$	Storage temperature	-40	+125	°C
Tc	Case temp	-20	85	°C
V_{pulse}, $T_{width(T2)}$*	Voltage surge on vbat		14 20	V μs

Note: Vpulse and Twidth are described below:



$T_1 = 1.25 \times T = 8 \times (1 \pm 20\%)\mu s$

$T_2 = 20 \times (1 \pm 20\%)\mu s$

4.2 Recommended operating conditions

UCP1301 is recommended to operate under the conditions list in following table.

Table 4-1 Recommended operating conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD	Supply voltage	3.3		5.5	V

4.3 Thermal characteristics

The thermal characteristics are as shown infollowing table.

Table 4-2 Thermal characteristics

Symbol	Parameter	Condition	Value	Unit
Theta JA	Junction-to-Ambient thermal resistance	Air flow: 0 m/sec	66.3	°C/watt

4.4 ESD characteristics

The ESD characteristics are shown in following table.

Table 4-3 ESD characteristics

Symbol	Parameter	Condition	Value	Unit
HBM	Human Body mode	ESDA/JEDEC JS-001-2017	±2000	V
CDM	Charge Device Mode	JEDEC EIA/JESD22-C101F	±800	V

4.5 DC characteristics

For the following table, T_c = -20 to +85 °C, VDD= 3.6V, unless otherwise specified.

Table 4-4 DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply voltage	3.3		5.5	V
Ioff	Power down leakage, VDD= 3.6V,T_c =27°C			1	uA
IIC interface					
VDD_IIC	IIC power supply. (external pull-high)	1.62		5.5	V
V_{IL_IIC}	Input voltage Low-level	0		0.3x VDD_IIC	V
V_{IH_IIC}	Input voltage High-level	0.7x VDD_IIC		VDD_IIC	V
PDM interface					

Symbol	Parameter	Min	Typ	Max	Unit
VDD_PDM	PDM power supply	1.62		5.5	V
V_{IL_PDM}	Input voltage Low-level	0		0.3x VDD_PDM	V
V_{IH_PDM}	Input voltage High-level	0.7x VDD_PDM		VDD_PDM	V

4.6 AC characteristics

The AC characteristics of a pin include input and output capacitance, which determines the loading for external drivers or for other load analysis. The AC characteristic also includes a de-rating factor, which indicates how much faster or slower the AC timings get with different loads.

Table 4-5 Standard input, output and I/O pin AC characteristics

Symbol	Parameters	Min	Typical	Max	Units
C_{in}	Input capacitance, all standard input and IO pins			3.5	pF
C_{load}	Output capacitance, all standard output and IO pins			30	pF
T_{dr}	Output de-rating falling edge on all standard output and I/O pins, from 30 pF load		0.313		ns/pF

Note:

1. The AC specifications are tested with a 15 pF load as indicated in below figure.

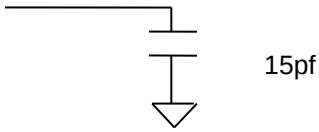


Figure 4-1 Test circuit of an I/O pin

2. The output capacitance and de-rating falling edge are measured under the condition of maximum driving strength: 1.6mA @ 1.8 V.

5 Power Management

5.1 Overview

UCP1301 is integrated power management unit (PMU) supports direct connection to the battery. All blocks in the PMU are specifically tailored to fit the needs of various baseband platforms with low cost and low quiescent power.

PMU contains the following blocks:

- Under Voltage Lock-out (UVLO) and Over Voltage Lock-out (OVLO)
- Built-in band-gap and oscillator
- Over Temperature Protect (OTP)
- Boost converter

5.2 RSTN

Whole chip reset pin. Chip reset(disable) at RSTN=0, chip actived at RSTN=1.

5.3 UVLO/OVLO

UVLO and OVLO circuit is to protect the system from abnormal power supply. If the power supply voltage is below 2.8V or above 5.5V for 1ms or longer, it indicatesthat the power supply voltage is out of operation range and the chip will power off automatically.

5.4 OTP

Over temperature protect is integrated in UCP1301. Chip will power off automatically when the temperature higher than 150℃. The protection will release and chip will auto reboot with registers kept, when temperature drops below 135℃ for auto-recovery function.

5.5 Oscillator

Internal oscillator is integrated for Class-D and boost converter. The frequency is 1.6MHz by default settings(1.2MHz~2MHz customized). Boost converter works at 1.6MHz, and Class-D amplifier works at half of boost switching frequency, 800kHz.

5.6 Boost

UCP1301 integrates a current-mode boost converter for Class-D powering. The default output voltage is 8.5V, and it can be set by register 0x08[10:7].

The soft-start function is built-in boost converter, to prevent in-rush current at start-up. Over-voltage-protect and Short-protect function is integrated.

5.6.1 Over voltage protect (OVP)

When Boost output voltage exceeds 20% of the setting value, OVP function will be active. System will power off immediately and reboot in 50ms to check boost output voltage.

5.6.2 Short circuit protect (SCP)

System will power off when SCP occurs. This function can prevent chip from extra high current or burn out when boost output short to ground.

6 Audio PA

6.1 Introduction

6.1.1 Features

- Current and Voltage sensing feedback for Smart Amplifier application
- Embedded Boost voltage:8.5V
- Low noise:
  9uV (gain=0dB class AB receiver THD+N=-92dB)
  17uV (gain=0dB class D receiver THD+N=-84dB)
  33uV (gain=22dB class AB spk THD+N=-90dB)
  33uV (gain=22dB class Kspk THD+N=-80dB)
- High SNR
  105dB (gain=0dB class AB receiver)
  102dB(gain=0dB class D receiver)
  103dB (gain=22dB class AB spk)
  104dB (gain=22dB class K spk)
- THD+N(max)
  -92dB(class AB receiver)
  -84dB (class D receiver)
  -90dB (class AB spk)
  -80dB(class K spk)
- Multi-level AGC
- Output power:
  4.2W (vbat=4.2v@8ohm classK speaker mode)
  0.58W(vbat=4.2v@8ohmreceiver mode)
- Speaker/receiver amplifier for 2-in-1 speaker application
- High PSRR:
  -100dB (gain=0dB class AB receiver)
  -92dB(gain=0dB class D receiver)
  -92dB (gain=22dB class AB spk)
  -90dB (gain=22dB class K spk)

- Efficiency:
  >80%(classK 2.1W @8ohm vboost=8.5v)
  >83.6%(classK 2.1W@8ohm vboost=6.5v)
- Low pop noise:<500uV (all mode)
- Current and Voltage sensing feedback for AEC reference application
- Support analog differential/single-end input, analog differential output
- Support cut-off frequency <30Hz for Cin and Rin @18dB~24dB gain
- Support Class-AB/ Class-D driver in receiver mode
- Support Class-D / Class-AB driver in speaker boost mode (Class-K)
- Support boost bypass mode to VBAT
- Class-D switching frequency customized(0.6MHz~1MHz)

6.1.2 Application Diagram

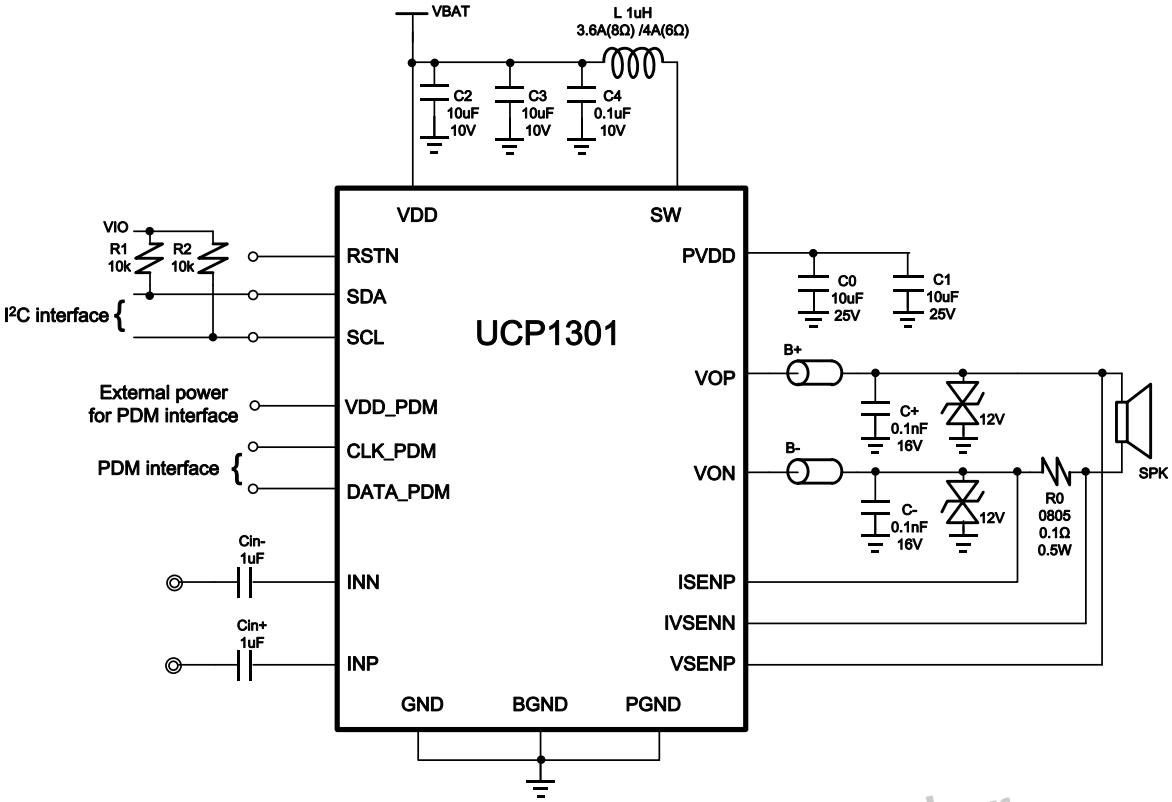


Figure 6-1 UCP1301 Typical Application Diagram

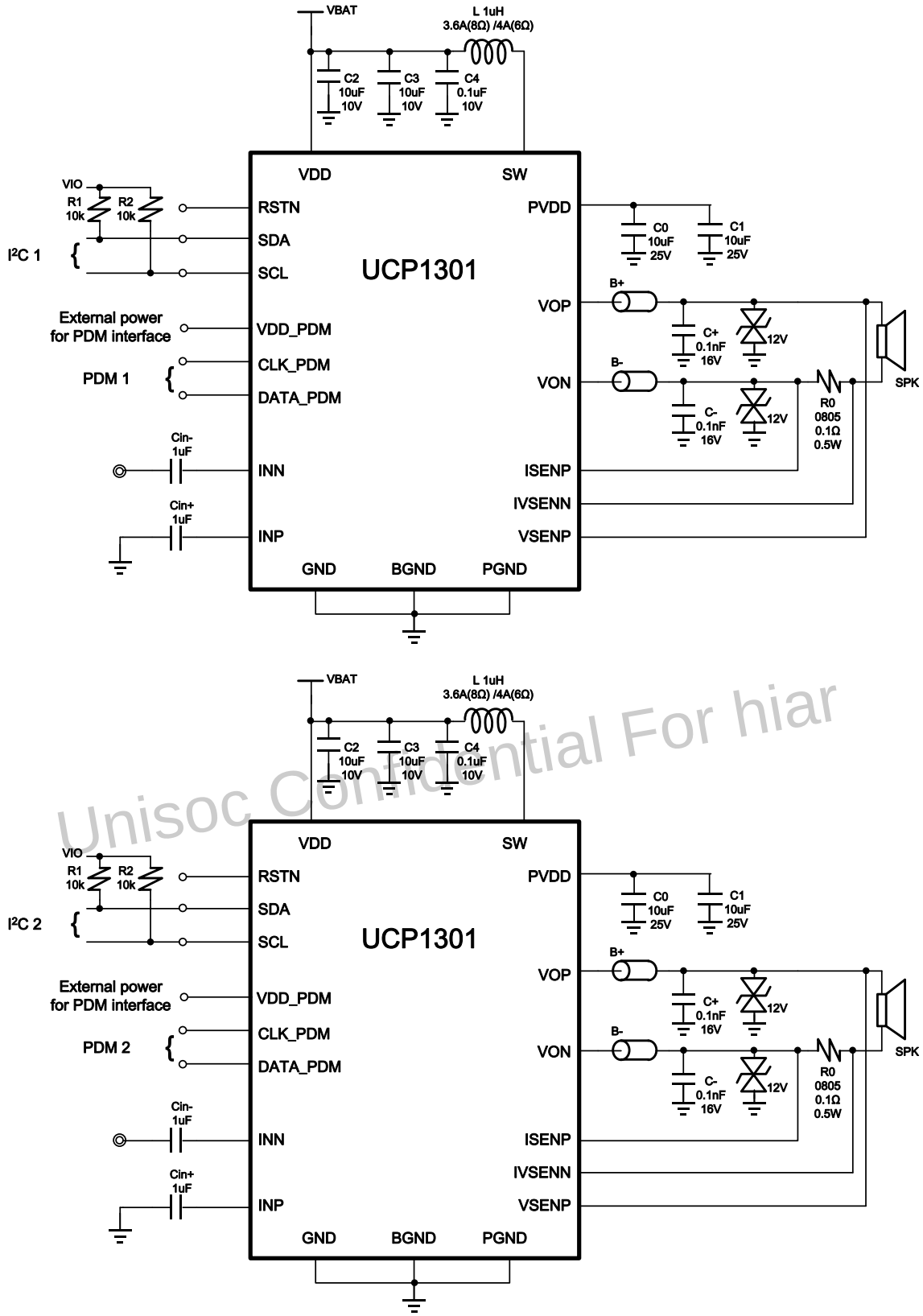


Figure 6-2 UCP1301 Smart PA Stereo Application Diagram

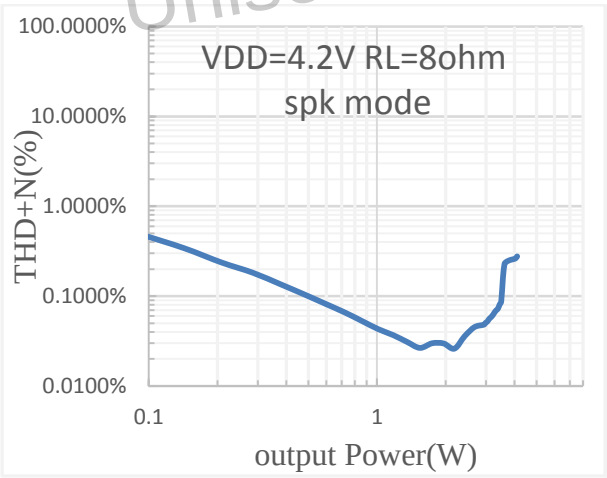
6.2 Audio PA Typical CHARACTRISTICS

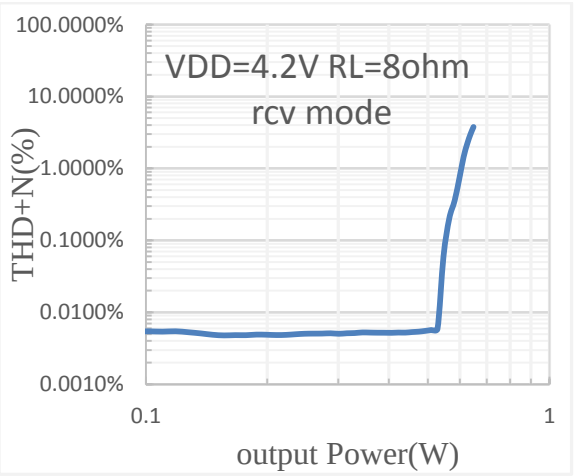
6.2.1 Electronic characteristics

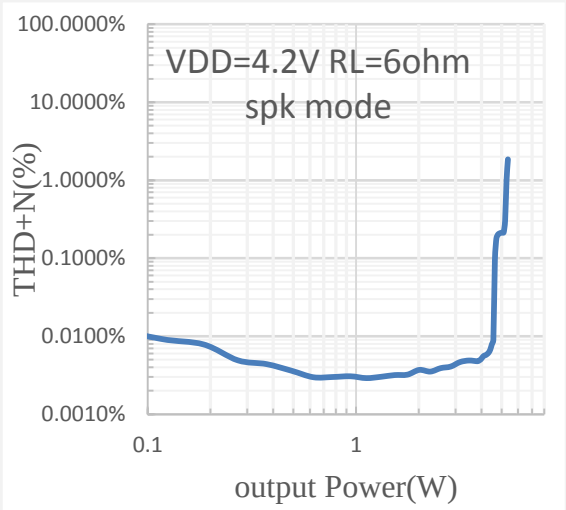
Parameters		Test Conditions	Min.	Typical	Max.	Unit
ClassK mode						
Vos	output offset voltage		-500	0	500	uV
Efficiency	Boost+ClassD total efficiency	VDD=4.2V, PVDD=8.5V, Rl=8ohm, Po=2.1W, THD+N=0.1%		80		%
		VDD=4.2V, PVDD=6.5V, Rl=8ohm, Po=2.1W, THD+N=0.1%		83.6		%
Iq	Speaker quiescent current			18.7		mA
Fosc	pwm frequency			800		kHz
PSRR		VDD=4.2V, Vpp-sin=300mV, 217Hz		-90		dB
		VDD=4.2V, Vpp-sin=300mV, 1kHz		-80		dB
SNR		VDD=4.2V, PVDD=8.5V, Po=4.1W, Av=8V/V, THD+N=1%, Rl=8ohm		104		dB
En	Speaker output noise	Av=22dB, 20Hz to 20kHz, A-weighting		34		uV
		Av=16dB, 20Hz to 20kHz, A-weighting		33		uV
Av	Speaker max gain			27		dB
Rin	Speaker input resistor	Av=16V/V		3		kohm
		Av=8V/V		5		kohm
THD+N		VDD=4.2V, Po=0.6W, Rl=8ohm, f=1kHz, PVDD=8.5V		0.015		%
Po	output power	THD+N=1%, Rl=8ohm, VDD=4.2V, PVDD=8.5V		4.1		W
		THD+N=1%, Rl=8ohm, VDD=4.2V, PVDD=6.5V		2.3		W
		THD+N=1%, Rl=6ohm, VDD=4.2V, PVDD=8.5V		4.6		W
		THD+N=1%, Rl=4ohm, VDD=4.2V, PVDD=8.5V		5.2		W
ClassD reciver mode						
Vos	output offset voltage		-500	0	500	uV
Efficiency	ClassD efficiency	VDD=4.2V, Rl=8ohm, Po=0.58W, THD+N=0.1%		85		%
Iq	Speaker quiescent current			9.4		mA
Fosc	pwm frequency			800		kHz
PSRR		VDD=4.2V, Vpp-sin=300mV, 217Hz		-90		dB
		VDD=4.2V, Vpp-sin=300mV, 1kHz		-80		dB
SNR		VDD=4.2V, PVDD=8.5V, Po=4.1W, Av=8V/V, THD+N=1%, Rl=8ohm		104		dB
En	Speaker output noise	Av=1V/V, 20Hz to 20kHz, A-weighting		17		uV
Av	gain			0		dB
Rin	Speaker input resistor			7.5		kohm
THD+N		VDD=4.2V, Po=0.6W, Rl=8ohm, f=1kHz, PVDD=8.5V		0.015		%
Po	output power	THD+N=1%, Rl=8ohm, VDD=4.2V		0.58		W
		THD+N=1%, Rl=6ohm, VDD=4.2V		0.71		W
		THD+N=1%, Rl=4ohm, VDD=4.2V		1.1		W

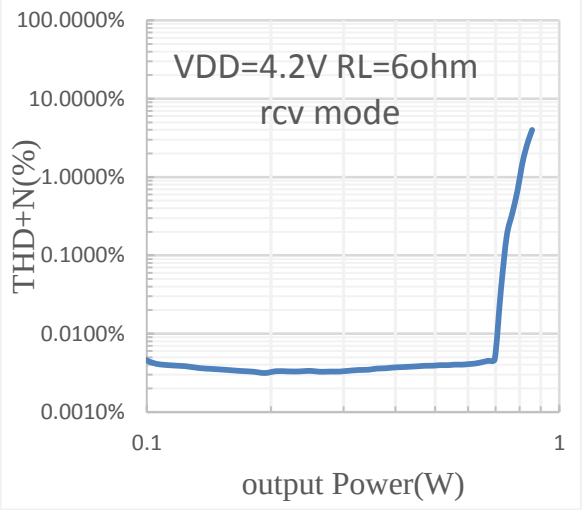
ClassAB speaker mode						
Vos	output offset voltage		-500		500	uV
Efficiency	Boost+ClassAB total efficiency	VDD=4.2V, PVDD=6.5V, Rl=8ohm, Po=2W, THD+N=0.02%		67		%
Iq	Speaker quiecent current			14		mA
PSRR		VDD=4.2V, Vpp-sin=300mV, 217Hz		-90		dB
		VDD=4.2V, Vpp-sin=300mV, 1kHz		-92		dB
SNR		VDD=4.2V, PVDD=8.5V, Po=4.1W, Av=8V/V, THD+N=1%, Rl=8ohm		103		dB
En	Speaker output noise	Av=16V/V, 20Hz to 20kHz, A-weighting		38		uV
		Av=8V/V, 20Hz to 20kHz, A-weighting		33		uV
	Receiver output noise	Av=1V/V, 20Hz to 20kHz, A-weighting				uV
Av	Speaker max gain			27		dB
Rin	Speaker input resistor	Av=0V/V		3		kohm
		Av=8V/V		5		kohm
THD+N		VDD=4.2V, Po=0.6W， Rl=8ohm, f=1kHz, PVDD=8.5V		0.003		%
Po	output power	THD+N=1%, Rl=8ohm, VDD=4.2V, PVDD=6.5V		2		W
ClassAB reciver mode						
Vos	output offset voltage		-500		500	uV
Efficiency	Boost+ClassAB total efficiency	VDD=4.2V, Rl=8ohm, Po=0.5W, THD+N=-94dB		54		%
	Receiver quiecent current			9.6		mA
PSRR		VDD=4.2V, Vpp-sin=300mV, 217Hz		-90		dB
		VDD=4.2V, Vpp-sin=300mV, 1kHz		-92		dB
SNR		VDD=4.2V, PVDD=8.5V, Po=4.1W, Av=8V/V, THD+N=1%, Rl=8ohm		105		dB
En	Receiver output noise	Av=1V/V, 20Hz to 20kHz, A-weighting		9		uV
Av	Receiver gain			0		dB
Rin	Speaker input resistor	Av=0V/V		3		kohm
		Av=8V/V		5		kohm
THD+N		VDD=4.2V, Po=0.6W， Rl=8ohm, f=1kHz, PVDD=8.5V		0.003		%
Po	output power	THD+N=1%, Rl=8ohm, VDD=4.2V, PVDD=6.5V		0.58		W

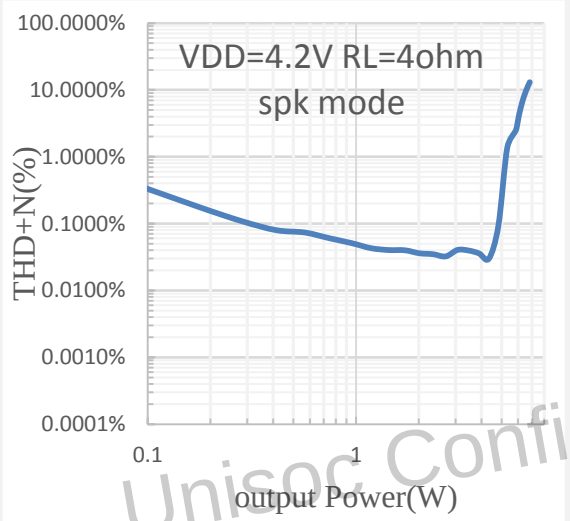
6.2.2 Typical characteristics

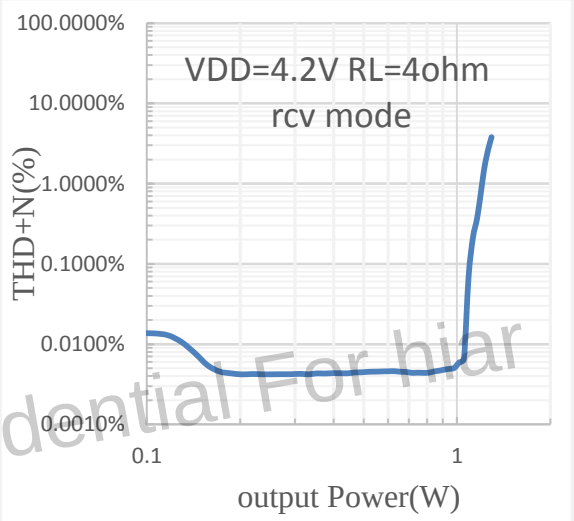


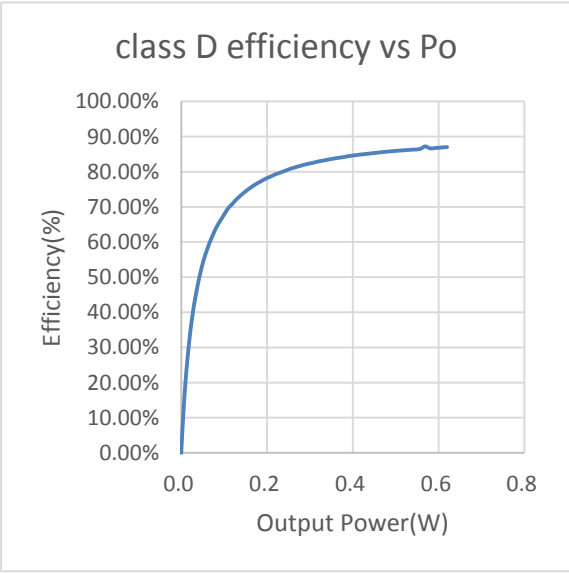


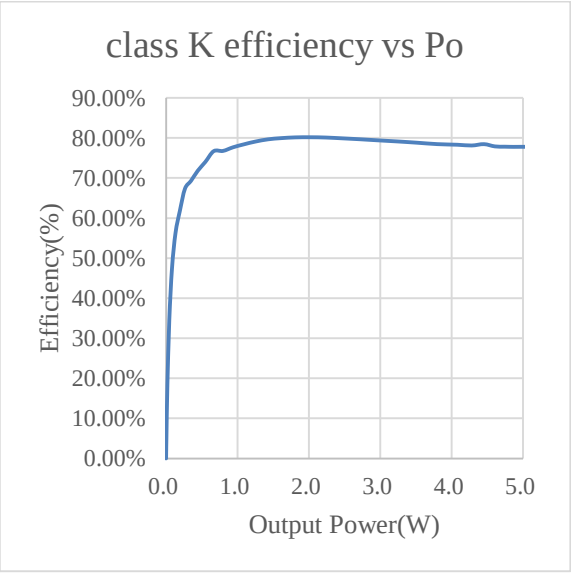


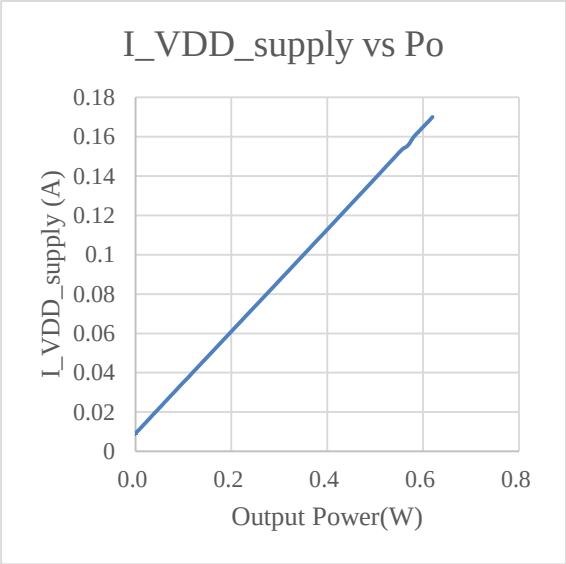


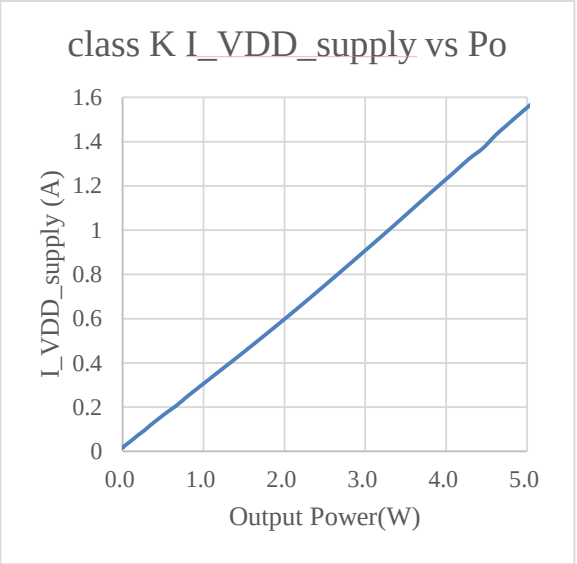


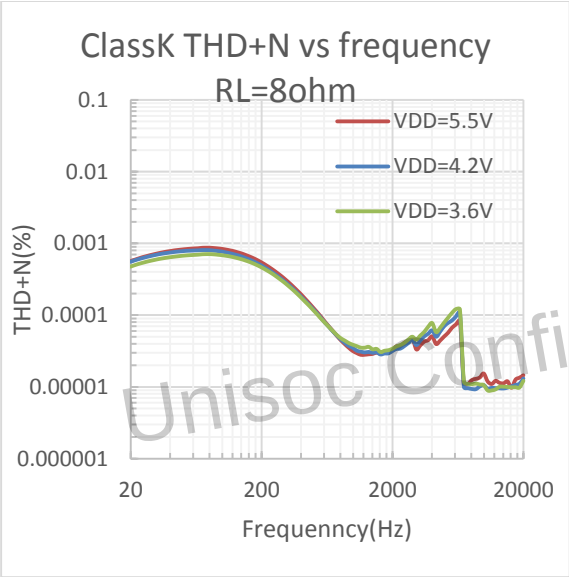


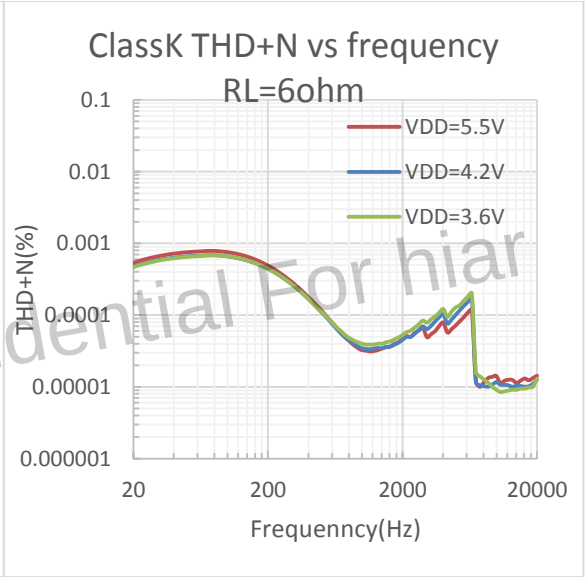


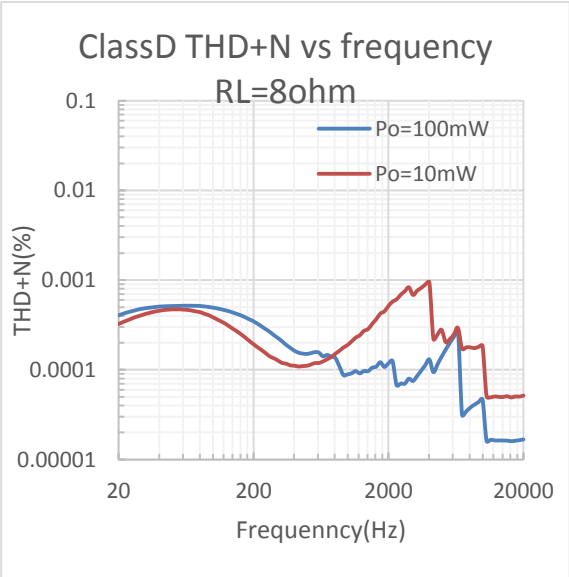


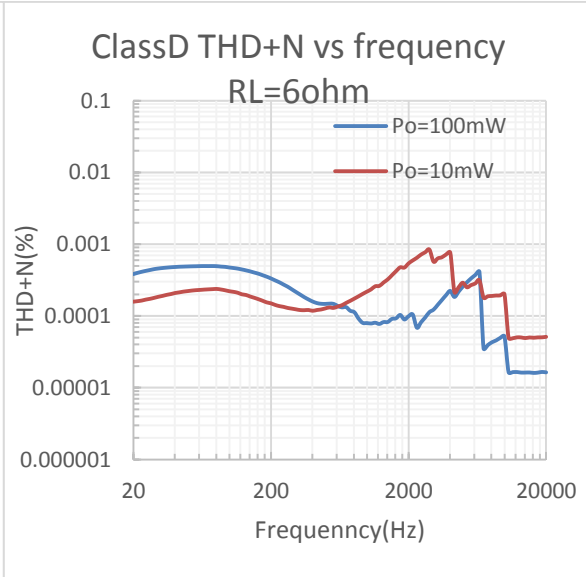


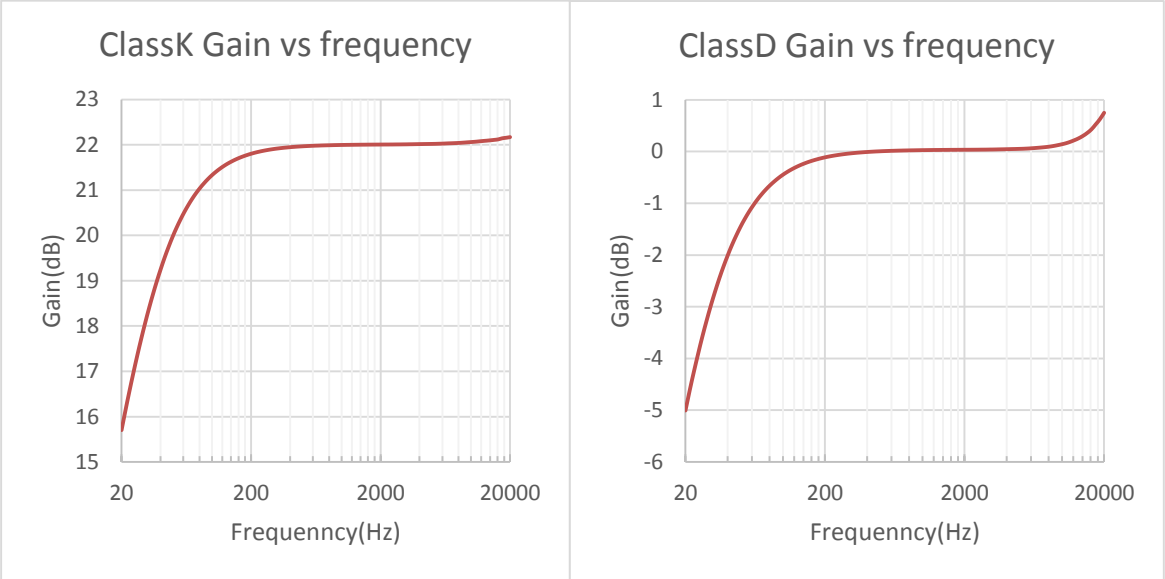












6.2.3 Over current protect

When the current of Class-D&Class-AB power-MOS exceeds the setting value, OCP function will be active. System will power off immediately and reboot in 50ms to check the current of power-MOS .

6.3 IVsense

6.3.1 Overview

The IVSENSE is a low pass filter followed by a 15bit sigma-delta ADC for Class-D output signal test. It is used to form the smart PA.

6.3.2 Function description

The Isense filter has 12dB/18dB/24dB gain setting by 2bit register. The Vsense fitlter has -11dB/-14dB/-17dB gain setting by 2bit register. Both the filters are used to filter out-band noise of Audio signal, especially the Class-D modulation frequency at about 800KHz. The ADCs following the two filters are the copy of same design. It is a 15bit sigma-delta modulator in Audio band with 1bit data output.

6.3.3 Control registers

Offset	Regname	bit	Field name	r/w	reset value	description
0x000F	IV_SENSE_FILTER_REG0	[31:16]	Reserved	RO	16'h0	
		[15:13]	Reserved	RO	3'h0	
		[7:6]	RG_AUD_PA_VS_G	RW	2'h1	Select the Vsense's gain: 2'b0x; gain=-11dB; 2'b10; gain=-14dB; 2'b11; gain=-17dB;
		[5:4]	RG_AUD_PA_IS_G	RW	2'h1	Select the Isense's gain: 2'b00; gain=12dB; 2'b01; gain=18dB; 2'b1x; gain=24dB;

		[3]	RG_AUD_PA_SVSNSAD	RW	1'h0	Enable PA Vsense's input path switches 0: disable 1: enable
		[2]	RG_AUD_PA_SISNSAD	RW	1'h0	Enable PA Isense's input path switches 0: disable 1: enable
		[1]	RG_AUD_PA_VSNS_EN	RW	1'h0	Enable PA Vsense's opamp 0: disable 1: enable
		[0]	RG_AUD_PA_ISNS_EN	RW	1'h0	Enable PA Isense's opamp 0: disable 1: enable

7 Function Modules

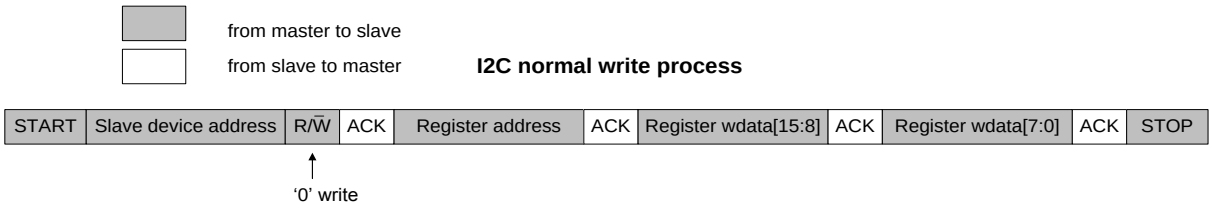
7.1 I2C

7.1.1 Feature

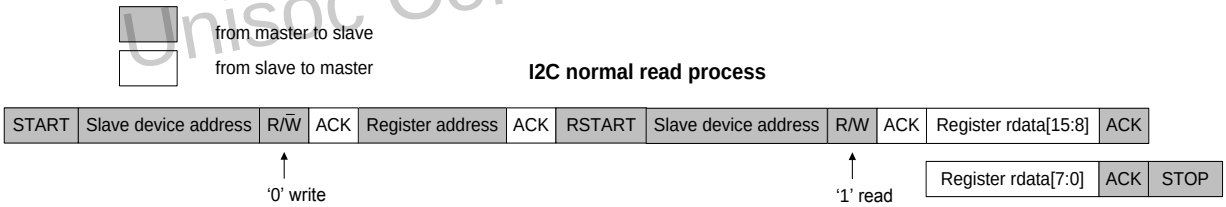
- I2C slave interface
- Two bus lines, a serial data line(SDA) and a serial clock line(SCL)
- 7bit slavedevice address (7'b1011000).
- Bus speed up to 400kbit/s (high speed mode)

7.1.2 Application Notes

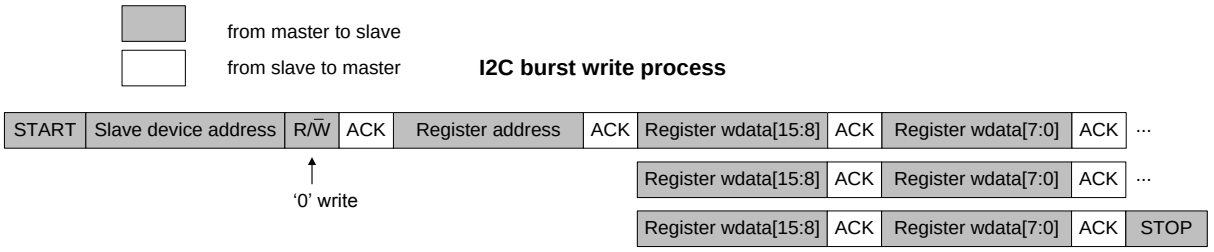
Normal write: master transfers a 16-bitdata written to the corresponding 8-bits register address.



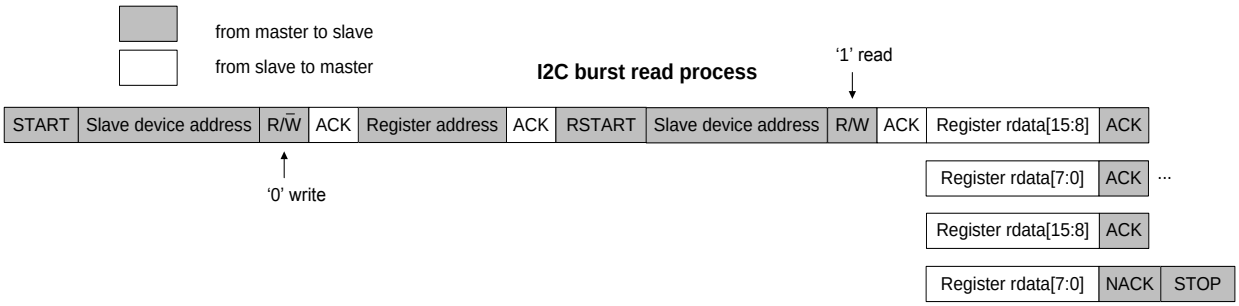
Normal read: master receives a 16-bit data read from the corresponding 8-bits register address.



Burst write: master transfers several 16-bitdata written to the corresponding 8-bits register addresses, each ACK will automatically increase the register address by 1.



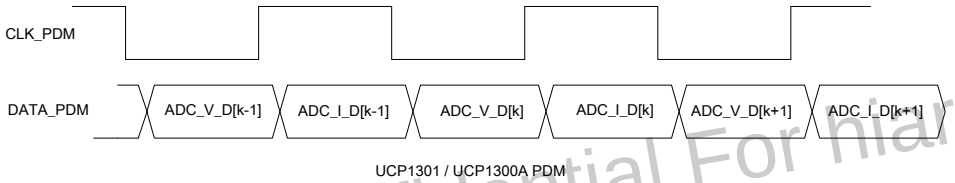
Burst read: master receives several 16-bit data readfrom the corresponding 8-bits register addresses, and each ACK will automatically increase the register address by 1.



7.2 PDM

7.2.1 Feature

- PDM interface for IV sensing feedback
- Double Data Rate.



7.2.2 Control registers

IVsens controller base address: 0x0F ~ 0x11

0x000F	IV_SENSE_FILTER_REG0	IV_SENSE_FILTER_REG0
0x0010	IV_SENSE_ADC_REG0	IV_SENSE_ADC_REG0
0x0011	IV_SENSE_ADC_REG1	IV_SENSE_ADC_REG1

7.2.2.1 IV_SENSE_FILTER_REG0

0x0000000F			IV_SENSE_FILTER_REG0(0x00000850)									IV_SENSE_FILTER_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RG_AUD_SP_VCMO_S		RG_AUD_PA_	RG_AUD_PA_	Reserved	RG_AUD_PA_VS_G		RG_AUD_PA_IS_G		RG_AUD_PA_	RG_AUD_PA_	RG_AUD_PA_	RG_AUD_PA_I

						SP_CHOP_VSEN	SP_CHOP_ISEN						SVSNSAD	SISNSAD	VSNS_EN	SNS_EN
Type	RO			RW		RW	RW	RO	RW		RW		RW	RW	RW	RW
Reset	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0

IV_SENSE_FILTER_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 13]	RO	NA	0	
RG_AUD_SP_VCMO_S	[12: 11]	RW	NA	0x1	Sellect I/Vsense output VCM: 2'b00; 0.5*AVDD_VB; 2'b01; 0.45*AVDD_VB; 2'b10; 0.425*AVDD_VB; 2'b11; 0.4*AVDD_VB;
RG_AUD_PA_SP_CHOP_VSEN	[10]	RW	NA	0	Enable PA Vsense's CHOP function 0: disable 1: enable
RG_AUD_PA_SP_CHOP_ISEN	[9]	RW	NA	0	Enable PA Isense's CHOP function 0: disable 1: enable
reserved	[8]	RO	NA	0	
RG_AUD_PA_VS_G	[7: 6]	RW	NA	0x1	Sellect the Vsense's gain: 2'b0x; gain=-11dB; 2'b10; gain=-14dB; 2'b11; gain=-17dB;
RG_AUD_PA_IS_G	[5: 4]	RW	NA	0x1	Sellect the Isense's gain: 2'b00; gain=12dB; 2'b01; gain=18dB; 2'b1x; gain=24dB;
RG_AUD_PA_SVSNSAD	[3]	RW	NA	0	Enable PA Vsense's input path switches 0: disable 1: enable
RG_AUD_PA_SISNSAD	[2]	RW	NA	0	Enable PA Isense's input path switches 0: disable 1: enable
RG_AUD_PA_VSNS_EN	[1]	RW	NA	0	Enable PA Vsense's opamp 0: disable 1: enable
RG_AUD_PA_ISNS_EN	[0]	RW	NA	0	Enable PA Isense's opamp 0: disable

					1: enable

7.2.2.2 IV_SENSE_ADC_REG0

0x00000010			IV_SENSE_ADC_REG0(0x00000557)									IV_SENSE_ADC_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_AUD_ADPGA_IBIAS_EN	RG_AUD_VCM_VREF_BUF_EN	RG_AUD_VREF_SFCUR	RG_AUD_AD_DATA_INVERSE_V	RG_AUD_AD_DATA_INVERSE_I	RG_AUD_AD_CLK_RST_V	RG_AUD_AD_CLK_EN_V	RG_AUD_AD_CLK_RST_I	RG_AUD_AD_CLK_EN_I	RG_AUD_ADC_V_RST	RG_AUD_ADC_V_EN	RG_AUD_ADC_I_RST	RG_AUD_ADC_I_EN	RG_VB_EN	RG_AUD_AD_D_GATE_V	RG_AUD_AD_D_GATE_I
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1

IV_SENSE_ADC_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RG_AUD_ADPGA_IBIAS_EN	[15]	RW	NA	0	ADC bias enable 0: disable 1: enable
RG_AUD_VCM_VREF_BUF_EN	[14]	RW	NA	0	ADCI / ADCV vcm & vref buffer enable 0: disable 1: enable
RG_AUD_VREF_SFCUR	[13]	RW	NA	0	not used
RG_AUD_AD_DATA_INVERSE_V	[12]	RW	NA	0	ADCV output data inverse polarity 0: normal polarity 1: inverse polarity
RG_AUD_AD_DATA_INVERSE_I	[11]	RW	NA	0	ADCI output data inverse polarity 0: normal polarity 1: inverse polarity
RG_AUD_AD_CLK_RST_V	[10]	RW	NA	0x1	ADCV clock reset 0: reset uneffective 1: reset effective
RG_AUD_AD_CL	[9]	RW	NA	0	ADCV clock enable

K_EN_V					0: disable ADCR clock 1: enable ADCR clock
RG_AUD_AD_CLK_RST_I	[8]	RW	NA	0x1	ADCI clock reset 0: reset uneffective 1: reset effective
RG_AUD_AD_CLK_EN_I	[7]	RW	NA	0	ADCI clock enable 0: disable ADCL clock 1: enable ADCL clock
RG_AUD_ADC_V_RST	[6]	RW	NA	0x1	ADCV integrator reset 0: not reset 1: reset effect
RG_AUD_ADC_V_EN	[5]	RW	NA	0	ADCV enable 0: disable ADC 1: enable ADC
RG_AUD_ADC_I_RST	[4]	RW	NA	0x1	ADCI integrator reset 0: not reset 1: reset effect
RG_AUD_ADC_I_EN	[3]	RW	NA	0	ADCI enable 0: disable ADC 1: enable ADC
RG_VB_EN	[2]	RW	NA	0x1	ADC output data enable 0: disable adc output to 00 1: enable adc output
RG_AUD_AD_D_GATE_V	[1]	RW	NA	0x1	ADC V output data gating 0: no gating ADC output 1: ADC 2bit output gating to 01
RG_AUD_AD_D_GATE_I	[0]	RW	NA	0x1	ADC I output data gating 0: no gating ADC output 1: ADC 2bit output gating to 01

7.2.2.3 IV_SENSE_ADC_REG1

0x00000011			IV_SENSE_ADC_REG1(0x00000042)									IV_SENSE_ADC_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								RG_AUD_ADPGA_VCMI_V		RG_AUD_ADPGA_IBIAS_SEL				RG_AUD_DAC_I_ADJ	
Type	RO								RW		RW				RW	
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

IV_SENSE_ADC_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
RG_AUD_ADPGA_VCMI_V	[7: 6]	RW	NA	0x1	AD VCM select
RG_AUD_ADPGA_IBIAS_SEL	[5: 2]	RW	NA	0	AD and PGA bias current select IBIAS_SEL[3:2]=00, PGA bias current=10uA IBIAS_SEL[3:2]=01, PGA bias current=7.5uA IBIAS_SEL[3:2]=10/11, PGA bias current=5uA IBIAS_SEL[1:0]=00, ADC bias current=10uA IBIAS_SEL[1:0]=00, ADC bias current=7.5uA IBIAS_SEL[1:0]=10/11, ADC bias current=5uA
RG_AUD_DAC_I_ADJ	[1: 0]	RW	NA	0x2	not used

7.2.3 Application

Set “RG_AUD_AD_D_GATE_I”=0, and “RG_AUD_PA_ISNS_EN”=1 to enable I-sense data path.

Set “RG_AUD_AD_D_GATE_V”=0, and “RG_AUD_PA_VSNS_EN”=1 to enable V-sense data path.

7.3 Global Register

7.3.1 Register Address Map

Base address: 0x0000

Offset Addr	Name	Description
0x0002	MODULE_EN	MODULE_EN
0x0003	SOFT_RST	SOFT_RST
0x0004	PMU_REG0	PMU_REG0
0x0005	PMU_REG1	PMU_REG1
0x0006	PMU_RESERVED	PMU_RESERVED
0x0007	BST_REG0	BST_REG0
0x0008	BST_REG1	BST_REG1
0x0009	BST_REG2	BST_REG2
0x000A	BST_RESERVED	BST_RESERVED

0x000B	CLSD_REG0	CLSD_REG0
0x000C	CLSD_REG1	CLSD_REG1
0x000D	CLSAB_REG0	CLSAB_REG0
0x000E	CLS_RESERVED	CLS_RESERVED
0x000F	IV_SENSE_FILTER_REG0	IV_SENSE_FILTER_REG0
0x0010	IV_SENSE_ADC_REG0	IV_SENSE_ADC_REG0
0x0011	IV_SENSE_ADC_REG1	IV_SENSE_ADC_REG1
0x0012	RESERVED_REG0	RESERVED_REG0
0x001E	PDM_PH_SEL	PDM_PH_SEL
0x001F	Reserved	Reserved
0x0020	Reserved	Reserved
0x0021	Reserved	Reserved
0x0022	Reserved	Reserved
0x0023	Reserved	Reserved
0x0024	Reserved	Reserved
0x0025	Reserved	Reserved
0x0026	Reserved	Reserved
0x0027	Reserved	Reserved
0x0028	Reserved	Reserved
0x0029	Reserved	Reserved
0x002A	Reserved	Reserved
0x002B	Reserve	Reserve
0x002C	Reserve	Reserve
0x002D	Reserve	Reserve
0x002E	Reserve	Reserve
0x002F	AGC_EN	AGC_EN
0x0030	PIN_REG0	PIN_REG0
0x0031	PIN_REG1	PIN_REG1
0x0032	RESERVED_REG1	RESERVED_REG1

7.3.1.1 MODULE_EN

0x00000002			MODULE_EN(0x00000002)									MODULE_EN				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved													CLSD_ACTIVE	BST_ACTIVE	CHIP_EN
Type	RO													RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

MODULE_EN

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 3]	RO	NA	0	
CLSD_ACTIVE	[2]	RW	NA	0	classD module enable 0: Disable 1: Enable
BST_ACTIVE	[1]	RW	NA	0x1	boost module enable 0: Disable 1: Enable
CHIP_EN	[0]	RW	NA	0	chip enable 0: Disable 1: Enable

7.3.1.2 SOFT_RST

0x00000003			SOFT_RST(0x00000000)									SOFT_RST				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															SOFT_RST
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SOFT_RST

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

reserved	[15: 1]	RO	NA	0	
SOFT_RST	[0]	RW	NA	0	soft reset

7.3.1.3 PMU_REG0

0x00000004			PMU_REG0(0x000002B4)									PMU_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RG_PMU_OVLO_ENB	RG_PMU_OTP_ENB	RG_PMU_PWM_AUTOTRACK_EN	RG_PMU_PWM_BIT		RG_PMU_PWM_AMPL			RG_PMU_VBAT_DETECT_BIT		RG_PMU_AVDD_BIT		
Type	RO			RW	RW	RW	RW		RW			RW		RW		
Reset	0	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0

PMU_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 13]	RO	NA	0	
RG_PMU_OVLO_ENB	[12]	RW	NA	0	OVLO detect disable
RG_PMU_OTP_ENB	[11]	RW	NA	0	over-temperature protection disable 1'b0: default, OTP function enable 1'b1: OTP disable
RG_PMU_PWM_AUTOTRACK_EN	[10]	RW	NA	0	Triangle amplitude auto-tracking control 1'b0: auto-track vboost output voltage 1'b1: auto-track disable. Triangle amplitude controlled by register RG_PWM_AMPL[2:0]
RG_PMU_PWM_BIT	[9: 8]	RW	NA	0x2	PWM peak to peak voltage: 00:typical-400mV 01 : typical-200mV 10:typical 11: typical+200mV
RG_PMU_PWM_AMPL	[7: 5]	RW	NA	0x5	PWM peak to peak voltage: 000: 1.375V 001 : 1.5V

					010: 1.625V 011 : 1.75V 100: 1.875V 101 : 2V 110: 2.125V 111 : 2.25V Default3'b101
RG_PMU_VBAT_DETECT_BIT	[4: 3]	RW	NA	0x2	Gain protect voltage 00: Vbat=3.45V 01: Vbat=3.55V 10: Vbat=3.65V 11: Vbat=3.75V (default 2'b10)
RG_PMU_AVDD_BIT	[2: 0]	RW	NA	0x4	avdd output voltage: 000:3.08V 001 : 3.10V 010: 3.13V 011 : 3.17V 100: 3.20V 101 : 3.23V 110: 3.26V 111 : 3.29V Default3'b100

7.3.1.4 PMU_REG1

0x00000005			PMU_REG1(0x000001EF)									PMU_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			bst_votrim_sw_sel		pmu_osc1p6m_clsd_sw_sel						RG_PMU_OSC1P6M_CLSD_TRIM				
Type	RO			RW		RW						RW				
Reset	0	0	0	0		0						0	1	1	1	1

PMU_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 13]	RO	NA	0	
bst_votrim_sw_sel	[12]	RW	NA	0	1: select bst_votrim from normal register 0: select bst_votrim from normal efuse bit map

pmu_osc1p6m_clsd_sw_sel	[10]	RW	NA	0	1: select clsd_trim from normal register 0: select clsd_trim from normal efuse bit map
RG_PMU_OSC1P6M_CLSD_TRIM	[4: 0]	RW	NA	0xf	clock output frequency: 00000:100KHz 00001 : 200KHz 00010:300KHz 00011 :400KHz 00100: 500KHz 00101 :600KHz 00110:700KHz 00111:800KHz 01000: 900KHz 01001: 1MHz 01010: 1.1MHz 01011:1.2MHz 01100: 1.3MHz 01101: 1.4MHz 01110: 1.5MHz 01111: 1.6MHz 10000:1.7MHz 10001 :1.8MHz 10010:1.9MHz 10011 :2MHz 10100:2.1MHz 10101 2.2MHz 10110:2.3MHz 10111: 2.4MHz 11000:2.5MHz 11001:2.6MHz 11010: 2.7MHz 11011: 2.8MHz 11100: 2.9MHz 11101: 3MHz 11110: 3.1MHz 11111:3.2MHz Default5'b01111

7.3.1.5 PMU_RESERVED

0x00000006	PMU_RESERVED(0x00000000)											PMU_RESERVED				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PMU_RESERVED

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

7.3.1.6 BST_REG0

0x00000007	BST_REG0(0x00000000)											BST_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved	RG_BST_BYPASS	RG_BST_RC		RG_BST_OVP_ENB	RG_BST_NSR		RG_BST_LP	RG_BST_ISENSE		RG_BST_ILIMITP		RG_BST_ILIMIT		RG_BST_FPWM	RG_BST_ANTIRING_ENB
Type	RO	RW	RW		RW	RW		RW	RW		RW		RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BST_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
RG_BST_BYPASS	[14]	RW	NA	0	bypass mode 1'b0: default, boost mode 1'b1: bypass mode
RG_BST_RC	[13: 12]	RW	NA	0	compensator R 2'b00: default, 200kohm 2'b01: 2'b10: 2'b11:
RG_BST_OVP_ENB	[11]	RW	NA	0	over voltage protect 1'b0: default, with over voltage protect 1'b1: OVP disable
RG_BST_NSR	[10: 9]	RW	NA	0	Nside slew rate control 2'b00: default, x1 2'b01: x0.75 2'b10: x0.5 2'b11: x0.25
RG_BST_LP	[8]	RW	NA	0	low power mode 1'b0: default, normal mode 1'b1: low power mode
RG_BST_ISENSE	[7: 6]	RW	NA	0	current sense ratio 2'b00: default, 0.5ohm 2'b01: 2'b10: 2'b11:
RG_BST_ILIMITP	[5: 4]	RW	NA	0	current limit threshold for Pside

					2'b00: default, 1.5A 2'b01: 2A 2'b10: 2.5A 2'b11: 3A
RG_BST_ILIMIT	[3: 2]	RW	NA	0	peak current limit threshold 2'b00: default, 4A 2'b01: 4.2A 2'b10: 4.4A 2'b11: 4.6A
RG_BST_FPWM	[1]	RW	NA	0	force PWM mode 1'b0: default, PFM/PWM auto mode 1'b1: force PWM mode
RG_BST_ANTIRING_ENB	[0]	RW	NA	0	antiring function 1'b0: default, antiring enable 1'b1: antiring disable

7.3.1.7 BST_REG1

0x00000008	BST_REG1(0x00000580)											BST_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	RG_BST_VOTRIM				RG_BST_VOSEL				RG_BST_VL		RG_BST_VH		RG_BST_SLOPE		RG_BST_SHORT_ENB
Type	RO	RW				RW				RW		RW		RW		RW
Reset	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0

BST_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
RG_BST_VOTRIM	[14: 11]	RW	NA	0	PVDD output voltage trimming. 15.625mV/step 4'b1111: -15.625mV ~ 4'b1000: -125mV 4'b0111: +109.375mV

					~ 4'b0000: default, +0mV
RG_BST_VOSEL	[10: 7]	RW	NA	0xb	PVDD output voltage selection. 250mV/step 4'b1111: 9.5V ~ 4'b1100: 8.75V 4'b1011: default, 8.5V 4'b1010: 8.25V ~ 4'b0000: 5.75V
RG_BST_VL	[6: 5]	RW	NA	0	PFM lower threshold 2'b00: default, 0.65V 2'b01: 2'b10: 2'b11:
RG_BST_VH	[4: 3]	RW	NA	0	PFM upper threshold 2'b00: default, 0.7V 2'b01: 2'b10: 2'b11:
RG_BST_SLOPE	[2: 1]	RW	NA	0	slope compensation
RG_BST_SHORT_ENB	[0]	RW	NA	0	short protect 1'b0: default, with short protect 1'b1: short protect disable

7.3.1.8 BST_REG2

0x00000009			BST_REG2(0x00000000)									BST_REG2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											RG_BST_ZXOFFSET			RG_BST_ZXDET_ENB	RG_BST_WELLSEL_ENB
Type	RO											RW			RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BST_REG2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 5]	RO	NA	0	
RG_BST_ZXOFFSET	[4: 2]	RW	NA	0	zero cross offset
RG_BST_ZXDET_ENB	[1]	RW	NA	0	zero cross function disable
RG_BST_WELLSEL_ENB	[0]	RW	NA	0	auto well voltage selection

7.3.1.9 BST_RESERVED

0x0000000A			BST_RESERVED(0x00000000)									BST_RESERVED				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BST_RESERVED

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

7.3.1.10 CLSD_REG0

0x0000000B			CLSD_REG0(0x000082AB)									CLSD_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TIME_FOR_CLSD_CIN_FAST		TIME_BETWEEN_BST_CLSD		RG_ADC_CLK_DATA_ED	CLSD_DEPOP_TIME		Reserved	RG_CLSD_PCC_EN	RG_CLSD_DEADTIME		RG_CLSD_SLOPE		RG_CLSD_OCP		RG_CLSD_MODE_SEL

				GE												
Type	RW		RW		RW	RW		RO	RW		RW		RW		RW		RW	
Reset	1	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1

CLSD_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
TIME_FOR_CLSD_CIN_FAST	[15: 14]	RW	NA	0x2	time for clsd cin fast: 00: 10ms 01: 15ms 10: 20ms 11: 25ms
TIME_BETWEEN_BST_CLSD	[13: 12]	RW	NA	0	time between boost en and clsd en: 00: 1ms 01: 1.5ms 10: 2ms 11: 3ms
RG_ADC_CLK_DATA_EDGE	[11]	RW	NA	0	undifined function bit
CLSD_DEPOP_TIME	[10: 9]	RW	NA	0x1	depop step time,00:20us,01:30us;10:40us;11:50us
reserved	[8]	RO	NA	0	
RG_CLSD_PCC_EN	[7]	RW	NA	0x1	enable bit of pcc, enable when 1, disable when 0.
RG_CLSD_DEADTIME	[6: 5]	RW	NA	0x1	classD outstage control deadtime,00,01,10,11-]increasing the deadtime
RG_CLSD_SLOPE	[4: 3]	RW	NA	0x1	classD output slope selection;00,01,10,11-]increaing the slope.
RG_CLSD_OCP	[2: 1]	RW	NA	0x1	classD over current protect point selction; 00,01,10,11 increasing the threshold of OCP.
RG_CLSD_MODE_SEL	[0]	RW	NA	0x1	mode selection of classd: spk mode when 1,reciver mode when 0.

7.3.1.11 CLSD_REG1

0x0000000C			CLSD_REG1(0x00000004)									CLSD_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Name	Reserved										READ_ADC_FLAG_DLY			READ_CLSD_FLAG_DLY		
Type	RO										RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

CLSD_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 6]	RO	NA	0	
READ_ADC_FLAG_DLY	[5: 3]	RW	NA	0	ADC calibration flag delay 000: 20us 001: 100us 010: 200us 011: 300us …… 111: 700us
READ_CLSD_FLAG_DLY	[2: 0]	RW	NA	0x4	classD calibration flag delay 000: 20us 001: 100us 010: 200us 011: 300us …… 111: 700us

7.3.1.12 CLSAB_REG0

0x0000000D			CLSAB_REG0(0x00000000)									CLSAB_REG0				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved										RG_CLSAB_OCP_S	RG_CLSAB_OCP_PD	RG_CLSAB_IB		RG_CLSAB_RSTN	RG_CLSAB_MODE_EN
Type	RO										RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLSAB_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 6]	RO	NA	0	
RG_CLSAB_OCP_S	[5]	RW	NA	0	ClassAB over current protect point selction; 0,1 increasing the threshold of OCP.
RG_CLSAB_OCP_PD	[4]	RW	NA	0	ClassAB over current protect circuit power down signal 0 = power up 1 = power down
RG_CLSAB_IB	[3: 2]	RW	NA	0	ClassAB bias current decreasing level for less Quiescent current 00 = Ib x 4/4 01 = Ib x 4/6 10 = Ib x 4/8 11 = Ib x 4/10
RG_CLSAB_RSTN	[1]	RW	NA	0	
RG_CLSAB_MODE_EN	[0]	RW	NA	0	

7.3.1.13 CLS_RESERVED

0x0000000E			CLS_RESERVED(0x00000000)									CLS_RESERVED				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLS_RESERVED

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

7.3.1.14 IV_SENSE_FILTER_REG0

0x0000000F	IV_SENSE_FILTER_REG0(0x00000850)	IV_SENSE_FILTER_REG0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			RG_AUD_SP_VCMO_S		RG_AUD_PA_SP_CHOP_VSEN	RG_AUD_PA_SP_CHOP_ISEN	Reserved	RG_AUD_PA_VS_G		RG_AUD_PA_IS_G		RG_AUD_PA_SVSNSAD	RG_AUD_PA_SISNSAD	RG_AUD_PA_VSNS_EN	RG_AUD_PA_ISNS_EN
Type	RO			RW		RW	RW	RO	RW		RW		RW	RW	RW	RW
Reset	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0

IV_SENSE_FILTER_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 13]	RO	NA	0	
RG_AUD_SP_VCMO_S	[12: 11]	RW	NA	0x1	Select I/Vsense output VCM: 2'b00; 0.5*AVDD_VB; 2'b01; 0.45*AVDD_VB; 2'b10; 0.425*AVDD_VB; 2'b11; 0.4*AVDD_VB;
RG_AUD_PA_SP_CHOP_VSEN	[10]	RW	NA	0	Enable PA Vsense's CHOP function 0: disable 1: enable
RG_AUD_PA_SP_CHOP_ISEN	[9]	RW	NA	0	Enable PA Isense's CHOP function 0: disable 1: enable
reserved	[8]	RO	NA	0	
RG_AUD_PA_VS_G	[7: 6]	RW	NA	0x1	Select the Vsense's gain: 2'b0x; gain=-11dB; 2'b10; gain=-14dB; 2'b11; gain=-17dB;
RG_AUD_PA_IS_G	[5: 4]	RW	NA	0x1	Select the Isense's gain: 2'b00; gain=12dB; 2'b01; gain=18dB; 2'b1x; gain=24dB;
RG_AUD_PA_SVSNSAD	[3]	RW	NA	0	Enable PA Vsense's input path switches 0: disable

					1: enable
RG_AUD_PA_SISNSAD	[2]	RW	NA	0	Enable PA Isense's input path switches 0: disable 1: enable
RG_AUD_PA_VSNS_EN	[1]	RW	NA	0	Enable PA Vsense's opamp 0: disable 1: enable
RG_AUD_PA_ISNS_EN	[0]	RW	NA	0	Enable PA Isense's opamp 0: disable 1: enable

7.3.1.15 IV_SENSE_ADC_REG0

0x00000010			IV_SENSE_ADC_REG0(0x00000557)									IV_SENSE_ADC_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_AUD_ADPGA_IBIAS_EN	RG_AUD_VCM_VREF_BUF_EN	RG_AUD_VREF_SFCUR	RG_AUD_AD_DATA_INVERSE_V	RG_AUD_AD_DATA_INVERSE_I	RG_AUD_AD_CLK_RST_V	RG_AUD_AD_CLK_EN_V	RG_AUD_AD_CLK_RST_I	RG_AUD_AD_CLK_EN_I	RG_AUD_ADC_V_RST	RG_AUD_ADC_V_EN	RG_AUD_ADC_I_RST	RG_AUD_ADC_I_EN	RG_VB_EN	RG_AUD_AD_D_GATE_V	RG_AUD_AD_D_GATE_I
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1

IV_SENSE_ADC_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RG_AUD_ADPGA_IBIAS_EN	[15]	RW	NA	0	ADC bias enable 0: disable 1: enable
RG_AUD_VCM_VREF_BUF_EN	[14]	RW	NA	0	ADCI / ADCV vcm & vref buffer enable 0: disable 1: enable
RG_AUD_VREF_SFCUR	[13]	RW	NA	0	not used
RG_AUD_AD_DA	[12]	RW	NA	0	ADCV output data inverse polarity

TA_INVERSE_V					0: normal polarity 1: inverse polarity
RG_AUD_AD_DATA_INVERSE_I	[11]	RW	NA	0	ADCI output data inverse polarity 0: normal polarity 1: inverse polarity
RG_AUD_AD_CLK_RST_V	[10]	RW	NA	0x1	ADCV clock reset 0: reset uneffective 1: reset effective
RG_AUD_AD_CLK_EN_V	[9]	RW	NA	0	ADCV clock enable 0: disable ADCR clock 1: enable ADCR clock
RG_AUD_AD_CLK_RST_I	[8]	RW	NA	0x1	ADCI clock reset 0: reset uneffective 1: reset effective
RG_AUD_AD_CLK_EN_I	[7]	RW	NA	0	ADCI clock enable 0: disable ADCL clock 1: enable ADCL clock
RG_AUD_ADC_V_RST	[6]	RW	NA	0x1	ADCV integrator reset 0: not reset 1: reset effect
RG_AUD_ADC_V_EN	[5]	RW	NA	0	ADCV enable 0: disable ADC 1: enable ADC
RG_AUD_ADC_I_RST	[4]	RW	NA	0x1	ADCI integrator reset 0: not reset 1: reset effect
RG_AUD_ADC_I_EN	[3]	RW	NA	0	ADCI enable 0: disable ADC 1: enable ADC
RG_VB_EN	[2]	RW	NA	0x1	ADC output data enable 0: disable adc output to 00 1: enable adc output
RG_AUD_AD_D_GATE_V	[1]	RW	NA	0x1	ADC V output data gating 0: no gating ADC output 1: ADC 2bit output gating to 01
RG_AUD_AD_D_GATE_I	[0]	RW	NA	0x1	ADC I output data gating 0: no gating ADC output 1: ADC 2bit output gating to 01

7.3.1.16 IV_SENSE_ADC_REG1

0x00000011			IV_SENSE_ADC_REG1(0x00000042)									IV_SENSE_ADC_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								RG_AUD_ADPGA_VCMI_V		RG_AUD_ADPGA_IBIAS_SEL				RG_AUD_DAC_I_ADJ	
Type	RO								RW		RW				RW	
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

IV_SENSE_ADC_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
RG_AUD_ADPGA_VCMI_V	[7: 6]	RW	NA	0x1	AD VCM select
RG_AUD_ADPGA_IBIAS_SEL	[5: 2]	RW	NA	0	AD and PGA bias current select IBIAS_SEL[3:2]=00, PGA bias current=10uA IBIAS_SEL[3:2]=01, PGA bias current=7.5uA IBIAS_SEL[3:2]=10/11, PGA bias current=5uA IBIAS_SEL[1:0]=00, ADC bias current=10uA IBIAS_SEL[1:0]=00, ADC bias current=7.5uA IBIAS_SEL[1:0]=10/11, ADC bias current=5uA
RG_AUD_DAC_I_ADJ	[1: 0]	RW	NA	0x2	not used

7.3.1.17 RESERVED_REG0

0x00000012		RESERVED_REG0(0x0000FF00)									RESERVED_REG0				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_RESERVED0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

RESERVED_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RG_RESERVED0	[15: 0]	RW	NA	0xff00	reserve bits [0]: oscillator test en. Reuse INN/INP for CLK_1P6M_DIG/CLK_1P6M_CLAS calibration. [2:1]: Boost current sense compensator adjust. [3]: pmu ana_test_en. [7:4]: internal AVDD32 calibration [15:8]: POR reset flag

7.3.1.18 PDM_PH_SEL

0x0000001E			PDM_PH_SEL(0x00000000)									PDM_PH_SEL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							BST_OVP_FLAG_CLR	BST_OVP_FLAG	BST_OCP_FLAG_CLR	BST_OCP_FLAG	IDETECT_FLAG_CLR	IDETECT_FLAG	OTP_FLAG_CLR	OTP_FLAG	PDM_PH_SEL
Type	RO							WC	RO	WC	RO	WC	RO	WC	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PDM_PH_SEL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
BST_OVP_FLAG_CLR	[8]	WC	NA	0	0: no effect 1: clean BST_OVP flag
BST_OVP_FLAG	[7]	RO	NA	0	0: no BST OVP 1: BST_OVP
BST_OCP_FLAG_CLR	[6]	WC	NA	0	0: no effect 1: clean BST_OCP flag
BST_OCP_FLAG	[5]	RO	NA	0	0: no BST_OCP

					1: BST_OCP
IDETECT_FLAG_CLR	[4]	WC	NA	0	0: no effect 1: clean IDETECT flag
IDETECT_FLAG	[3]	RO	NA	0	0: no IDETECT 1: IDETECT
OTP_FLAG_CLR	[2]	WC	NA	0	0: no effect 1: clean OTP flag
OTP_FLAG	[1]	RO	NA	0	0: no OTP 1: OTP
PDM_PH_SEL	[0]	RW	NA	0	PDM_PH_SEL 1:inv select ivsen @ posedge and negedge pdm-clk

7.3.1.19 AGC_EN

0x0000002F			AGC_EN(0x00000000)									AGC_EN				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															AGC_EN
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AGC_EN

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 1]	RO	NA	0	
AGC_EN	[0]	RW	NA	0	AGC enable

7.3.1.20 PIN_REG0

0x00000030			PIN_REG0(0x000011CC)									PIN_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Name								SCL_FUNC_DRV		SCL_WPU	SCL_WPDO	SDA_FUNC_DRV		SDA_WPU	SDA_WPDO
Type								RW		RW	RW	RW		RW	RW
Reset								1	1	0	0	1	1	0	0

PIN_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description(IO Voltage=1.8V)
reserved	[31: 16]	RO	NA	0	
SCL_FUNC_DRV	[7: 6]	RW	NA	0x3	SCL pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
SCL_WPU	[5]	RW	NA	0	SCL pad pull up enable 0: disable 1: enable
SCL_WPDO	[4]	RW	NA	0	SCL pad pull down enable 0: disable 1: enable
SDA_FUNC_DRV	[3: 2]	RW	NA	0x3	SDA pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
SDA_WPU	[1]	RW	NA	0	SDA pad pull up enable 0: disable 1: enable
SDA_WPDO	[0]	RW	NA	0	SDA pad pull down enable 0: disable 1: enable

7.3.1.21 PIN_REG1

0x00000031			PIN_REG1(0x000000CC)									PIN_REG1				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INP_FUNC_DRV		INP_W	INP_WPD	INN_FUNC_DRV		INN_W	INN_WPD	CLK_PDM_FUNC_DR		CLK_PD	CLK_PD	DATA_PDM_FUNC_		DATA_PD	DATA_PD

			PU	O			PU	O	V		M_WPU	M_WPDO	DRV		M_WPU	M_WPDO
Type	RW		RW	RW	RW		RW	RW	RW		RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0

PIN_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description(IO Voltage=1.8V)
reserved	[31: 16]	RO	NA	0	
INP_FUNC_DRV	[15: 14]	RW	NA	0	INP pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
INP_WPU	[13]	RW	NA	0	INP pad pull up enable 0: disable 1: enable
INP_WPDO	[12]	RW	NA	0	INP pad pull down enable 0: disable 1: enable
INN_FUNC_DRV	[11: 10]	RW	NA	0	INN pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
INN_WPU	[9]	RW	NA	0	INN pad pull up enable 0: disable 1: enable
INN_WPDO	[8]	RW	NA	0	INN pad pull down enable 0: disable 1: enable
CLK_PDM_FUNC_DRV	[7: 6]	RW	NA	0x3	CLK_PDM pad driving select 00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
CLK_PDM_WPU	[5]	RW	NA	0	CLK_PDM pad pull up enable 0: disable 1: enable
CLK_PDM_WPDO	[4]	RW	NA	0	CLK_PDM pad pull down enable 0: disable 1: enable
DATA_PDM_FUN	[3: 2]	RW	NA	0x3	DATA_PDM pad driving select

C_DRV					00: 0.4mA 01: 0.8mA 10: 1.2mA 11: 1.6mA
DATA_PDM_WPU	[1]	RW	NA	0	DATA_PDM pad pull up enable 0: disable 1: enable
DATA_PDM_WPDO	[0]	RW	NA	0	DATA_PDM pad pull down enable 0: disable 1: enable

7.3.1.22 RESERVED_REG1

0x00000032	RESERVED_REG1(0x0000FF00)											RESERVED_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RG_RESERVED1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

RESERVED_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RG_RESERVED1	[15: 0]	RW	NA	0xff00	reserve bits [0]: class D 3rd en [1]: class AB depop en [2]: class AB depop dg [3]: class D 3dB [4]: class AB 3dB [7]: bst ocp reboot enable [8]: class D AVG

8 Application Information

8.1 Feedback Resistor Rsense(R0) Selection

See the following table for reference

YAGEO	PE0805FRE470R1Z	100m ohm	1%	0.5W	0805

8.2 Input capacitor Selection

gain(dB)	Rin (k ohm)	gain(dB)	Rin (k ohm)	gain(dB)	Rin (k ohm)	gain(dB)	Rin (k ohm)
17	1.9	5.5	5.2	-6.0	10.0	-17.5	13.3
16.5	1.9	5.0	5.4	-6.5	10.2	-18.0	13.4
16	2.1	4.5	5.6	-7.0	10.4	-18.5	13.5
15.5	2.2	4.0	5.8	-7.5	10.6	-19.0	13.5
15	2.3	3.5	6.0	-8.0	10.8	-19.5	13.6
14.5	2.4	3.0	6.3	-8.5	10.9	-20.0	13.7
14	2.5	2.5	6.4	-9.0	11.1	-20.5	13.8
13.5	2.6	2.0	6.6	-9.5	11.3	-21.0	13.8
13	2.7	1.5	6.9	-10.0	11.4	-21.5	13.9
12.5	2.9	1.0	7.1	-10.5	11.6	-22.0	13.9
12	3.0	0.5	7.3	-11.0	11.7	-22.5	14.0
11.5	3.2	0.0	7.5	-11.5	11.9	-23.0	14.1
11	3.3	-0.5	7.7	-12.0	12.0	-23.5	14.1
10.5	3.4	-1.0	7.9	-12.5	12.2	-24.0	14.2
10	3.6	-1.5	8.1	-13.0	12.3	-24.5	14.2
9.5	3.8	-2.0	8.4	-13.5	12.4	-25.0	14.3
9	3.9	-2.5	8.6	-14.0	12.5	-25.5	14.3
8.5	4.1	-3.0	8.8	-14.5	12.7	-26.0	14.3
8	4.3	-3.5	9.0	-15.0	12.8	-26.5	14.4
7.5	4.4	-4.0	9.2	-15.5	12.9	-27.0	14.4
7	4.7	-4.5	9.4	-16.0	13.0	-27.5	14.5
6.5	4.8	-5.0	9.7	-16.5	13.1	-28.0	14.5
6	5.0	-5.5	9.8	-17.0	13.2		

If smart PA fuction is used, input capacitor is selected if 1uF;

If smart PA fuction is not used,input capacitor is not limited.

The -3dB frequency points of high pass filter is shown below:

$$f_H = \frac{1}{2*\pi*R_{in}*C_{in}} \text{(Hz)}$$

8.3 PCB and Device Layout Consideration

See the following items for PCB placement and layout notice:

- Put the chip UCP130x close to speaker connector
- Put the Rsense R0=0.1ohm, close to speaker connector
- Put the PVDD output capacitor close to PVDD pin
- Put the input capacitor close to INN/INP pins, with differential parallel trace
- The trace of inductor to SW pin should be as short as possible
- The current capability of trace width:
  BGND pin ~1.5A
  PVDD pin ~1A
  PGND pin ~1A
  VOP/VON pins ~2A
- The trace of VSENP/IVSENN/ISENN should be as short as possible, with differential parallel trace (The trace IVSENN should route between VSENP and ISENP)

8.4 Smart Amplifier Design Guide with Unisoc FB-*SmarAmp*™V3.0 algorithm

Overall

- Need speaker rear chamber sealing, Speaker+Box design is MUST
- Unisoc help on SPK music playback tuning(except for EQ). Need 5pcs~10pcs final speaker+box(housing) tuning
- Not suitable for PCBA shipping project
- For speaker front port design, +90 degree port is preferred
- For dual speakers design, recommend two speakers distance > 10cm with separated Boxes

■ Step1 – Select Speaker Vendors

- To select Unisoc approval vendor AVL is recommended
- To select speaker vendor which speaker parts is dedicated for Smart PA is MUST. (ex: AAC, Haosheng, Keysound, JIANGSU MIDI….etc)
- Provide speaker datasheet, and Xmax, Tmax, Tcoeff(alpha) parameters to Unisoc

■ Step2 – Speaker Box Design

- To Speaker Box Design is MUST, with leakage hole is preferred
- Ask speaker vendor to ship Speaker+Box is MUST
- Need to take antenna pattern into consideration
- Provide Speaker+Box samples 5pcs~10pcs to Unisoc

■ Step3 – HW SCH/PCB Design

- Contact with Unisoc for help and review

■ Step4 – Turn on FB-*SmarAmp*™V3.0 Algorithm

- Contact with Unisoc for help and review

■ Step5 – For Speaker 2nd Source

- All speaker's performance, TS parameters, Xmax, Tmax, Tcoeff(alpha), DC offset…etc need to be the same between main/second source
- To select Unisoc approval vendor AVL is recommended

- To select speaker vendor which speaker parts is dedicated for Smart PA is MUST. (ex: AAC, Haosheng, Keysound, JIANGSU MIDI….etc)

Step6 – MP Requirements

- For Alpha customer, if there is fail samples, Unisoc will help to check total phone performance and analyze first, both before/after MP
- Both for main/second source speaker components, need to meet the following spec. after MP:

1. F0 tolerance < +/-10%
2. Bl tolerance < +/- 10% (Bl is one TS parameter)
3. Re tolerance < +/-10% (Re is one TS parameter)
4. X DC offset tolerance < 0.1 x Xmax @ rated power
5. Xmax no tolerance, 100% all meet spec.
6. Tmax no tolerance, 100% all meet spec.
7. Tcoeff(alpha) should use the same material