

Change History



Version	Date	Change content	
V1.0	2020.2.5	First Version 121	
1.1.0	signs Confide	Sullai.	
UI	lisoc Co:		



- Overview hiar fidential For hiar
- 2 Thermal control architecture
- 3 PCB thermal design notes
- 4 Mechanical thermal design notes
- 5 Thermal test notes
- 6 TIM application notes

Overview



Main heat source showed as below, onfidential For hiar

- ➤ BB—UDS710
- ➤ Modem—UDX710
- > PMIC—UMP510G5
- > Modem PMIC SUMP510G5
- ➤ Charge IC
- >4G/3G/2G PA
- > NR PA
- > Transceiver—UMT710 , UMT710L
- >WCN—UMW2651
- > LCD backlight
- ➤ Camera flashlight

Thermal control architecture

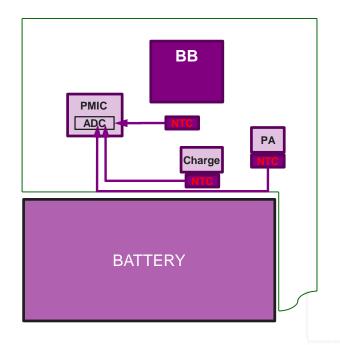


- Thermal management architecture For hiar
 Unisoc Continues For hiar

Thermal sensors



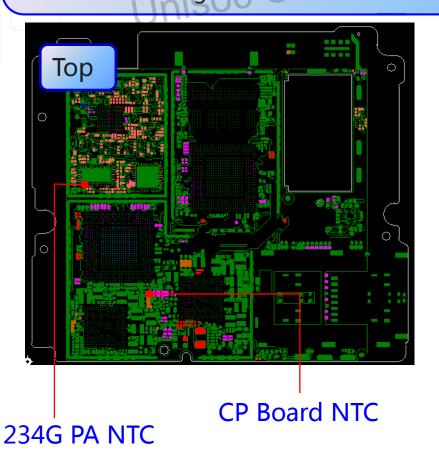
Thermal Sensor	Description	Range	Precision
CPU sensor	In BB sidential Fo	-40~125°C	+/- 2.5C @ 0~100C,
GPU Sensor	InBBNTIGETTION	-40~125°C	or else +/- 5C
Board Sensor	NTC on PCB middle area	-40~125°C	±5°C
PA sensor	NTC near PA	-40~125°C	±5°C
Charge sensor	NTC near charge IC	-40~125°C	±5°C

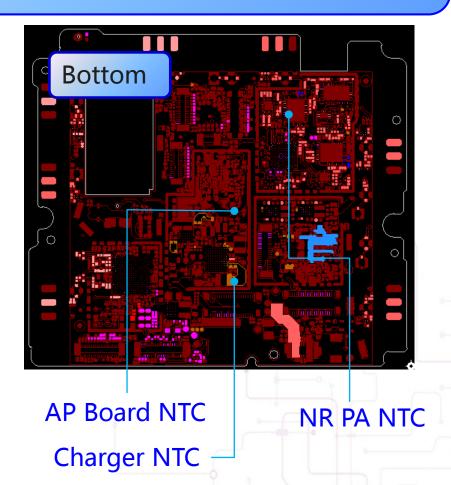


Thermal Sensors Placement - 1



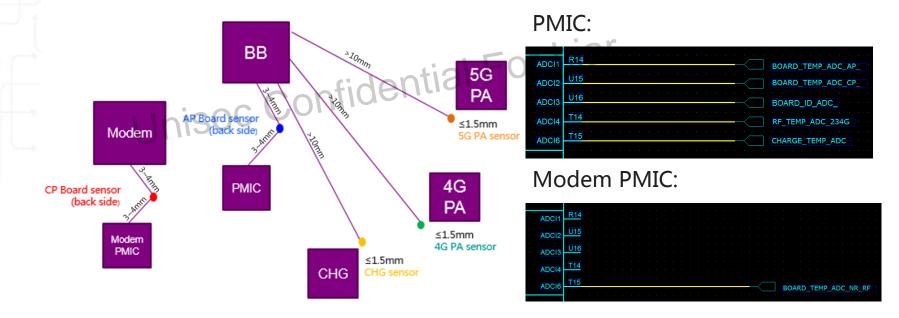
Strongly recommend Five thermal sensors(NTC) on the board, the first two is applied to monitor the board temperature of AP and CP part, the third one to monitor the Charger IC and the last two to monitor the 234G PA and NR PA.





Thermal Sensors Placement - 2

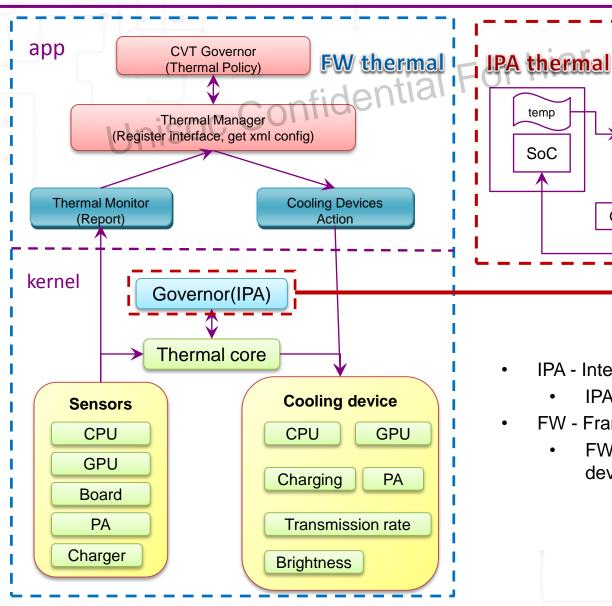


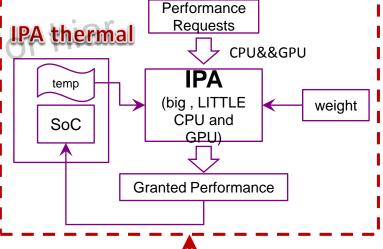


- > Shall strictly follow the NTC placement rules and ADC channel connect rules shown as above.
- The AP Board sensor is critical to the thermal management software algorithm, removing is prohibited. It shall be placed on the opposite side of BB and PMU.
- The CP Board sensor is recommended to be placed on between modem and modem PMIC. It shall be placed on the opposite side of modem.
- For the fast charging(>10W) or linear charging (<0.7A), the CHG sensor shall be placed within 1.5mm of CHG IC. For the switch charging(≥0.7A), the CHG sensor is recommended to be placed within 1.5mm of the switching IC to control the charging current precisely.
- The PA sensors monitors PAs temperature when PA power back-off is expected to be triggered. It shall be placed within 1.5mm of the PA. If there is no need to conduct modem thermal mitigation, the RF sensors(PA NTC) may be unpopulated.

Thermal Control architecture







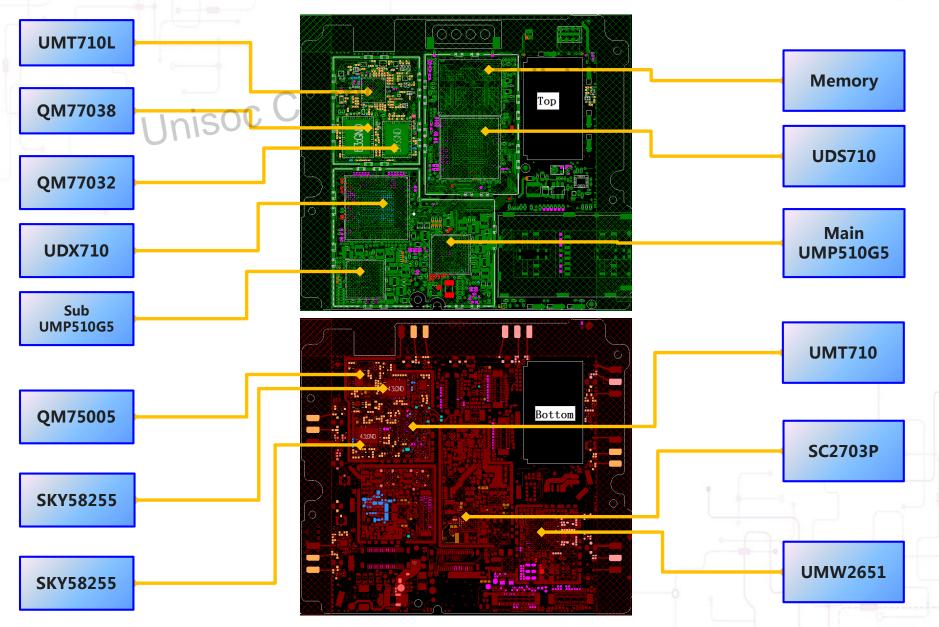
- IPA Intelligent power allocation
 - IPA thermal control CPU & GPU
- FW Framework
 - FW thermal control cooling devices in different scenarios



- Placement consideration dential For hiar
- Routing consideration
- Stack up consideration
- AP consideration
- **CP** consideration
- PA consideration
- PMIC and transceiver consideration
- Sensor consideration
- **TCXO** consideration

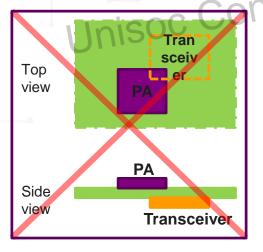
Recommended placement







Placement consideration

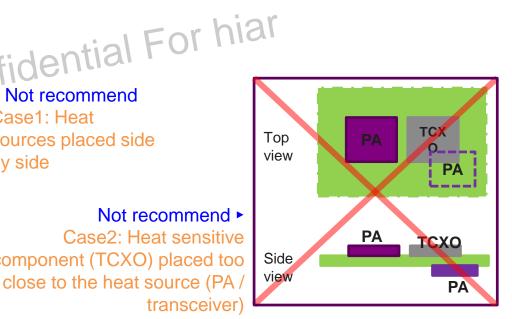


Not recommend

Case1: Heat sources placed side by side

Not recommend ▶

Case2: Heat sensitive component (TCXO) placed too close to the heat source (PA/ transceiver)



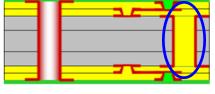
- PCB smaller than 2500mm² would have extreme high thermal risk. 3000mm² or larger is recommended to avoid high thermal risk.
- Heat source should keep away from board edge by 3mm at least.
- Heat source should keep away from each other by 5mm at least.



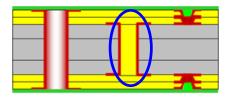
Routing consideration
 Confidential For hiar

➤ It is recommended to design buried via holes instead of blind via holes, with 0.25mm via diameter and ½ OZ plating thickness.

Buried Via:

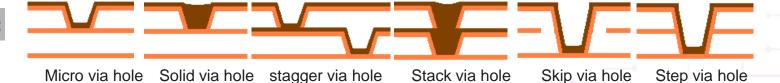






Through via Stack via

Blind Via:



PCB Stackup - 2: 12HDI-4 (4+4+4)



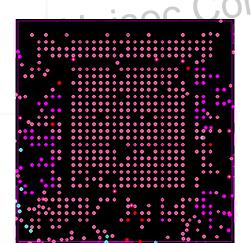
• The adjacent layer to power plane or traces must be a complete GND plane, that can reduce the effective inductance of PDN. The recommended stack-up is:

Layers S						ckness: 0.82				31	/F0 1	/0.0 I
Type		Drill				Permittivity	Loss tangant	Thickness after Process			(50ohms +/-10%)	(90ohms +/-10%)
GT P/N:	Structure		ıre	Material	(mil)			(mm)	Ref. layer	Line Width (um)	Line Width/ Spacing (um)	
								0.71	0.018			
Top		I			Cu			0.94	0.024	L2	86	83/92
	Ц	L			рр	3.4	0.009	1.93	0.049			
L2		L			Cu			0.75	0.019			
	Ц	L			рр	3.4	0.009	1.93	0.049			
L3	Ш	L	1		Cu			0.75	0.019	L2/L4	50	50/100
	Ш	L			рр	3.4	0.009	1.93	0.049			
L4		L			Cu			0.75	0.019			
	Ш	L			рр	3.4	0.009	1.93	0.049			
L5	Ш	L			Cu			0.75	0.019	L4/L6	50	51/99
	Ц	L	┸		рр	3.4	0.009	1.89	0.048			
L6	Ц	L			Cu			0.87	0.022			
	Ц	L			core	3.6	0.008	2.28	0.058			
L7	Ш	L			Cu			0.87	0.022			
	Ц	L			рр	3.4	0.009	1.89	0.048			
L8	Ш	L			Cu			0.75	0.019	L7/L9	50	52/98
	Ц	L			рр	3.4	0.009	1.93	0.049			
L9	Ц	L			Cu			0.75	0.019			
	Ц	L			рр	3.4	0.009	1.93	0.049			
L10	Ш	L			Cu			0.75	0.019	L9/L11	50	50/100
		L			рр	3.4	0.009	1.93	0.049			
L11		Ĺ			Cu			0.75	0.019			
		L			рр	3.4	0.009	1.93	0.049			
Bottom					Cu			0.94	0.024	L11	88	85/90
								0.71	0.018			
							Total :	32.52	0.826			

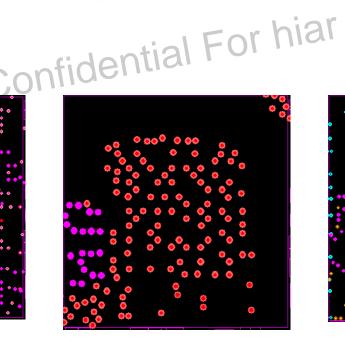
- UMS710 placement only supports the double sides. The minimum PCB stackup is 12HDI-4.
- GND, top and bottom layer thickness are no less than 0.5oz after planting.
- > 2 GND layers at least.
- Suggest bottom or bottom-1 layer is GND



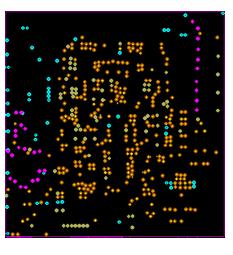
BB consideration



Via through L1~L5



Via through L5~L8

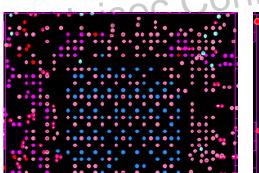


Via through L8~L12

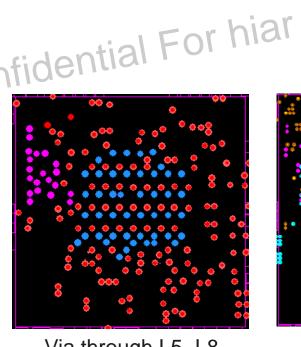
- ➤ Blind vias through L1~L5 no less than 450 pcs.
- ➤ Buried vias through L5~L8 no less than 140 pcs.
- ➤ Blind vias through L8~L12 no less than 350 pcs.
- Blind and buried vias should be well-distributed.
- Connect GND pad with trace narrow than pad size.



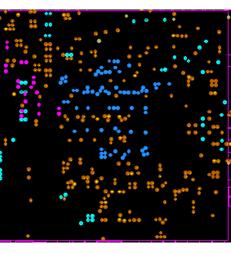
Modem consideration



Via through L1~L5



Via through L5~L8

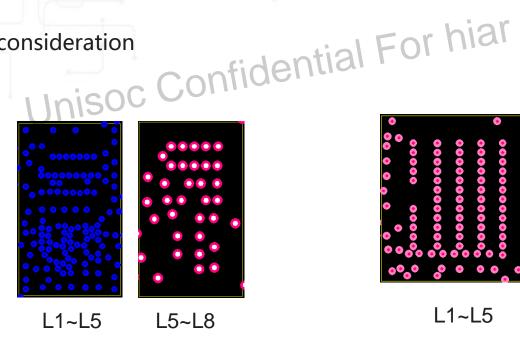


Via through L8~L12

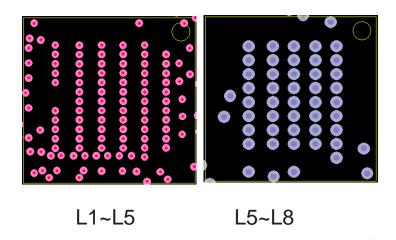
- ➤ Blind vias through L1~L5 no less than 450 pcs.
- ➤ Buried vias through L5~L8 no less than 140 pcs.
- ➤ Blind vias through L8~L12 no less than 350 pcs.
- Blind and buried vias should be well-distributed.
- Connect GND pad with trace narrow than pad size.



PA consideration



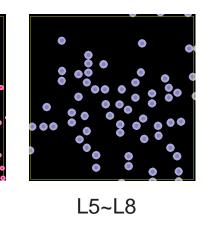
- Blind vias through L1~L3 no less than 65pcs.
- Buried vias through L3~L8 no less than 35pcs.



- Blind vias through L1~L3 no less than 75pcs.
- Buried vias through L3~L8 no less than 40pcs.
- The vias should be welldistributed.



PMIC and transceiver consideration For hiar UMP510G5 Included the consideration of the consid

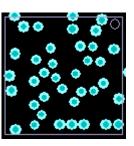


- ➤ L1~L3 blind vias no less than 80 pcs.
- ➤ L3~L8 buried vias no less than 32 pcs.

L1~L5

UMT710/UMT710L





L1~L5

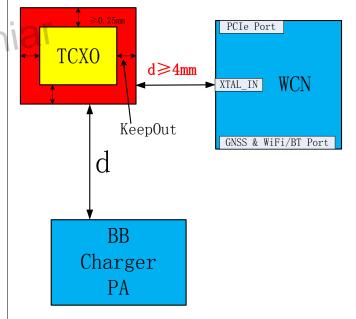
L5~L8

- ➤ L1~L3 blind vias no less than 60 pcs.
- ➤ L3~L8 buried vias no less than 37 pcs.
- The vias should be welldistributed.

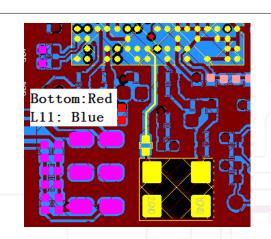


WCN TCXO Placement:

- TCXO shall be placed first inside the shielding case, Keep ≥1mm away from the PCB edge.
 Don' t refer to the PCB Main GND.
- Keep the TCXO ≥4mm away from the WCN at least. Keep the TCXO away from the PCIe port and GNSS & WiFi/BT port of the WCN chip.
- keep the TCXO≥15mm away from the heat sources on the same side(i.e., PA,BB and Charger).
- 4. keep the TCXO≥10mm away from the heat sources that on the opposite side (i.e., PA, BB and Charger). Don't place any heat sources(PMU etc.) directly on the opposite side of TCXO.
- keep out all TCXO components ≥0.25mm away from the surrounding metal.
- 6. TCXO PCB footprint with 4 pads is better than that with 6 pads for thermal isolation consideration.



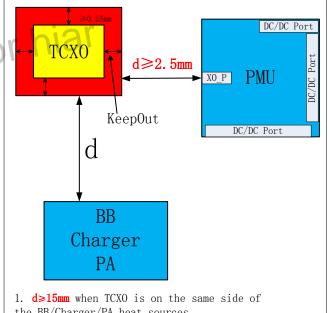
- 1. d≥15mm when TCXO is on the same side of the BB/Charger/PA heat sources.
- 2. $d \ge 10mm$ when TCXO is on the opposite side of the BB/Charger/PA heat sources .



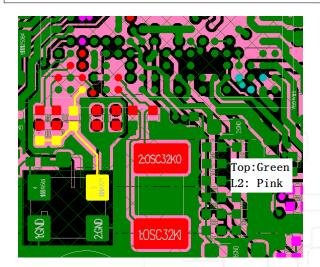


Main PMU TCXO Placement and layout guidelines! IniSOC

- 1. The main PMU TCXO only provides the system clock, rather than the GNSS clock.
- 2. Keep the TCXO ≥2.5mm away from the main PMU at least. Keep the TCXO away from the DC/DC ports of the PMU chip.
- 3. Except for the No.1 and No.2, all other placement and layout guidelines shall strictly follow the guidelines of the WCN TCXO placement and layout.



- the BB/Charger/PA heat sources.
- 2. d≥10mm when TCXO is on the opposite side of the BB/Charger/PA heat sources.





- Graphite sheet and heat pipe

 Camera consider
- Camera consideration
- Fingerprint module consideration
- Shielding can consideration
- Mechanical consideration



LED

Total thermal solution

UDS710/UDX710/PMIC

Thermal pad

Copper foil

Heat pipe

Graphite sheet

Copper foil

- ➤ Suggest to add metal frame between LCM and PCB.
- ➤ Suggest to add heat pipe on metal frame. Qmax should be better than 4.5W.
- ➤TIM must be applied between UDX710/UDS710 and heat pipe, K should be better than 3w/mk.
- ➤TIM must be applied between PMIC and shielding can, K should be better than 3w/mk.
- Consider to attach graphite sheet on back cover to cool down heat spot, K in x-y should better than 1500 w/mk.
- ➤ Strongly suggest to place LCM LED and PCB on opposite position.

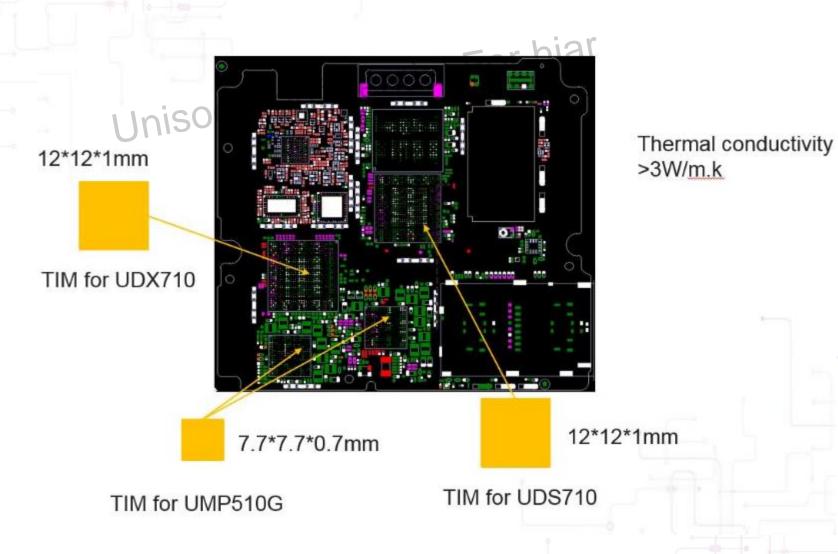




3raphite sheet thermal conductivity >1500W/m.k

Heat Pipe size 115*8*0.37mm, soldering to Al-Mg frame

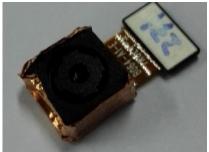






Camera consideration
 Unisoc Confidential For hiar





- ➤ Suggest to surround camera with copper foil, and attach it to metal frame with thermal pad.
- ➤ Suggest to use high efficiency LED as flash light and LCD backlight ,30% is preferred.

Thermal design notes



Fingerprint module consideration
 Unisoc Confidential For hiar





- Suggest to mount fingerprint module to back cover, and connect to PCB by S sharp FPC, it could prevent heat spread to back cover.
- ➤ Do not mount fingerprint module to PCB directly.

Thermal Test notes



- Recommended test procedure ntial For hiar
- Thermal debug procedure
- Thermal debug tool

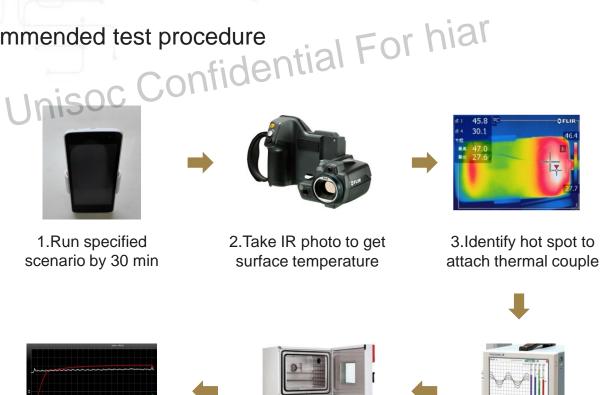


Recommended test equipment

Test Equipment	Model	Figure	Function	
Thermal chamber	BINDER KB-115- E3.1		Keep specified temperature	
Infrared camera	FLIR T420		Identify hot spot	
Data logger	YOKOGAWA GP10		Get accurate temperature curve	
Thermal couple	Omega TT-K-36-SLE		Attach to hot spot and connect to date logger	



Recommended test procedure



- 6.Log temperature curve changed with time
- 5. Put test phone into chamber and Keep specified temperature and still airflow
- 4.Connect thermal couple to data logger

Thermal Test notes



nisoc Confidential For hiar Thermal debug procedure Check scenario Adjust CPU Adjust Failed power, frequency charging backlight/camera case and cores current power Adjust Optimize Add thermal Final verify LCD system material performance backlight



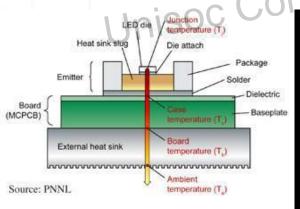
Unisoc Confidential For hiar Thermal debug tool Thermal tuner apk Manual adjust Auto adjust AP frequency Management parameter Current dynamic adjustment AP cores Charging current LCD brightness dynamic adjustment LCD brightness Log temperature sensor Log frequency and cores

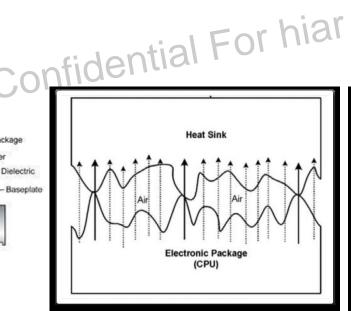


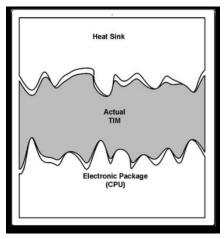
- TIM in Consumer Electronicsential For hiar
- Properties of TIM
- Thermal pad introduction
- Graphite sheet introduction
- Graphite sheet application examples
- Graphite sheet application notes
- Nano Silica Baloon Insulator
- Heat Pipe



TIM introduction







- ➤ Overheating is the most critical issue in the computer industry. It limits further miniaturization, power, performance and reliability.
- ➤ Various interfaces exist between high power, heat generating components and heat sinks.
- Sometimes, there will be only a small contact area between the two surfaces at this interface (sometimes as low as 3%), due to the micro-scale surface roughness. The surface irregularity is the primary cause of thermal contact resistance.
- Thermal interface materials are required to enhance the contact between the surfaces, and decrease thermal interfacial resistance.



Properties of TIM Confidential For hiar Phase								
Property	Tapes	Liquid Adhesives	Greases	Gels and Pastes	Elastomeric Pads	Phase Change Materials	Graphite	
Bulk Thermal Conductivity								
Low Interfacial Resistance								
Low Bond								
Line Thickness								
Application Precision								
Ease of Manufacture								
Longevity								
Reworkability								
Stress Relief								
Low cost								
		Excellent		Good		Moderate		

Poor



Thermal pad introduction

Thermal Pads die cut to a precise shape,

> ready for assembly.



Advantages

- ➤ Clean and easy to handle
- ➤ Can be die---cut in the precise shape needed for the application
- ➤ Simplifies assembly
- ➤ High conductivity
- ➤ High dielectric strength
- ➤ Gap Filling
- ➤ Naturally Tacky
- ➤ Soft/Outstanding compression performance

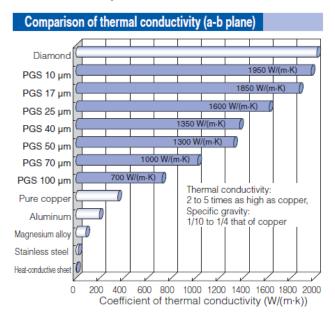
Disadvantages

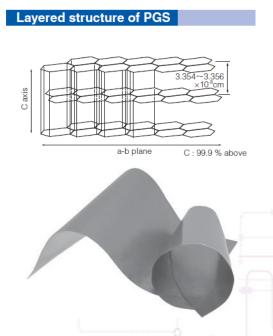
>To work effectively, thermal pads may require high clamping pressure



Graphite sheet introduction

nfidential For hiar PGS (Pyrolytic Graphite Sheet) is a thermal interface material which is very thin, synthetically made, has high thermal conductivity, and is made from a highly oriented graphite polymer film. It is ideal for providing thermal management/heatsinking in limited spaces or to provide supplemental heat-sinking in addition to conventional means. This material is flexible and can be cut into customizable shapes.

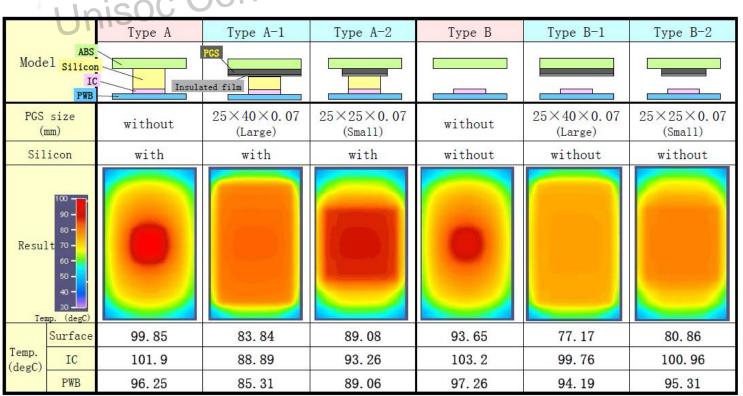






Graphite sheet application examples For hiar

Confidential For hiar



没有PGS石墨导热片时,发热源(IC)的温度在ABS表面上热量集中在一个点上。有PGS石墨导热片时,PGS石墨导热片聚集热量并使之扩散。

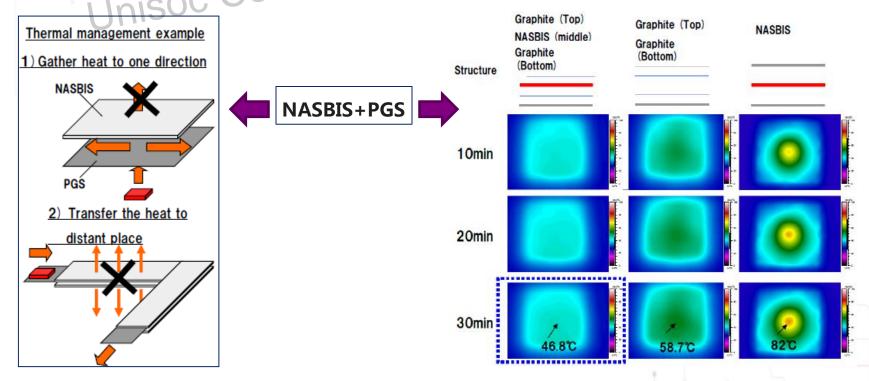
PGS石墨导热片根据目的不同(降低发热源的温度、降低表面温度)可以自由选择其构成。



- Graphite sheet application notes
 Unisoc Confidential For hiar
- Graphite sheet is soft, do not rub or touch it with rough materials to avoid scratching it.
- Lines or folds in the Graphite sheet may affect thermal conductivity.
- Graphite sheet has conductivity, should avoid to cover antenna zone.



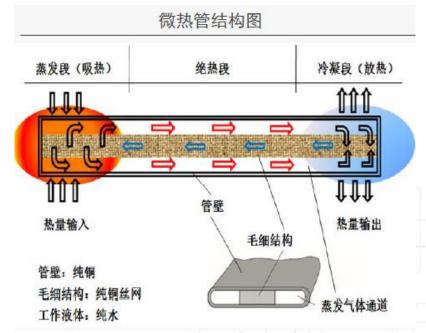
- Nano Silica Baloon Insulator
- itial For hiar Combining thermal insulation material with PGS enables thermal management in cellphone.





- Heat pipe
- Heat pipe is a passive heat conduction element with high performant Phase-change theory and capillarity, the heat conduction efficiently increase more than hundreds and thousands times than the pure copper of the same material.
- The wick structure for attract liquid distribute over the inner surface of heat pipe. The liquid is attracted back to the evaporate side by the capillary force of the wick.







THANKS







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