

distributed memory management unit

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graph TD; DMMU[distributed memory management unit] <--> P1[processor]; DMMU <--> P2[processor]; DMMU <--> P3[processor]; DMMU <--> P4[processor]; P1 <--> M1[memory]; P2 <--> M2[memory]; P3 <--> M3[memory]; P4 <--> M4[memory];
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The diagram illustrates a distributed memory management unit architecture. At the top, a single horizontal box labeled "distributed memory management unit" spans the width of the diagram. Below this box, there are four identical vertical stacks. Each stack consists of a "processor" box in the middle and a "memory" box at the bottom. A double-headed vertical arrow connects each processor to the distributed memory management unit above it, and another double-headed vertical arrow connects each processor to its respective memory box below it. This structure suggests that the management unit oversees multiple processors, each of which has its own dedicated local memory.

processor

processor

processor

processor

memory

memory

memory

memory