Bachelor's Thesis Project

The Design of Discrete Time Delta-Sigma Modulators

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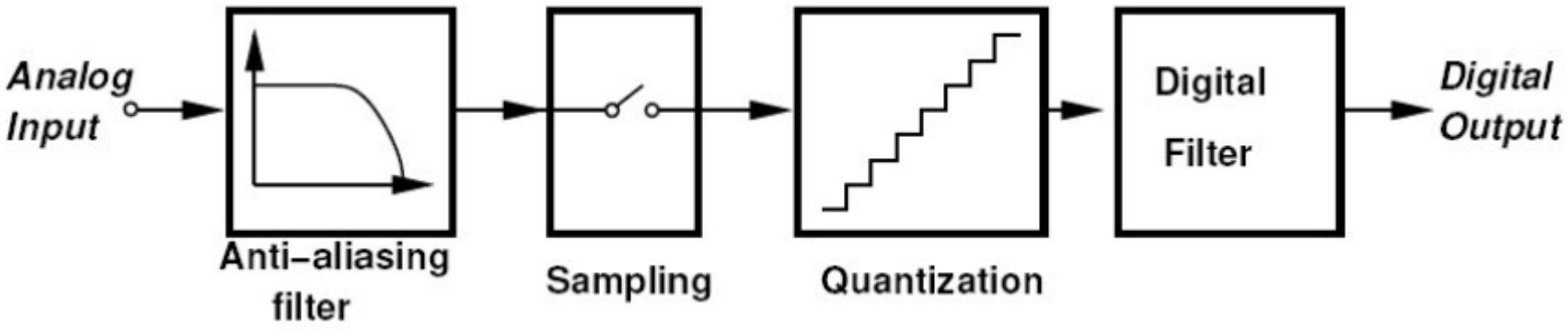
Introduction and Motivation

1) ADC design for analog front-end interface
2) Low bandwidth application
3) Key components – Pre-filter, sampler, quantizer, decimator



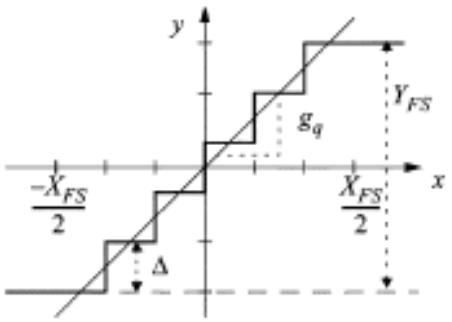
Fundamentals

1) No overload quantizer error limited to $\pm \frac{\Delta}{2}$

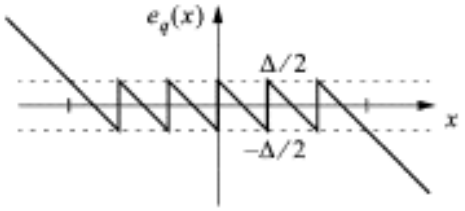
$$\Delta = \frac{V_{full-scale}}{2^N - 1}$$

$$q \sim U\left(-\frac{\Delta}{2}, \frac{\Delta}{2}\right)$$

$$E[q^2] = \frac{\Delta^2}{12}$$



(a)



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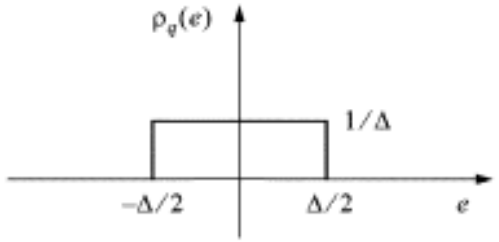

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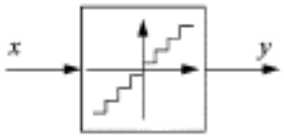

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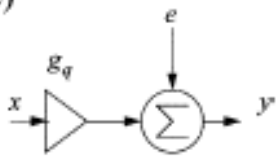


(d)

Fundamentals

2) Nyquist-rate converters

$$f_s = 2B$$

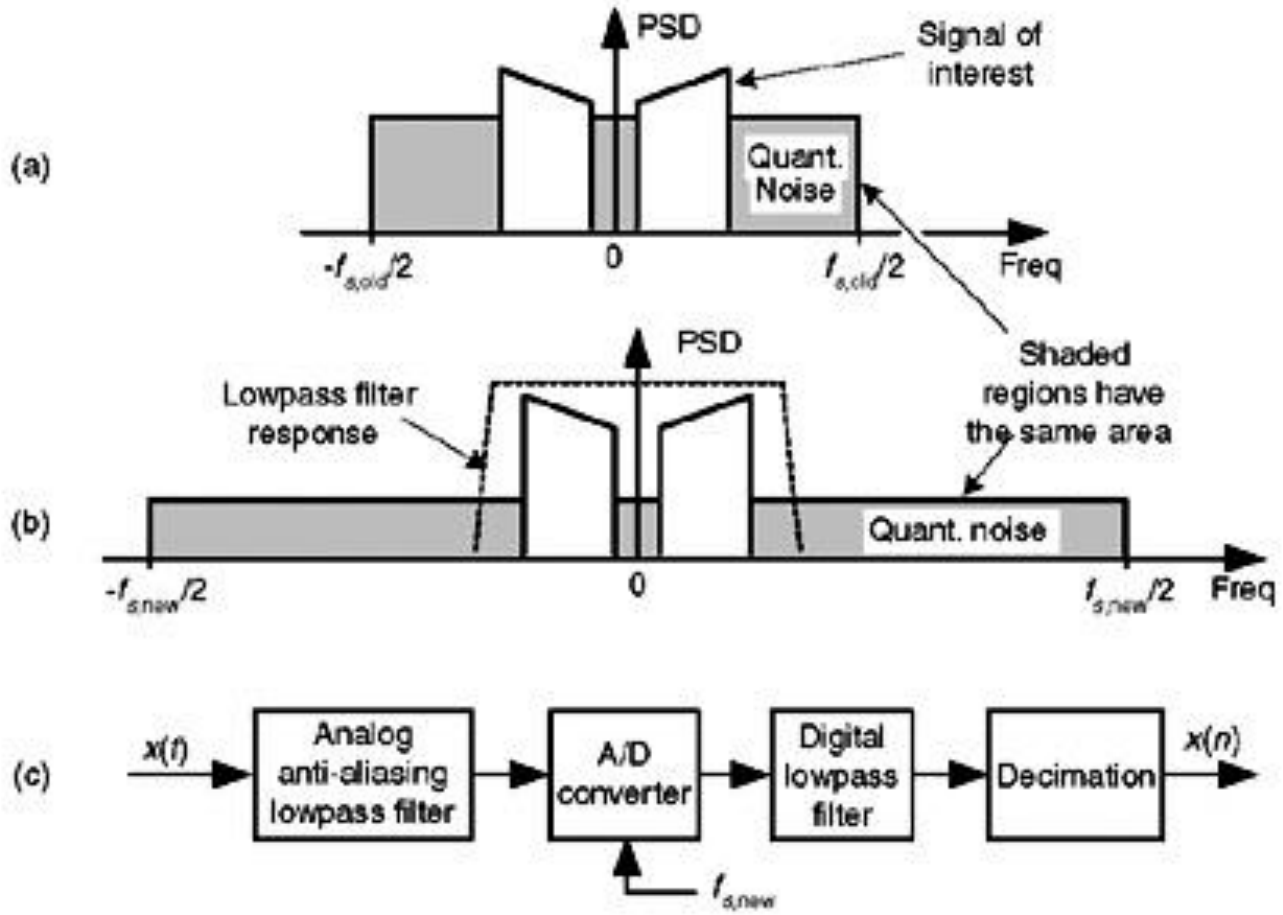
$$DR_{dB} = 20\log_{10}\left(\frac{V_{full-scale}}{\Delta}\right) = 20\log_{10}\left(2^N - 1\right) \approx 6.02N$$

$$SNR_{dB} = 10\log_{10}\left(\frac{\frac{1}{2}\left(V_{full-scale}/2\right)^2}{\Delta^2/12}\right) \approx 6.02N + 1.76$$

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02}$$

Fundamentals

3) Oversampled converters



Fundamentals

3) Oversampled converters

$$f_s = 2B \cdot OSR >> 2B$$

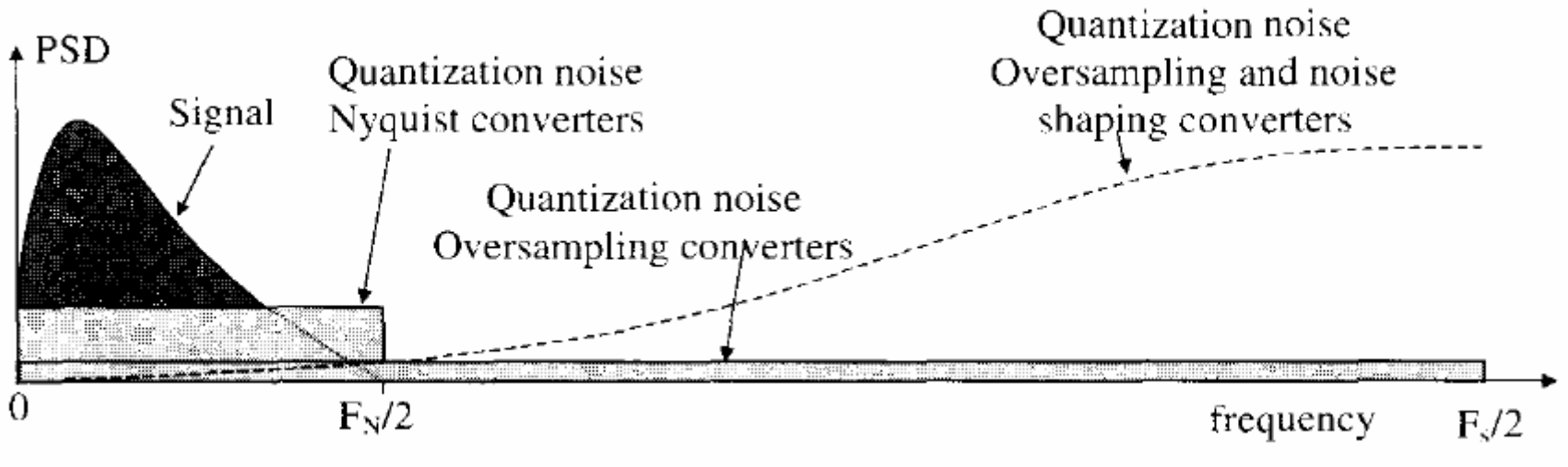
$$SNR_{dB} = 10\log_{10}\left(\frac{\frac{1}{2}\left(V_{full-scale}/2\right)^2}{\Delta^2/12 \cdot OSR}\right) \approx 6.02N + 1.76 + 10\log_{10}(OSR)$$

- Able to achieve equivalent performance for smaller values of N compared to Nyquist-rate converters

Fundamentals

4) Noise-shaping converters

- Further reduce noise floor in signal band by high-pass filtering the noise to higher frequencies near $\frac{f_s}{2}$



Delta-Sigma Modulation Theory

1) Oversampled + noise shaping converter

$$STF(z) = \frac{G(z)}{1 + G(z) \cdot H(z)}$$

$$NTF(z) = \frac{1}{1 + G(z) \cdot H(z)}$$

$$STF(z) = z^{-1}$$

$$NTF(z) = (1 - z^{-1})$$

$$G(z) = \frac{z^{-1}}{1 - z^{-1}}$$

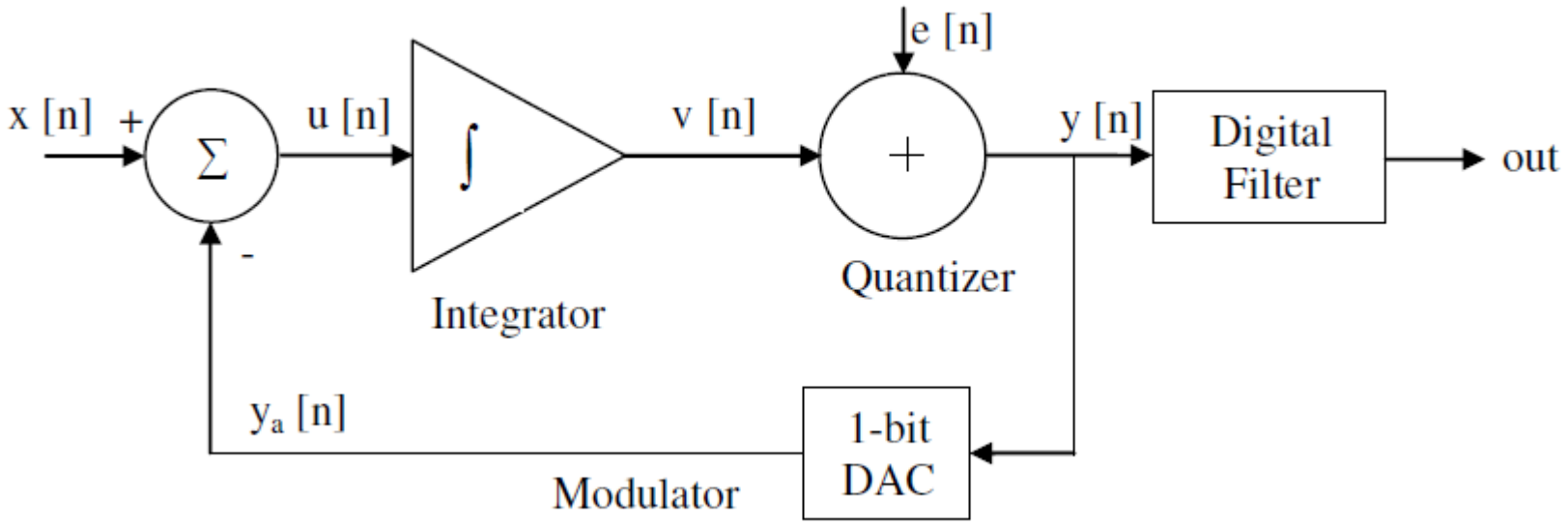
$$H(z) = 1$$

- Thus, negative feedback with feed-forward integrator and unity gain feed-back

Delta-Sigma Modulation Theory

2) General Delta-Sigma converter

- B = quantizer resolution, L = integrator order



$$SQNR_{dB} = 10log_{10}(\frac{3\pi}{2}(2^B - 1)^2 \cdot (2L+1)(\frac{OSR}{\pi})^{2L+1})$$

Delta-Sigma Modulation Theory

3) Discrete time (DT) and continuous time (CT) implementations

- DT – discrete time integrator (switched cap.)
- CT – continuous time integrator (RC, Gm-C filters), sampling done prior to quantization
- DT – no mismatch, no timing issues
- CT – no pre-filtering required, higher speeds
- DT chosen here as speed not critical

1-bit, 2nd-order Modulator

1) Requirements

- Resolution ≥ 10 bits
- Input signal bandwidth ≤ 1 kHz
- Sampling frequency = 1 MHz

$$f_{in}P = f_s m \qquad P = 2^{15} = 32768 \qquad OSR = \frac{f_s}{2f_{in}} = 496.5$$

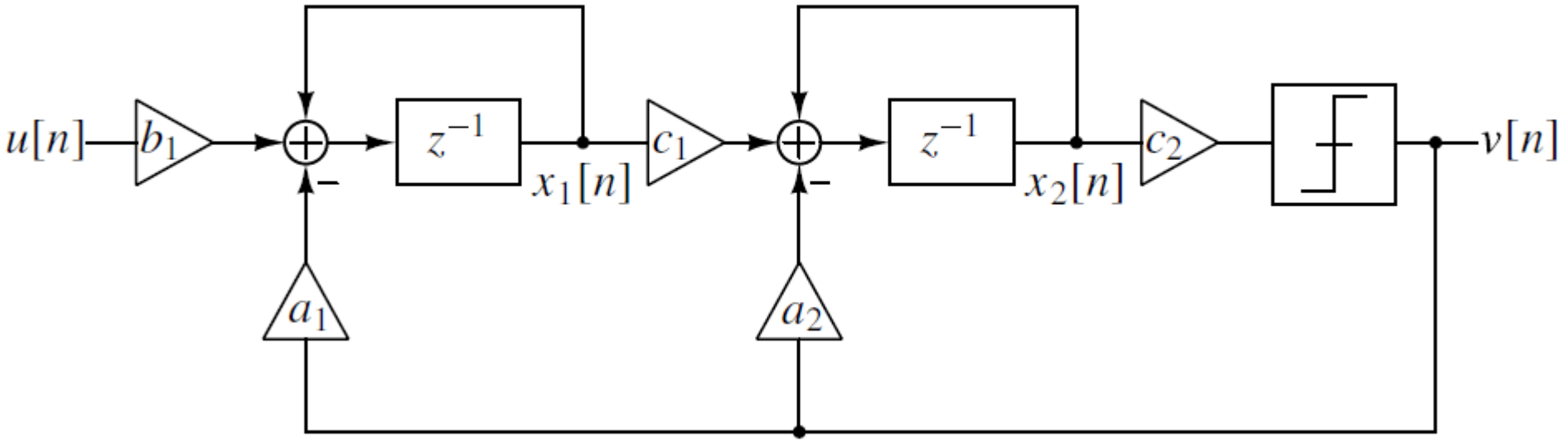
$$m = 33 \qquad f_{in} = 993Hz$$

- Full-scale range = 0.9 $\pm$ 0.1 V

1-bit, 2nd-order Modulator

2) NTF selection

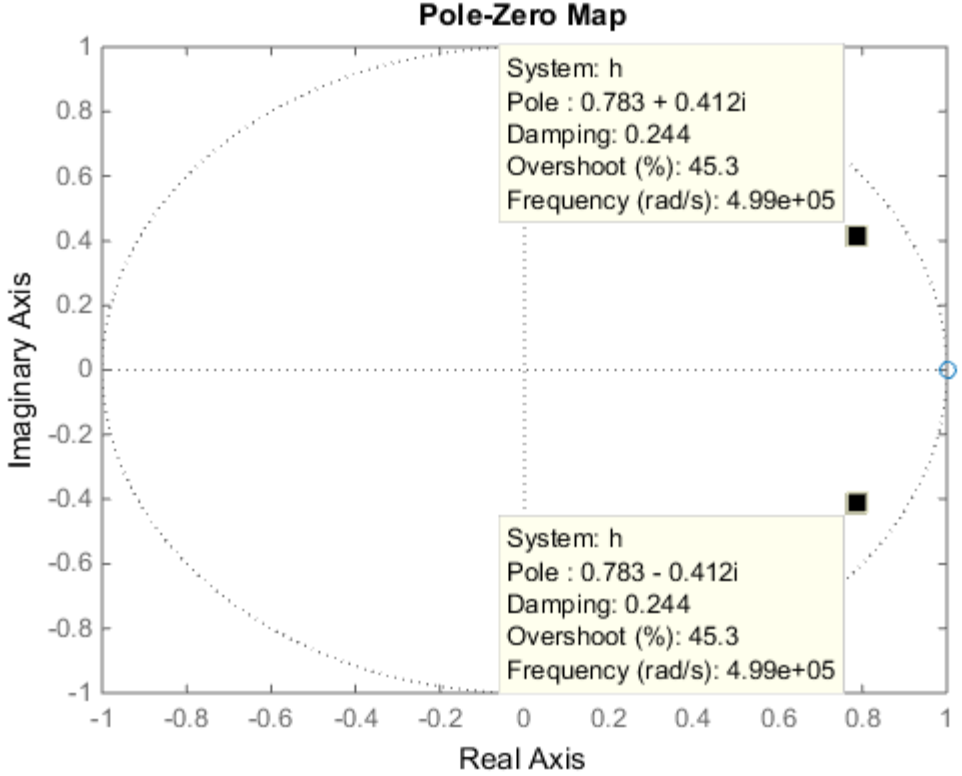
- CIFB – cascaded integrator feedback
- MATLAB simulations (Delta-Sigma Toolbox)



1-bit, 2nd-order Modulator

2) NTF selection

$$NTF(z) = \frac{(1 - z^{-1})^2}{0.7835z^{-2} - 1.567z^{-1} + 1}$$



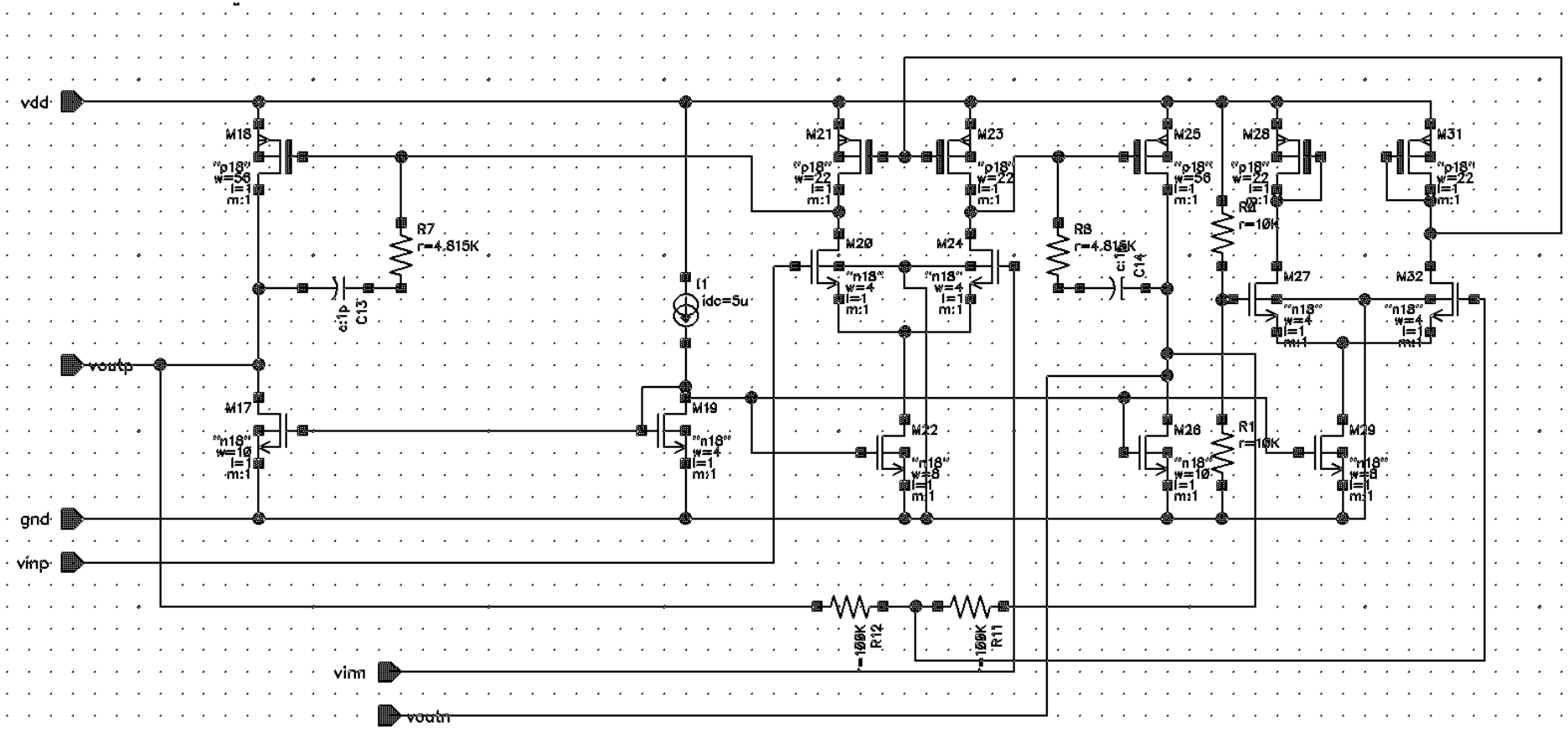
1-bit, 2^{nd}-order Modulator

3) Op amp design

- Fully differential 2-stage Miller compensated
- DC gain ≥ 60 dB => 92 dB
- Unity gain frequency ≥ 5 MHz => 6.135 MHz
- Output swing ≈ 0 – 1.8 V => 0.1 – 1.7 V
- Phase margin ≥ 60^{o} => 87.55^{o}
- Chopper stabilized to reduce flicker noise

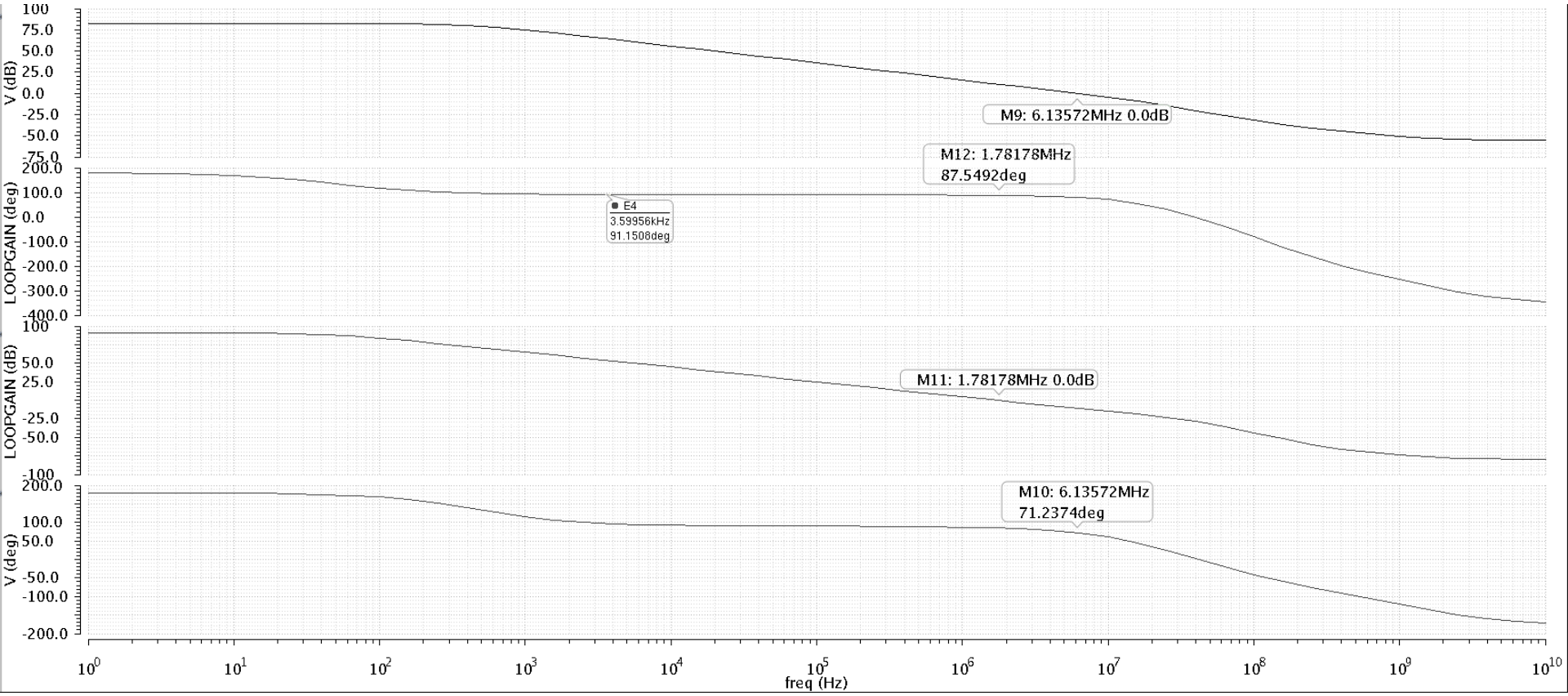
1-bit, 2nd-order Modulator

3) Op amp design



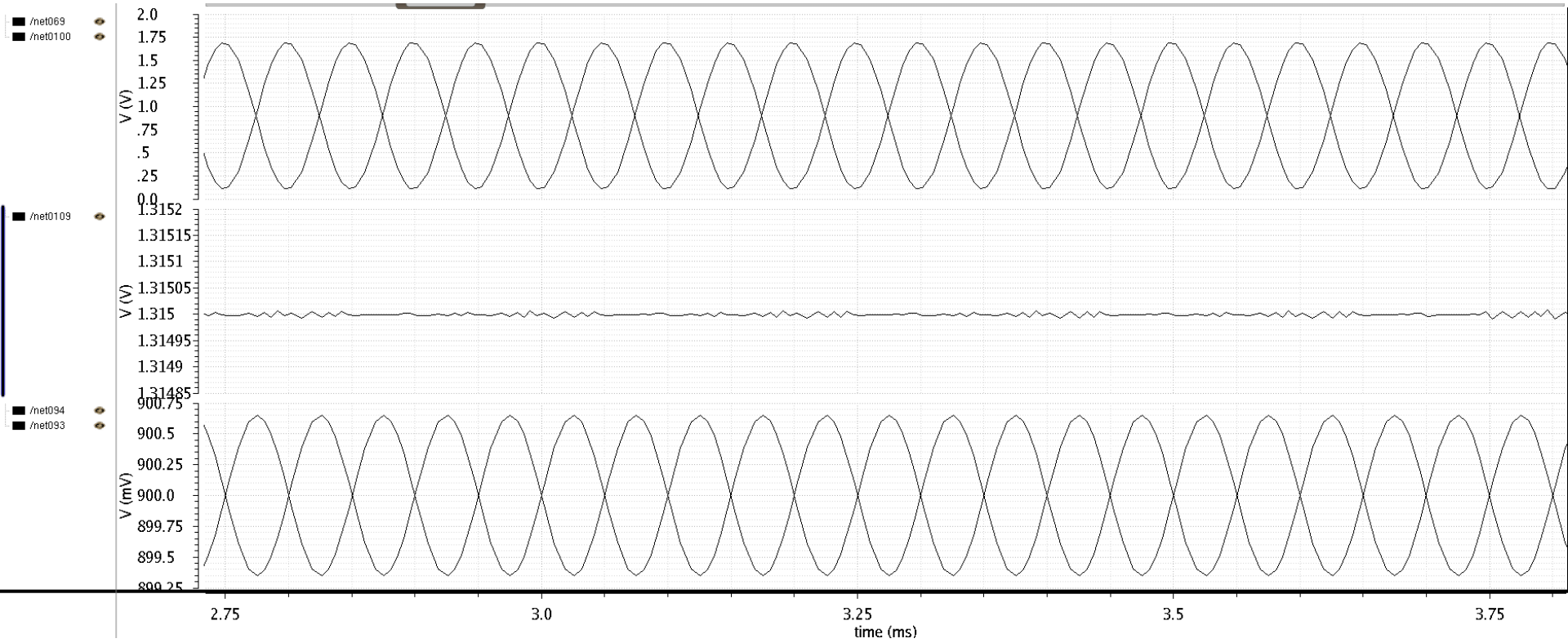
1-bit, 2nd-order Modulator

3) Op amp design



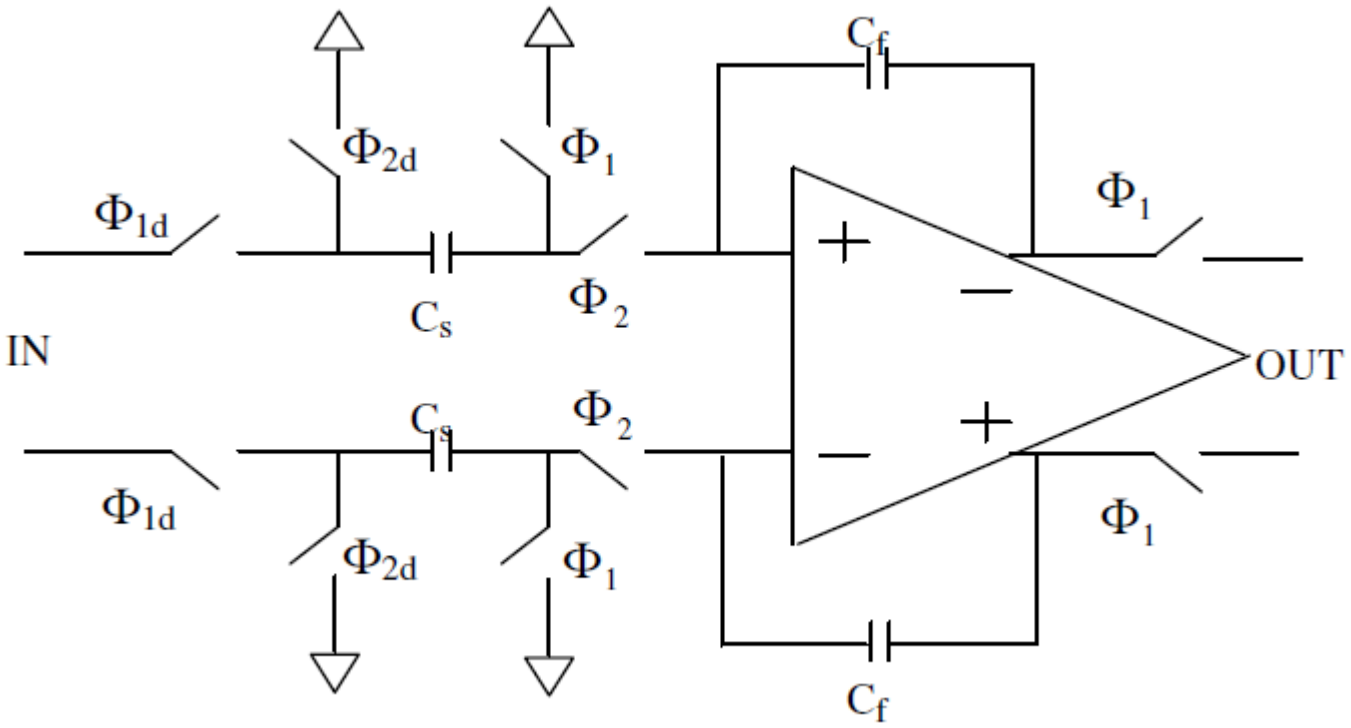
1-bit, 2nd-order Modulator

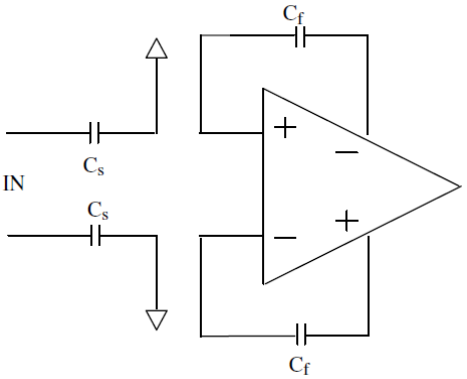
3) Op amp design

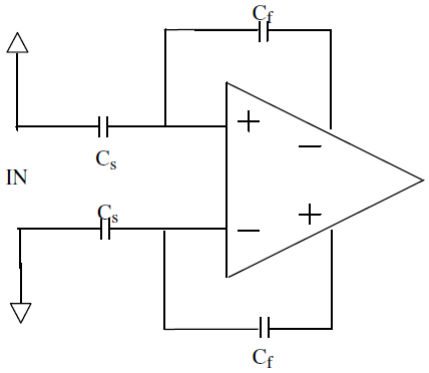


1-bit, 2nd-order Modulator

4) Switched capacitor integrator design







$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_s}{C_f}\frac{z^{-1}}{1-z^{-1}}$$

1-bit, 2nd-order Modulator

4) Switched capacitor integrator design

1-bit, 2nd-order Modulator

5) Capacitor sizing

$$\overline{v_n^2} = \frac{0.5 \cdot (0.05)^2}{10^{8.5}} = \frac{4kT}{C_s \cdot 496.5}$$

$$C_{s1} = 8.44\,pF \Rightarrow 15\,pF$$

$$C_{f1} = \frac{V_{ref}}{a_1} C_{s1} = 30\,pF$$

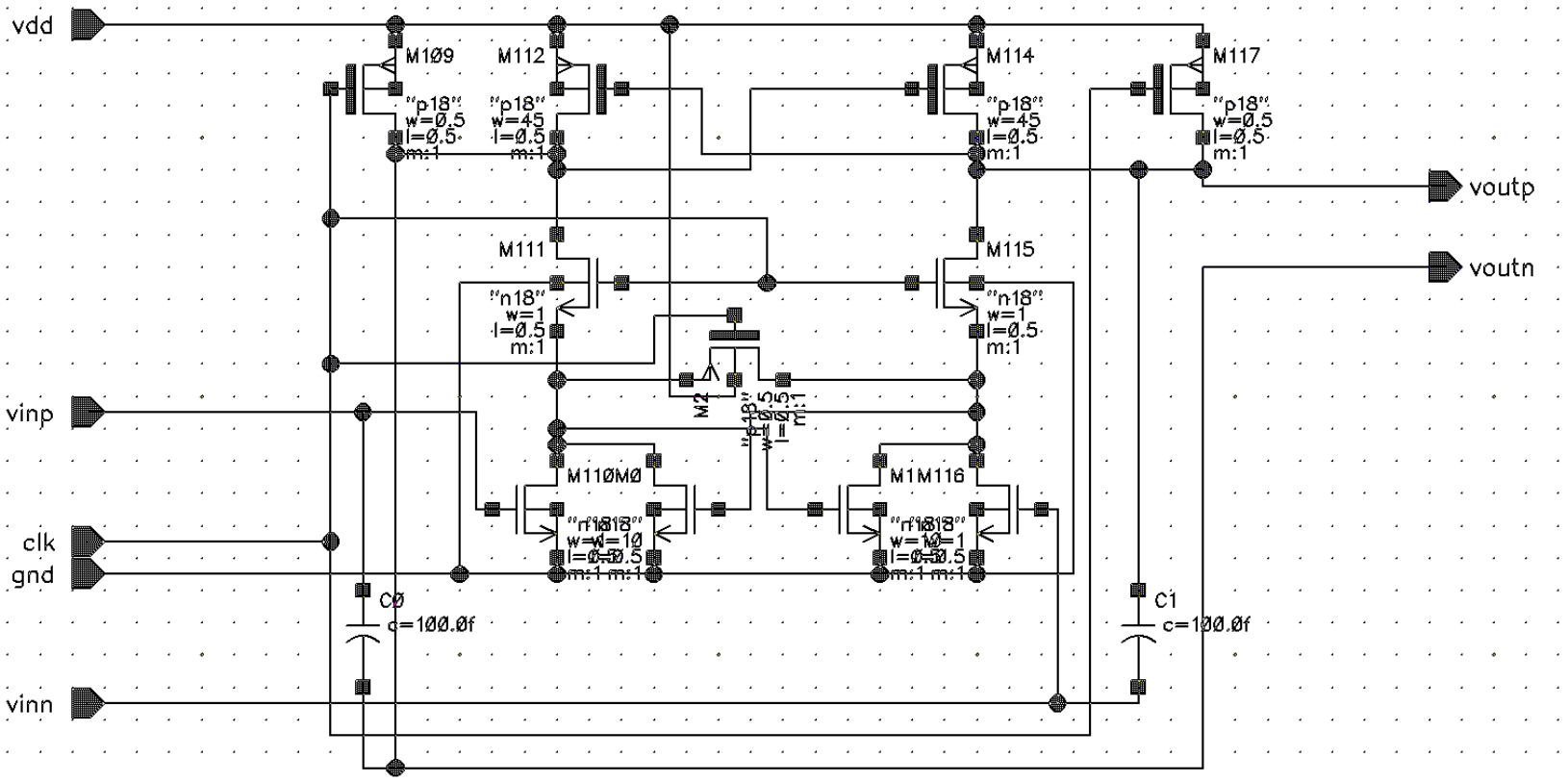
$$C_{s2} = 15\,pF$$

$$C_{f2} = \frac{V_{ref}}{a_2} C_{s2} = c_1 = 30\,pF$$

1-bit, 2nd-order Modulator

6) 1-bit quantizer design

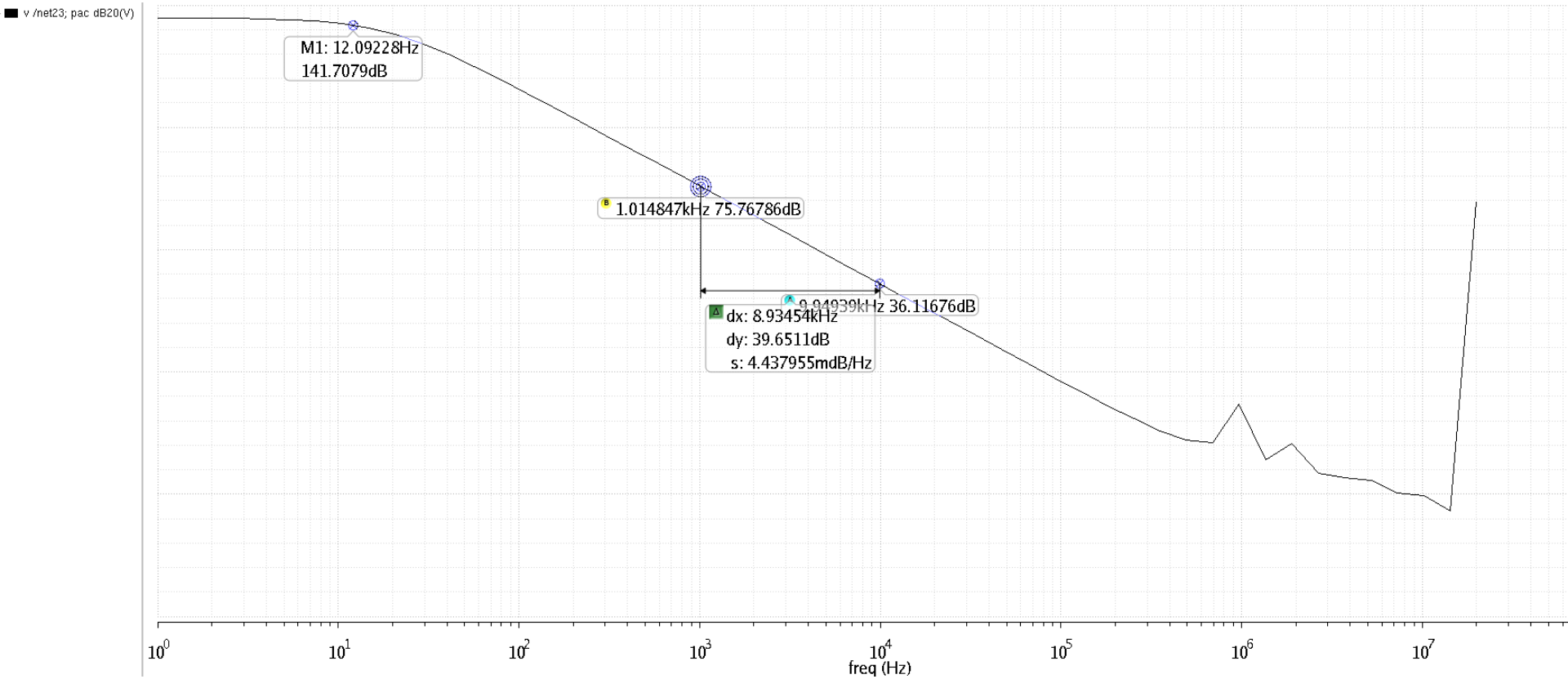
- Regenerative comparator – StrongARM latch



1-bit, 2nd-order Modulator

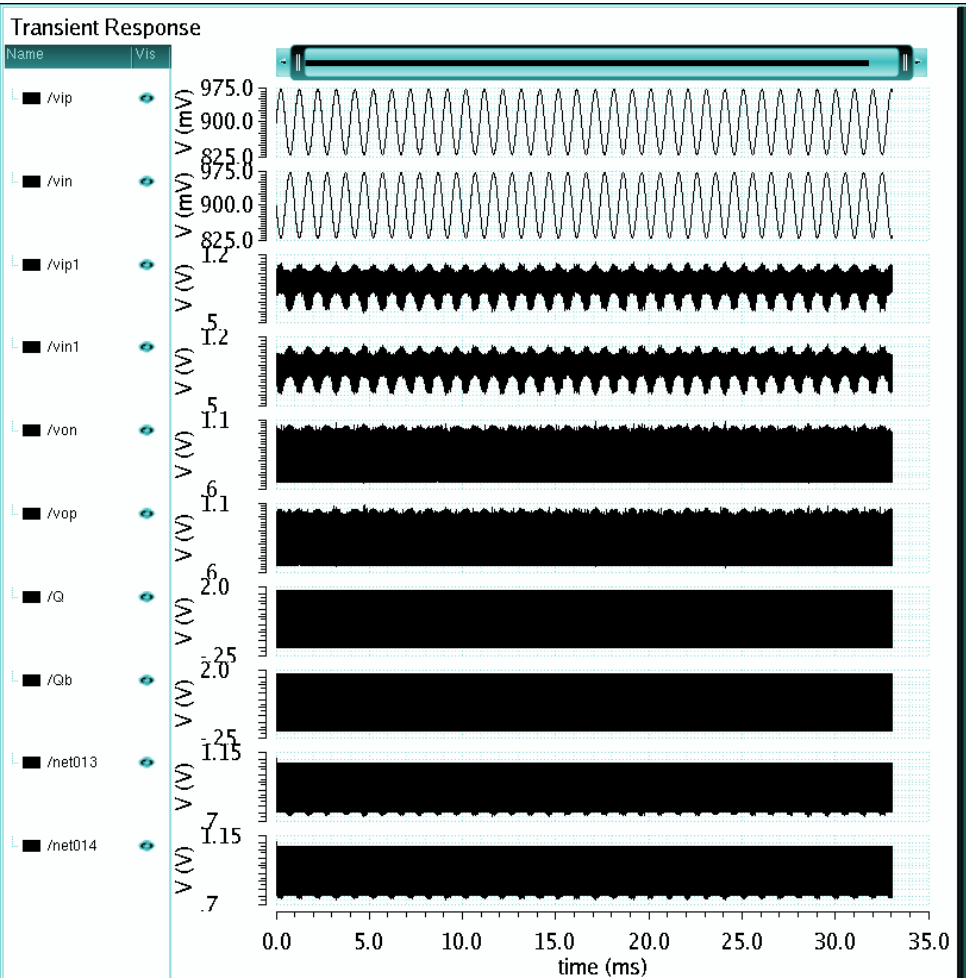
7) Complete modulator

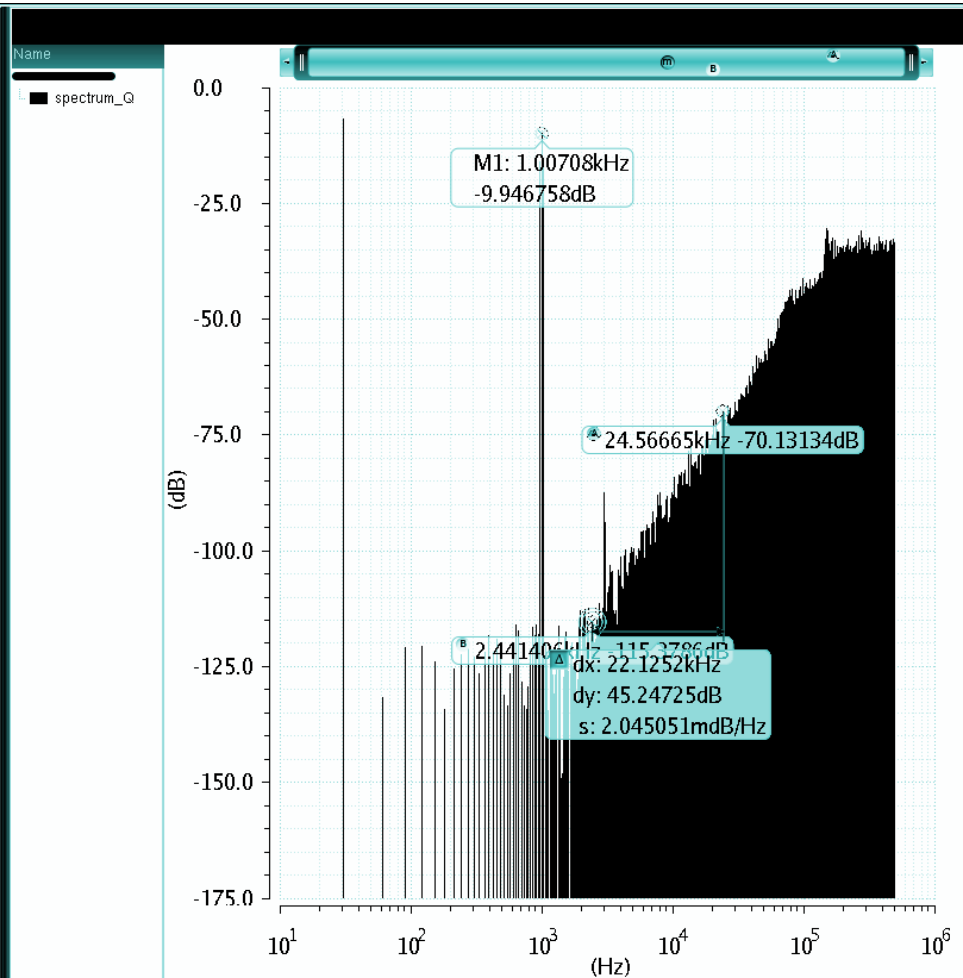
- Cascaded integrators



1-bit, 2nd-order Modulator

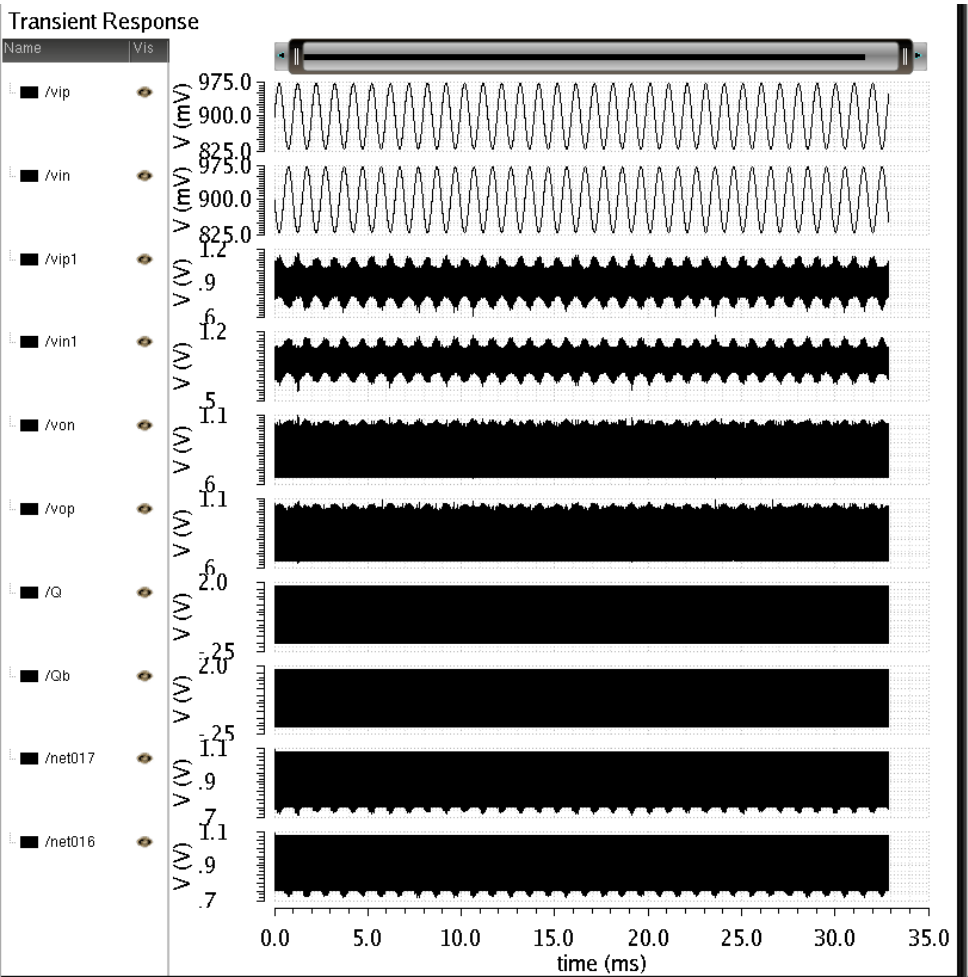
7) Complete modulator

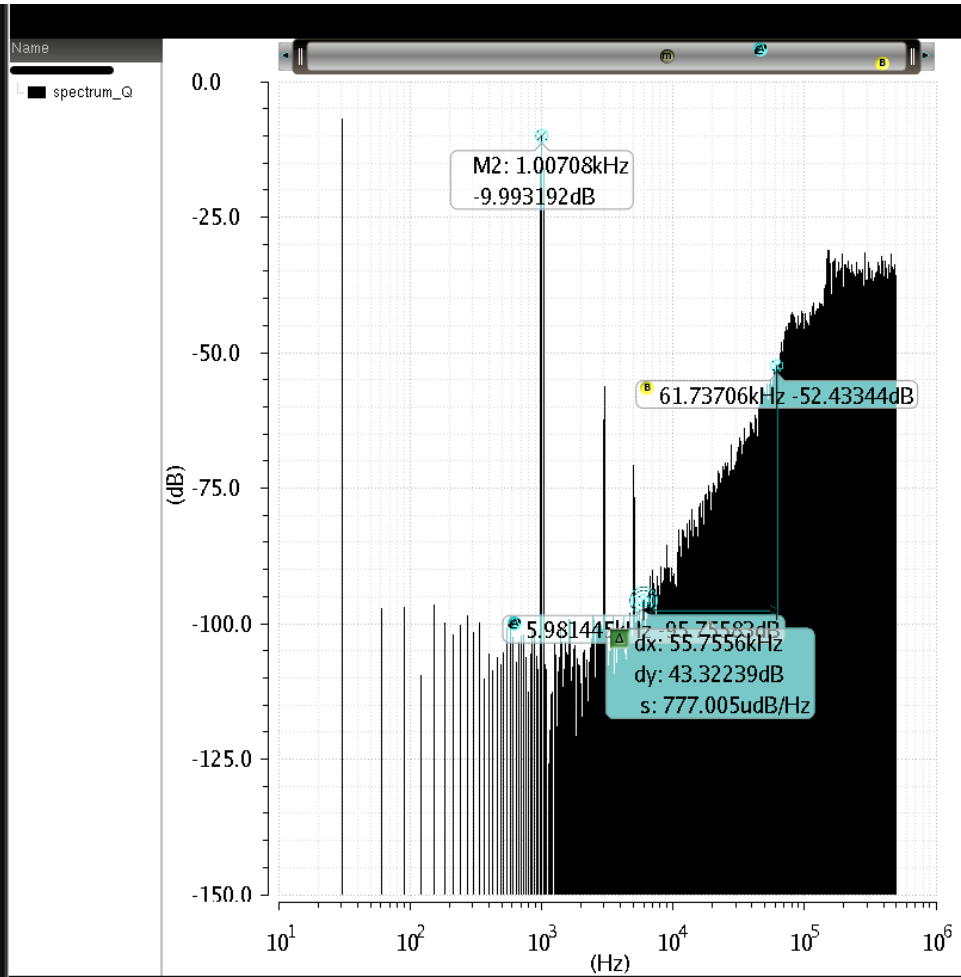




1-bit, 2nd-order Modulator

7) Complete modulator





1-bit, 2^{nd}-order Modulator

7) Complete modulator

- SQNR = 96.5 dB => SNR = 77.83 dB
- SFDR = 106 dB => SFDR = 86.6 dB
- ENOB = 15.73 bits => ENOB = 12.64 bits
- Thermal noise major bottleneck

Multi-bit, Multi-stage Modulator

1) Dynamic element matching
- Multi-bit quantizer with multi-bit DAC
- Randomizes connections between unit elements to tackle DAC non-linearity
2) Leslie-Singh architecture
- Second stage contains multi-bit quantizer
- Replaces 1-bit quantizer noise with multi-bit

Summary

1) Successfully designed 1-bit, 2^{nd}-order modulator with > 12 bit resolution
2) Extension to multi-bit, multi-stage to be performed next
3) Comparison of discrete time, continuous time and hybrid architectures