The Design of Discrete Time Delta-Sigma Converters

Project-I (EC47001) report submitted to

Indian Institute of Technology, Kharagpur

in partial fulfilment for the award of the degree of

Bachelor of Technology

in

Electronics & Electrical Communication Engineering

by

Nishant Mehrotra

(14EC10034)

Under the supervision of

Prof. Pradip Mandal

Department of Electronics & Electrical Communication Engineering

Indian Institute of Technology, Kharagpur

Autumn Semester, 2017-18

November 29, 2017

DECLARATION

I certify that

(a) The work contained in this report has been done by me under the guidance of my supervisor.

(b) The work has not been submitted to any other Institute for any degree or diploma.

(c) I have conformed to the norms and guidelines given in the Ethical Code of Conduct of the Institute.

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DEPARTMENT OF ELECTRONICS & ELECTRICAL COMMUNICATION ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

KHARAGPUR - 721302, INDIA

CERTIFICATE

This is to certify that the project report entitled "**The Design of Discrete Time Delta-Sigma Converters**" submitted by **Nishant Mehrotra** (Roll No. 14EC10034) to Indian Institute of Technology, Kharagpur towards partial fulfilment of requirements for the award of degree of Bachelor of Technology in Electronics & Electrical Communication Engineering is a record of bona fide work carried out by him under my supervision and guidance during Autumn Semester, 2017-18.

Date: November 29, 2017

Place: Kharagpur

Prof. Pradip Mandal
Department of Electronics & Electrical
Communication Engineering
Indian Institute of Technology,
Kharagpur
Kharagpur - 721302, India

Abstract

Name of the student: **Nishant Mehrotra** Roll No: **14EC10034**

Degree for which submitted: **Bachelor of Technology**

Department: **Department of Electronics** & **Electrical Communication Engineering**

Thesis title: **The Design of Discrete Time Delta-Sigma Converters**

Thesis supervisor: **Prof. Pradip Mandal**

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The aim of this thesis is the design and analysis of a high-resolution analog-to-digital converter for an analog front-end interface. A discrete time oversampled, noise-shaping delta-sigma converter has been chosen for the same. The design flow for a 1-bit, 2nd-order discrete time $\Delta - \Sigma$ modulator is presented, along with two possible multi-bit, multi-stage extensions to the work.

Acknowledgements

I would like to thank Prof. Pradip Mandal for advising me in this project, and the Advanced VLSI Laboratory, IIT Kharagpur for providing the required circuit design tools. I express my heartfelt gratitude to my parents for always believing in me.

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List of Abbreviations

1. $\Delta - \Sigma$ - *delta-sigma*
2. *ADC - analog-to-digital converter*
3. *CIFB - cascaded integrator feedback*
4. *CMFB - common mode feedback*
5. *CMOS - complementary metal-oxide-semiconductor*
6. *CT - continuous time*
7. *DAC - digital-to-analog converter*
8. *DEM - dynamic element matching*
9. *DR - dynamic range*
10. *DT - discrete time*
11. *DWA - data weighted averaging*
12. *ENOB - effective number of bits*
13. *FIR - finite impulse response*
14. *MATLAB - matrix laboratory*
15. *NMOS - n-type metal-oxide-semiconductor*
16. *NTF - noise transfer function*
17. *OSR - oversampling ratio*
18. *PAC - periodic alternating current*
19. *PM - phase margin*
20. *PMOS - p-type metal-oxide-semiconductor*
21. *PN - pseudo-random noise*
22. *SNDR - signal-to-distortion ratio*
23. *SNR - signal-to-noise ratio*
24. *SQNR - signal-to-quantization noise ratio*
25. *SR - set-reset*
26. *STF - signal transfer function*
27. *UGF - unity-gain frequency*

Bachelor's Thesis Project Report

Nishant Mehrotra (14EC10034)

Advisor: Prof. Pradip Mandal

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1. **Motivation and Introduction:**

The goal is to design a high-resolution analog-to-digital converter for an analog front-end interface. Analog-to-digital converters (ADCs) are crucial links between the analog and digital domains. For a given application, different architectures may be used for different analog signal bandwidths and different available technologies. Nyquist-rate ADC's are used for high bandwidth conversion while oversampling, noise shaping delta-sigma converters are used for low and intermediate frequency signals, their range of applicability extending with faster switching speeds available. Analog front-end interfaces for biomedical and related applications have relatively low input signal bandwidth, and thus delta-sigma ($\Delta - \Sigma$) converters are natural choices for such applications.

$\Delta - \Sigma$ converters are well suited for low bandwidth, high-resolution acquisition, and their low cost makes them good ADC choices for many applications. They combine an analog delta-sigma modulator with a more complex digital decimation filter. Accuracy depends on the noise and linearity performance of the modulator, which uses high performance amplifiers. They have been widely used in high resolution audio products, such as MP3 players and cell phones, primarily due to the narrow bandwidth requirements in digital audio applications.

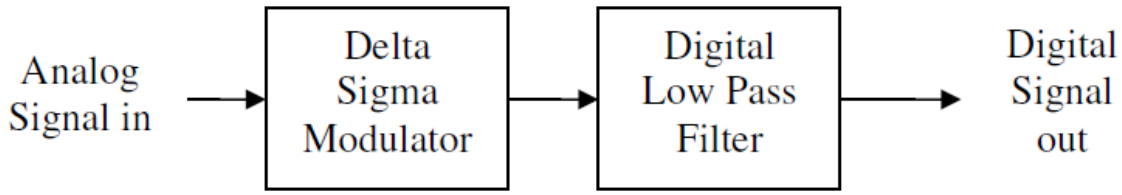


Figure 1: Block diagram of an example application [1]

$\Delta - \Sigma$ converters come into the category of oversampled converters. Oversampling converters, in contrast to Nyquist-rate converters, are systems that sample the input signal at a frequency much greater than the Nyquist frequency. The primary advantage of oversampled converters is the relaxed analog pre-filter design, whereas Nyquist-rate converters require analog filters with well-defined and sharp transition regions to prevent aliasing. $\Delta - \Sigma$ converters, in particular, are preferred over other oversampled converters due to their higher signal-to-noise ratios (SNR) and their insensitivity to analog circuit mismatches. They trade off resolution in time for resolution in amplitude to allow the toleration of circuit imperfections, and achieve greater resolution than that of their constituent components. To further increase the resolution, $\Delta - \Sigma$ converters employ noise shaping to high pass filter the quantization noise out of the signal band. The shaped noise is then removed by the decimation filter and thus a high resolution ADC is obtained.

2. **Fundamentals:**

(a) *Analog-to-digital conversion theory:*

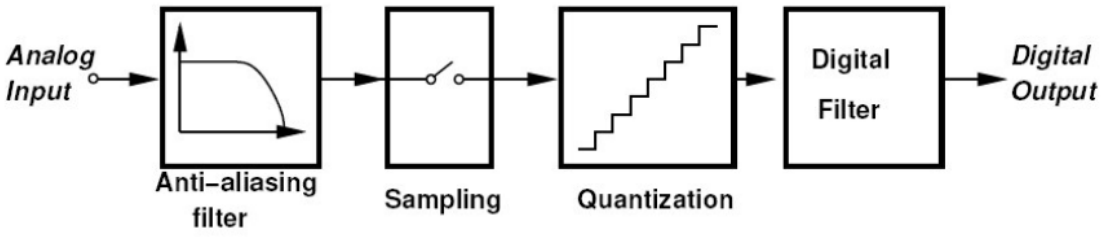


Figure 2: Block diagram of an example ADC application [1]

An anti-aliasing filter limits the bandwidth of the analog input signal before sampling is performed. A basic sample-and-hold circuitry can be used for sampling, while a N-bit quantizer maps the held analog value to a particular value in the set of 2^N discrete values. The difference between the original input and the digital output is referred to as the quantization error, or equivalently as the quantization noise. An example of the same is illustrated in Figure 3.

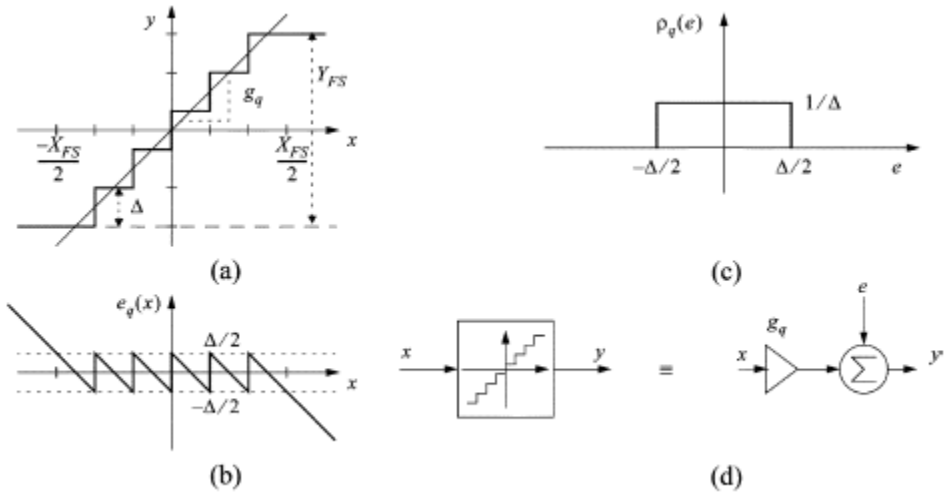


Figure 3: Quantization error example [9]

This error is limited by the sampling frequency used and the resolution of the converter. If the signal doesn't exceed the full swing, the error is uniformly distributed (with mean 0) and limited to $\pm\frac{V_{fullscale}}{2\cdot(2^N-1)}$ where $V_{fullscale}$ is the full swing of the ADC. If the converter becomes overloaded, the quantization noise exceeds the above limits.

The dynamic range of an ADC is defined as the range of input signals resolvable by the converter. Thus, it is defined as the ratio of the full-scale amplitude and $\Delta = \frac{V_{fullscale}}{2^N-1}$, and thus $DR_{dB} = 6.02 \cdot N$.

The signal-to-noise ratio (SNR) is the ratio of the signal power to the noise power. Considering only the quantization noise, the equivalent noise power is $P_{q.noise} = \frac{\Delta^2}{12}$. Thus, the SNR is

$$SNR_{dB} = 6.02 \cdot N + 1.76$$

The signal-to-noise distortion ratio (SNDR) is defined as the ratio of the signal power to the total power of the noise and signal harmonics.

The effective number of bits (ENOB) is defined as

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02}$$

.

(b) *Oversampled converters:*

The oversampling ratio (OSR) is defined as the ratio of the sampling frequency to the Nyquist rate frequency i.e. $OSR = \frac{f_s}{2 \cdot f_{in}}$. Oversampled converters have OSR > 1, whereas Nyquist rate converters have OSR $= 1$. Thus, for an oversampled converter,

$$SNR_{dB} = 6.02 \cdot N + 1.76 + 10 \cdot log_{10}(OSR)$$

Thus, we see that it is possible to use a lower bit quantizer and still achieve performance similar to that of a Nyquist-rate ADC. Also, doubling the OSR increases the SNR by 3 dB. Also, the amount of quantization noise in the signal band reduces by a factor of OSR due to its spreading over a larger frequency range as compared to the Nyquist rate.

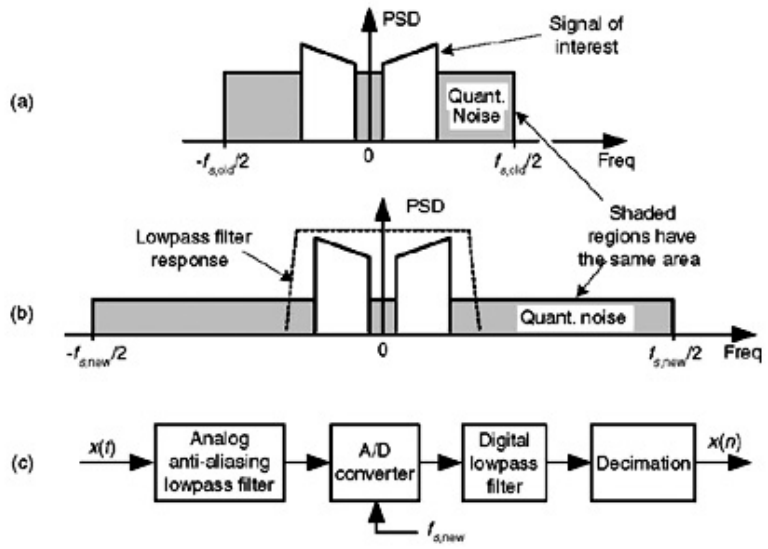


Figure 4: Quantization noise in Nyquist and oversampled converters [3]

3. $\Delta - \Sigma$ **Modulation Theory:**

(a) *Introduction:*

For a normal feedback system with open loop feed-forward gain G(z) and feedback gain H(z), the signal and noise transfer functions for signal X(z) and noise E(z) (added after the feed-forward transfer function) inputs may be derived as:

$$STF(z) = \frac{G(z)}{1 + G(z) \cdot H(z)}$$

$$NTF(z) = \frac{1}{1 + G(z) \cdot H(z)}$$

Also, $Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot E(z)$. For an all pass STF and high pass NTF, we can see that the noise will get shaped to higher frequencies while the signal band will be restricted to frequencies near DC. Thus, for low frequency applications, G(z) is chosen to be a low pass filter and is implemented as an integrator. Cascaded integrators may also be used, and the order of a modulator is defined as the number of integrators. The number of zeros in the NTF equals the order of the modulator, L.

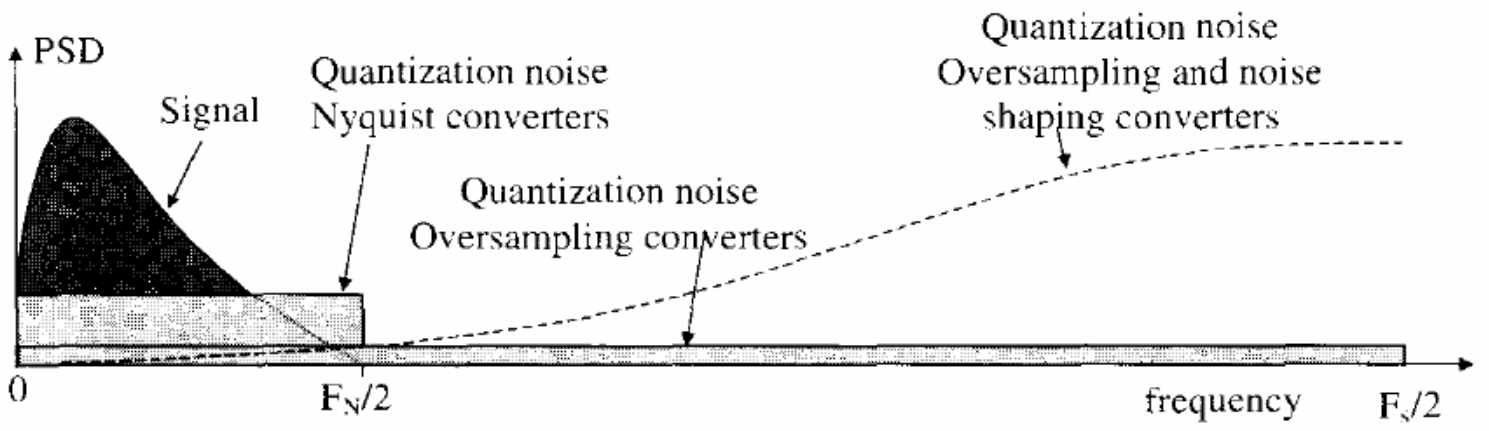


Figure 5: Noise shaping and oversampling converters [1]

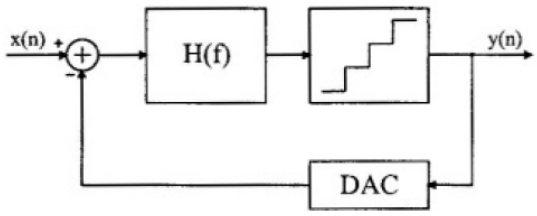


Figure 6: General $\Delta - \Sigma$ converter block diagram [4]

For a discrete time integrator, G(z) may be derived as $G(z) = \frac{z^{-1}}{1-z^{-1}}$. Modeling the feedback element i.e. DAC by a unity gain transfer function for simplicity, we obtain $H(z) = 1$. Therefore, $Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z)$ for a first order modulator. In general, $Y(z) = z^{-L} \cdot X(z) + (1 - z^{-1})^L \cdot E(z)$ for a modulator with order L. For an all pass STF and high pass NTF, we can see that the noise will get shaped to higher frequencies while the signal band will be restricted to frequencies near DC. Thus, for low frequency applications, G(z) is chosen to be a low pass filter and is implemented as an integrator. A 1-bit, 1st-order discrete time (DT) $\Delta - \Sigma$ modulator is shown in Figure 7.

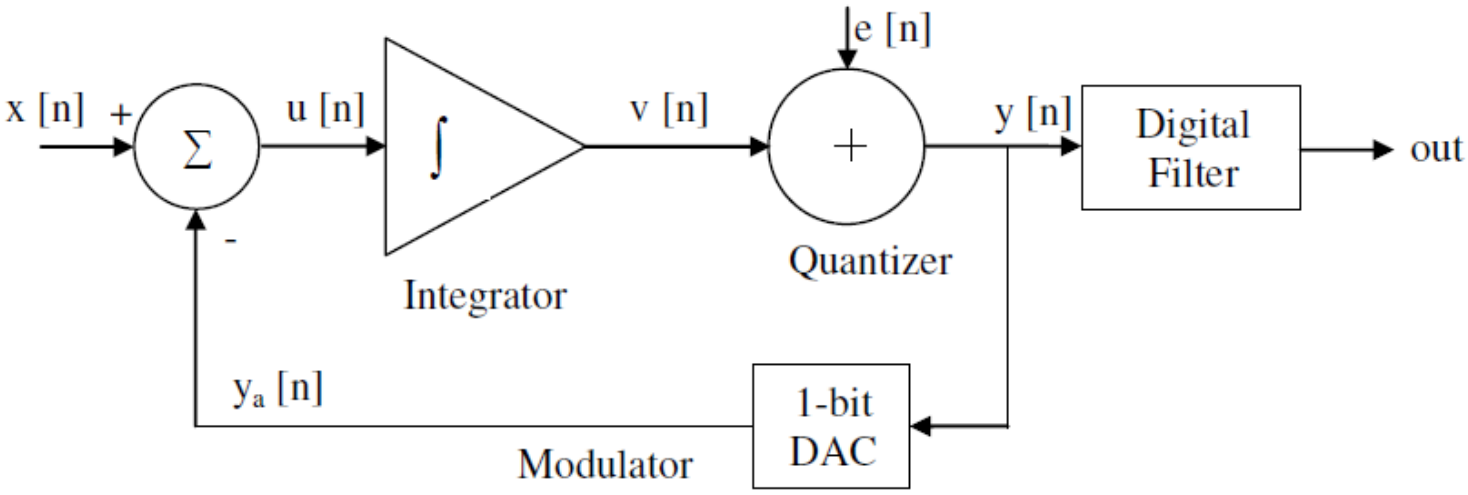


Figure 7: 1-bit, 1st-order DT $\Delta - \Sigma$ modulator block diagram [1]

Thus, $u[n] = x[n] - y_a[n]$, $v[n] - v[n-1] = u[n-1]$, $y[n] = v[n] + e[n]$ and $y[n] = y_a[n]$ on modeling the DAC as a unity gain ideal element. We may intuitively understand the time behavior of the modulator as that it accumulates the error and changes its decision accordingly. Thus, it is able to track the input signal on an average. The signal-to-quantization noise ratio (SQNR) for a general Lth-order modulator with a B-bit quantizer may be derived, and is found out to be:

$$SQNR_{dB} = 10log_{10}(\frac{3\pi}{2}(2^B - 1)^2 \cdot (2L + 1)(\frac{OSR}{\pi})^{2L+1})$$

For a practical modulator, the input signal is analog in nature. Thus, the two possible implementations of the above structure are either discrete time (DT) or continuous time (CT).

A discrete time $\Delta - \Sigma$ modulator uses discrete time integrators and processes the whole signal at sampling clock instances. In contrast, a continuous time modulator processes the signal in continuous time and only samples it prior to the quantizer. DT modulators have the advantage of doing away with the issue of resistor mismatch in current CMOS technology as the integrator is implemented via a switched capacitor circuit, thus allowing close matching of capacitors. Process variations also prevent the accurate estimation of time constants in CT integrators. DT integrators have the added advantage of being insensitive to clock jitter and the slewing of individual analog blocks is relatively relaxed in discrete time implementations. However, higher oversampling rates are possible with continuous time implementations. Another advantage of CT modulators is the lack of analog pre-filtering required. Thus, huge power savings and higher speeds are possible with CT implementations. In this thesis, a DT modulator is chosen to be designed due to the relaxed speed requirements for the given analog front-end application.

4. **1-bit, 2nd-order DT $\Delta - \Sigma$ Converter Design:**

(a) *Introduction:*

A fully differential 1-bit, 2nd-order DT modulator is implemented in SCL's 180 nm CMOS process, with 1.8 V supply voltage. The common mode voltage is chosen as $\frac{V_{DD}}{2} = 0.9V$ and for an differential input signal with total amplitude up to 0.2 V, the reference voltage V_{ref} is chosen to be 0.2 V. Thus, $V_{ref}^{+} = 1V$ and $V_{ref}^{-} = 0.8V$ for each differential rail. The input signal is assumed to be band-limited to around 1 kHz. A sampling rate of 1 MHz is chosen in this application. Thus, the exact value of f_{in} must be chosen for ensuring proper operation of the ADC. For a sinusoidal input signal x[n] with period P, we have: $x[n] = Acos(2\pi \cdot \frac{f_{in}n}{f_s} = Acos(2\pi \cdot \frac{f_{in}(n+P)}{f_s}$, which will only be periodic if $\frac{f_{in}P}{f_s} = m$ where m and P are relatively prime. For simplicity, P is chosen as a power of 2. Therefore, in our design, P = $2^{15} = 32768$, m = 33 i.e. $f_{in} = 0.993kHz$. Thus, the oversampling ratio is 496.5 here.

i. Resolution $\geq$ 10 bits
ii. Input signal BW $\leq$ 1 kHz
iii. Sampling frequency = 1 MHz
iv. Oversampling ratio = 496.5
v. Full scale voltage range = $\pm$0.1 V
vi. Supply voltage = 1.8 V

(b) *Noise transfer function (NTF) selection:*

For a resolution of around 15 bits, a SQNR of around 100 dB is the target specification. Also, while single order modulators are inherently stable, increasing the modulator order increases the SNR. Thus, a 2nd-order modulator is to be designed. The topology chosen is the 2nd-order cascaded integrator feedback (CIFB) modulator [6].

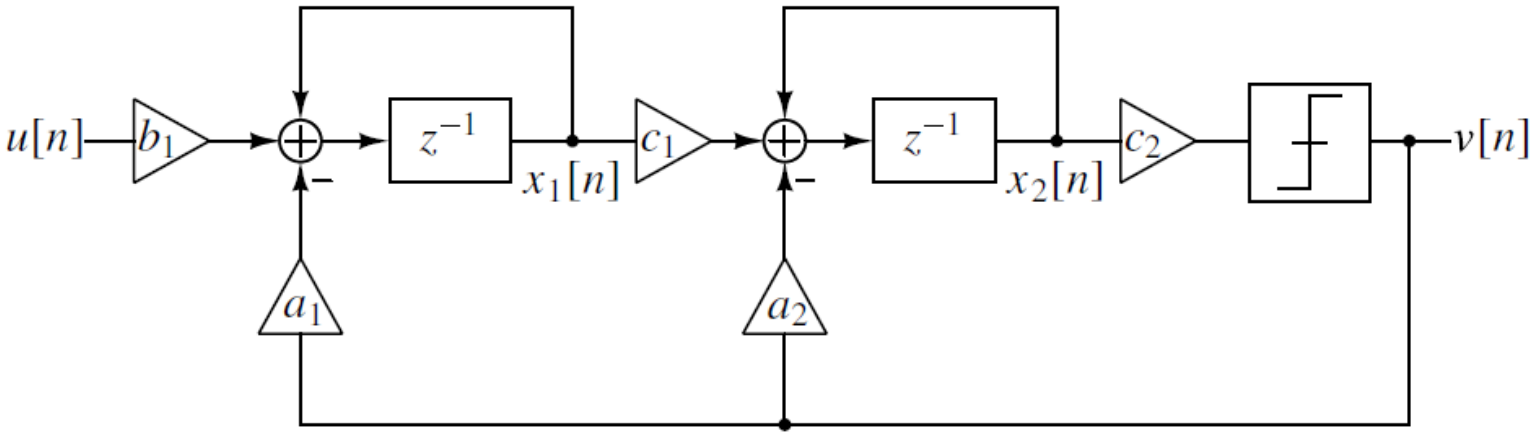


Figure 8: 1-bit, 2nd-order CIFB modulator [6]

Instead of choosing the conventional $(1 - z^{-1})^2$ as the NTF, a less aggressive function is chosen so as to not jeopardize the modulator's stability for inputs close to the full scale. Thus, MATLAB simulations using the Delta-Sigma Toolbox were performed for the CIFB modulator, and the resulting NTF had the form $NTF(z) = \frac{(1-z^{-1})^2}{0.4415z^{-2}-1.225z^{-1}+1}$. For conservativeness, the maximum normalized swings of each state variables was kept as 0.5, while the maximum input swing normalized to the full scale was kept as 0.9. However, for precise matching of capacitors, the capacitance ratios were kept in the powers of 2. Thus,

the NTF is recalculated with the above specifications and had the form $NTF(z) = \frac{(1-z^{-1})^2}{0.7835z^{-2}-1.567z^{-1}+1}$. Surprisingly, the derived NTF strongly matches with the well-known Boser-Wooley [7] implementation, which has the form $NTF(z) = \frac{(1-z^{-1})^2}{0.75z^{-2}-1.5z^{-1}+1}$. The modulator is clearly stable (from the pole-zero plot) as the poles of the NTF lie within the unit circle. The associated MATLAB codes may be found in the appendix section of this thesis.

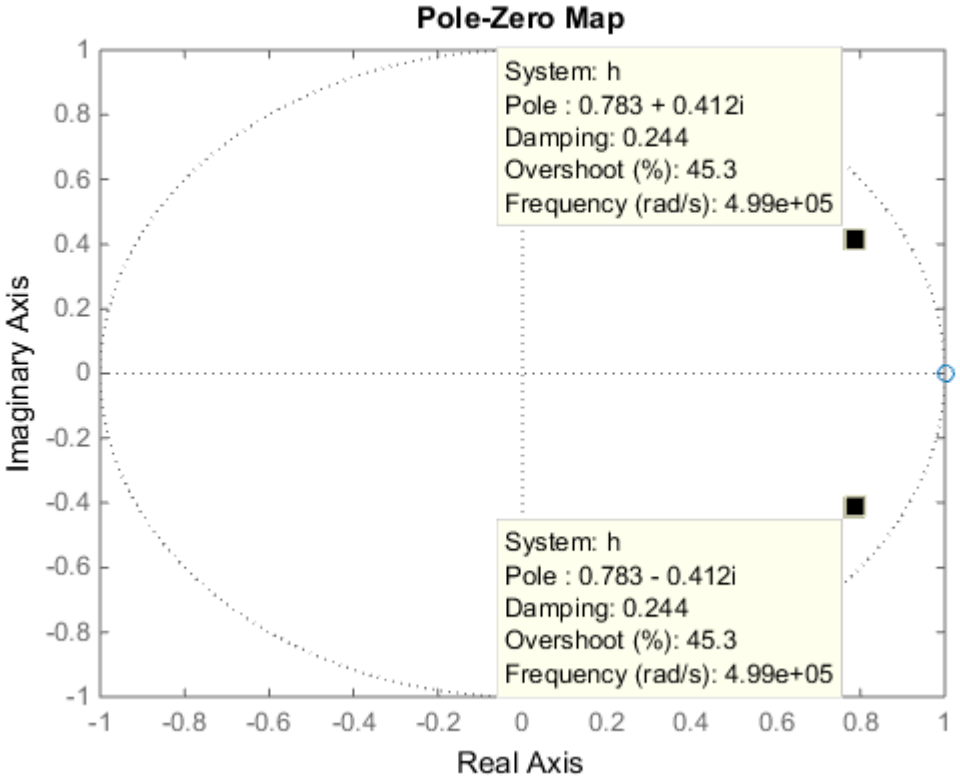


Figure 9: Pole-zero plot of derived NTF

(c) *Switch:*

Switches are implemented as transmission gates to reduce the effect of charge injection. The length of transistors is kept minimum to minimize area.

$$(W/L)_{NMOS} = \frac{0.9\mu m}{0.18\mu m}$$

$$(W/L)_{PMOS} = \frac{4.5\mu m}{0.18\mu m}$$

(d) *Operational amplifier:*

The unity gain frequency (UGF) of the constituent operational amplifiers in the integrators must be at least five to ten times the sampling frequency to ensure proper operation. Thus, $UGF \geq 5 \cdot f_s$. Additionally, the output must swing nearly rail-to-rail for proper integrator implementation. The gain requirements aren't very stringent, and greater than 60 dB gain suffices for our application. Thus, keeping in mind the requirement of rail-to-rail output swing, a fully differential two-stage Miller compensated op amp with resistive common mode feedback (CMFB) is designed. The specifications are as follows:

i. DC gain ($A_v(0)$) $\geq$ 60 dB
ii. Unity gain frequency (UGF) $\geq$ 5 MHz
iii. Output voltage swing $\sim$ rail-to-rail supply = 0 - 1.8 V
iv. Phase margin $\geq 60^\circ$

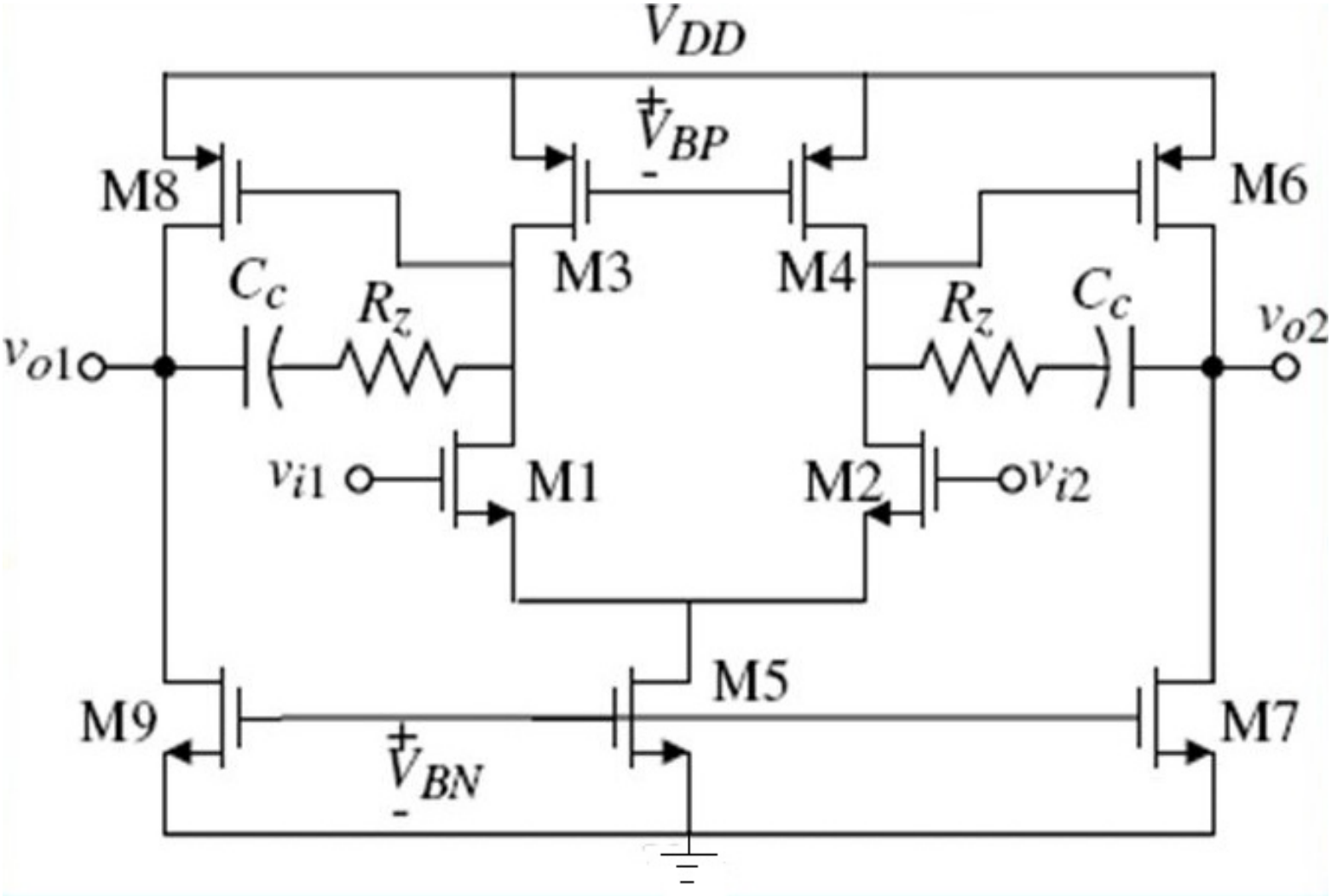


Figure 10: Fully differential two-stage Miller compensated op amp [1]

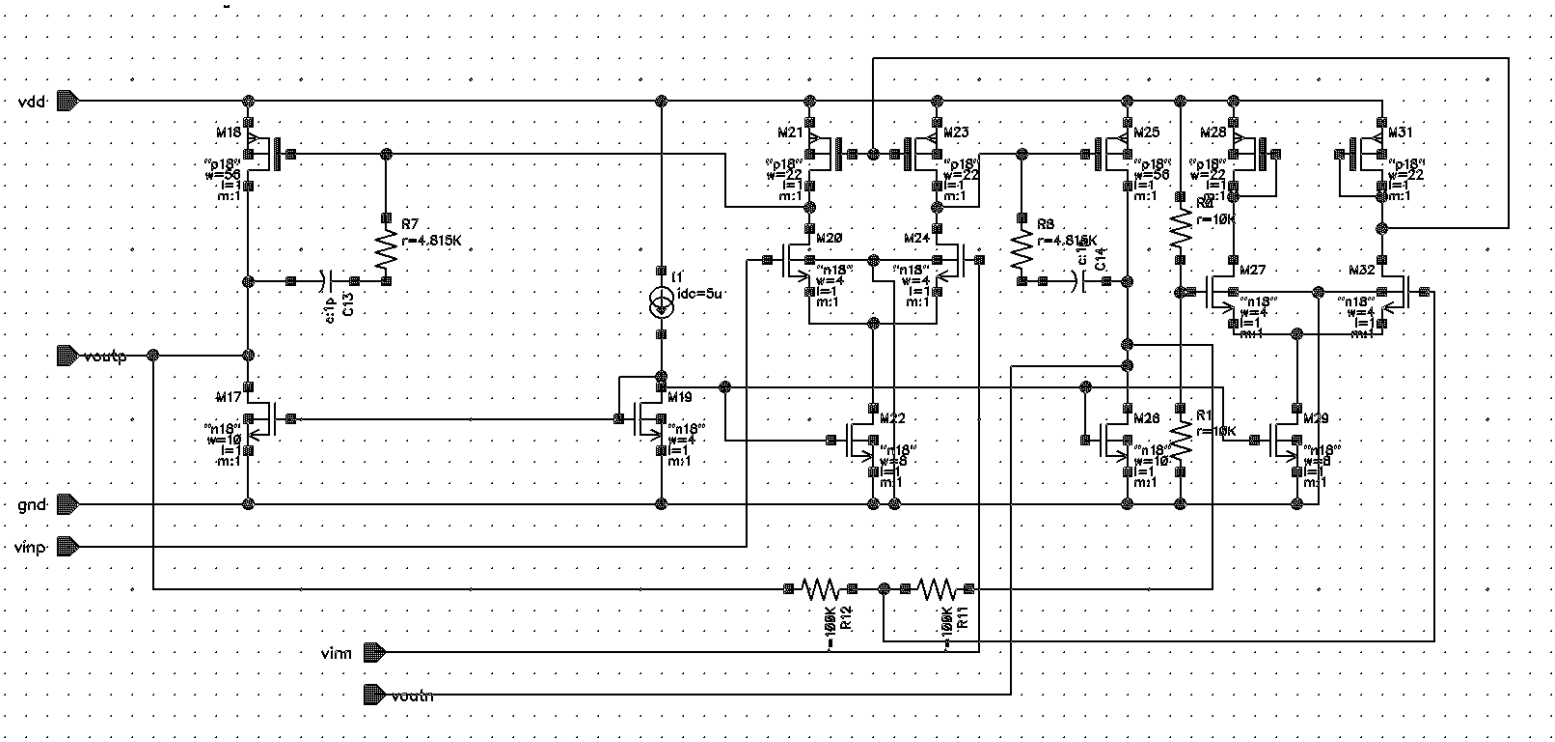


Figure 11: Fully differential two-stage Miller compensated op amp with CMFB

i. *Two-stage transistor sizes*
   A. Mirrored current = 5 μ A
   B. $(W/L)_{M19} = \frac{4\mu m}{1\mu m}$
   C. $(W/L)_{M17} = (W/L)_{M26} = \frac{10\mu m}{1\mu m}$
   D. $(W/L)_{M22} = \frac{8\mu m}{1\mu m}$
   E. $(W/L)_{M20} = (W/L)_{M24} = \frac{4\mu m}{1\mu m}$
   F. $(W/L)_{M21} = (W/L)_{M23} = \frac{22\mu m}{1\mu m}$
   G. $(W/L)_{M18} = (W/L)_{M25} = \frac{56\mu m}{1\mu m}$
   H. $R_c = R_7 = R_8 = 4.815k\Omega$
   I. $C_c = C_{13} = C_{14} = 1pF$
   J. $C_L = 1pF$

ii. *Common mode feedback transistor sizes*
   A. $R_0 = R_1 = 10k\Omega$
   B. $(W/L)_{M29} = \frac{8\mu m}{1\mu m}$
   C. $(W/L)_{M27} = (W/L)_{M32} = \frac{4\mu m}{1\mu m}$
   D. $(W/L)_{M28} = (W/L)_{M31} = \frac{22\mu m}{1\mu m}$
   E. $R_{12} = R_{11} = 100k\Omega$

The obtained results are as follows:

i. $A_v(0) = 92dB$
ii. Output swing = 0.1 - 1.7 V
iii. UGF = 6.135 MHz
iv. PM = 87.55°

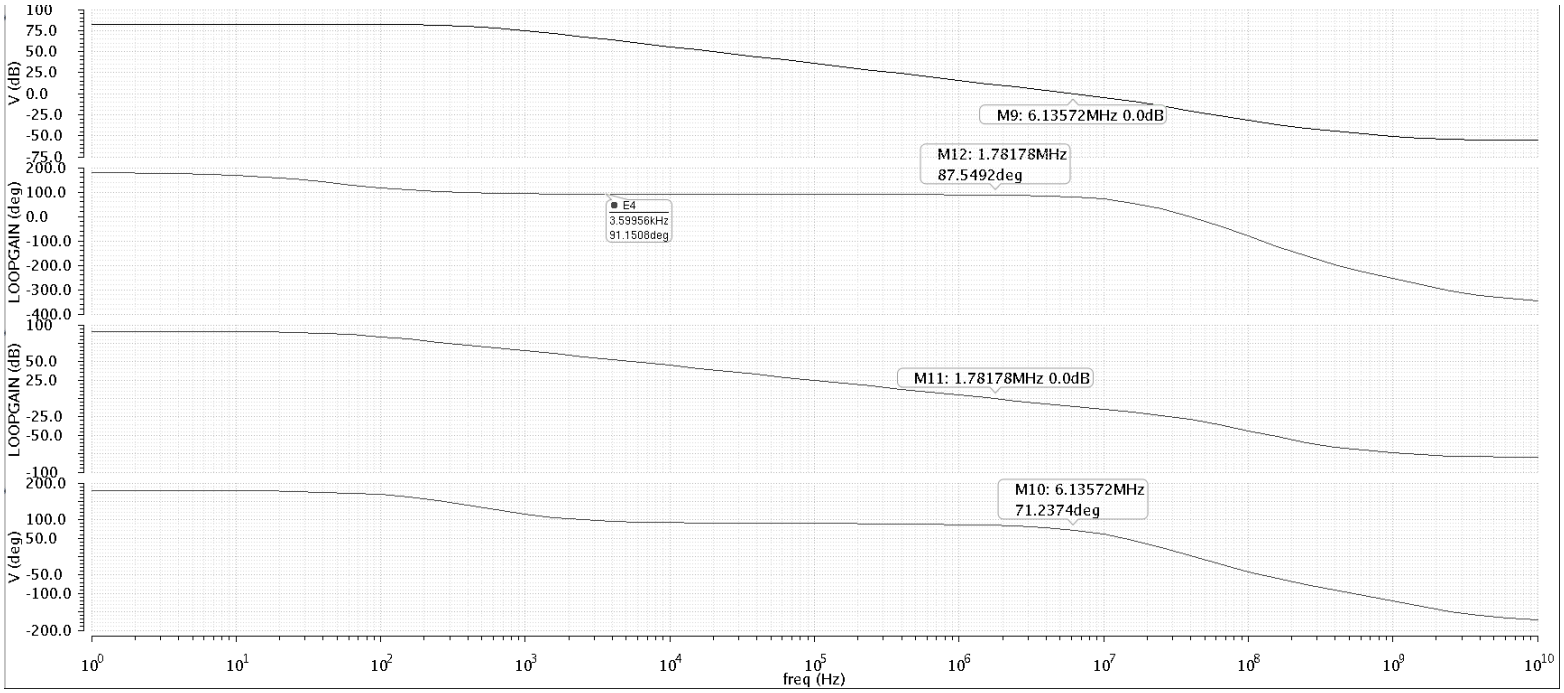


Figure 12: Frequency response of designed op amp

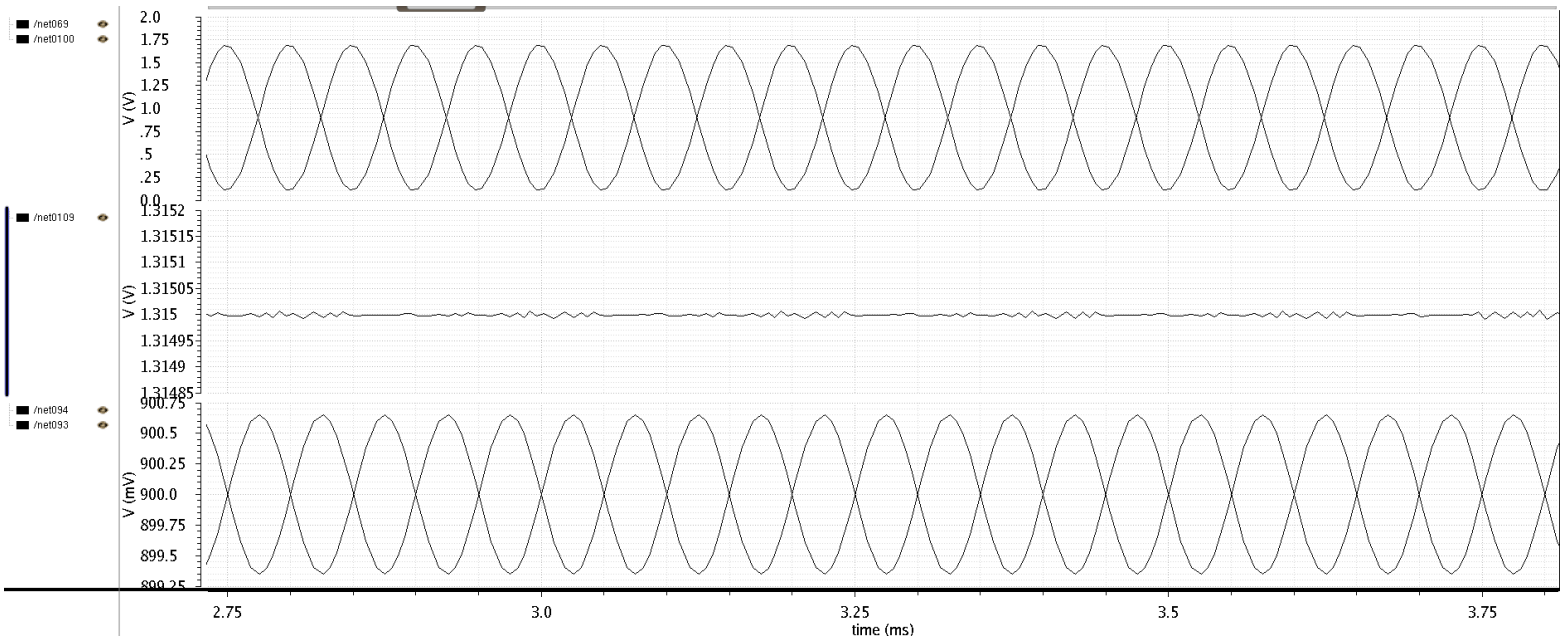


Figure 13: Output swing and common mode feedback operation of designed op amp

The op amp exhibits dominant flicker noise at lower frequencies, and the input referred noise is $20\mu V$ when integrated over a frequency range from 0.01 Hz to 150 Hz. Thus, to reduce the noise, the op amp must be chopper stabilized.

(e) *Switched capacitor integrator:*

A continuous time integrator using resistors and capacitors cannot be implemented accurately in CMOS because of up to 30% resistor variation. Thus, switched capacitor circuits are used as capacitor matching is relatively well controlled, and mismatches rarely exceed 1%. The given implementation is parasitic insensitive, and it makes use of bottom plate sampling by using delayed and non-overlapping clocks Φ_1, Φ_{1d}, Φ_2 and Φ_{2d}. By opening the switches operating on phases Φ_1 and Φ_2 before those operating on Φ_{1d} and Φ_{2d}, the charge injected through In^+ and In^- remains constant, and hence cancels out differentially. For simplicity, the operation of the circuit is shown with equivalent delayed and non-delayed phases.

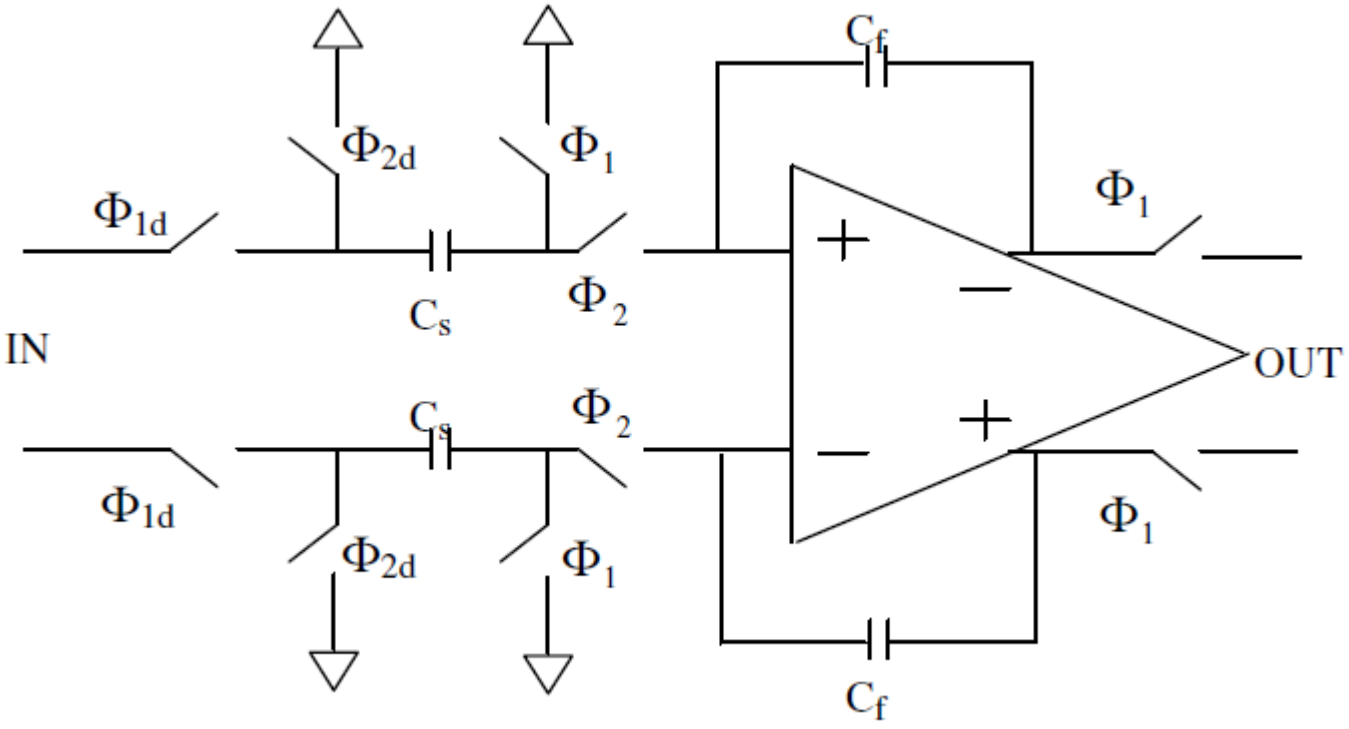


Figure 14: Fully differential switched capacitor integrator [1]

(a) Phase Φ_1

(b) Phase Φ_2

Figure 15: Switched capacitor integrator circuit operation in each phase [1]

Assuming an ideal op amp (with infinite gain), we may derive the equations governing the integrator operation as follows:

$$V_{out}[n] = V_{out}[n-1] + \frac{C_s}{C_f} V_{in}[n-1]$$

Taking the Z transform on both sides,

$$V_{out}(z) = z^{-1} \cdot (V_{out}(z) + \frac{C_s}{C_f} V_{in}(z))$$

i.e.

$$V_{out}(z) = \frac{C_s}{C_f} \cdot \frac{z^{-1}}{1 - z^{-1}} V_{in}(z)$$

Ideally, the response of the modulator must be completely linear across the whole frequency range. However, due to non-idealities such as finite op amp gain and limited slew rate and unity gain frequency may saturate the integrator's response at low frequency values. Thus, a figure of merit for the behavior of a switched capacitor integrator can be the cut-off frequency below which it saturates. Periodic AC analysis (PAC) was performed on the designed switched capacitor integrator and $f_{cut-off}$ was obtained as 18.75 Hz, which is much lower than input signal frequency. Also, the response remains linear till 25 MHz and above with a -20 dB/decade slope.

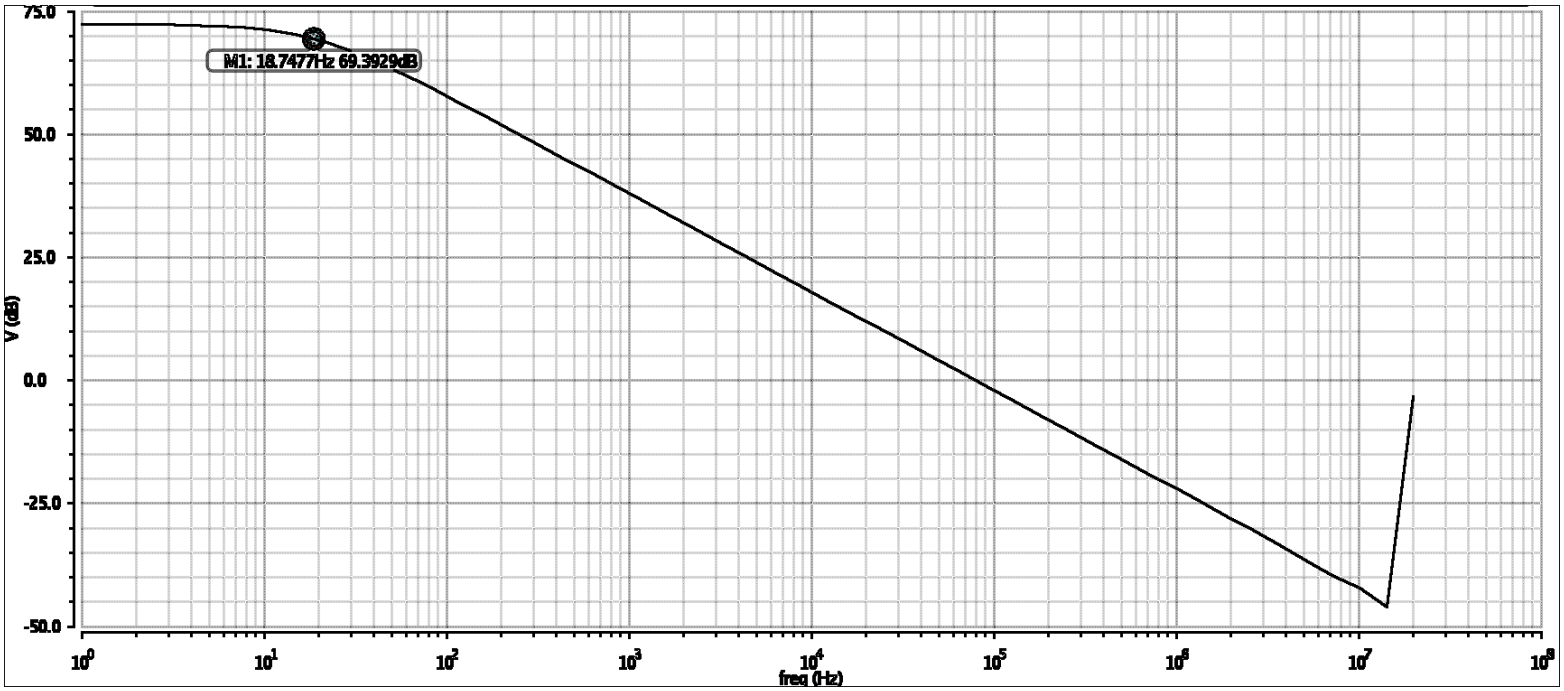


Figure 16: PAC response of switched capacitor integrator

(f) *Capacitor sizing:*

Capacitor sizing plays an extremely important role in the design of a $\Delta - \Sigma$ modulator. The thermal noise analysis of a switched capacitor integrator yields: $\overline{v_n^2} = \frac{4kT}{C_s \cdot OSR}$ Targeting a SNR of around 85 dB leads to an estimate of C_s as follows:

$$\overline{v_n^2} = \frac{0.5 \cdot (0.05)^2}{10^{8.5}} = \frac{4kT}{C_s \cdot 496.5}$$

i.e. $C_s = 8.44pF$. For conservativeness, the value 15 pF is chosen. The other capacitance values may be calculated from the CIFB coefficients as follows: $C_{s1}/C_{f1} = a_1/V_{ref} = 0.5$, $C_{s2}/C_{f2} = a_2/V_{ref} = c_1 = 0.5$,. Thus, $C_s = 15pF$ and $C_f = 30pF$ for both the integrators.

(g) *1-bit quantizer:*

A $\Delta - \Sigma$ modulator differs from other ADCs in the way that it doesn't require a quantizer with resolution equal to the resolution of the modulator as a whole. Therefore, accuracy isn't a stringent requirement in the design of the quantizer. For combined sample-and-hold and comparator functionalities, a regenerative comparator i.e. a clocked comparator is an optimal design choice. Also, as the comparator offset, hysteresis and noise effects are suppressed by the modulator loop, they don't present significant challenging requirements in the design flow. A variation of the StrongARM latch has been designed here. For using the clocked comparator as a quantizer, a SR latch is placed after it.

The comparator works on the principle of dynamic digital logic, which uses two clock phases for generating an output - a pre-charge phase and an evaluation phase. An NMOS input transistor pair is drain-coupled to a NMOS cross-coupled pair. Another cross-coupled PMOS pair is separated from the NMOS pair by control transistors. PMOS pre-charge transistors are drain-coupled to the PMOS cross-coupled pair. A PMOS shunting transistor is used to shunt the input pair drains during the pre-charge phase. During the pre-charge phase, the comparator doesn't follow the input signal as the control transistors are switched off and the pre-charge transistors charge the output to the positive rail. During the evaluation phase, the output voltages start dropping from the positive rail and the NMOS cross-coupled pair's drain voltages start rising. If one of the inputs is higher, then the corresponding drain voltage drops faster and turns the opposite PMOS transistor on. Thus, the regenerative action of the cross-coupled pairs pull the outputs to the negative and positive rails respectively. The control transistor sizes are kept equal to the input pair to efficiently trade-off the minimum resistance and capacitance requirements for high speed operation. The other transistors are sized similarly. Two 100 fF capacitors are placed in a negative feedback configuration to add some hysteresis to the comparator.

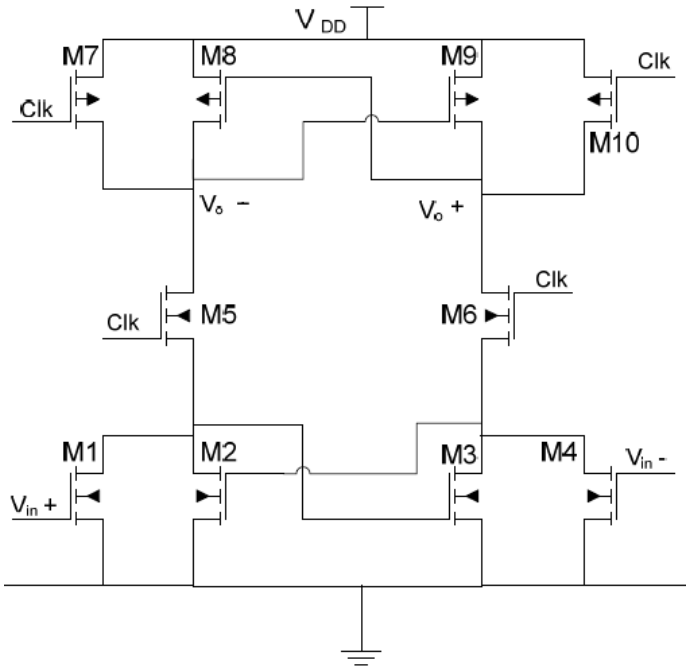


Figure 17: Regenerative comparator [1]

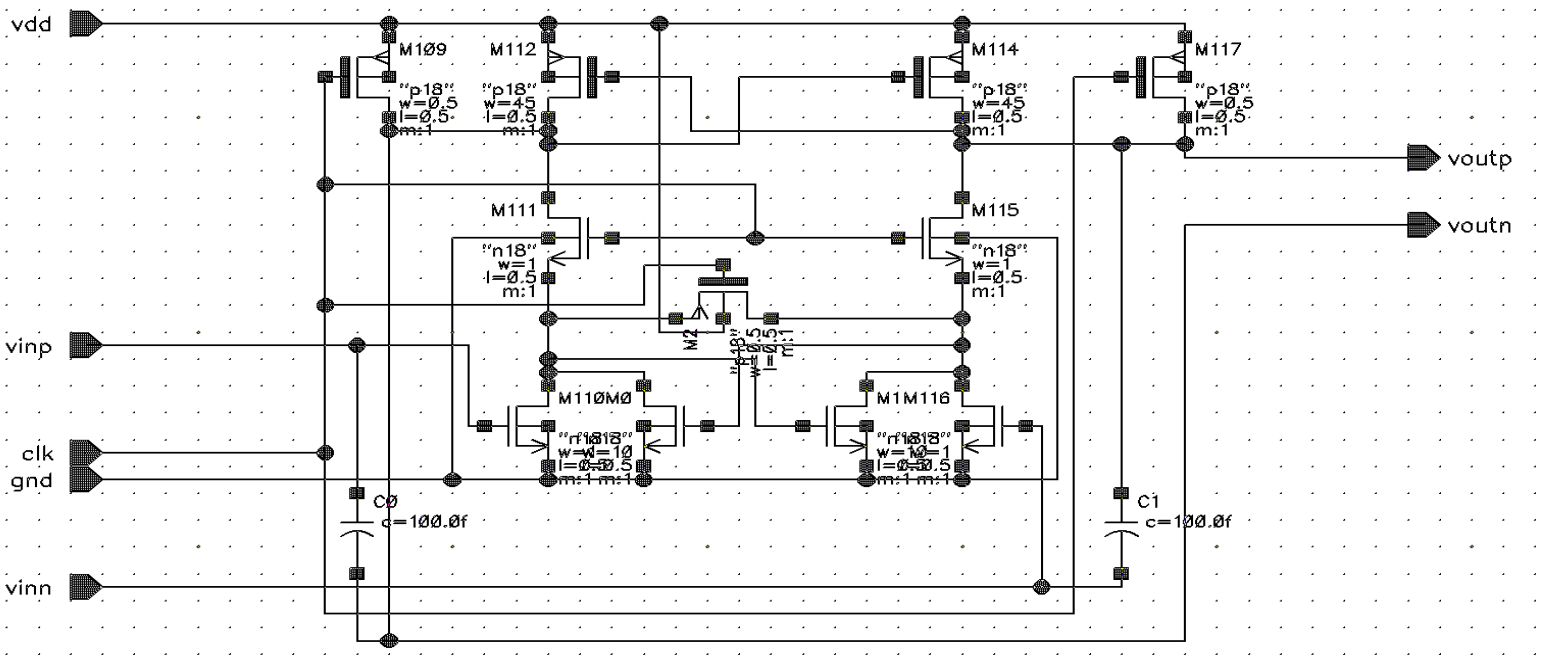


Figure 18: Regenerative comparator

i. *Regenerative comparator transistor sizes*

A. $(W/L)_{M0} = (W/L)_{M1} = \frac{10\mu m}{0.5\mu m}$

B. $(W/L)_{M110} = (W/L)_{M116} = \frac{1\mu m}{0.5\mu m}$

C. $(W/L)_{M2} = \frac{0.5\mu m}{0.5\mu m}$

D. $(W/L)_{M111} = (W/L)_{M115} = \frac{1\mu m}{0.5\mu m}$

E. $(W/L)_{M112} = (W/L)_{M114} = \frac{45\mu m}{0.5\mu m}$

F. $(W/L)_{M109} = (W/L)_{M117} = \frac{0.5\mu m}{0.5\mu m}$

G. $C_0 = C_1 = 100fF$

(h) *1-bit DAC:*

The 1-bit DAC is implemented using transmission gates to switch between $V_{ref}^{-} = 0.8V$ and $V_{ref}^{+} = 1V$ on the basis of the quantizer output.

(i) *Chopper:*

As discussed earlier, a chopper and anti-chopper pair is placed at the input and output terminals of the op amp to reduce the flicker noise. A chopper is constructed using transmission gates and is operated at $\frac{f_s}{2}$ to prevent noise aliasing from occurring.

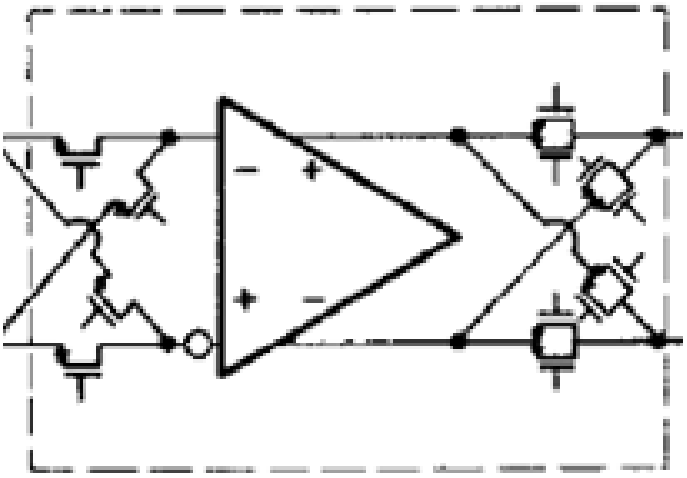


Figure 19: Chopper stabilized op amp[10]

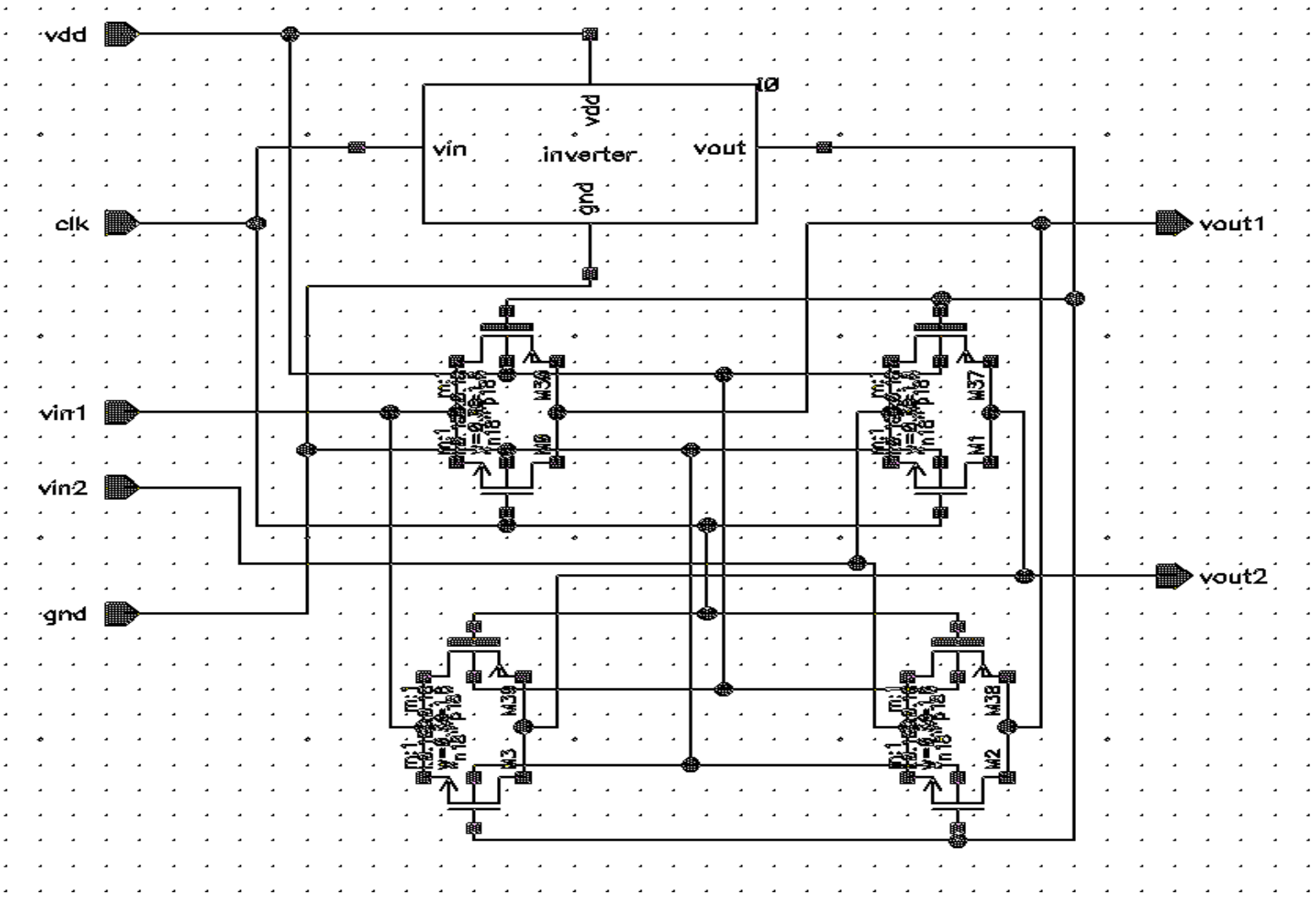


Figure 20: Chopper

(j) *Complete* $\Delta - \Sigma$ *modulator:*

Having designed and tested individual components, the whole $\Delta - \Sigma$ modulator is instantiated and simulated. The PAC of the two cascaded integrators agrees with theory, and exhibits a cut-off frequency of 12.1 Hz and is linear in the region of operation with a -40 dB/decade slope.

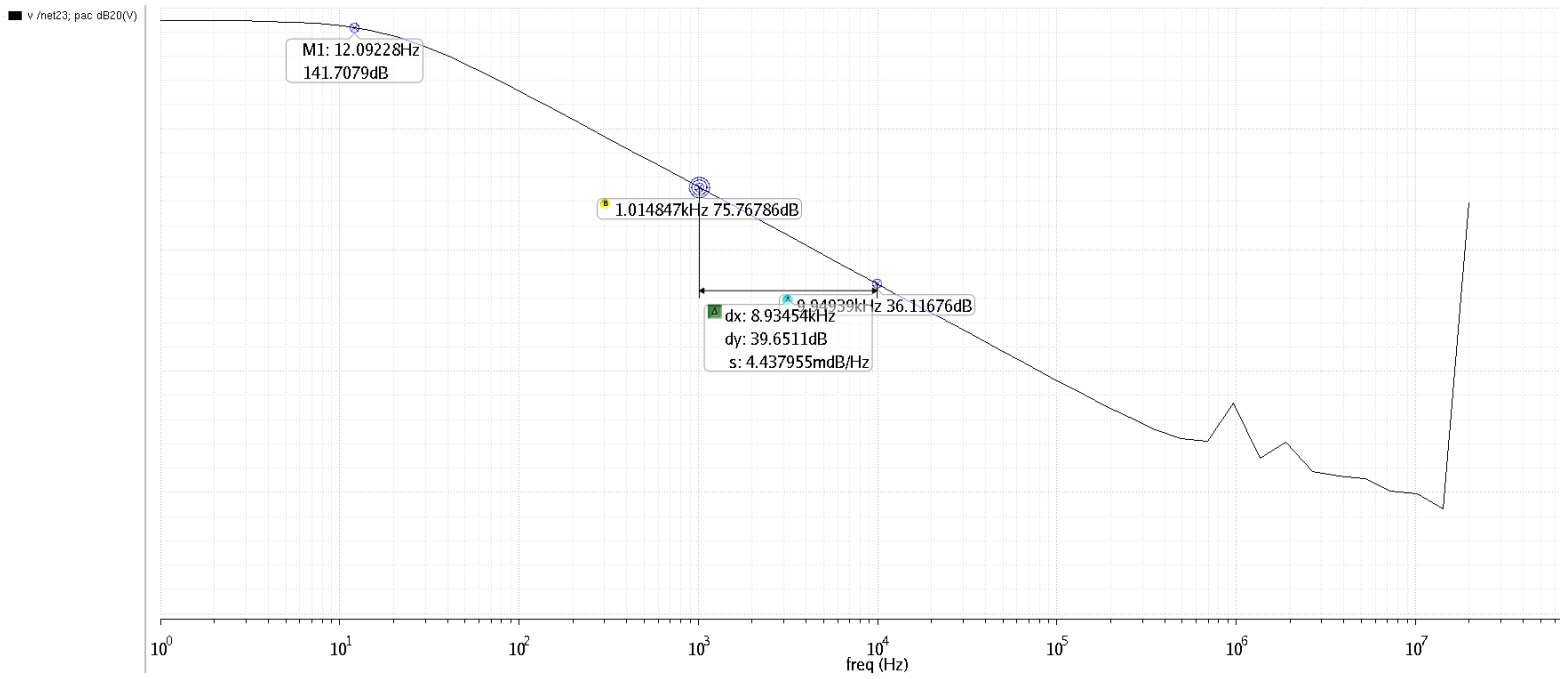


Figure 21: PAC response of cascaded integrators

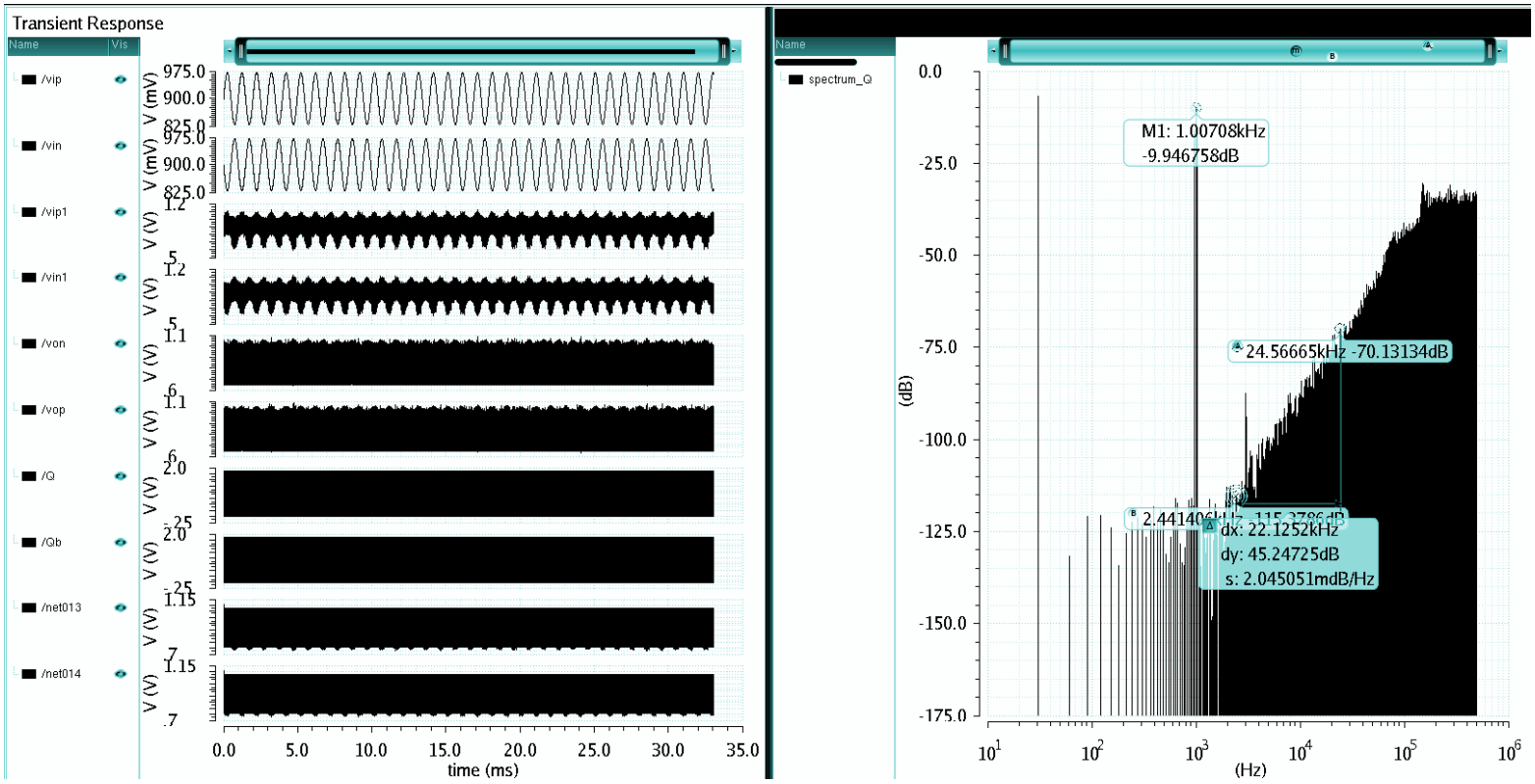


Figure 22: 1-bit, 2nd-order $\Delta - \Sigma$ modulator output (SQNR)

The simulations are performed for a sinusoidal input with frequency f_{in}. The spectral analysis is performed over N = 32768 samples, which corresponds to more than the $64 \cdot OSR$ samples required for proper estimation of noise. A Hanning window is used to window the data to lessen the effects of spectral spreading [5]. The spectrum of the modulator output clearly exhibits noise shaping with ≥ 40 dB/decade slope. The obtained performance parameters are as follows:

i. SQNR = 96.5 dB
ii. SFDR = 106 dB
iii. THD = 0 %
iv. ENOB = 15.73 bits

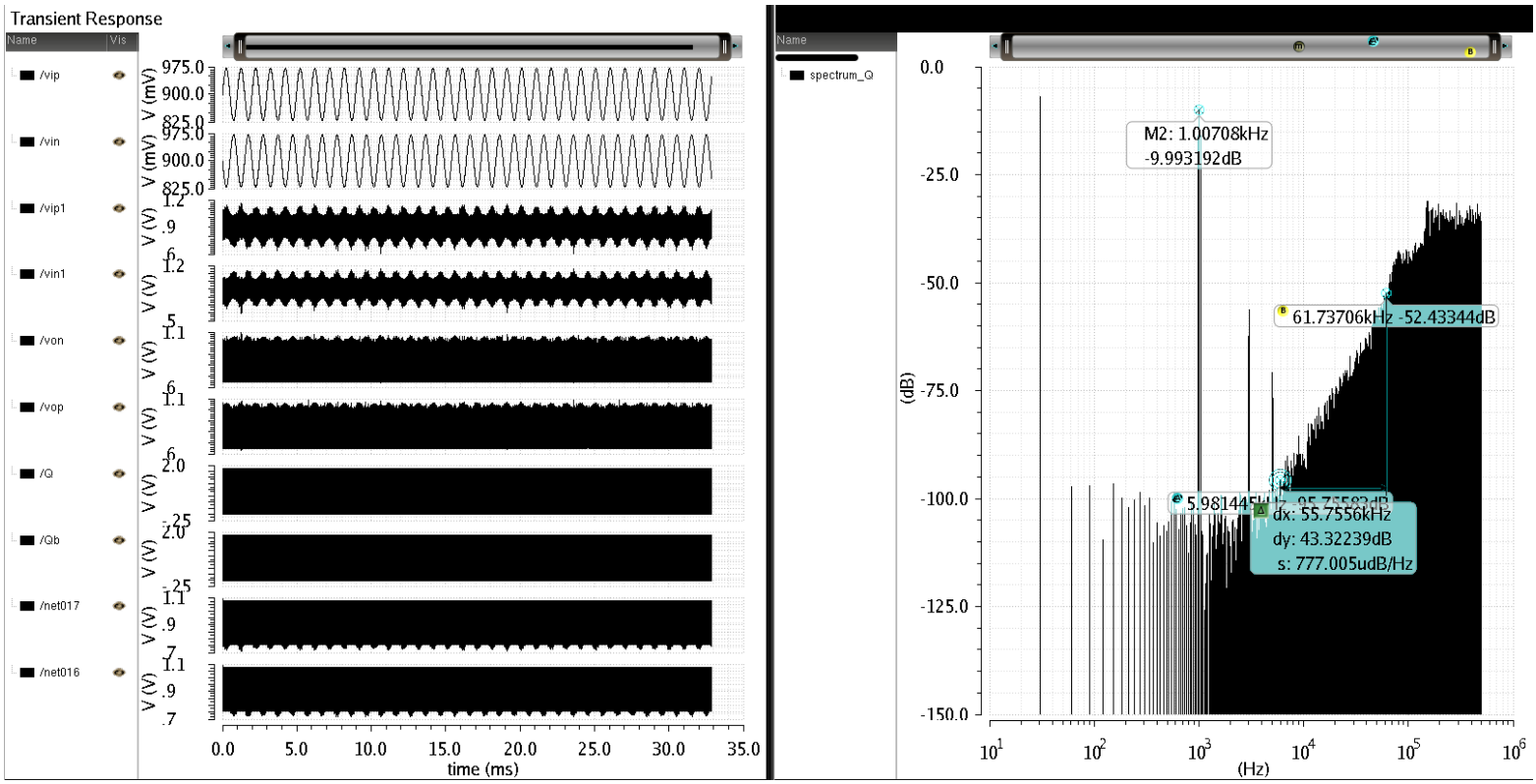


Figure 23: 1-bit, 2nd-order $\Delta - \Sigma$ modulator output (SNR)

i. SNR = 77.83 dB
ii. SFDR = 86.6 dB
iii. THD = 0 %
iv. ENOB = 12.64 bits

The final results obtained suggest that the thermal noise floor is a major bottleneck in an ADC design. While flicker noise contribution can be lessened via the addition of a chopper and anti-chopper pair, careful consideration must be given to minimize thermal noise power.

5. **Multi-bit, Multi-stage DT $\Delta - \Sigma$ Converter Design:**

(a) *Introduction:*

The formula for the SQNR suggests that increasing the number of bits in the quantizer would increase the SQNR by 6 dB proportionally. Therefore, to obtain slightly better performance, a 2-bit, 2nd-order $\Delta - \Sigma$ modulator may be designed. However, multi-bit quantizers lead to reduced stability of the modulator. Additionally, DAC non-linearity becomes a critical issue for multi-bit feedback in the $\Delta - \Sigma$ loop. Many algorithms have been suggested to combat DAC non-linearity, such as dynamic element matching (DEM), data weighted averaging (DWA), etc. A simplified version of the DEM technique has been implemented here for a 2-bit, 2nd-order modulator.

(b) *2-bit quantizer:*

A 2-bit quantizer may be constructed by using a flash ADC. By using a resistive ladder between the supply rails, the respective reference voltages may be generated, and passed to appropriate comparators. While various variations of the regenerative comparator implemented for the 1-bit quantizer case exist in the literature, a simpler approach has been favored in this work by simply reusing the designed comparator. The designed quantizer compares the negative differential signal with $V_{ref}^{-} + \frac{V_{ref}^{+} - V_{ref}^{-}}{6}$, $V_{ref}^{-} + \frac{5 \cdot (V_{ref}^{+} - V_{ref}^{-})}{6}$ and the positive differential signal each, and performs digital logic operations on them to yield the two bits.

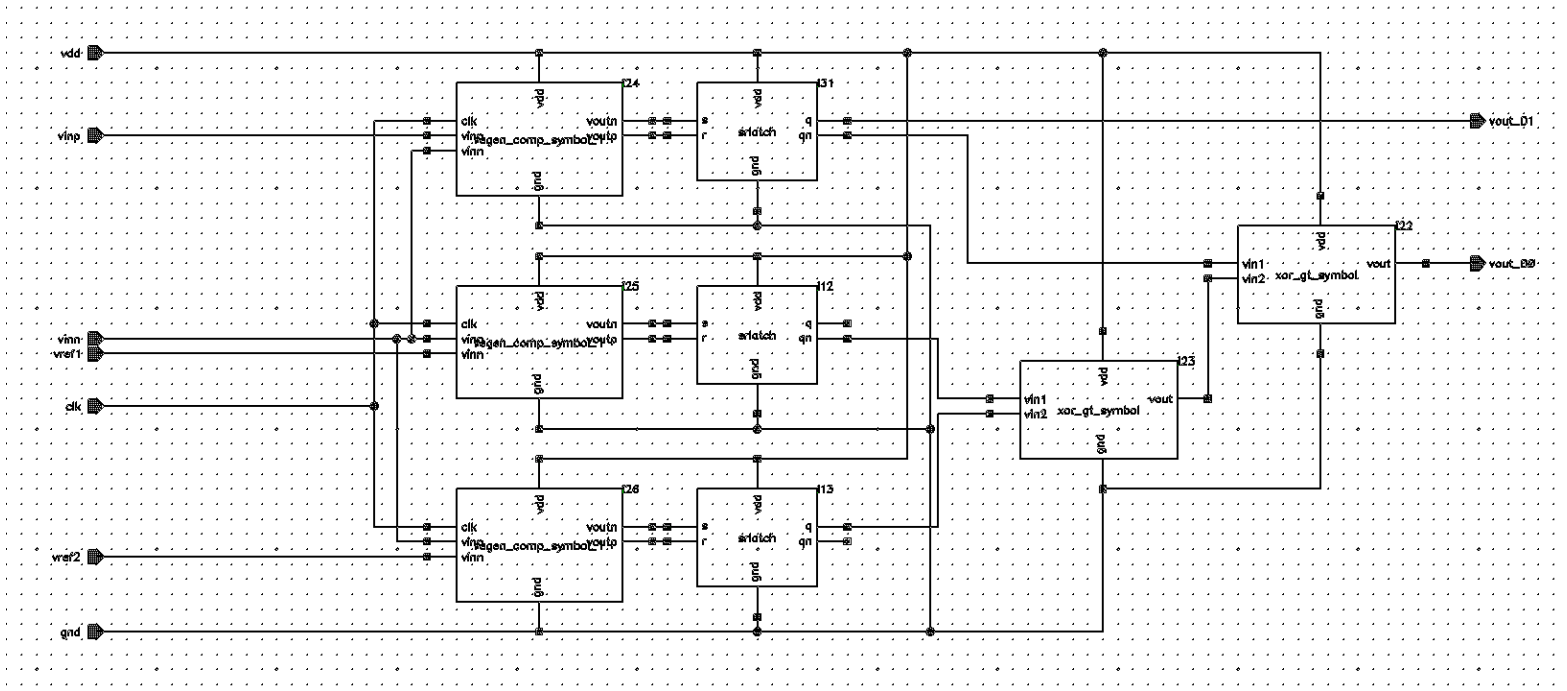


Figure 24: 2-bit quantizer

(c) *2-bit DAC:*

A 2-bit DAC may be implemented by simply using 3 analog multiplexers to select between the reference voltages depending on the 2 digital codeword bits.

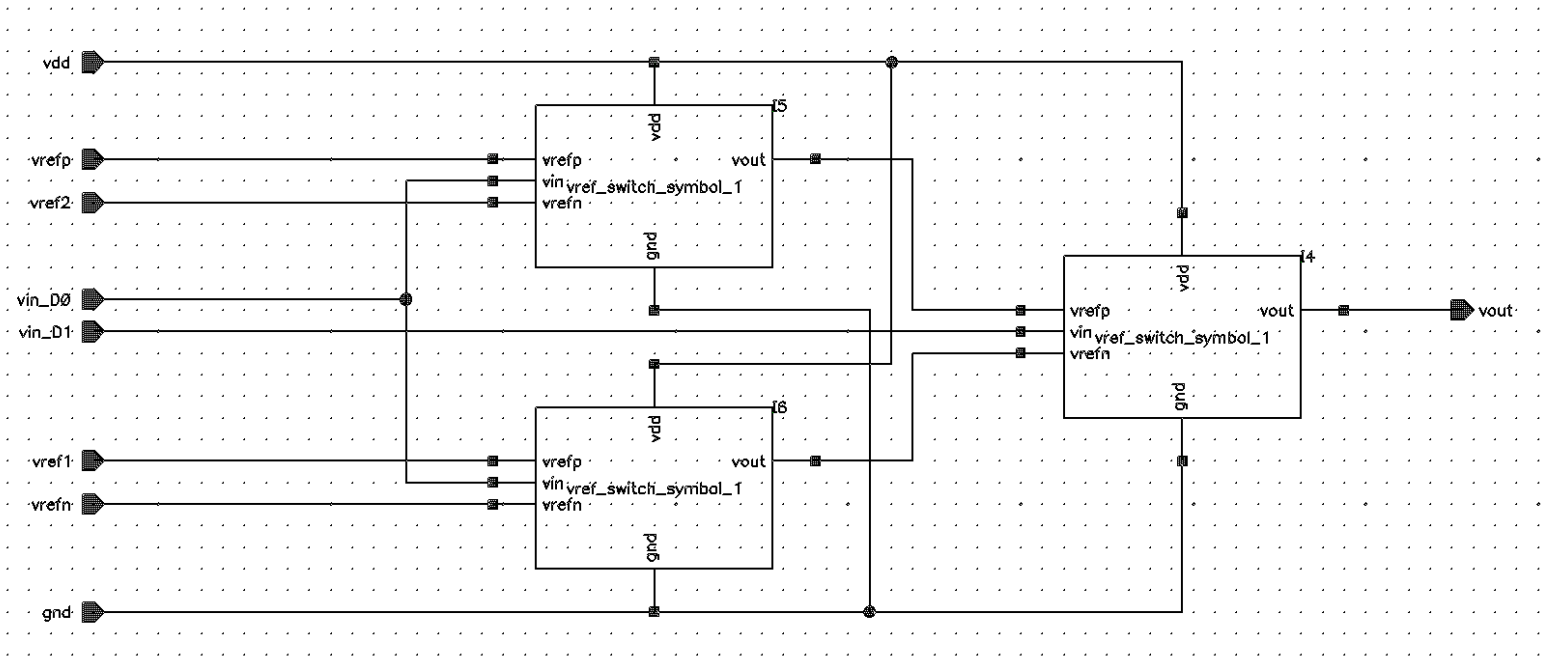


Figure 25: 2-bit DAC

(d) *Dynamic element matching technique:*

The DEM technique consists of using each unit element in a DAC implementation equally, instead of the conventional architecture where each element is utilized only when the input signal lies within its range. Thus, the functionality for the same may be achieved by using a pseudo-random noise (PN) sequence to switch between the unit elements. The designed DAC output matches well with that of a conventional DAC.

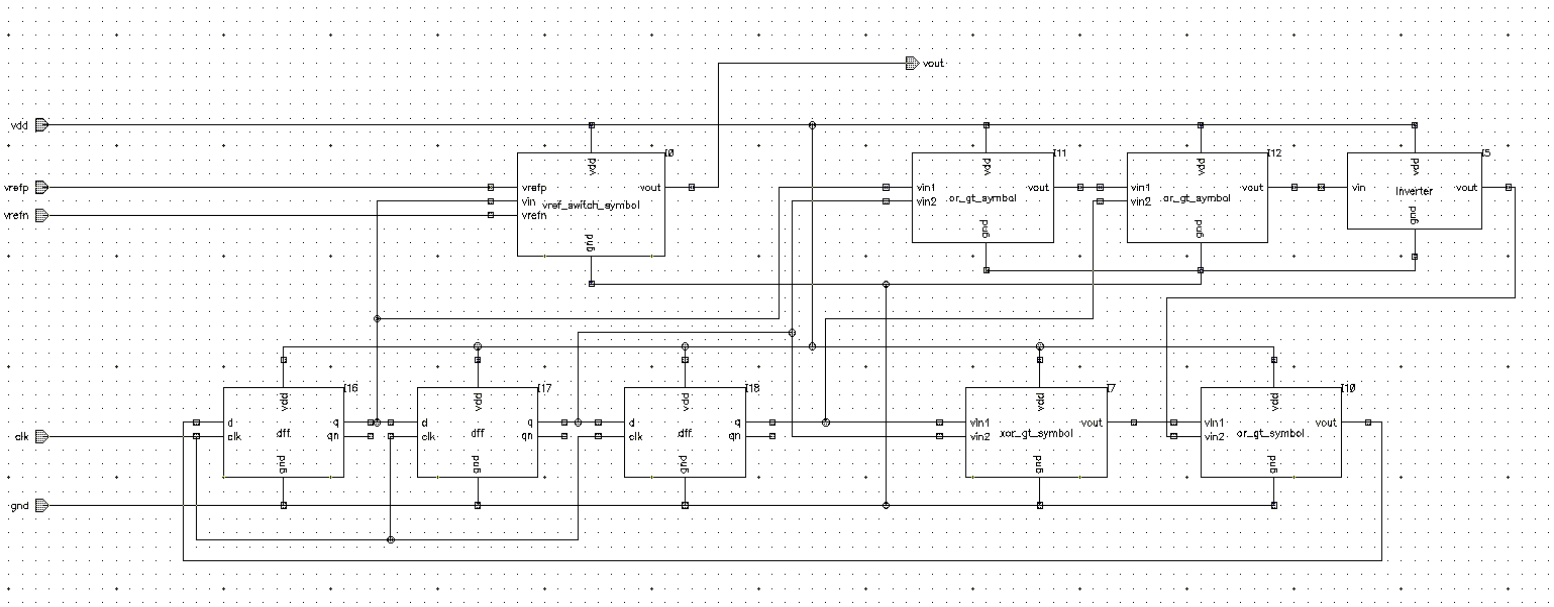


Figure 26: PN sequence generator

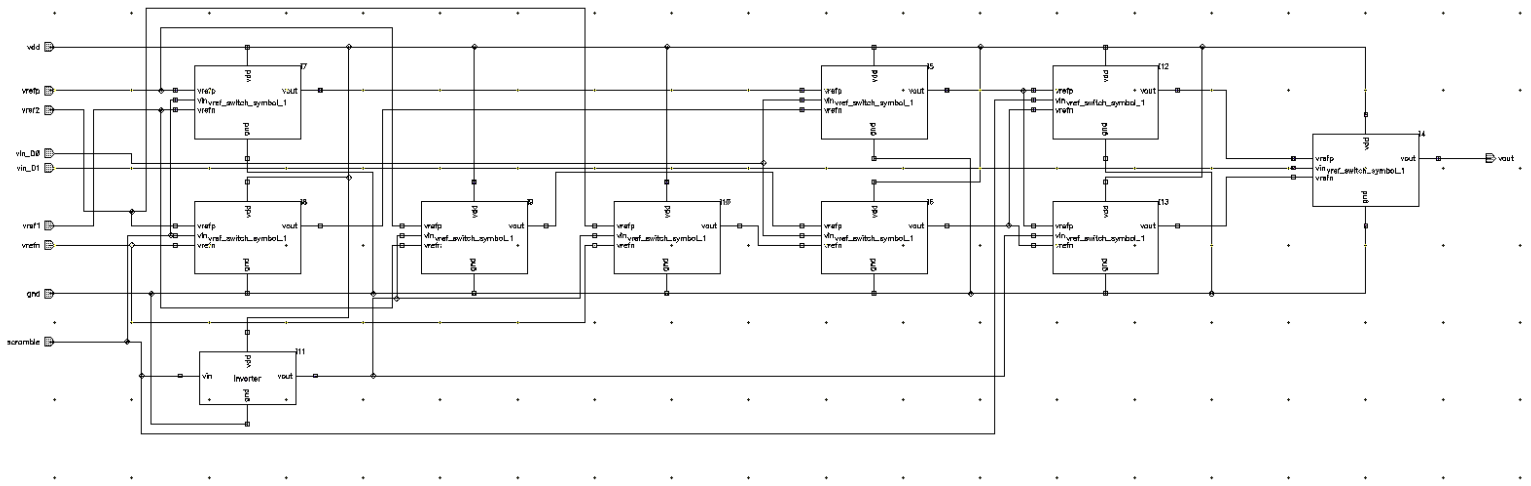


Figure 27: 2-bit DAC with DEM technique

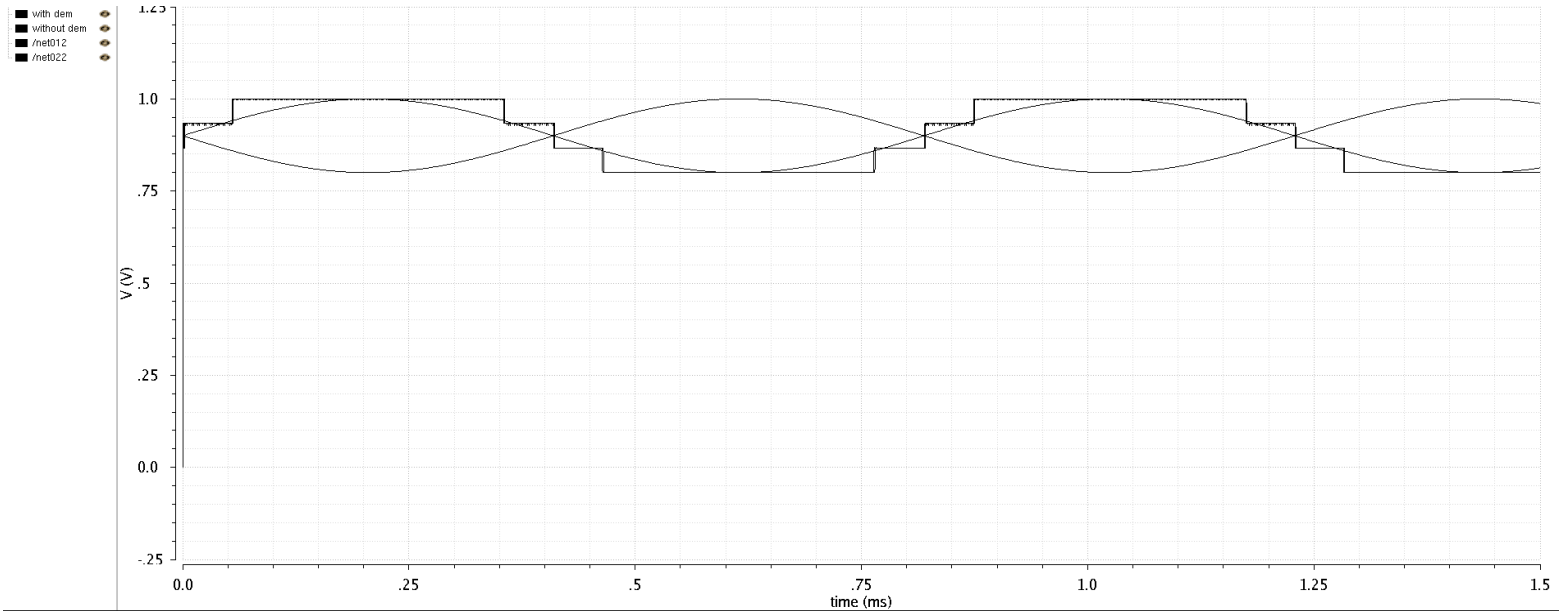


Figure 28: 2-bit DAC output with and without DEM technique

(e) *Leslie-Singh architecture:*

The Leslie-Singh architecture is a 2-stage modulator architecture that uses a multi-bit quantizer to replace the larger 1-bit quantizer error with the smaller error of the corresponding B-bit quantizer. The same is accomplished via FIR filters $H_1(z)$ and $H_2(z)$. Thus, significant improvement in SQNR may be expected from this architecture. Here, $B = 2$ and the first stage modulator has order 2.

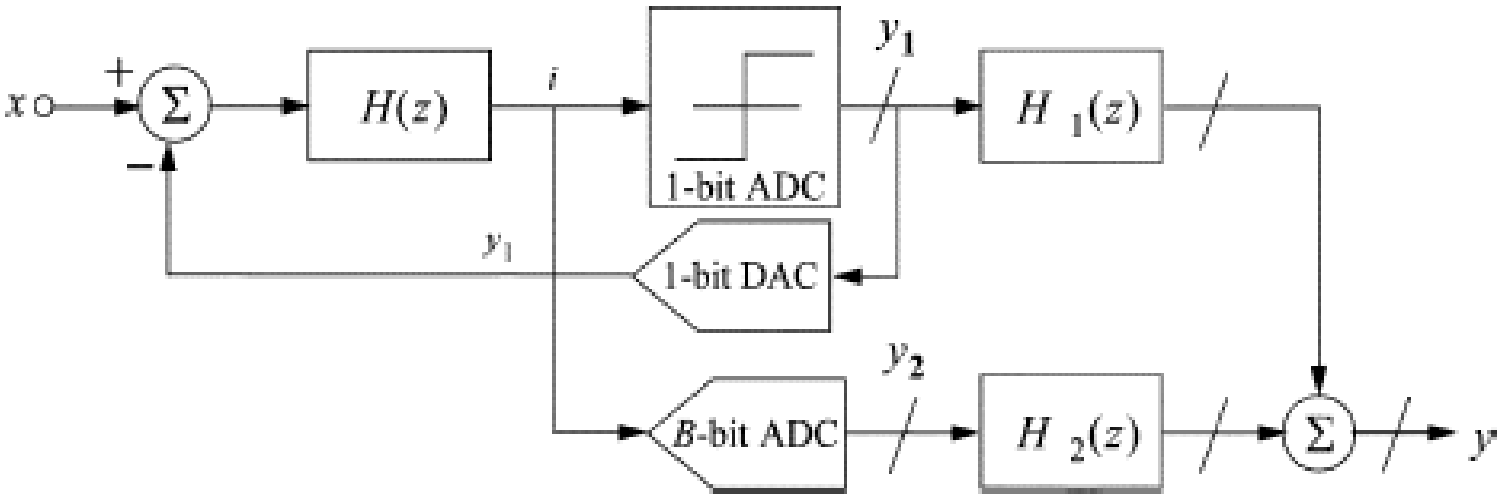


Figure 29: Leslie-Singh architecture [6]

The filter transfer functions are chosen in such a manner that the resulting output V(z) exhibits 2nd-order noise shaping with quantizer error $E_2(z)$. Thus, considering the modulator equation derived earlier:

$$0.2165z^{-2}X(z) + (1 - z^{-1})^2 E_1(z) = (0.7835z^{-2} - 1.567z^{-1} + 1)Y_1(z)$$

.
From the figure, we obtain:

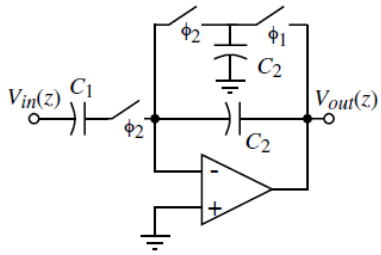
$$H_1(z)Y_1(z) + H_2(z)(Y_1(z) - E_1(z) + E_2(z)) = Y(z)$$

i.e.

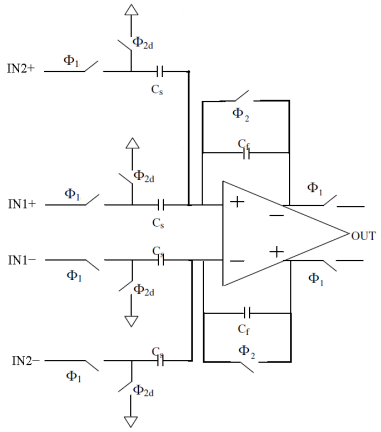
$$(H_1(z) + H_2(z))Y_1(z) - H_2(z)E_1(z) + H_2(z)E_2(z) = Y(z)$$

.
Now, $H_1(z)$ and $H_2(z)$ must be chosen in such a manner so as to cancel out the $E_1(z)$ term from the above equation while exhibiting 2nd-order noise shaping in $E_2(z)$. Therefore, choosing $H_2(z) = (1-z^{-1})^2$ for 2nd-order noise shaping, we obtain $H_1(z) = 0.2165 - 0.2165(1 - z^{-1})^2$.

The FIR filters are constructed by using switched capacitor derivative circuits with transfer function $\frac{V_{out}(z)}{V_{in}(z)} = \frac{-C_1}{C_2}(1 - z^{-1})$ and switched capacitor adders with transfer function $\frac{V_{out}(z)}{V_{in1}(z)+V_{in2}(z)} = \frac{-C_s}{C_f}$.



(a) Switched capacitor derivative circuit [8]



(b) Switched capacitor adder circuit

Figure 30: Switched capacitor derivative and adder circuits

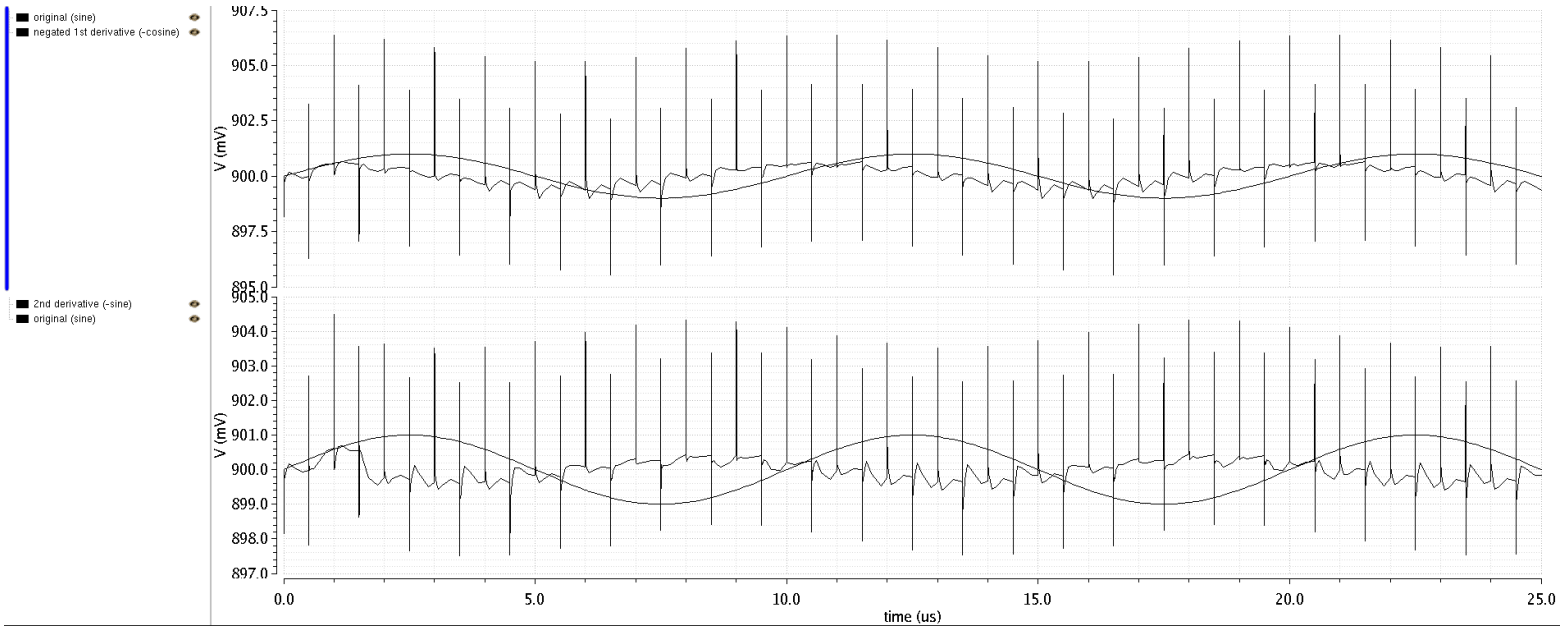


Figure 31: Switched capacitor derivative circuit output

6. **Summary:**

   A 1-bit, 2nd-order discrete time $\Delta - \Sigma$ modulator with resolution greater than 12 bits has been successfully designed for an analog front-end application. The performance of the designed modulator suggests that further enhancement may be achieved by using multi-bit, multi-stage techniques. Two such techniques have been discussed and partly implemented.

7. **Future Work:**

   The complete system-level analysis for the multi-bit, multi-stage design is the immediate future work to be performed. Additional future work might be the design of a complete front-end with combined signal conditioning amplifier and $\Delta - \Sigma$ ADC blocks. Such a system will enable extreme power and area savings compared to traditional circuits with separate amplifier and data converter modules.

8. **References:**

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[10] Wang, C.-K., Castello, R., Gray, P. (1986). A scalable high-performance switched-capacitor filter. IEEE Journal of Solid-State Circuits, vol. 21, pp. 57 – 64, February 1986.

9. **Appendix:**

(a) *Delta Sigma Toolbox Codes:*

i. *Main function:*

```
N = 32768; fs = 1e6; f = (33*fs)/N; Au = [-100:5:-10 -9:1:0]; snr = zeros(1,numel(Au));
u = 3*sin(2*pi*f.*(0:1/fs:N/fs)); w = (10e-4).*normrnd(0,1,1,N+1);
order = 2; OSR = N/66; nlev = 2;
ntf = synthesizeNTF(order,OSR); plotPZ(ntf);
for i=1:numel(Au)
    [snr(i),v] = sd_test_func(N,fs,f,10^(Au(i)/20)*u,w,order,OSR,ntf,nlev);
end
[sqnr, amp] = simulateSNR(ntf,OSR,[],[],nlev);
figure;
plot(Au,snr); hold on; plot(amp,sqnr); grid on;
form = 'CIFB'; [a,g,b,c] = realizeNTF(ntf,form); b(2:end) = 0;
ABCD = stuffABCD(a,g,b,c,form);
ABCDs = scaleABCD(ABCD,nlev,0,0.5,[],0.9);
[a,g,b,c] = mapABCD(ABCDs,form);
```

ii. *Subsidiary function:*

```
function [snrv,v] = sd_test_func (N,fs,f,u,w,order,OSR,ntf,nlev)
ut = u+w;
[vw,xnw,xmaxw,yw] = simulateDSM(w,ntf,nlev);
[v,xn,xmax,y] = simulateDSM(u,ntf,nlev);
[vt,xnt,xmaxt,yt] = simulateDSM(ut,ntf,nlev);
fx = -0.5*fs:fs/N:0.5*fs; fint = (0.5*N+3):((0.5*N+1)+N*1.5*f/fs);
hwv = fftshift(abs(fft(v'.*hanning(N+1)))./(N+1); hwvw = fftshift(abs(fft(vw'.*hanning(
    N+1)))./(N+1);
hwut = fftshift(abs(fft(ut'.*hanning(N+1)))./(N+1); hwvt = fftshift(abs(fft(vt'.*
    hanning(N+1)))./(N+1);
hwu = fftshift(abs(fft(u'.*hanning(N+1)))./(N+1); hwuw = fftshift(abs(fft(w'.*hanning(N
    +1)))./(N+1);
snru = 10*log10(sum(hwu(fint).^2)/sum(hwuw(fint).^2)); snrv = 10*log10(sum(hwv(fint).^2)
    /sum(hwvw(fint).^2));
end
```

Note: The Delta-Sigma Toolbox is available online: https://in.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox